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A 17MHz Wide-band Isolated Current Sensor for D-mode GaN Half-bridge

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Abstract

Inductor current sensing is demonstrated using a 20A range, 17MHz bandwidth galvanically isolated current sensor for D-mode GaN power device. The current sensor utilizes gain compensation to eliminate on-resistance PVT variations of the current-detecting MOSFET. Sensor output is up-converted and transferred through on-chip HV isolation capacitors. A calibration loop across the isolation is formed to keep the gain constant.

1. Introduction

A GaN power converter requires multiple current sensors to increase power efficiency and safety margin. Sensors are used in series with an inductor for PWM control, and in series with each power device for over-current protection and short-circuit protection. The number of these current sensors should be decreased, because they cause excess power dissipation and increase converter volume. One possible way is to calculate the inductor current from two drain current sensors as shown in Fig.1 [1]. Wide-band current sensors are necessary, because inductor current is switched between high-side and low-side switches, while conventional inductor current sensor only need to monitor average current. However, wide bandwidth and high accuracy isolated current sensor has not been demonstrated. In a shunt resistor and an isolation amplifier configuration, signal bandwidth is limited to < 1MHz because it uses an ADC to achieve high linearity [2]. This configuration also suffers with the shunt resistor power dissipation and large propagation delay. A Hall sensor is isolated in nature, but it suffers from magnetic interference, thermal drift and limited bandwidth. A shunt resistor and ADC-less isolation amplifier [3] provides wide-band current sensor and isolation, however extra power is dissipated at shunt resistor.

The aim of this work is to demonstrate inductor current sensing with wide-band and shunt-resistor-less isolated drain current sensor for a depletion-mode (D-mode) GaN cascaded with a low-voltage MOSFET (LVMOS). The cascaded GaN is known to have higher reliability and freedom of threshold voltage design compared to an enhancement-mode (E-mode) GaN. We propose using the voltage drop across a MOSFET and an ADC-less isolation amplifier as shown in Fig.1.

2. System and Circuit Design

Although the proposed configuration provides wide-band current sensing, it suffers from current to voltage conversion gain (trans-impedance) variation in both LVMOS on-resistance and ADC-less isolation amplifier. These gain variation sources have different requirements, and need different compensation techniques. LVMOS on-resistance compensation should track fast temperature changes induced by current change in AC line phase, load current, etc. An analog feedback technique suits well. Conversely, the isolation amplifier gain compensation needs a wide phase and gain margin and an analog solution does not work effectively. A calibration technique is appropriate. We propose a hybrid feedback- and calibration-loop configuration to track trans-impedance variation caused by faster temperature change of an LVMOS and slower temperature change of an isolation amplifier as shown Fig.2.

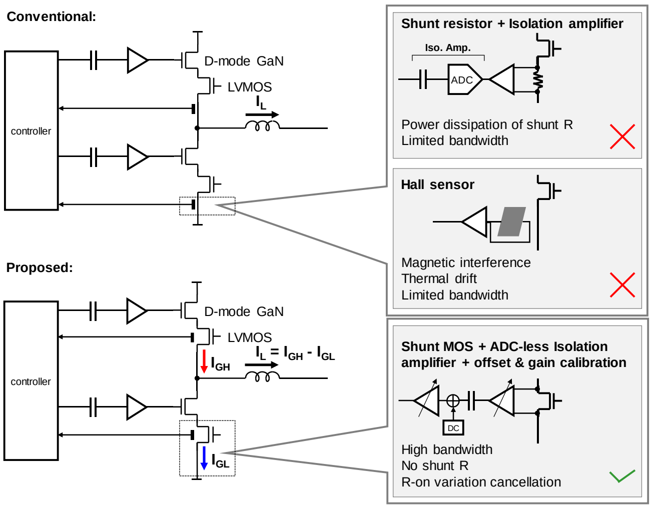

Fig. 1 Conventional and proposed current sensing method.

LVMOS on-resistance is compensated on Chip1. To maximize the sensor bandwidth, the signal path is kept outside the feedback-loop. As shown in Fig.2, IREF1 and a replica LVMOS (1/α width of LVMOS in series with the GaN power device) generates a reference voltage proportional to the on-resistance. The feedback loop controls the trans-conductance (gm) of variable gm cell such that gm is inversely proportional to the replica LVMOS on-resistance. An identical variable gm-cell is used to convert current I_{GL} to I_{SENSE} in the signal path. Output voltage V_{SENSE1} depends on LVMOS size ratio α and R_F in Fig.2. This configuration enables measuring both positive and negative current unlike a common configuration [4]. V_{SENSE1} is up-converted and transferred to the low-voltage side by a passive mixer and on-chip high-voltage capacitors on Chip3. Then it is down-converted and low-pass filtered on Chip2 to obtain a baseband signal. Gain of the ADC-less isolation amplifier (V_{SENSE2}/ V_{SENSE1}) is calibrated to a ratio between a reference voltage generated by band-gap reference 2 (BGR2) on Chip2 and a reference voltage generated by BGR1 on Chip1. The accuracy of the calibration depends on the matching of the two bandgap references. Brokaw's BGR is used. NPN bipolar transistors in CMOS technology show lower β, which increases temperature coefficient variation. To reduce the sensitivity to β variation, a base resistance R_B is added to the NPN transistors. BGRs are trimmed to have the minimum temperature coefficient and absolute value difference by two-point calibration at 27 and 80°C, because Chip1 and Chip2 experience large temperature difference induced by large difference of power dissipation and high thermal resistance across the isolation barrier. A variable gm-cell on Chip2 is controlled by an 8-bit voltage-DAC using a reference voltage generated by BGR2. DC offset of ADC-less isolation amplifier is calibrated using an 8-bit current-DAC in advance to the gain-calibration.

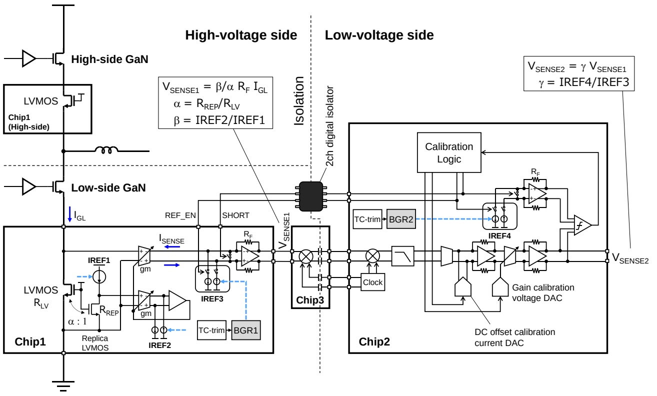

Fig. 2 Block diagram of a low-side isolated current sensor.

3. Measurement Results

Figure 3 top left shows temperature dependence of on-resistance of the LVMOS and trans-impedance of the current sensor (Chip1) from two different wafers. The on-resistance almost doubles from -40 to 125 °C, while the trans-impedance maintains +/-2 % accuracy. The error is caused by temperature dependence of poly-silicon resistor R_F and feedback loop residual error. Temperature dependence of trans-impedance of current sensor through isolation amplifier (Chip1 through Chip2) is shown in the top right. Isolation amplifier gain decreases with increasing temperature without calibration due to decrease of clock amplitude in Chip3, while gain variation is eliminated within +/-1.5% with calibration. Frequency response of Chip1 and Chip1 through Chip2 are shown in the bottom left. Current sensor linearity up to 20 A is also shown. Figure 4 compares inductor current and high-side and low-side GaN current measured by proposed method in a high-side double-pulse test. Accumulation and reverse current are detected by the high-side and low-side current sensor, respectively. Figure 5 shows the PCB layout of the main power loop and die photos of Chip 1 to 3.

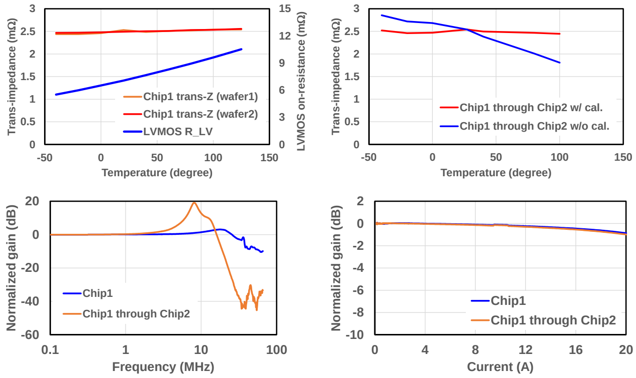

Fig. 3 Current sensing characteristics.

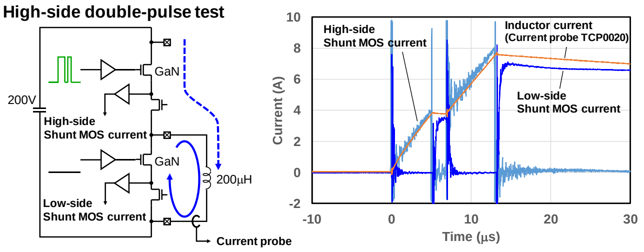

Fig. 4 High-side double-pulse test setup and high-side and low-side current sensor waveform.

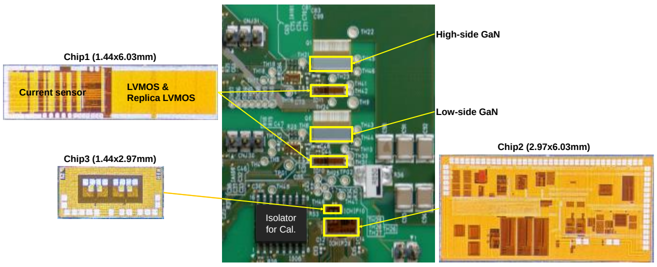

Fig. 5 Printed circuit board & die photo.

4. Conclusions

Inductor current sensing with wide-band and shunt-resistor-less isolated current sensors is successfully demonstrated. Current sensor and isolator temperature variation is reduced by a hybrid feedback- and calibration-loop configuration.

References

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