TOSHIBA



# Design Method to Improve Clamping Capability of Parasitic pn Diodes Utilizing Newly Developed Equivalent Circuit Model of SBD-Embedded SiC MOSFETs

**Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are attracting attention as a new generation of power devices due to their superior characteristics. Schottky barrier diode (SBD)-embedded MOSFETs have also been expanding into the mainstream due to their ability to reduce performance degradation caused by the operation of parasitic pn diodes in devices. However, the maximum current density at which the operation of parasitic pn diodes does not occur (hereafter abbreviated as $J_{umax}$) decreases with rising temperature, creating a problem for the high-temperature application of SBD-embedded SiC MOSFETs.**

**In order to prevent $J_{umax}$ from decreasing at high temperatures, the Toshiba Group has developed a novel design method for SBD-embedded SiC MOSFETs that makes it possible to simulate $J_{umax}$ using a simple structure model and design devices with an enhanced value of $J_{umax}$. Experiments on prototype 3.3 kV SBD-embedded SiC MOSFETs with structures designed by this method have confirmed that these structures achieve 4.7 times higher $J_{umax}$ compared with the conventional structure.**

## 1. Introduction

Power electronics technology is becoming increasingly important to reduce power loss of electric systems and thereby help alleviate environmental issues, including global warming and the depletion of fossil fuels. The use of silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) helps to considerably reduce the power loss particularly of high-voltage, high-frequency applications. Their market is expanding as they attract plenty of attention as a new generation of power devices.

A conventional SiC MOSFET has a parasitic pn diode as shown in **Figure 1.** The electrical characteristics of the SiC MOSFET degrade when the parasitic pn diode is used as a free-wheeling diode. When holes are injected through the parasitic pn diode, basal plane dislocations (BPDs) in an SiC wafer develop into a stacking fault because of the energy released through the recombination of electrons and holes, causing an increase in device resistance (Figure 1(b)).

To prevent the conduction of the parasitic pn diode, the Toshiba Group is developing SiC MOSFETs with an embedded Schottky barrier diode (SBD)[1]. They suppress the conduction of the parasitic pn diode (i.e., clamp the voltage across it) by passing free-wheel current through the embedded SBD. We demonstrated that the SBD-embedded SiC MOSFETs provide higher reliability than conventional SiC MOSFETs[1].

However, the parasitic pn diode in the SBD-embedded MOSFET also conducts when an increase in current density during conduction causes a certain voltage to be applied across the parasitic pn diode. $J_{umax}$, the maximum current density at which the parasitic pn diode does not conduct, indicates its clamping capability. We confirmed that $J_{umax}$ decreases particularly at high temperature[1]. It is therefore important to further increa se $J_{umax}$ of the SBD-embedded SiC MOSFET requiring high-temperature operation.

To develop SBD-embedded SiC MOSFETs with higher $J_{umax}$, it is necessary to correctly identify the device parameters that determine $J_{umax}$.

With this as a background, we have created a new equivalent circuit model for an SBD-embedded SiC MOSFET to extract these device parameters and derive design guidelines for increasing $J_{umax}$. This report details our experiment conducted to increase the $J_{umax}$ of an SBD-embedded SiC MOSFET based on these design guidelines.

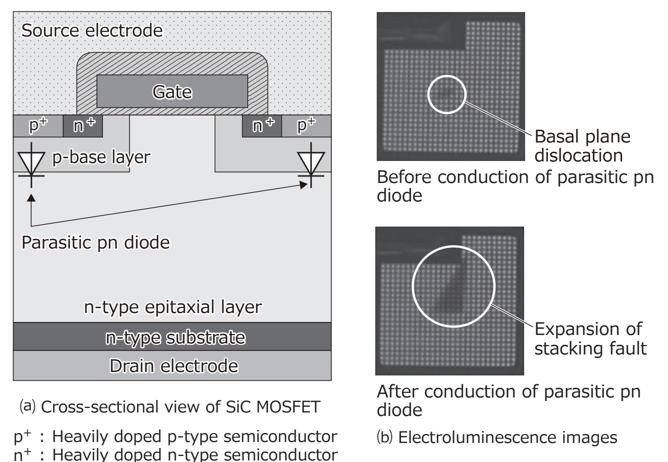


**Figure 1. Cross-sectional structure of SiC MOSFET and expansion of stacking fault caused by operation of parasitic pn diodes in SiC**—When the parasitic pn diode conducts, the stacking fault in the SiC MOSFET expands, causing degradation of its electrical characteristics.

©2022Toshiba Electronic Devices & Storage Corporation

# 2. Equivalent circuit models for an SBD-embedded SiC MOSFET

## 2.1 Conventional equivalent circuit model

**Figure 2** shows the conventional equivalent circuit model for an SBD-embedded MOSFET[1][2]. $V_k$ is Schottky voltage, $R_{JBS}$ is the junction barrier-controlled Schottky (JBS) resistance, and $R_{sp}$ is the spreading resistance. Letting A be the chip area, the $J_{umax}$ of this equivalent circuit is expressed as follows:

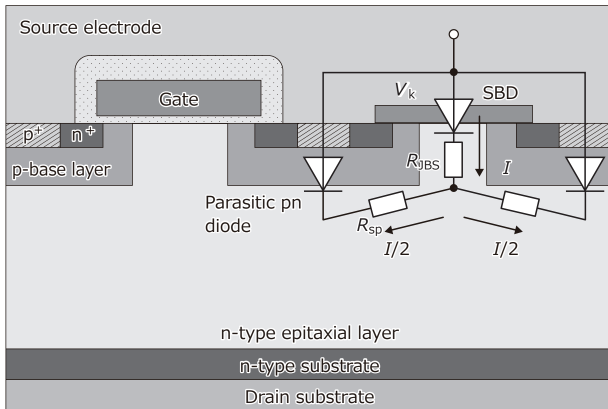


**Figure 2. Conventional equivalent circuit model of SBD-embedded SiC MOSFET**—This model is widely used for device design because it concisely represents the device parameters that determine $J_{umax}$.

$$J_{umax} = \frac{V_{on} - V_k}{R_{JBS} - R_{sp}/2} \cdot A^{-1}$$

where $V_{on}$ is the turn-on voltage of the parasitic pn diode. Equation 1 concisely expresses the device parameters that determine $J_{umax}$. It is therefore used as a guide for device design to increase $J_{umax}$. However, we have confirmed, as shown in **Figure 3**, that the result of this equation does not match the result of a calculation using technology computer-aided design (TCAD) and that of an experiment irrespective of the value of $R_d/(R_{JBS}+R_{sp})$, i.e., the ratio of resistance of the drift layer ($R_d$) to $R_{JBS}+R_{sp}$[3]. It was confirmed in advance that the result of the TCAD calculation closely matches that of the experiment.

To identify what is wrong with the conventional circuit model, we examined the current distribution inside the device using TCAD. **Figure 4**(a) shows the result of calculating the amount of current flowing under the p-base region in the horizontal direction ($J_x$). $J_x$ decreases at a constant slope toward the center of the device when $R_d/(R_{JBS}+R_{sp})$ is large whereas it decreases sharply at the end of the p-base when $R_d/(R_{JBS}+R_{sp})$ is small[3]. These results contradict the conventional equivalent circuit model that assumes all of the current flows to the drift layer via $R_{sp}$. As shown in Figure 4(b), the monotonic decrease of $J_x$ is presumably due to two causes: 1) symmetric device structure and 2) $R_d$ that is not negligibly small with respect to $R_{sp}$[3]. This indicates the need to take the current flowing to the drift layer into consideration regardless of the magnitude of $R_d$.

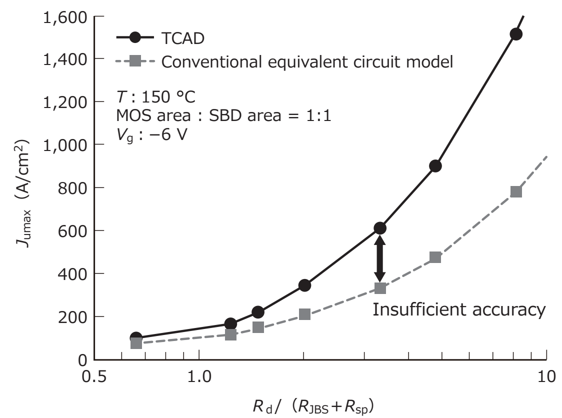


**Figure 3. $J_{umax}$ calculated using conventional equivalent circuit**—Since the $J_{umax}$ estimate obtained using the conventional equivalent circuit model is inaccurate, it can only be used for a limited range of devices.

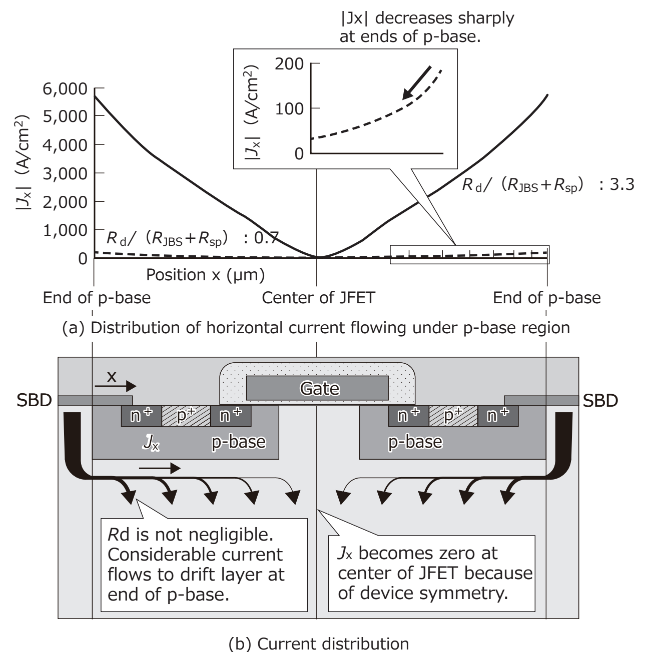


**Figure 4. Issues involved in conventional equivalent circuit**—$J_x$ decreases as it approaches the center of the junction field-effect transistor (JFET). The conventional equivalent circuit model does not take this effect into consideration.

©2022 Toshiba Electronic Devices & Storage Corporation

# 2.2 New equivalent circuit model and design guidelines for increasing $J_{umax}$

To take the current flowing to the drift layer into consideration, we have created a ladder circuit model shown in **Figure 5**. $N_{step}$ is the number of steps comprising the ladder circuit, $R_{dmos}$ is the resistance of the drift layer in the MOS region, and $R_{dsbd}$ is the resistance of the drift layer in the SBD region.

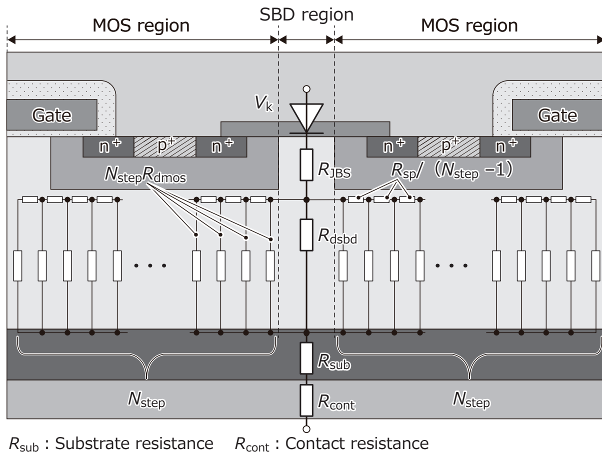


**Figure 5. Ladder circuit model of SBD-embedded SiC MOSFET**—We have created a new equivalent circuit model using a ladder circuit to evaluate the effect of the decrease in $J_x$.

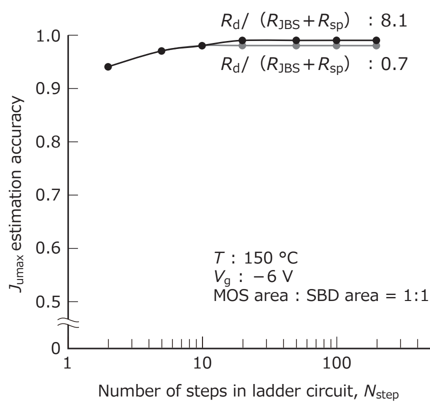


**Figure 6. Dependence of $J_{umax}$ prediction accuracy on number of steps of ladder circuit**—The ladder circuit allows accurate estimation of $J_{umax}$ regardless of the magnitude of $R_d/(R_{JBS}+R_{sp})$. Since the dependence of $J_{umax}$ on $N_{step}$ is slight, even a ladder circuit with an $N_{step}$ of 2 provides an accurate estimate.

We utilized this ladder circuit to calculate $J_{umax}$ to evaluate whether it matches the result of calculation using TCAD. **Figure 6** shows how the number of steps in the ladder circuit affects the matching accuracy.

Irrespective of $N_{step}$, the ladder circuit model provides a relative accuracy of more than 0.94 with respect to TCAD, much higher than the accuracy of less than 0.78 achieved by the conventional equivalent circuit model. The result obtained using the ladder circuit model closely matches the TCAD result regardless of the magnitude of $R_d$, indicating that $J_{umax}$ can be estimated accurately by taking the current flowing to the drift layer into consideration.

Figure 6 also indicates that reducing $N_{step}$ does not have a significant impact on the estimation of $J_{umax}$. Even a ladder circuit with an $N_{step}$ of 2 provides high $J_{umax}$ estimation accuracy[(3)].

A ladder circuit with an $N_{step}$ of 2 can be simply modeled as shown in **Figure 7**. In this case, $J_{umax}$ is expressed as follows:

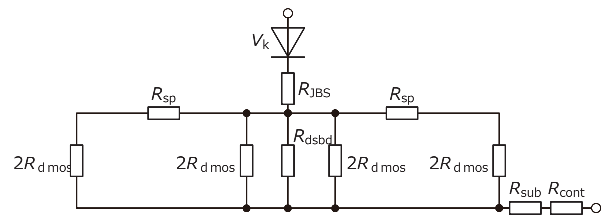


**Figure 7. Ladder circuit model for $J_{umax}$ when number of steps is 2**—Although the new equivalent circuit model for the SBD-embedded SiC MOSFET is simple, it provides high accuracy in the estimation of $J_{umax}$.

$$J_{umax} = \frac{(V_{on} - V_k)\cdot A^{-1}}{\left\{ R_{JBS} + \dfrac{R_{sp}}{4 + \dfrac{2R_{dmos}}{R_{dsbd}} + R_{sp}\cdot\left(\dfrac{1}{R_{dsbd}} + \dfrac{1}{R_{dmos}}\right)} \right\}}$$

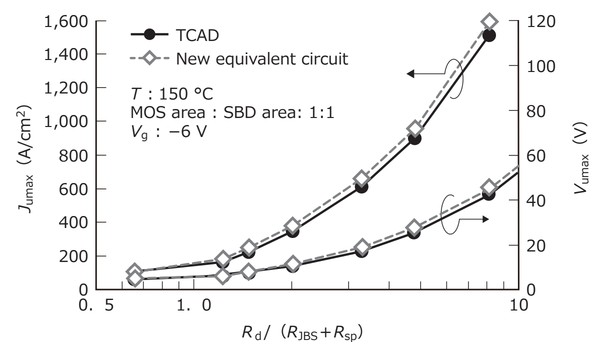


**Figure 8. Results of calculations of $J_{umax}$ and maximum voltage to clamp operation of parasitic pn diodes ($V_{umax}$) using ladder circuit model**—The new equivalent circuit model allows accurate estimation of not only $J_{umax}$ but also $V_{umax}$, the maximum voltage at which the parasitic pn diode does not conduct.

©2022 Toshiba Electronic Devices & Storage Corporation

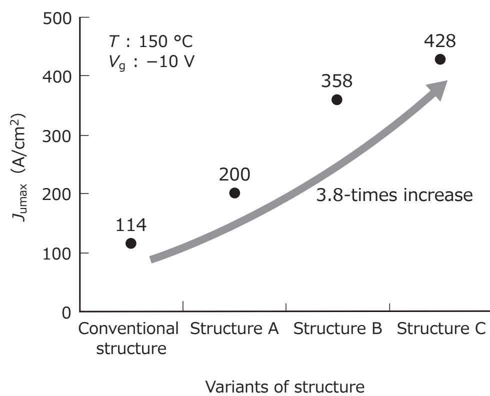


**Figure 9. Improvement of $J_{umax}$ of 3.3 kV prototype SBD-embedded SiC MOSFETs with newly designed structures**—SBD-embedded SiC MOSFETs with newly designed structures provide much higher $J_{umax}$ than the one with a conventional structure.

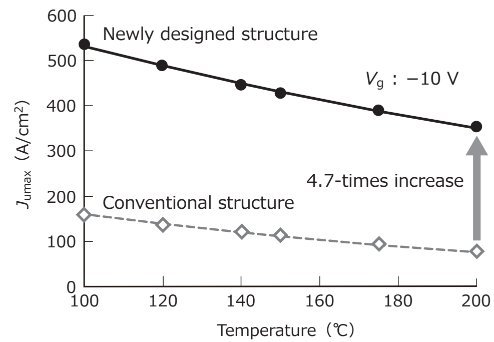


**Figure 10. Temperature dependence of $J_{umax}$ of prototype 3.3 kV SBD-embedded SiC MOSFET with newly designed structure**—The SBD-embedded SiC MOSFET with Structure C provides a 4.7—times higher $J_{umax}$ than the one with a conventional structure at 200°C.

Figure 7 is the newly developed equivalent circuit model for the SBD-embedded SiC MOSFET, and Equation 2 gives the value of $J_{umax}$ based on this circuit model(3). To identify the device parameters that determine $J_{umax}$ and derive guidelines for increasing $J_{umax}$, it is crucial to simplify an equivalent circuit model and a $J_{umax}$ equation as shown above.

We have evaluated whether the new equivalent circuit model provides $J_{umax}$ that matches the result of calculation using TCAD. **Figure 8** shows the dependence of $J_{umax}$ on $R_d/(R_{JBS}+R_{sp})$ as well as the results of calculations of the maximum voltage at which the parasitic pn diode does not conduct ($V_{umax}$). It indicates that both the $J_{umax}$ and $V_{umax}$ values obtained using the new equivalent circuit model match the results of TCAD closely.

Although the new equivalent circuit model and Equation 2 are simple, they provide an estimate of $J_{umax}$ that accurately matches the result of an experiment. Therefore, Equation 2 gives design guidelines for increasing $J_{umax}$. Specifically, to increase $J_{umax}$, it is important to: 1) reduce $R_{JBS}$ and $R_{sp}$ and 2) increase $R_{dmos}/R_{dsbd}$ and $1/R_d$.

# 3. Experiment on the $J_{umax}$ of 3.3 kV SBD-embedded SiC MOSFETs

Based on the derived design guidelines, we have experimentally verified the $J_{umax}$ of 3.3 kV prototype SBD-embedded SiC MOSFETs. **Figure 9** shows the $J_{umax}$ of these prototypes at 150°C. The SBD-embedded SiC MOSFET with a conventional structure has a $J_{umax}$ of 114 A/cm$^2$ whereas all the prototypes with newly designed structures provide considerably higher $J_{umax}$. In particular, the SBD-embedded SiC MOSFET with Structure C has achieved a $J_{umax}$ of 428 A/cm$^2$, 3.8-times higher than the one with a conventional structure(3). All the new structures provide a withstand voltage equivalent to that of the conventional structure. The increase in $J_{umax}$ without any trade-offs helps improve the reliability of SBD-embedded SiC MOSFETs.

Lastly, **Figure 10** compares the temperature dependence of $J_{umax}$ between the SBD-embedded SiC MOSFETs with Structure C and a conventional structure. The SBD-embedded SiC MOSFET with Structure C provides a $J_{umax}$ of 352 A/cm$^2$, 4.7-times higher than the one with a conventional structure(3). The substantial increase in $J_{umax}$ is a promising result toward the realization of an SBD-embedded SiC MOSFET with an operating temperature of 200°C or higher.

# 4. Conclusion

We have created a new equivalent circuit model for SBD-embedded SiC MOSFETs and derived device design guidelines for increasing $J_{umax}$ based on it. Based on these design guidelines, we have developed prototype devices and increased the $J_{umax}$ of 3.3 kV SBD-embedded SiC MOSFETs considerably. The increased $J_{umax}$ helps improve the high-temperature reliability of SBD-embedded SiC MOSFETs. We will continue to work on the development of SBD-embedded SiC MOSFETs capable of operating at a temperature exceeding 200°C.

©2022 Toshiba Electronic Devices & Storage Corporation

## References

(1) Furukawa, M. at el. 2020. “1.2 kV-Class SiC MOSFET Equipped with Embedded SBD for Improvement of Reliability.” Toshiba Review. 75 (6): 19–23. Accessed September 14, 2021. https://www.global.toshiba/content/dam/toshiba/migration/corp/techReviewAssets/tech/review/2020/06/75_06pdf/a05.pdf.

(2) Kawahara, K. et al. 2017. "6.5 kV schottky-barrier-diode-embedded SiC-MOSFET for compact full-unipolar module." Proceedings of 2017 International Symposium on Power Semiconductor Devices and IC's (ISPSD). Sapporo, 2017-05, IEEE: 41–44.

(3) Ohashi, T. et al. 2021. "Improved Clamping Capability of Parasitic Body Diode Utilizing New Equivalent Circuit Model of SBD-embedded SiC MOSFET." Proceedings of the 33rd International Symposium on Power Semiconductor Devices and IC’s (ISPSD 2021). Virtual Conference, 2021-05, IEEE: 79–82.

©2022 Toshiba Electronic Devices & Storage Corporation