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Analysis of Dependence of dV_{CE}/dt on Turn-off Characteristics with a 1200 V Double-gate IGBT

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Abstract

The double-gate drive is a remarkable gate control technique for dramatically reducing turn-off loss in Si-IGBTs by increasing dV_{CE}/dt. However, no detailed analysis of the relation between dV_{CE}/dt and the turn-off mechanism has been reported. The double-gate drive allows the dV_{CE}/dt of IGBTs to increase beyond the maximum dV_{CE}/dt of 7000 V/s in conventional gate drives.

1. Introduction

The limits of silicon have recently made it increasingly difficult to improve the performance of Si-IGBTs (Insulated Gate Bipolar Transistors) through modification of chip structures alone. Gate-control techniques have therefore attracted attention as a means to reduce energy loss throughout the system, including IGBTs and FRDs (Fast-Recovery Diodes). Double-gate (DG) IGBT technology is one such gate-control technique [1, 2]. The DG drive reduces energy loss by using a device with two gates controlled at different timings. According to these reports, increasing dV_{CE}/dt during turn-off reduces turn-off loss. However, no discussion of the relation between turn-off dV_{CE}/dt and turn-off losses in DG IGBTs has been reported. In this study, we therefore fabricated a DG IGBT and analyzed the dependence of dV_{CE}/dt on turn-off operations.

2. Device design and gate-drive method

We fabricated a 1200 V, 100 A DG IGBT (Fig. 1) having two gates—a main gate (MG) and a control gate (CG)—connected to separated gate pads. A dummy trench connected to the emitter electrode is formed between the MG and CG.

Figure 2 shows the timing chart of the gate drive during turn-off, and Fig. 3 shows a conceptual diagram of carrier movement during turn-off switching. Period 1 is the conducting state. V_{MGE} and V_{CGE} (voltage from the emitter to MG and CG) are 15 V. When –15V is applied to CG, the N channel formed along the CG disappears and a p channel is formed (period 2). Holes can then be easily drained through the p channel, regardless of the MG state. Further, the amount of stored carrier near the emitter side of the n-base layer becomes smaller. This causes the depletion region formed in the n-base layer to extend rapidly in period 3, increasing dV_{CE}/dt and shortening the turn-off time. The duration of period 2 is called the "turn-off delay time" (DT).

3. Results and discussion

We performed switching measurements using the fabricated DG IGBT. All measurements described below were performed at room temperature with a 600 V supply voltage (V_{CC}). Turn-off dV_{CE}/dt is defined as the rate of increase in V_{CE} from 50% to 90% of V_{CC}.

3.1 Gate resistance dependence of the turn-off dV_{CE}/dt

We confirmed gate resistance dependence (R_G) of turn-off characteristics by varying R_G from 3.9 to 82 Ω. Figure 4 shows the measured relation between R_G and dV_{CE}/dt, and Fig. 5 shows the measured relation between dV_{CE}/dt and turn-off loss. In the case of DT 0 µs, the MG and CG are simultaneously turned off. In this mode, operation of the DG IGBT is the same as that of a conventional IGBT having one gate. As R_G decreases, the value of dV_{CE}/dt increases, peaking at about 7000 V/µs when DT is 0 µs. However, dV_{CE}/dt can increase to about 12,000 V/µs at DT 5 µs. This increase in dV_{CE}/dt is what reduces turn-off loss. Compared with the case where dV_{CE}/dt is less than 7000 V/µs, higher turn-off loss is observed at DT 5 µs.

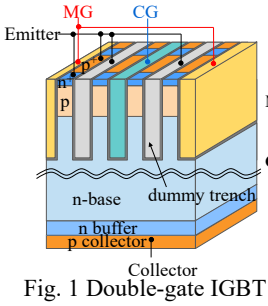


Fig. 1 Double-gate IGBT structure

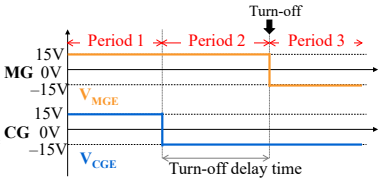


Fig. 2 Gate drive method during turn-off switching

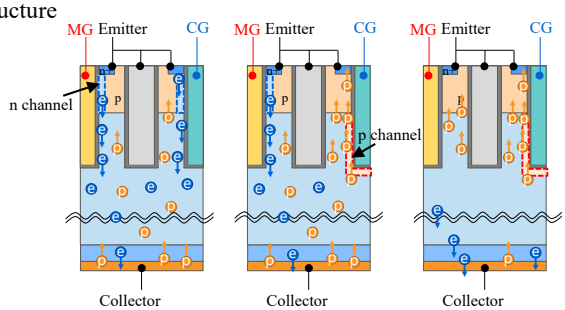


Fig. 3 Conceptual diagram during turn-off switching

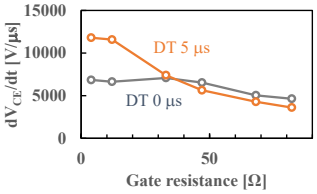


Fig. 4 Measured relations between gate resistance and dV_{CE}/dt

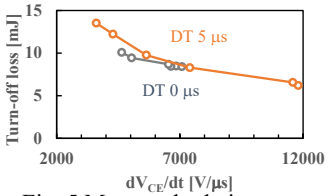


Fig. 5 Measured relations between dV_{CE}/dt and turn-off loss

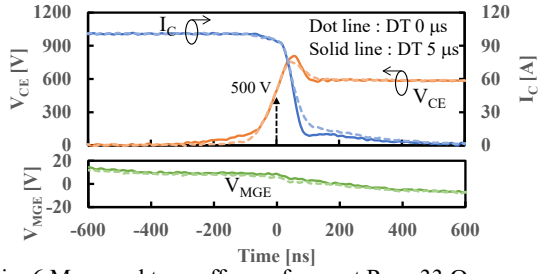


Fig. 6 Measured turn-off waveforms at R_G = 33 Ω

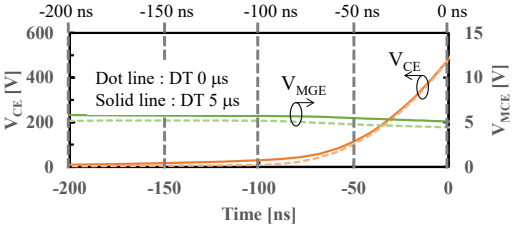
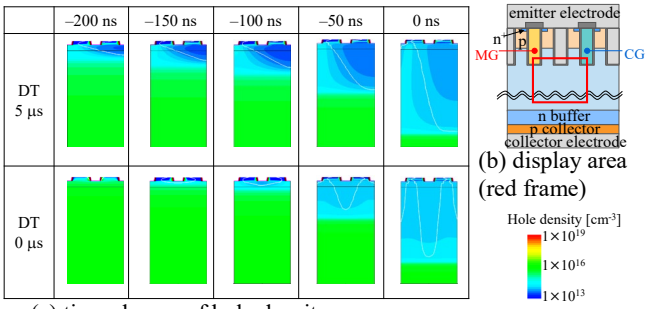


Fig. 7 Simulated turn-off waveforms at R_G = 33 Ω



(a) time change of hole density

(b) display area (red frame)

Fig. 8 Simulated hole density

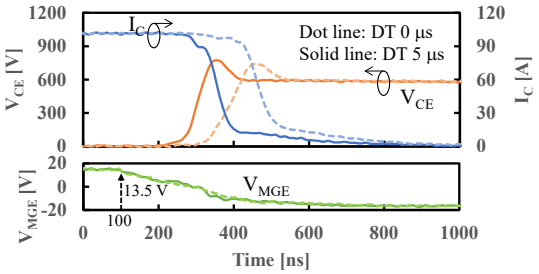


Fig. 9 Measured turn-off waveforms at R_G = 3.9 Ω

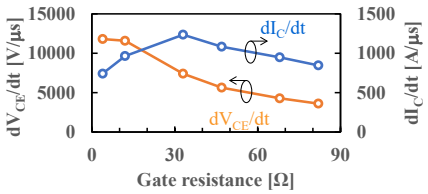


Fig. 10 Measured behavior of dI_C/dt and dV_{CE}/dt in turn-off at DT 5 µs

3.2 Turn-off characteristics with R_G = 33 Ω

When R_G is 33 Ω, dV_{CE}/dt at DT 0 µs and 5 µs is respectively 7100 V/µs and 7400 V/µs. Turn-off losses at DT 0 and 5 µs are nearly equal (8.4 and 8.3 mJ, respectively). Figure 6 shows turn-off waveforms when R_G = 33 Ω. In that figure, V_{CE} is 500 V at 0 ns on the time axis. When DT is 5 µs, step-up of V_{CE} is in a range of < 300 V. However, the corrector current I_C decreases more rapidly than at DT 0 µs, due to the rapid hole drain through the P channel along the CG.

We performed a TCAD simulation to analyze the phenomenon of V_{CE} step-up at low voltage. Figure 7 shows the simulated turn-off waveforms. In that figure, V_{CE} is 500 V at 0 ns. Figure 8 shows hole densities at 0, –50, –100, –150, and –200 ns in Fig. 7. In the case of DG drive at DT 5 µs, the stored carriers rapidly drain near the emitter side interface, mainly near CG. However, during that period V_{MGE} remains constant due to the Miller effect, so the n channel along MG does not disappear and electron injection continually occurs. Extension of the depletion region does not occur during this period, and V_{CE} change remains slow. The depletion region extends at almost the same speed at both DT 0 µs and 5 µs after the Miller period.

3.3 Turn-off characteristics with R_G = 3.9 Ω

Figure 9 shows turn-off waveforms when R_G = 3.9 Ω. In that figure, V_{MGE} is 13.5 V at 100 ns on the time axis. When R_G is 3.9 Ω, dV_{CE}/dt at DT 0 and 5 µs are 6800 and 11,800 V/µs. A clear effect of reduced turn-off loss by using a DG drive is observed at R_G = 3.9 Ω. Turn-off losses at DT 0 and 5 µs are 8.5 and 6.2 mJ, respectively. The reduction ratio of turn-off loss when using the DG drive is 27%, as in previous reports [1, 2].

Figure 10 shows measured R_G dependences of dV_{CE}/dt and dI_C/dt characteristics at DT 5 µs. Here, dI_C/dt is defined as the rate of decrease in I_C from 90% to 50%. As R_G decreases from 82 Ω, dV_{CE}/dt and dI_C/dt increase. dV_{CE}/dt increases until Rg = 3.9 Ω, though dI_C/dt reaches a maximum at 33 Ω. The region over which dV_{CE}/dt increases without increasing dI_C/dt is called the "semi-controllable region" [3]. This phenomena is caused by the reason that IGBT is bipolar device. Because hole injection occurs after electrons reach the collector electrode, hole current continuously flows for a while after electron injection stops. We found that dV_{CE}/dt increases of the DG IGBT occur in this semi-controllable region. Further, surge voltage caused by the product of parasitic inductance and dI_C/dt is also suppressed to low levels, despite the high dV_{CE}/dt.

4. Conclusion

We analyzed the dependence of dV_{CE}/dt on turn-off characteristics in a 1200 V DG IGBT. When dV_{CE}/dt is less than the maximum dV_{CE}/dt of a conventional gate drive, using a DG drive increased turn-off loss. The DG drive allowed dV_{CE}/dt of IGBT to increase beyond the maximum dV_{CE}/dt of the conventional gate-drive. Increases in dV_{CE}/dt by the DG IGBT occur in the semi-controllable region, while increases in dI_C/dt are limited.

References

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