Investigating the Highly Tolerant LDMOS Cell Array Design against the Negative Carrier Injection and the ESD Events

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Abstract—Optimum LDMOS array layout design is proposed which is tolerant against not only the negative carrier injection but also the ESD events. Both are indispensable features of the LDMOS, however, they have trade-off relation from cell array design point of view. Both characteristics are affected by N-guard ring resistance and its smaller value is better for negative carrier injection, but worse for ESD tolerance. The best structure in this study has increased allowable negative injection current by 40% compared to the reference structure, while TLP failure current ($I_{\text{f}}$) degradation was suppressed to only 9%, and total area increase was kept to less than 15%.

Keywords—LDMOS; cell array design; negative carrier injection; ESD events

I. INTRODUCTION

Tolerance against a negative carrier injection is an important characteristics of power ICs. When the negative carriers are injected into the switching devices (Injector) drain, parasitic bipolar transistor turns on and minority carriers are injected into the substrate, which results in undesirable influence on the surrounding devices (Sensor). To prevent the impact from the carrier injection, electrical device isolation by a deep trench and/or applying a heavy-doped substrate are effective, however, those are accompanied with process cost increase. As for a pn-junction isolation, to keep the device distance or to insert the N-guard ring ($N_{\text{gr}}$) between the devices both increase a chip size. Many studies have been done to analyze and model the minority carrier injection into substrate [1-2]. Nevertheless, few papers are found which analyze the LDMOS array layout design against a parasitic
bipolar transistor. In this study, the optimum LDMOS array layout design is proposed which is tolerant against not only negative carrier injection but also the ESD events, both are indispensable features of the LDMOS.

II. DEVICE STRUCTURES AND EXPERIMENT

Cross-sectional views of the studied structures are shown in Fig. 1. Parasitic bipolar transistor, Tr.C exists in N_{gr}-drain-shorted structure (Fig. 1(a)) and Tr.A/Tr.B/Tr.C are inherent in N_{gr}-drain-isolated structure (Fig. 1(b)). As for the drain-shorted structure, if the drain is biased negatively, the N_{gr} is biased simultaneously, so that both current are equivalent \( I_{d}\text{inj} = I_{n}\text{inj} \). Thus the defined \( \alpha \) \( (I_{s}\text{sen}/I_{d}\text{inj}) \) is equal to Tr.C’s \( \alpha \) \( (I_{s}\text{sen}/I_{n}\text{inj}) \). Here, lower \( \alpha \) results in higher tolerance against negative carrier injection. On the contrary, for the drain-isolated structure, Tr.A lies between drain and N_{gr}, so that \( \alpha \) is described as a product of Tr.C’s \( \alpha \) \( (I_{s}\text{sen}/I_{d}\text{inj}) \) and Tr.A’s \( \alpha \) \( (I_{n}\text{inj}/I_{d}\text{inj}) \), hence \( \alpha \) decreases drastically as shown in Fig. 2. It also indicates that wider N_{gr} decreases \( \alpha \) more due to Tr.B base width increase. In order to understand \( \alpha \) dependence on N_{gr} width in detail, 2D-TCAD simulation (Synopsys Sentaurus) was carried out (Fig. 3-5).

Fig. 2: Defined \( \alpha \) \( (=I_{s}\text{sen}/I_{d}\text{inj}) \) characteristics of drain-shorted, drain-isolated structure (N-guard ring = 7 μm), and drain-isolated structure with widen-N-guard ring (N-guard ring = 20 μm). Distance is defined in Fig. 1(a).

Fig. 3: Simulated curves of \( I_{s}\text{sub} \) vs. \( I_{d}\text{inj} \) of drain-isolated structures. N-guard ring widths are 7 μm and 20 μm. Distance is defined in Fig. 1(a).

Fig. 4: TCAD simulation results of eCurrent density distribution of drain-isolated structures. N-guard ring widths are 7 μm and 20 μm. Simulated conditions: \( I_{d}\text{inj} = -100 \mu \text{A}, -1 \text{mA}, -10 \text{mA}, V_{n}\text{inj} = V_{n}\text{sen} = V_{sub} = V_{n}\text{sen} = V_{d}\text{sen} = 0\text{V} \). Injector and sensor gates are omitted.

Fig. 5: 1D profiles of electrostatic potential of drain-isolated structures. N-guard ring widths are 7 μm and 20 μm. The profiles describe the electrostatic potential at dashed line in x-direction as shown in Fig. 4.
impact of $R_v$ and $R_{NBL}$, various LDMOS cell array layouts, shown in Fig. 6, are studied. When measuring the negative carrier injection, sensor device locates on the left of the injector devices. Fig. 7 shows measured $I_{neg}$ vs. $I_{inj}$ curve of a reference layout (No.1) and $I_d$ is defined as $-I_{neg}$ at $I_{neg} = 1 \mu A$. Larger $I_d$ indicates smaller $\alpha$ and leads to reduce the undesirable influence on the sensor device.

III. RESULTS AND DISCUSSIONS

A. Negative Carrier Injection

Negative carrier injection dependence on LDMOS array design layout was studied in Fig. 8. Even for the same cell size of 3600 cells, each layout shows different $I_d$. To understand the $I_d$ difference among the layouts, parameter focused on $R_{NBL}$ is investigated, which is the maximum area of divided array ($Area_{max}$). As shown in Fig. 9, there is a correlation between $I_d$ and $Area_{max}$. The larger $Area_{max}$ results in the higher $R_{NBL}$, thus the NBL potential shifts negative, which turns on $Tr.C$ easily and leads to $I_d$ decrease. Although in the same $Area_{max}$ case, some layouts show different $I_d$. For the further investigation, $Area_N$ ($N_{guard}$ area) dependence is evaluated as shown in Fig. 10. Smaller $Area_N$ results in higher $R_V$, which leads to $I_d$ decrease, because of the $N_{guard}$ potential negatively shifts. To describe the relationship between $I_d$ and cell array layout universally, "$N_{factor}$ ($Area_N/Area_{max}$)" is introduced. The smaller $N_{factor}$ corresponds to the larger total $N_{guard}$ resistance. Fig. 11 shows good correlation between $I_d$ and $N_{factor}$.

![Fig. 6: Measured LDMOS structures (3600 cell). Sensor is settled on the left side. Layout No.1 as a reference. N-guard ring widths are 7 μm (No.11), 15 μm (No.10), and 20 μm (the others); and No.7 has 40 μm-wide N-guard ring only at sensor side and the others have 20 μm.](image)

![Fig. 7: Measured curve of $Id_{neg}$ vs. $I_{neg}$ of reference layout No.1. Defined $Id$ as a current of $-Id_{neg}$ when $I_{neg} = 1 \mu A$.](image)

![Fig. 8: Dependence of $Id$ on various LDMOS cell array layouts.](image)

![Fig. 9: Dependence of $Id$ on $Area_{max}$ (maximum area of divided array). Even though the $Area_{max}$ of layout No.2, 9, 10, and 11 are equivalent, the $Id$ differs among the layouts.](image)

![Fig. 10: Dependence of $Id$ on $Area_N$ ($N_{guard}$ area). All structures have equivalent $Area_{max}$.](image)

![Fig. 11: Dependence of $Id$ on the $N_{factor}$ ($Area_N/Area_{max}$). Layout No.11 is the exception, which has a high resistance at $N$+GR/NBL connection with narrow $N_{guard}$.](image)
B. ESD Events

The LDMOS also requires ESD tolerance, thus TLP measurement is studied as well (Fig. 12). As shown in Fig. 13, the TLP failure current, $I_{T2}$, tends to decrease as $N_{factor}$ increases. Layout No.8 and 6 are the exceptions due to unbalanced division of the device array that accompanies with local current concentration. In the drain-isolated structure case, $N_{gr}$ is open state during the TLP test, however, $N_{gr}$ voltage ($V_{n}$) influences the $Tr.E$ (parasitic bipolar transistor) action [3]. Fig. 14 shows $I_{T2}$ dependence on $V_{n}$ evaluated for similar layout No.2 and 10. When the $V_{n}=-0.3\,\text{V}/0\,\text{V}$, both layouts show low $I_{T2}$ owing to $Tr.E$ action, which turns on when $V_{n} < V_{c}$. As for $V_{n} = 5\,\text{V}$, high $I_{T2}$ value achieved because $Tr.E$ does not turn on. It is noted that $I_{T2}$ depends on the layout in the $N_{gr}$=open condition (actual TLP condition). Layout No.10 keeps the same $I_{T2}$ as $V_{n} = 5\,\text{V}$ case, although layout No.2 shows $I_{T2}$, which is as low as $V_{n} = -0.3\,\text{V}/0\,\text{V}$ case.

V case. It is considered that $N_{gr}$ resistance is high enough in No.10 to shift $V_{n}$ positive, so that the $Tr.E$ does not turn on and $I_{T2}$ remains higher. Lower $N_{gr}$ resistance (higher $N_{factor}$) is better for $I_{T2}$, though $I_{T2}$ has an inflection point. In conclusion, totally considering the $Id$, $I_{T2}$, and total area as shown in Fig. 15, layout No.10 is a suitable structure for injector, which has the sufficient tolerance against both the negative carrier injection and the ESD events, which achieving minimum total area increase. Therefore, the LDMOS cell array layout has to be carefully designed by taking $N_{factor}$ into consideration. In this study, new parameter $N_{factor}$ is introduced and the suitable LDMOS cell array layout is proposed, which can realize the high tolerance against the negative carrier injection and the ESD events.

IV. CONCLUSIONS
Optimum LDMOS array layout design is proposed which is tolerant against not only the negative carrier injection but also the ESD events. Both are indispensable features of the LDMOS, however, they have trade-off relation from cell array design point of view. Both characteristics are affected by N-guard ring resistance and its smaller value is better for negative carrier injection, but worse for ESD tolerance. In this study, suitable layout has been proposed, which has increased allowable negative injection current by 40% compared to the reference structure, while TLP failure current degradation was suppressed to only 9%, and total area increase was kept to less than 15%.

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