K. Komatsu *et al.*, "Investigating the Highly Tolerant LDMOS Cell Array Design against the Negative Carrier Injection and the ESD Events," *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 2020*, pp. 404-407, doi: 10.1109/ISPSD46842.2020.9170188

Investigating the Highly Tolerant LDMOS Cell Array Design against the Negative Carrier Injection and the ESD Events

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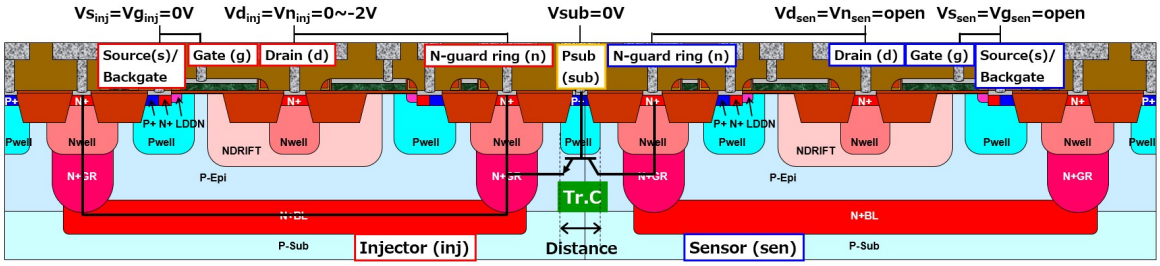
***Abstract*—Optimum LDMOS array layout design is proposed which is tolerant against not only the negative carrier injection but also the ESD events. Both are indispensable features of the LDMOS, however, they have trade-off relation from cell array design point of view. Both characteristics are affected by N-guard ring resistance and its smaller value is better for negative carrier injection, but worse for ESD tolerance. The best structure in this study has increased allowable negative injection current by 40% compared to the reference structure, while TLP failure current (It_2) degradation was suppressed to only 9%, and total area increase was kept to less than 15%.**

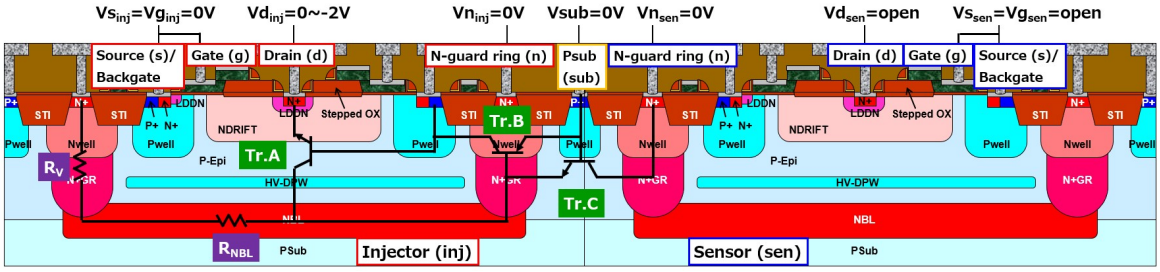
Keywords—LDMOS; cell array design; negative carrier injection; ESD events

I. INTRODUCTION

Tolerance against a negative carrier injection is an important characteristics of power ICs. When the negative carriers are injected into the switching devices (Injector) drain, parasitic bipolar transistor turns on and minority carriers are injected into the



(a) N-guard ring-drain shorted structure



(b) N-guard ring-drain isolated structure

Fig. 1: Cross-sectional views of (a) drain-shorted structure and (b) drain-isolated structure of 18V NchLDMOS. Measurement conditions of negative carrier injection are shown in the figure. Parasitic bipolar transistors, *Tr.C* and *Tr.A/Tr.B/Tr.C* exist in each structure. N-guard ring related resistors, R_v and R_{NBL}. Definition is as follows, $\alpha = In_{sen}/Id_{inj}$, $\alpha_A = In_{inj}/Id_{inj}$, *and* $\alpha_C = In_{sen}/In_{inj}$.

substrate, which results in undesirable influence on the surrounding devices (Sensor). To prevent the impact from the carrier injection, electrical device isolation by a deep trench and/or applying a heavy-doped substrate are effective, however, those are accompanied with process cost increase. As for a pn-junction isolation, to keep the device distance or to insert the N-guard ring (N_{gr}) between the devices both increase a chip size. Many studies have been done to analyze and model the minority carrier injection into substrate [1-2]. Nevertheless, few papers are found which analyze the LDMOS array layout design against a parasitic

bipolar transistor. In this study, the optimum LDMOS array layout design is proposed which is tolerant against not only negative carrier injection but also the ESD events, both are indispensable features of the LDMOS.

II. Device Structures and Experiment

Cross-sectional views of the studied structures are shown in Fig. 1. Parasitic bipolar transistor, *Tr.C* exists in N_{gr}-drain-shorted structure (Fig. 1(a)) and *Tr.A*/*Tr.B*/*Tr.C* are inherent in N_{gr}-drain-isolated structure (Fig. 1(b)). As for the drain-shorted structure, if the drain is biased negatively, the N_{gr} is biased simultaneously, so that both current are equivalent ($Id_{inj} = In_{inj}$). Thus the defined α (In_{sen}/Id_{inj}) is equal to *Tr.C*'s α_C (In_{sen}/In_{inj}). Here, lower α results in higher tolerance against negative carrier injection. On the contrary, for the drain-isolated structure, *Tr.A* lies between drain and N_{gr}, so that α is described as a product of α_C and *Tr.A*'s α_A (In_{inj}/Id_{inj}), hence α decreases drastically as shown in Fig. 2. It also indicates that wider N_{gr} decreases α more due to *Tr.B* base width increase. In order to understand α dependence on N_{gr} width in detail, 2D-TCAD simulation (Synopsys Sentaurus) was carried out (Fig. 3-5). Fig. 3 shows that *Isub* of N_{gr} =7 μm case is 2 to 6 order of magnitude larger than N_{gr} = 20 μm case at the same Id_{inj}. Fig. 4 is the eCurrent density distributions. At Id_{inj} = -100 μA, electron flows from Injector N_{gr} to Injector drain in both N_{gr} width cases. As the Id_{inj} increases, the electron from Sensor N_{gr} starts to flow to Injector N_{gr}. This phenomenon was observed above Id_{inj} = -1 mA in N_{gr} =7 μm case and -10 mA in N_{gr} =20 μm case. Fig. 5 shows the 1D profiles of the electrostatic potential of both structures. The voltage difference between Injector N_{gr} and P-substrate is always smaller in N_{gr} =7 μm case compared to 20 μm case, and the N_{gr}/P-substrate junction becomes forward-biased in N_{gr} =7 μm case and emits minority carrier (electron) into the substrate, which behavior is not observed in N_{gr} = 20 μm case (Fig. 4). This different behavior is due to the N_{gr} resistance difference. The resistance of N_{gr} =7 μm case is larger than 20 μm case so that the N_{gr} voltage easily drops when electron flows inside the N_{gr}. Therefore, it is assumed that the parameter R_v (N_{gr} vertical resistance) has a relation with α. Moreover, R_{NBL}, which is related to LDMOS's array size, also affects α. To analyze the

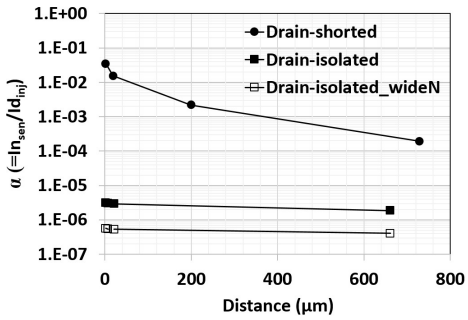


Fig. 2: Defined α (=In_{sen}/Id_{inj}) characteristics of drain-shorted, drain-isolated structure (N-guard ring = 7 μm), and drain-isolated structure with widen-N-guard ring (N-guard ring = 20 μm). Distance is defined in Fig. 1(a).

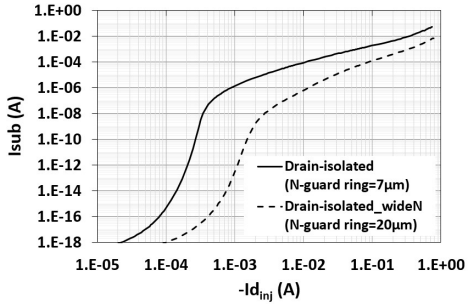


Fig. 3: Simulated curves of *Isub* vs. Id_{inj} of drain-isolated structures. N-guard ring widths are 7 μm and 20 μm. Simulated conditions: Id_{inj} =-1x10^{-5} A ~ -1 A, $Vs_{inj} = Vn_{inj} = Vsub = Vn_{sen} = Vs_{sen} = Vd_{sen}$ = 0V. Injector and sensor gates are omitted.

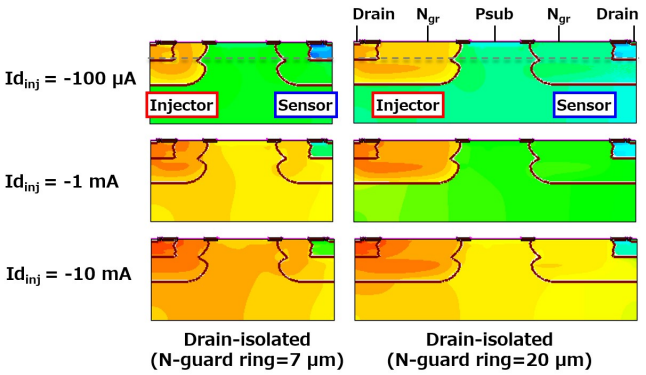
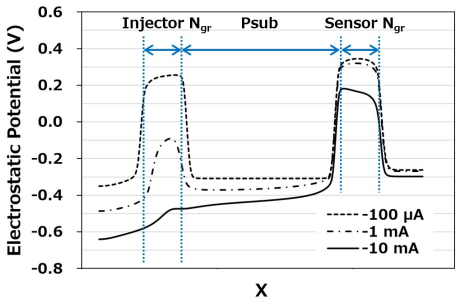
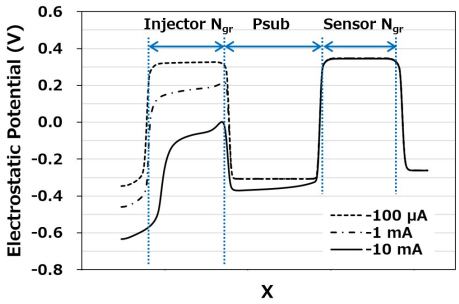


Fig. 4: TCAD simulation results of eCurrent density distribution of drain-isolated structures. N-guard ring widths are 7 μm and 20 μm. Simulated conditions: Id_{inj} = -100 μA, -1 mA, and -10 mA, $Vs_{inj} = Vn_{inj} = Vsub = Vn_{sen} = Vs_{sen} = Vd_{sen}$ = 0V. Injector and sensor gates are omitted.



(a) Drain-isolated structure (N-guard ring = 7 μm)



(b) Drain-isolated structure (N-guard ring = 20 μm)

Fig. 5: 1D profiles of electrostatic potential of drain-isolated structures. N-guard ring widths: (a) 7 μm and (b) 20 μm. The profiles describe the electrostatic potential at dashed line in x-direction as shown in Fig. 4.

impact of R_v and R_{NBL}, various LDMOS cell array layouts, shown in Fig. 6, are studied. When measuring the negative carrier injection, sensor device locates on the left of the injector devices. Fig. 7 shows measured In_{sen} vs. Id_{inj} curve of a reference layout (No.1) and Id_i is defined as $-Id_{inj}$ at In_{sen} =1 μA. Larger Id_i indicates smaller α and leads to reduce the undesirable influence on the sensor device.

III. Results and Discussions

A. Negative Carrier Injection

Negative carrier injection dependence on LDMOS array design layout was studied in Fig. 8. Even for the same cell size of 3600 cells, each layout shows different Id_i. To understand the Id_i difference among the layouts, parameter focused on R_{NBL} is investigated, which is the maximum area of divided array ($Area_{max}$). As shown in Fig. 9, there is a correlation between Id_i and $Area_{max}$. The larger $Area_{max}$ results in the higher R_{NBL}, thus the NBL potential shifts negative, which turns on *Tr.C* easily and leads to Id_i decrease. Although in the same $Area_{max}$ case, some layouts show different Id_i. For the further investigation, $Area_N$ (N_{gr} area) dependence is evaluated as shown in Fig. 10. Smaller Ar the be (A the be hig na

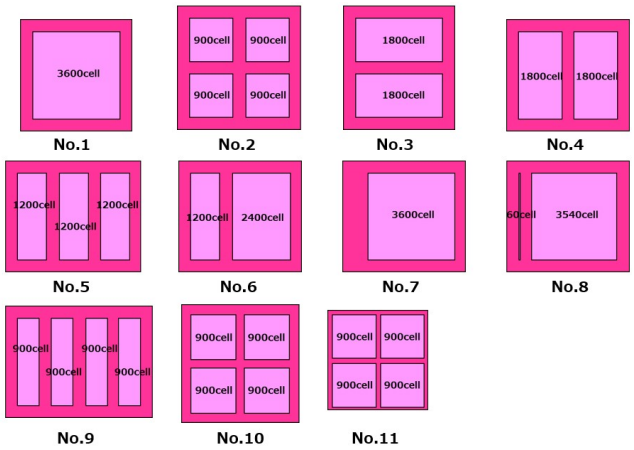


Fig. 6: Measured LDMOS structures (3600 cell). Sensor is settled on the left side. Layout No.1 as a reference. N-guard ring widths are 7 μm (No.11), 15 μm (No.10), and 20 μm (the others); and No.7 has 40 μm -wide N-guard ring only at sensor side and the others have 20 μm.

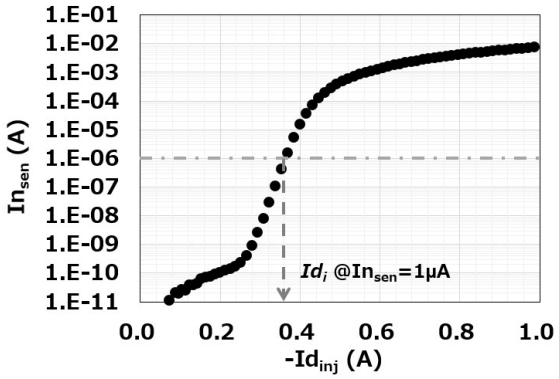


Fig. 7: Measured curve of Id_{inj} vs. In_{sen} of reference layout No.1. Defined Id_i as a current of $-Id_{inj}$ when In_{sen}=1 μA.

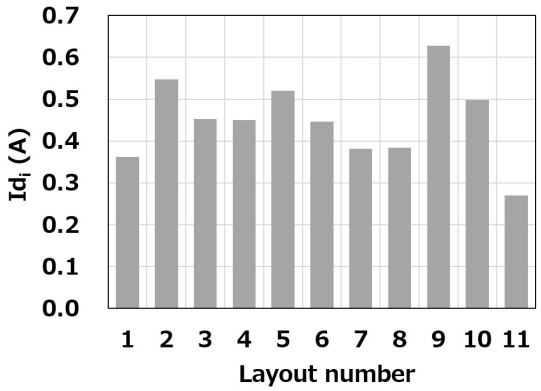


Fig. 8: Dependence of Id_i on various LDMOS cell array layouts.

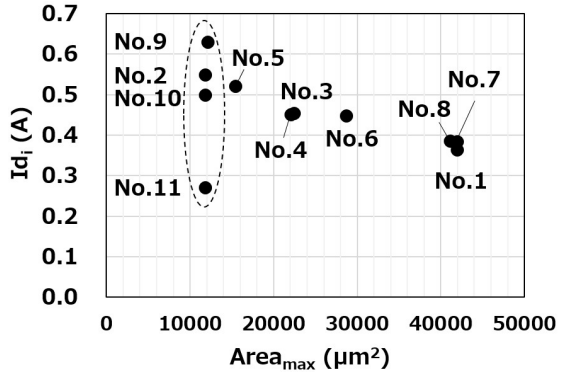


Fig. 9: Dependence of Id_i on $Area_{max}$ (maximum area of divided array). Even though the $Area_{max}$ of layout No.2, 9, 10, and 11 are equivalent, the Id_i differs among the layouts.

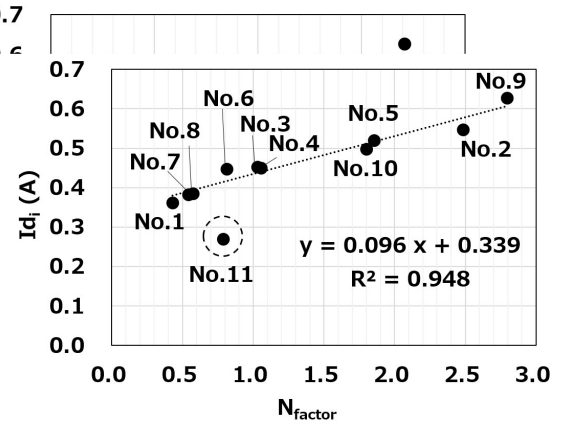


Fig. equiv

Fig. 11: Dependence of Id_i on the N_{factor} ($Area_N/Area_{max}$). Layout No.11 is the exception, which has a high resistance at N+GR/NBL connection with narrow N_{gr}.

B. ESD Events

The LDMOS also requires ESD tolerance, thus TLP measurement is studied as well (Fig. 12). As shown in Fig. 13, the TLP failure current, It_2, tends to decrease as N_{factor} increases. Layout No.8 and 6 are the exceptions due to unbalanced division of the device array that accompanies with local current concentration. In the drain-isolated structure case, N_{gr} is open state during the TLP test, however, N_{gr} voltage (V_n) influences the *Tr.E* (parasitic bipolar transistor) action [3]. Fig. 14 shows It_2 dependence on V_n evaluated for similar layout No.2 and 10. When the V_n =-0.3 V/0 V, both layouts show low It_2 owing to *Tr.E* action, which turns on when V_n<V_s. As for V_n =5 V, high It_2 value achieved because *Tr.E* does not turn on. It is noted that It_2 depends on the layout in the N_{gr}=open condition (actual TLP condition). Layout No.10 keeps the same It_2 as V_n =5 V case, although layout No.2 shows It_2, which is as low as V_n = -0.3 V/0 V case. It is considered that N_{gr} resistance is high enough in No.10 to shift V_n positive, so that the *Tr.E* does not turn on and It_2 remains higher. Lower N_{gr} resistance (higher N_{factor}) is better for Id_i, though It_2 has an inflection point. In conclusion, totally considering the Id_i, It_2, and total area as shown in Fig. 15, layout No.10 is a suitable structure for injector, which has the sufficient tolerance against both the negative carrier injection and the ESD events, which achieving minimum total area increase. Therefore, the LDMOS cell array layout has to be carefully designed by taking N_{factor} into consideration. In this study, new parameter N_{factor} is introduced and the suitable LDMOS cell array layout is proposed, which can realize the high tolerance against the negative carrier injection and the ESD events.

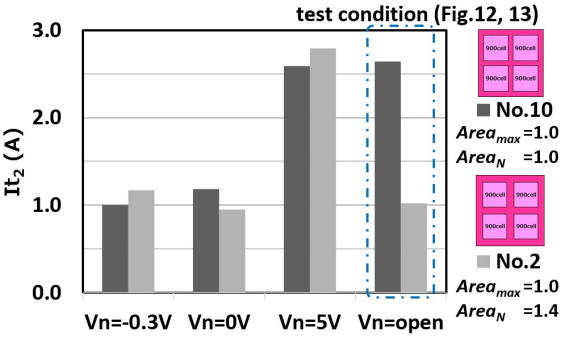


Fig. 14: It_2 comparison of layout No.10 and No.2, with modifying N_{gr} voltage (V_n) under TLP test. Both layouts have same $Area_{max}$ and different $Area_N$. V_n= -0.3V/0V/5V and open (actual TLP condition).

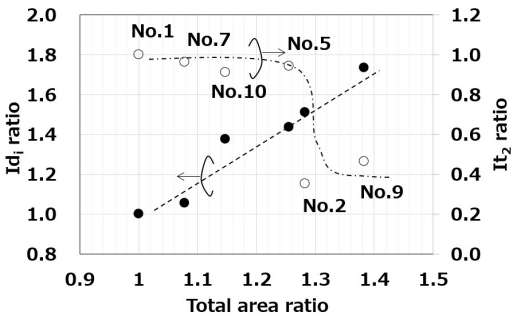


Fig. 15: Dependence of Id_i ratio and It_2 ratio on total area ratio. Both values are normalized by the value of No.1 as a reference.

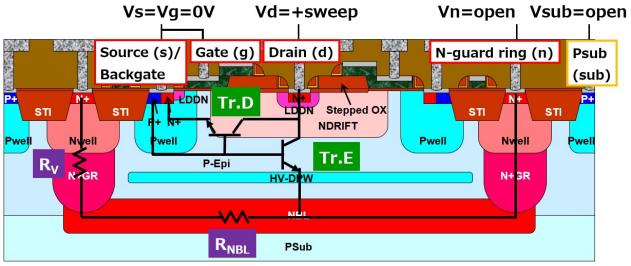


Fig. 12: Cross-sectional view of the drain-isolated 18V NchLDMOS. Measurement condition of TLP (pulse=100 ns). Parasitic bipolar transistors, *Tr.D* and *Tr.E* exist.

IV. CONCLUSIONS

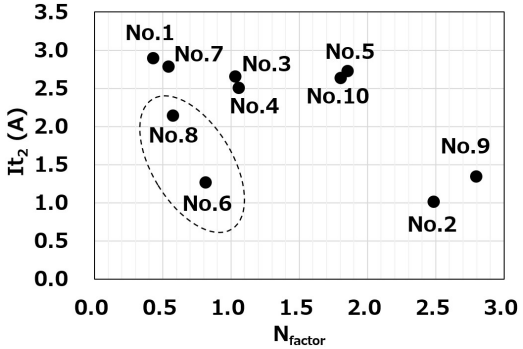


Fig. 13: Dependence of It_2 on N_{factor}. Layout No.8 and 6 are the exceptions due to unbalanced division of the device array that accompanies with local current concentration.

Optimum LDMOS array layout design is proposed which is tolerant against not only the negative carrier injection but also the ESD events. Both are indispensable features of the LDMOS, however, they have trade-off relation from cell array design point of view. Both characteristics are affected by N-guard ring resistance and its smaller value is better for negative carrier injection, but worse for ESD tolerance. In this study, suitable layout has been proposed, which has increased allowable negative injection current by 40% compared to the reference structure, while TLP failure current degradation was suppressed to only 9%, and total area increase was kept to less than 15%.

ACKNOWLEDGMENT

The authors would like to thank Dr. Kenya Kobayashi for his continuous encouragement and valuable support. The authors also express the deepest appreciation to the members of Japan Semiconductor Corporation for their continuous support of wafer production for this study.

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