Semiconductor Packaging and Assembly Technologies Supporting Evolution of Various Devices

Almost all appliances and systems that support everyday life in various spheres, including home appliances and information, industrial, medical, and transportation systems, contain semiconductor chips. The progress of packaging and assembly technologies for semiconductor chips and other electronic components is attracting a lot of attention. Drawing on the packaging and assembly technologies accumulated since the inception of the semiconductor industry, Toshiba has developed a broad range of products, including a package for large-capacity memory, a thermally enhanced small and lightweight IC, a sensing device designed for the Internet of Things (IoT), and other innovative products. We will continually improve our packaging and assembly technologies to address the needs of IoT and the information explosion.

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Foreword

Continuously Evolving Toshiba Semiconductor Packaging and Assembly Technologies

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Due to various technological innovations, everyday life is becoming better and more convenient. Almost all appliances and systems that support us in various areas, including home appliances, and information, industrial, medical and transportation systems, contain semiconductor chips. It is no exaggeration to say that small semiconductor chips are helping us lead satisfying and convenient lives.

In these circumstances, the progress of packaging and assembly technologies for semiconductor chips and other electronic components are taking on added importance. So far, the scaling of process technologies has enabled the progress of semiconductor chips, but it is expected to reach its limit in the near future. Therefore, semiconductor packaging and assembly technologies are attracting more attention as a driving force to further reduce the cost, enhance the functionality and improve the performance of semiconductor applications without relying on only device scaling. This is essential to address the needs of the Internet of Things (IoT) and exploding volumes of information.

Semiconductor packaging and assembly embrace various technologies such as material, surface treatment, bonding, electromagnetic characteristics, three-dimensional (3D) chip stacking, thermal dissipation, part integration, circuit implementation design and stress analysis and evaluation, to name just a few. In order to create more convenient products, it is necessary to improve and combine individual key technologies.

Mannen Jimeishou (a masterpiece of traditional Japanese horology) and a *karakuri* (mechanical) doll invented by Toshiba's founder, Hisashige Tanaka, were made using the very essence of the latest technologies available at that time. The wellspring of Toshiba's creativity has continued throughout the company's history since its founding. Toshiba's semiconductor business began in the 1950s and the company has since improved its semiconductor technologies as the business flourished. Drawing on semiconductor packaging and assembly technologies that are the fruits of decades of experience, we will continue to spur technological innovation and develop new products.

The SPECIAL REPORTS introduce hot technologies such as the electromagnetic compatibility (EMC) evaluation and a simulation technology in semiconductor design, and electromagnetic interference (EMI) shielding for semiconductor packages, as well as innovations supported by proven technologies such as a multi-die packaging solution for large-capacity memory, a thermally enhanced small and lightweight power amplifier IC and an environment sensing logger designed for IoT applications. These are just a few examples of the technological innovations achieved by Toshiba. I hope that you will find the SPECIAL REPORTS useful.

Trend

Toshiba's Progress in Developing Semiconductor Packages and Approaches to Packaging Technologies

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Toshiba has been continuously developing various types of semiconductor packages in response to the miniaturization of semiconductor devices supporting the advancement of electronic devices since the 1980s, including stacked-die packages for memory devices to achieve larger capacity, compact packages with high reliability to meet the increasing demand for electronics in automobiles, and ultra-small packages for information and communication devices to achieve lighter weight, thinner profile, and smaller size. These packages are contributing to the enhancement of performance and downsizing of electronic devices according to their applications.

In line with the ongoing evolution of the information society, we are continuing our efforts to realize smaller and more sophisticated semiconductor packages applying our cutting-edge packaging technologies with the need for semiconductor miniaturization technologies as a leading company in this field.

Toshiba's semiconductor package development

Electronic devices contain printed circuit boards on which various electronic components are soldered. Semiconductor chips are not mounted on printed circuit boards in bare form; instead, they are housed in a semiconductor package for protection. Semiconductor packages protect electronic circuitry from the external environment, provide electrical and mechanical connections with printed circuit boards, and dissipate heat generated by semiconductor devices.

Toshiba has provided various types of semiconductor packages to meet the evolving needs of electronic equipment, including high-pin-count, low-profile, and stacked-die packages (**Figure 1**)[(1)-(3)]. The following subsections briefly describe the changes in package styles since the 1980s.

In the1980s — Transition from through-hole packages to surface-mount packages

In 1985, we released laptop PCs that were dramatically smaller than the conventional desktop PCs. The mid-

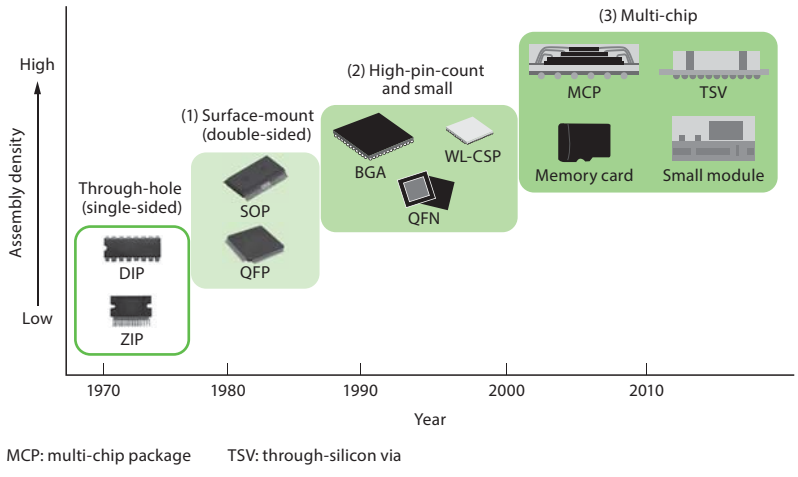

Figure 1. Trends in Toshiba high-density packages.
Package styles have evolved from the earlier through-hole packages to the latest multi-chip packages.

1980s saw rapid progress in the scaling of digital home appliances; small electronic devices such as portable CD players and handheld camcorders appeared on the market. Semiconductor packages that provide interconnections between electrical components and a printed circuit board made a significant contribution to reducing the size of these digital home appliances.

The initial semiconductor packages were through-hole packages mounted on one side of a printed circuit board, such as dual-in-line packages (DIPs) and zigzag-in-line packages (ZIPs).

As smaller and lighter packages appeared in the 1980s, we worked on the development of surface-mount technology and released various types of surface-mount packages that can be placed on both sides of a printed circuit board, including small outline packages (SOPs) and quad flat packages (QFPs).

In the late 1980s, we endeavored to further reduce the size and weight of semiconductor packages. As a result, we developed thin quad flat packages (TQFPs) and thin small-outline packages (TSOP) with a thickness of 1 mm, contributing to the reduction in size and weight of electronic devices.

In the 1990s — Transition from perimeter-leaded packages to area array packages

As downscaling of digital home appliances further advanced, digital cameras, portable MiniDisc players and cell phones appeared in the 1990s. SOPs and QFPs were standardized and became commodity packages. In response, we endeavored to develop technology for smaller surface-mount packages in order to increase board utilization. We developed ball grid arrays (BGAs) by using a printed circuit board as a package substrate, instead of a metal leadframe made of 42 alloy (*1) or copper, in order to place interconnection terminals across the bottom surface of the package as well as wafer-level chip scale packages (WL-CSPs) that place interconnection terminals across the chip surface during the front-end semiconductor process without using a package substrate. The size of a WL-CSP is very close to the size of the semiconductor chip. Furthermore, we released a variant of BGAs called fine-pitch ball grid arrays (FBGAs) with a ball pitch of 0.8 mm or less.

Around this time, we also developed smaller leadframe-based packages called quad flat non-leaded (QFN) packages.

After 2000 — Chip stacking and environmental considerations

As mobile devices using flash memory such as digital audio players, camera phones, smartphones, and tablets became popular in the 2000s, semiconductor packages became smaller and thinner at an accelerating pace. Furthermore, demand for three-dimensional (3D) chip stack technology increased to stack multiple chips in a package in order to further improve board utilization. In the 2000s, the industry worked to reduce the 2D footprint areas and shift to 3D assembly simultaneously.

We developed semiconductor packages in which memory and other chips are vertically stacked.

Furthermore, in response to the requirements of the Restriction of Hazardous Substances Directive (RoHS) and environmental concerns, we developed packages free of lead (Pb) and flame-retardant mold resin containing bromine and antimony compounds(*2) while maintaining the capability to withstand high soldering temperatures.

Changes to packaging requirements and technology development

The following subsections describe how the requirements for semiconductor packages changed according to the progress of electronic products in five fields: data storage, automotive, communication, general-purpose and new fields (**Table 1**).

Data storage devices

• Technologies to reduce size and increase storage capacity

In recent years, portable storage devices have transitioned to the use of memory cards using NAND flash memory instead of optical and magnetic disks such as compact discs (CDs) and hard disk drives (HDDs). For example, an early generation of an 8-Mbyte Secure Digital (SD) card consisting of one controller chip and one memory chip was 2.1 mm thick. A recent 128-Mbyte SD card consisting of one controller chip and eight memory chips is 1 mm thick. The capacities of storage devices in PCs and smartphones have also been increasing, spurring the need for thin packages in which multiple high-capacity memory chips are stacked (**Figure 2**).

A key enabler for these packages is a chip stacking technology to house many chips in a limited space. Although stacking more chips in thinner packages is required, reducing the chip thickness is not enough. It is necessary to grasp, both theoretically and empirically, the lower limit to the thickness of a chip to maintain proper operation and develop the following technologies to handle thin chips throughout the entire package assembly process (**see Column**).

(1) Dicing-before-grinding (DBG) technology
When a wafer is ground thin, it is subject to warpage due to residual stress induced during the for-

(*1) Nickel-iron alloy

(*2) In accordance with the definitions of "containing" stipulated in individual laws and regulations

Table 1. Changes in packages according to each application.

Item	Storage devices	Automobiles	Communication devices	General-purpose applications	New fields
Changes in applications	**Smaller size, higher speed, increased capacity** Migration from optical and magnetic disks such as CDs and HDDs to flash memory-based devices such as SD cards and SSDs	**Electrification** Prevalence of HEVs and EVs Increasing electrification of automobiles (e.g., ADAS)	**Smaller size, higher performance** Prevalence of smartphones Higher performance, smaller size, lower profile, higher speed, longer battery life	**Lower cost, smaller size** Requirements common to electronic devices, general home appliances and industrial equipment	**IoT** Internet connection of a very large number of devices
Package development	**Multi-chip stacking** Smaller size, higher memory capacity **Adoption of TSV technology** Performance improvement through 3D chip stacking	**Smaller size, higher heat resistance, noise-tolerant** Reliability in high-temperature environment of engine compartment, thermally enhanced small packages Establishment of EMC test environment	**Smaller modules** 3D packages EMI-shielding	**High-efficiency production, smaller size** Leadframe-based high-efficiency production COC technology	**Lower power, SiP** Integration of multiple chips in one package such as sensors, controllers, wireless communication chips

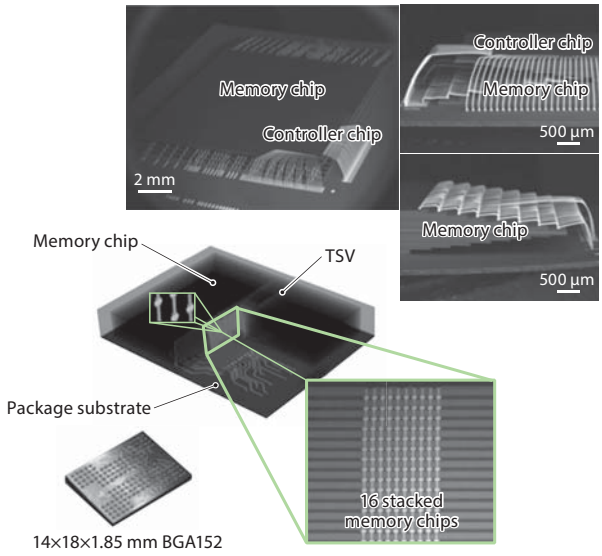

Figure 2. Packaging technologies for memories.
Memory capacities and speeds can be increased by stacking multiple chips vertically.

mation of the device circuitry. In addition, semiconductor chips could suffer nicks along their perimeter when wafers are singulated (diced) into individual chips. These nicks could then expand into full-blown cracks, considerably reducing manufacturing yields. In order to solve these problems, we developed a technology to perform half-cut dicing before wafer backgrinding and subsequent chip singulation.

(2) Wire bonding technology
The stacked chips and the package substrate are electrically interconnected using metal wires with a diameter of roughly 20 µm Since thin chips are vulnerable to nicks due to the load applied during wire bonding, the wire interconnect strength is secured by fine-controlling the bonding loads and ultrasound. Furthermore, in order to prevent bonding wires with complicated shapes from touching each other, we perform a simulation in advance to examine the relative positions of bonding wires and control their loop shapes at an accuracy of a few micrometers.

(3) Material development
Material development is important to realize thin packages for multi-chip stacking. We developed various materials, including high-rigidity protection tape to correct wafer warpage in order to make it possible to transport thin wafers from one process to another; a thin die bonding material to stack multiple chips close to each other; and mold resin with enhanced fluidity and moldability to reduce the resin thickness on a chip.

• Technologies to improve speed and reduce power consumption

In addition to high data storage capacity, high speed and low power consumption are required for notebook PCs and data servers.

A through-silicon via (TSV) technology provides higher performance and lower power consumption. In order to achieve TSV-based chip stacking, we developed technologies for the handling of thin chips and the bonding of chip-to-chip contacts. These technologies made it possible to stack more chips and significantly reduce the process time, with the result that a 16-die stacked NAND flash memory has been realized (Figure 2).

• Noise reduction technology

As communication equipment become smaller and more versatile, electromagnetic interference (EMI) noise produced by semiconductor devices on printed circuit

Column Challenges for package assembly processes

Figure A shows a typical flow of the semiconductor assembly process. There are various processes for different package styles, depending on application requirements (size, performance, thermal dissipation, reliability, etc.). For example, in order to reduce a decrease in chip strength due to wafer backgrinding, chemical mechanical polishing (CMP) may be used to remove the fractured layer. The diversifying processes make it necessary to develop new materials and processing technologies that meet the requirements for package assembly processes.

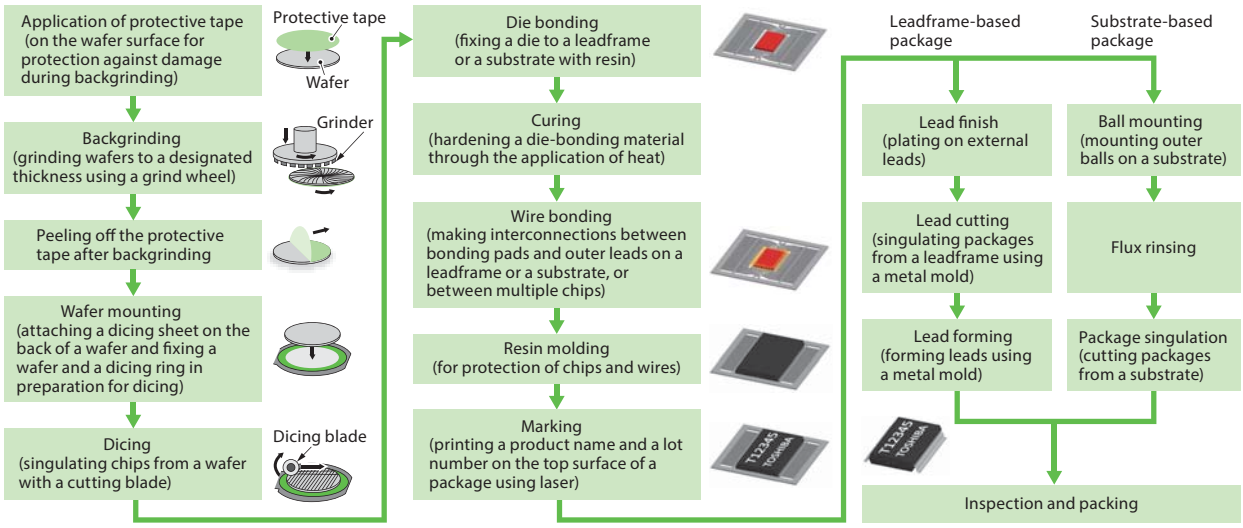

Figure A. Challenges for package assembly processes

boards has become troublesome. Conventionally, an entire printed circuit board has been covered with a metal shield in order to block EMI radiation. Instead, we have developed an EMI-shielding technology using a sputter deposition process and applied it to NAND flash memory in order to help reduce the size and thickness of electronic devices (see pages 19–22).

• Use of design-for-manufacturability (DFM) techniques

DFM takes manufacturing quality, productivity and cost into consideration at the design stage. By using DFM techniques for the development of solid-state drives (SSDs) and HDDs, we have optimized design rules and simulation models in order to improve quality and productivity (see pages 14–18).

Automobiles

Automobile production has been increasing year by year. Global automobile production is forecast to reach nearly 100 million units per year shortly (*3). The environmental and safety performances of automobiles have improved dramatically as represented by the prevalence of hybrid electric vehicles (HEVs), electric vehicles (EVs) and automobiles equipped with an advanced driver assistance system (ADAS) that will eventually enable self-driving. As electrical and electronic equipment constitutes large percentages of the volume, weight and cost of automobiles, a major challenge is to reduce its size and cost.

• Technologies for EVs and HEVs

We have developed an opto-isolated insulated-gate bipolar transistor (IGBT) gate pre-driver that combines photocouplers with IGBT drivers and other control circuitry for inverter applications for motor drive (see pages 23–26). This IGBT gate pre-driver integrates the low-voltage control circuitry on the input side and the high-voltage control circuitry on the output (motor) side in a single package and isolates the input and output sides with photocouplers. It helps to improve the board utilization of automotive electronic control units (ECUs).

• Technology to reduce heat resistance

Accompanying an increasing level of vehicle electrification, many ECUs are now placed in the engine compartment and other thermally harsh environments. Therefore, reduced heat resistance is necessary for elec-

(*3) Global automobile production in 2015 was 90.8 million units according to a survey by the Japan Automobile Manufacturers Association (JAMA)[4].

tronic parts.

For semiconductor devices in automobiles, their ambient temperatures and other environmental conditions must be taken into consideration in order to ensure that they will maintain stable operation for a long period of time. In order to meet this requirement, the surface temperature of semiconductor chips must generally be kept below 125 to 150°C regardless of the ambient conditions. To efficiently remove heat from semiconductor chips to the ambient environment, the thermal resistance of semiconductor packages must be reduced.

For example, due to the high-density assembly of electrical and electronic equipment in an engine compartment, it is sometimes required that the functional operation of semiconductor devices be guaranteed at an ambient temperature above 125°C. It is therefore necessary to use materials with high thermal conductivity in packages and improve their cross-sectional structure in order to reduce their thermal resistance. This is crucial to reduce the surface temperature of a chip in even small packages in order to ensure stable operation.

Our conventional four-channel power amplifier ICs for car audio applications were housed in a thermally enhanced through-hole package called a zigzag in-line package with heat sink (HZIP) to accommodate high current. In response to the requirements for smaller and thinner packages, we have developed a four-channel power amplifier IC in a shrink small-outline package with heat sink (HSSOP) that combines high thermal conductivity and high-density assembly (see pages 27–30).

• Solution for electromagnetic noise

Accompanying computerization of automobiles, malfunctions of electronic devices caused by electromagnetic noise have come under close scrutiny, causing electromagnetic compatibility (EMC) regulations for semiconductor devices to be tightened. In response, we have established an EMC test environment as stipulated by the International Electrotechnical Commission (IEC) so as to be able to readily provide EMC performance data for our semiconductor devices (see pages 9–13).

Communication devices

One of the most commonly used communication devices today is the smartphone. Smartphone manufacturers have launched various models, adding new features, reducing thickness and weight, and prolonging battery operating time.

Smartphones incorporate various means of wireless communication, including 3G (third generation), 4G (fourth generation), Wi-Fi, Bluetooth(†), near-field communication, a global positioning system (GPS) and a broadcasting receiver. Wireless communication circuitry entails difficult radio-frequency (RF) design as well as analog trimming and calibration. In order to help avoid design iteration and shorten development time, wireless communication circuitry is often provided as modules. Demand for lighter and more compact modules is increasing.

TransferJet™ is one of the near-field communication technologies that provides an easy means of sending and receiving a large amount of data at high speed. The TransferJet™ module has a 3D structure in which a silicon (Si) chip is embedded in the package substrate and passive RF components are placed on top of it. The entire module is encapsulated in resin with an EMI shield. The TransferJet™ module is 4.8 mm square and has a thickness of less than 1 mm, making it suitable for smartphone applications.

General-purpose applications

There is a need to reduce the size and thermal resistance of semiconductor devices for general-purpose applications, including office equipment, PCs, general home appliances, and industrial equipment. We possess the following advanced proprietary technologies especially for commonly used discrete semiconductor devices.

• Packages for small-signal devices

The requirements for the packages of small-signal devices include size reduction and high productivity. SL2 (0603) is an example of a package that meets these requirements. It is a super-small, low-cost package manufactured at a very high efficiency on a high-density matrix frame production line using the latest leadframe technology (see pages 31–35).

• Packages for optoelectronic devices

There is also strong demand for smaller packages for optoelectronic devices. In response, we have developed ultra-small photorelays. These photorelays are primarily used on test boards for semiconductor memory devices. Photorelays were initially intended to be used as a replacement for mechanical relays and then continued evolving to meet various market needs such as higher reliability, smaller size, higher operating frequency, and a higher current capability. In order to meet the size reduction requirement, it is important to develop technology to integrate multiple chips in a small package, including a light-emitting diode (LED), a photodiode array (PDA) and metal oxide semiconductor (MOS) devices. In 2014, we adopted chip-on-chip (COC) technology to develop a very small-outline non-leaded (VSON) package. Measuring 2.45 mm by 1.45 mm, the footprint area of the VSON package is 50% smaller than that of the conventional ultra-small-outline package (USOP) (**Figure 3**). We will endeavor to further

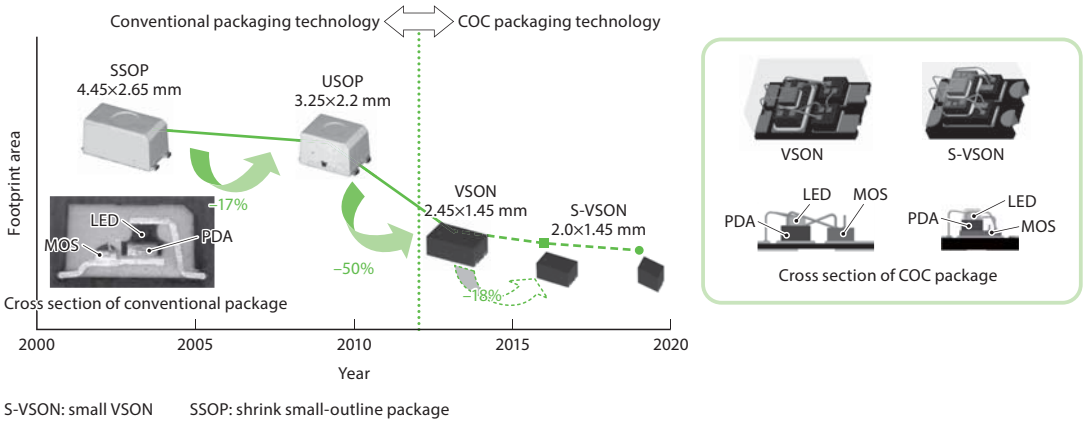

Figure 3. Trends in optoelectronic device packages.
Toshiba started using a COC structure starting with VSON packages in order to reduce package footprint areas.

reduce the COC package size by increasing a stack of chips from two to three.

• Power devices

Commonly used packages for power devices include TO-220 (TO: transistor outline), DPAK+ (DPAK: discrete packaging), SOP-Advance, and TSON-Advance (TSON: thin small-outline non-leaded). Each generation of packages has used a new internal interconnection process to increase current ratings.

For these packages, bonding technologies were the keys to success in increasing the current capacity, reducing resistance and improving thermal performance in order to increase current ratings. Bonding technologies evolved from wire bonding to aluminum straps, copper connectors, and combinations of a copper connector and heat radiating structures on both package surfaces (**Figure 4**).

New fields

Hardware for the Internet of Things (IoT), the internetworking of everything, consists of three major components: sensors, controllers and wireless communication devices. Millions of applications that combine these three components are available now. For example, we have developed an environmental sensing logger incorporating temperature, humidity, pressure, illuminance and shock sensors that is designed to monitor the changes in environmental conditions of product storage and freight transportation (see pages 36–40).

The single-chip implementation of an application-specific system-on-a-chip (SoC) entails a very complicated manufacturing process for Si chips and requires cost and a long lead time, making it difficult to meet customer needs or market requirements. In addition, since IoT devices are installed in many places, they need to be small and power-efficient. An effective solution

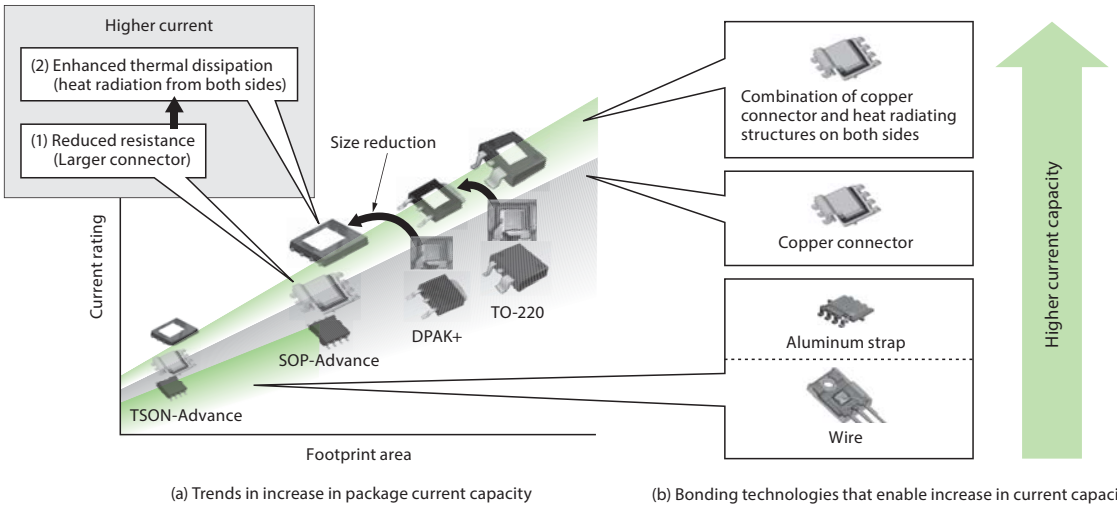

Figure 4. Trends in power device packages.
The interconnect platform fulfilled the requirements for reduced size and higher current by using a copper connector and heat radiating structures on both surfaces.

for developing small and low-cost IoT devices in a short period of time is to fabricate individual silicon chips using the optimal manufacturing process, and place and route them in one package called a system-in-a-package (SiP).

The SiP packaging technologies that have made it possible to produce diverse IoT devices with a short time-to-market come in various forms, including multi-chip packages (MCPs), package-on-package (PoP), Si/glass interposers, device embedded substrates and fan-out wafer-level packages (FOWLPs). It is therefore necessary to select the technology that best suits the requirements of individual products. Among various packaging technologies, FOWLPs are a promising next-generation technology for system integration for semiconductor applications. The following paragraphs describe the FOWLP technology.

Figure 5 shows the structures of FOWLPs. Silicon chips are ground thin, and the back of the chips is sealed in mold resin in which redistribution layers and solder balls are formed. Since the redistribution layers and the solder ball region can be wider than the chip surface area, FOWLPs are capable of providing more I/O connection points. Furthermore, the FOWLP technology provides a low-profile packaging solution since it does not require a package substrate.

The FOWLP technology also allows heterogeneous devices to be housed in a single package in a multi-chip configuration, making it possible to build a subsystem in a package. We have adopted the FOWLP technology for the analog front-end of a small sensor module with a wireless transmitter for monitoring pulse waves, cardiac potentials, body temperature and other bio-signals.

Furthermore, the FOWLP technology allows 3D chip stacking. The reduced chip-to-chip wire length helps to reduce parasitic inductance, improve high-frequency characteristics and reduce power consumption. Therefore, 3D FOWLPs are expected to be used for applications not only for the core circuitry of IoT devices but also for application processors, RF circuits and memory systems.

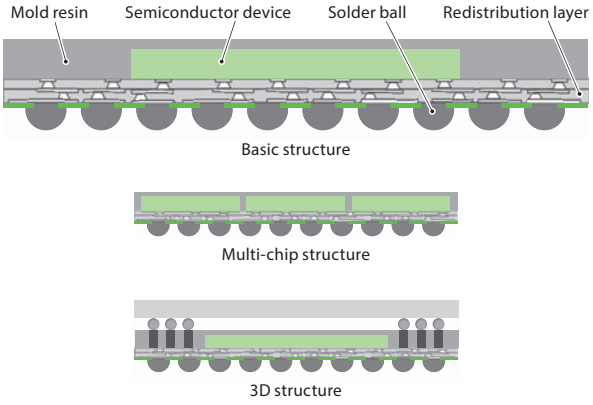

Figure 5. Structure of fan-out wafer level packages (FOWLPs).
FOWLPs meet the requirements for increased pin count and lower profile as well as multi-chip and 3D packaging for the integration of heterogeneous devices, making them a suitable solution for subsystem integration.

Future outlook

As electrification of various devices is at a sophisticated level, demand is growing for smaller and faster semiconductor devices with reduced thermal resistance and higher reliability, making package development even more important. We possess technologies for various devices including memory, discrete and mixed-signal devices. By combining them with packaging technologies, we will fulfill the requirements for semiconductor devices in the fields of storage, automotive, communication and general-purpose applications as well as new application fields.

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EMC Design Evaluation and Simulation Technologies to Support Noise-Tolerant Semiconductor Product Design

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With the expanding use of in-vehicle electronics in recent years, malfunctions of electrical equipment caused by electromagnetic noise have become a safety issue in the automotive field. In particular, electromagnetic compatibility (EMC) tolerance is an important evaluation item for electronic control unit (ECU) manufacturers when selecting semiconductor devices, in addition to performance, compactness, and cost.

In order to provide customers with information on the EMC tolerance of its semiconductor products at any time, Toshiba has constructed test environments complying with the IEC (International Electrotechnical Commission) 61967 series standards for electromagnetic interference (EMI) and IEC 62132 series standards for electromagnetic susceptibility (EMS). We have also established EMC simulation technologies to determine whether an abnormality is caused by our product or the printed circuit board (PCB) when the test result is unsatisfactory. In the event that a problem is identified in our semiconductor product by such simulation, we can immediately feed back the necessary countermeasures to the design. If a problem is identified in the peripheral circuit, on the other hand, we can provide customers with a specific solution based on the evaluation result. Our EMC design evaluation and simulation technologies can therefore not only strengthen semiconductor product development capabilities, but also contribute to the development of ECUs with high EMC tolerance.

1. Introduction

Due to the swift progress of electronic devices in recent years, many mechanically controlled systems have been computerized. This has made it possible to realize complicated control that was difficult to achieve before and rapidly improved the convenience of everyday life. However, accompanying computerization, malfunctions of electronic devices caused by electromagnetic noise have been attracting much attention as they pose a threat to safety. As a result, EMC regulations are being tightened worldwide.

In the field of automotive electronic devices, the Ministry of Land, Infrastructure, Transport and Tourism (MLIT) of Japan issued a notice on new standards concerning the Safety Regulations for Road Vehicles, based on United Nations ECE Regulation No. 10 for electromagnetic compatibility (EMC). Consequently, the EMC regulations were expanded to cover not only automobiles themselves but also all electronic devices installed in automobiles, i.e., electronic control units (ECUs)(*1). In response, ECU manufacturers now evaluate EMC performance in selecting semiconductor parts in addition to their functionality, size, and cost.

Toshiba has established a test environment based on the IEC standards on EMC test methods for semiconductor devices the IEC 61967 series (EMI test methods) and the IEC 62132 series (EMS test methods) in order to prepare in advance, or be ready to quickly provide on request, EMC performance data (**Table 1**).

Additionally, we have established an EMC simulation environment. In the event of unsatisfactory test results, we can now use the simulation environment to identify their cause, i.e., whether they are attributable to any semiconductor device or a circuit in its vicinity. If it turns out that a semiconductor device is the source of an EMC problem, we can now provide immediate feedback to the semiconductor design. If it turns out that the cause of the EMC problem lies in a peripheral circuit, we can suggest a remedy to our customers.

2. EMC regulations for semiconductor devices

2.1 International standards for the methods of EMC evaluation for semiconductor devices

There are multiple EMI and EMS test methods as

(*1) The EMC regulations now apply not only to new models manufactured on or after August 1, 2016 but also to existing models manufactured on or after October 28, 2016. Automakers are required to meet the EMC requirements to sell automobiles.

Table 1. EMC test methods and IEC standards for semiconductor devices

Category	Test method	Noise	International standard
EMI	General conditions and definitions	—	IEC 61967-1
	TEM cell method	Radiated	IEC 61967-2
	Surface scan method	Radiated	IEC 61967-3
	1Ω/150Ω direct coupling method	Conducted	IEC 61967-4
	WFC method	Conducted	IEC 61967-5
	MP method	Conducted	IEC 61967-6
	IC stripline method	Radiated	IEC 61967-8
EMS	General conditions and definitions	—	IEC 62132-1
	TEM cell method	Radiated	IEC 62132-2
	BCI method	Conducted	IEC 62132-3
	DPI method	Conducted	IEC 62132-4
	WBFC method	Conducted	IEC 62132-5
	IC stripline method	Radiated	IEC 62132-8
	Surface scan method	Radiated	IEC 62132-9

WBFC: Workbench Faraday Cage
MP: Magnetic Probe
Radiated: Method of evaluating noise emissions propagating through air
Conducted: Method of evaluating noise emissions propagating through wires and cables

* The 1Ω/150Ω direct coupling method is also known as the VDE method (VDE: Verband der Elektrotechnik, i.e., Association for Electrical, Electronic & Information Technologies of Germany).
* IEC 61967-7, IEC 62132-6, and IEC 62132-7 have been skipped.

shown in Table 1. It is necessary to consult with customers to select appropriate test methods according to objectives. The most frequently used test methods are the 1Ω/150Ω direct coupling method and the transverse electromagnetic (TEM) cell method for EMI, and the direct radio-frequency power injection (DPI) method, the bulk current injection (BCI) method, and the TEM cell method for EMS.

2.2 EMC test board for semiconductor devices

IEC 61967-1 and IEC 62132-1 provide specifications for the EMC test board for semiconductor devices. Key specifications for the test board are as follows:

(1) The board size must be 10 cm in width by 10 cm in length. This size is required for the TEM cell and IC stripline methods.
(2) The periphery of a test board must be plated with either tin or gold with a width of at least 5 mm.
(3) Vias must be at least 5 mm away from the periphery of a test board.

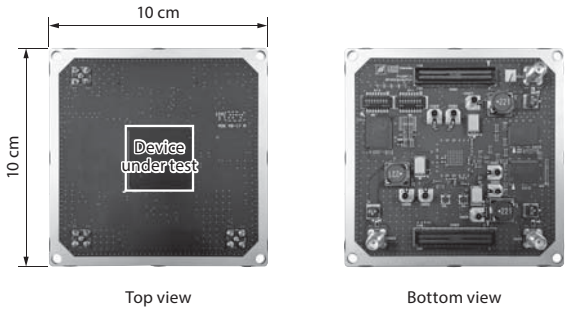

Figure 1. Example of PCB for EMC evaluation of semiconductor devices
This PCB is designed according to the IEC 61967-1 and IEC 62132-1 specifications.

(4) Holes must be drilled at four corners of a test board so that it can be fixed with screws.
(5) A board consisting of four or more layers is recommended.
(6) The device under test (DUT) must be mounted on the front side of a test board, and all the other parts on the back side.
(7) The unoccupied area of a test board should be covered with ground whenever it is practicable.
(8) The distance between adjacent vias must be 10 mm or less.

Figure 1 shows an example of an EMC test board for semiconductor devices.

2.3 BISS

The IEC standards listed in Table 1 provide a description of a test method, but not acceptance criteria. Whereas Japanese customers often require compliance with their respective in-house standards, more and more European customers are requesting the use of acceptance criteria specified in the Generic IC EMC Test Specification of the German Electrical and Electronic Manufacturers' Association (ZVEI: Zentralverband Elektrotechnik- und Elektronikindustrie e.V.) (also known as the Bosch, Infineon, Siemens VDO Specification, or BISS). **Figure 2** illustrates the acceptance criteria for the 150 Ω direct coupling method defined by the BISS. IC pins are classified into global and local pins, which are further divided into three classes (I, II and III). Whereas global pins use for input-output to outside the ECU board, and local pins use to inside the ECU board. Class III is for vehicle control ICs; Class II is for information and telecommunication ICs; and Class I is for the other types of ICs. As shown in Figure 2, the most stringent acceptance criteria apply to the global pins of vehicle control ICs (that use for input-output to outside the ECU board).

3. Verification using a test board

Figure 3 shows a setup for the measurement of a

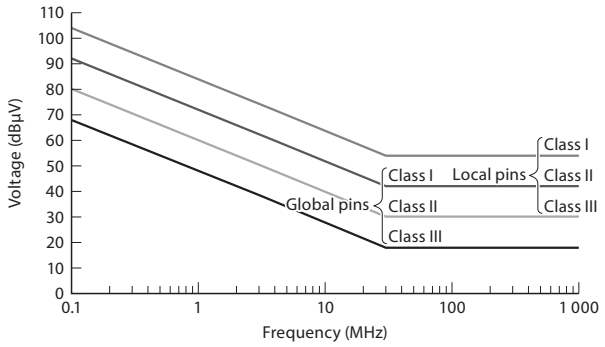

Figure 2. Acceptance criteria of 150 Ω direct coupling method according to BISS
There are different acceptance criteria for different pin types and different classes of applications.

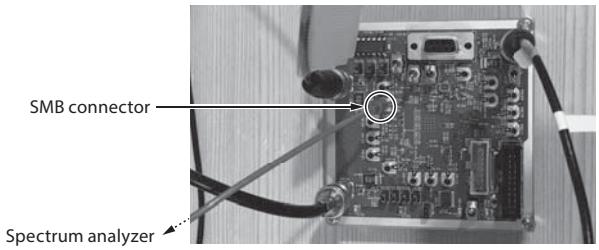

Figure 3. Measurement of microcontroller for automotive motor control using 150 Ω direct coupling method
SMB connectors (test pins) are connected to a spectrum analyzer with a cable.

microcontroller unit (MCU) for automotive motor control using the 150 Ω direct coupling method. This EMI test method measures conducted noise from IC pins and gives repeatable and reproducible results.

As shown in **Figure 4**, the 150 Ω direct coupling method places resistors, a capacitor, and an SMB (SubMiniature version B) connector that mounts as a test pin in the vicinity of the DUT. The conducted noise from the SMB connector are measured with a spectrum analyzer. Since it is difficult to add a measurement port like this to all DUT pins, power supply and global pins are given precedence. Local pins are tested according to their use and importance.

Figure 5 shows the result of measurement using 150Ω direct coupling method for a power supply pin of the automotive motor control MCU of Figure 3. This result

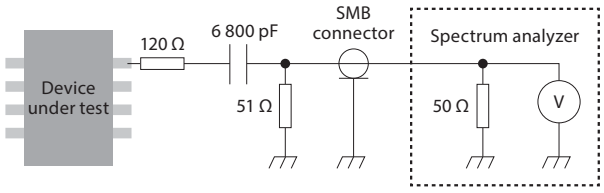

Figure 4. Test circuit used in 150 Ω direct coupling method
This circuit network is added to every test pin.

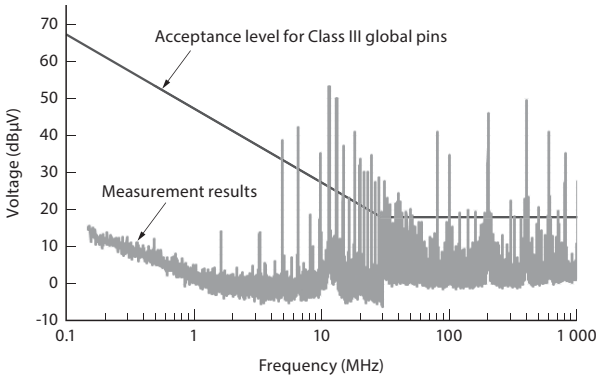

Figure 5. Result of measurement of noise level at 1.2 V power supply pin using 150 Ω direct coupling method
The power supply pin had large conducted noise without decoupling capacitors.

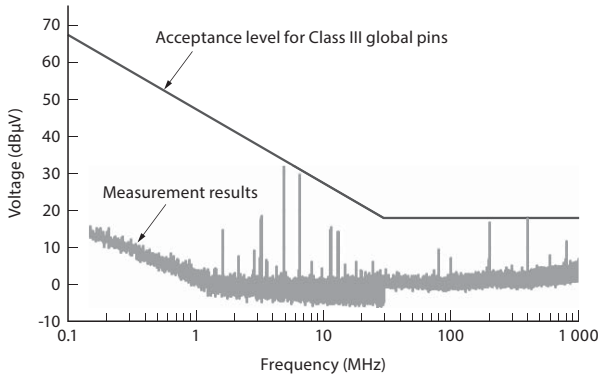

Figure 6. Result of measurement of noise at 1.2 V power supply pin after addition of decoupling capacitors using 150 Ω direct coupling method
The conducted noise were reduced considerably when decoupling capacitors were added.

is that capacitors is not mounted on the power supply pin, therefore it is different state in an actual application. In contrast, **Figure 6** shows the result of measurement when decoupling capacitors of 0.1 μF and 0.01 μF were added close to the power supply pin. It shows that the decoupling capacitors helped to reduce conducted noise significantly.

4. Verification using an electromagnetic field analysis

Section 3 showed that conducted noise can be sufficiently reduced by adding optimal decoupling capacitors. We performed an electromagnetic field analysis to determine whether the effect of decoupling capacitors can be predicted beforehand.

First of all, we created a simulation model for the test board (including the wiring model of the IC package) (**Figure 7**) to calculate the Z parameters between an external pin (port 1) of the IC and the SMB connector (port 2).

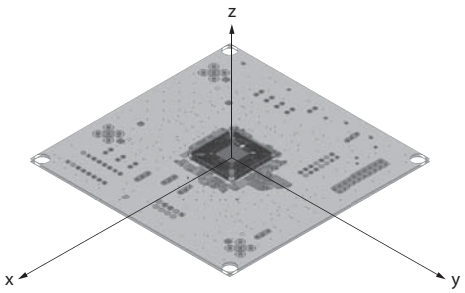

Figure 7. Simulation model of PCB for evaluation
The IC package is added to create a simulation model including its wiring model in order to perform an electromagnetic field analysis.

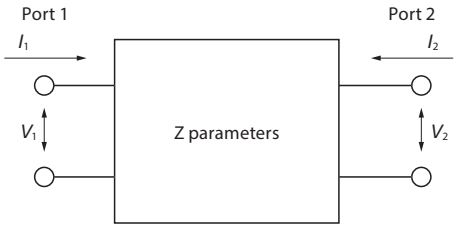

Figure 8. Four-pin network configuration
The Z parameters of a four-pin circuit network are used for an analysis. Here, port 1 is an external pin of the IC and port 2 is the SMB connector.

Next, a current model for port 1 was derived from the Z parameters. **Figure 8** shows a four-pin circuit network using the Z parameters. In this network, the voltage at each port, V_i (i=1, 2) has the following relationship with the current, I_i (i=1, 2):

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (1)$$

where, Z_{11} and Z_{22} are input and output impedances respectively, and Z_{12} and Z_{21} are transfer impedances. Since the current coming out of port 2, I_2, is considered to be zero, the current flowing into port 1, I_1, is calculated as follows:

$$I_1 = V_2 / Z_{21} \quad (2)$$

Since V_2 is a voltage at port 2 measured by the 150 Ω direct coupling method without using decoupling capacitors, I1 can be calculated by using Z_{21}, a Z parameter. **Figure 9** shows the current model derived by this method.

Lastly, we created a simulation model for a circuit with decoupling capacitors and performed an electromagnetic field analysis using it. **Figure 10** compares the transfer impedance (Z_{21}) with and without decoupling capacitors. It shows that Z_{21} dropped in the 3 to 1,000 MHz frequency range when the 0.1 μF and 0.01 μF decoupling capacitors were added in the vicinity of the power supply pin.

Figure 11 shows the result of an analysis using the

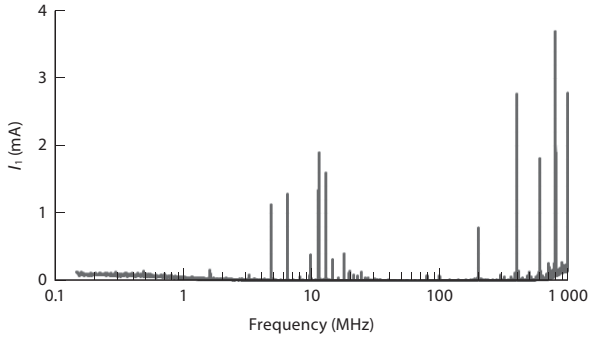

Figure 9. Current model extracted from measurement and simulation results
A current model was extracted from the result of measurement using the 150 Ω direct coupling method and the Z parameters.

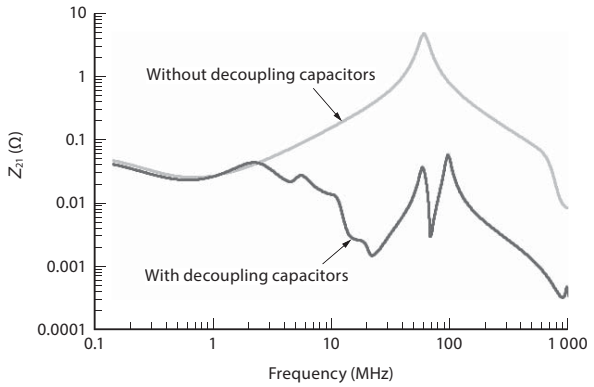

Figure 10. Comparison of transfer impedance (Z_{21}) with and without decoupling capacitors
Z_{21} was reduced in the frequency range between 3 MHz and 1 000 MHz by adding decoupling capacitors.

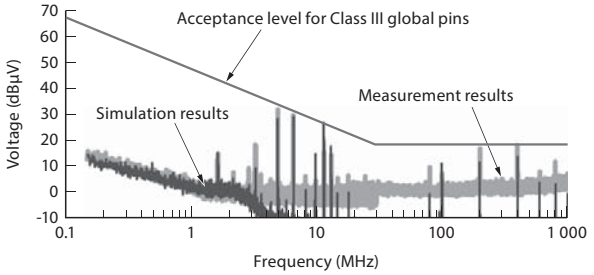

Figure 11. Comparison of simulation and measurement results
The frequencies at which the noise voltage peaked coincided between the simulation and measurement results. The differences in noise voltage between them were less than roughly 5 dBμV.

150 Ω direct coupling method when the current model of Figure 9 was added to the test board with decoupling capacitors (Z_{21} in the circuit of Figure 10 with decoupling capacitors). Figure 11 also shows the result of measurement after the addition of decoupling capacitors using the 150 Ω direct coupling method of Figure6. The frequencies at which the simulated and measured

noise voltages peaked coincide well, and the differences between them are less than roughly 5 dBμV. We consider that the differences between the simulated and measured noise voltages are caused by coupling due to crosstalk from other pins and the omission of non-major parts in the simulation model.

It was confirmed that an electromagnetic field analysis can predict conducted noise from a circuit with decoupling capacitors by using a current model derived from a circuit without decoupling capacitors. This current model can be used for the verification of layout designs of customers' boards before they are actually manufactured.

5. Conclusion

We have developed a semiconductor EMC test environment based on the IEC standards as well as a simulation technology to verify test results. We will use them to develop semiconductor products and to assist customers in developing ECUs with high EMC tolerance.

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Toshiba's DFM-Based Approach to Printed Circuit Boards for Storage Products

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There is a need for high-density mounting technologies for printed circuit boards (PCBs) installed in storage products such as solid-state drives (SSDs), hard disk drives (HDDs), and solid-state hybrid drives (SSHDs), in line with the increasing data storage capacity of such products. In particular, it is important to optimize the design specifications of large-scale controller chips and printed wiring boards (PWBs), which are the main components affecting manufacturing quality and productivity in the factory, in order to eliminate costly and time-consuming design change processes in the event of a failure.

Toshiba has applied an approach based on design for manufacturability (DFM) to PCBs for storage products at the initial stage of design, taking manufacturing quality, productivity, and production costs into consideration. By conducting a variety of simulation experiments using this approach, we have succeeded in assuring quality, reducing costs, and improving the productivity of PCB manufacturing.

1. Introduction

Toshiba provides SSDs, HDDs, SSHDs and other data storage products for mobile notebook PCs and enterprise servers. Our factory engages in the entire process from the design of PCBs to the assembly of units. NAND flash memories used as storage devices for SSDs and SSHDs are also designed and manufactured in-house. The designing and manufacturing divisions are collaborating to develop the products so as to facilitate feedback to each process.

Owing to an increase in the capacity of storage products, the space occupied by storage media in a unit is expanding, leaving less area on PCBs for control circuitry. Furthermore, in order to boost data access speeds and incorporate a feature for ensuring a highly secured data integrity, the number of electronic components and circuits on PCB are increasing. As a result, high-density PCB assembly is becoming indispensable.

The controller, a major component to be soldered on a PCB, is also becoming higher density and multifunction. Nowadays, a ball grid array (BGA) structure is more commonly used for a controller to realize higher pin count package. In order to further increase the pin count and reduce the size of the package to fit in a space-critical board, the pin has been becoming narrow-pitch on BGA packages, making it difficult to realize low-cost PCBs while maintaining high quality.

This report describes an example of a design-for-manufacturability (DFM) approach adopted for the development of an enterprise SSD (**Figure 1**), taking manufacturing quality, productivity and cost into consideration early in the design cycle.

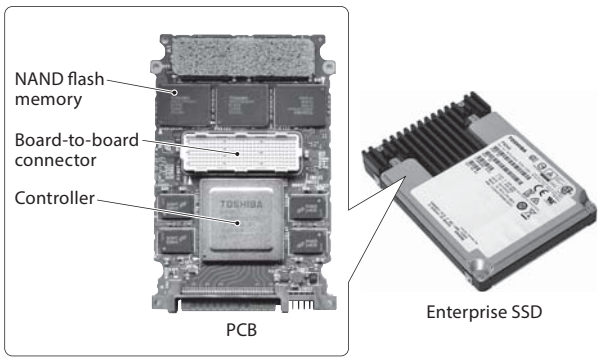


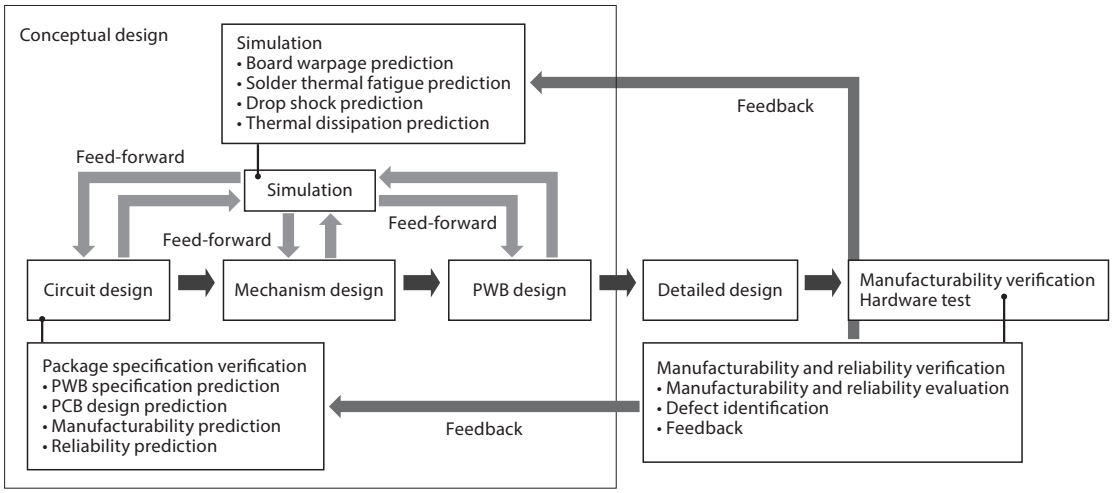
Figure 1. PCB installed in SSD for enterprise use
In order to realize a high-quality and low-cost PCB, a DFM-based approach is adopted, taking manufacturing quality, productivity and cost into consideration.

2. Overview of the use of DFM for PCB development

2.1 Flow of PCB development.

Figure 2 shows the flow of PCB development. The PCB development begins with conceptual design, which consists of circuit design, mechanism design, PWB design, and simulation, followed by detailed design, manufacturability verification, and a hardware test.

The entire design process is broadly divided into two phases: 1) conceptual design in which various ideas



* As is the case with conceptual design, feedback is provided during detailed design.

Figure 2. Flow of PCB development
The design process consists of two phases: conceptual design in which various ideas about a product are articulated and detailed design in which the conceptual design is further refined, detailed and translated into a product design.

about a product are articulated to develop a product specification and 2) detailed design in which the conceptual design is further refined, detailed, and translated into a product design.

2.2 Overview of the use of DFM

Generally, the term DFM means an engineering art of designing a product in such a way as to make it easier to manufacture. The term DFM as used herein refers to a design approach employed early in the design cycle (for example, in the conceptual design phase), which involves securing quality including solder joint reliability, improving productivity through adaptation to manufacturing capabilities, and reducing costs by optimizing PWB specifications.

As manufacturability verification and hardware testing are performed in-house, their results are fed back to the establishment of design rules and creation of simulation models. These are the steps to validate and correct the design approach, resulting in the enhanced accuracy of the DFM.

3. Finalization of package specifications and PWB designs

3.1 Design concerns

The package specifications are one of the determinants for the PWB specification; they affect the manufacturability and cost of a PWB, as well as the PCB manufacturability and the reliability of solder joints on the board. Since redesigning PCB after the detailed design is not easy, finalization of package specifications in the conceptual design phase is important.

Controllers have large size and high-pin-count package structure, which incur high development cost and purchase price. Therefore, optimizing the controller package specifications is crucial.

For example, a small BGA package with narrow pin pitch can be adopted to shrink the package footprint in order to realize high-density PCB. The reduction in solder pad size may be a concern for degradation of manufacturing quality of PCB, such as the decreased solder joint strength and increased variability in solder joint formation. Furthermore, a greater number of solder pins arranged at a narrower pitch restricts the flexibility in signal trace routing under the BGA package. Therefore, high-density PWB with a complicated manufacturing process is needed, which causes a concern for the PWB cost rise.

3.2 DFM

In order to alleviate design concerns, a DFM approach is adopted for the design of a PWB early in the design cycle according to the package specifications. The DFM process verifies the board assembly design, including the routability and overall layout of signal traces as well as the solder joint pad size compatible with the required solder joint reliability and the manufacturing capability. Additionally, this process verifies whether the package specifications are compatible with the PWB specification in accordance with the applications (**Figurer 3**).

4. Use of simulation techniques

Various types of simulation are performed to predict the behavior of PCBs in response to the loads that the product might face during manufacturing process or in the field when used in various conditions. We provide the result feedback in the early stage of the product design.

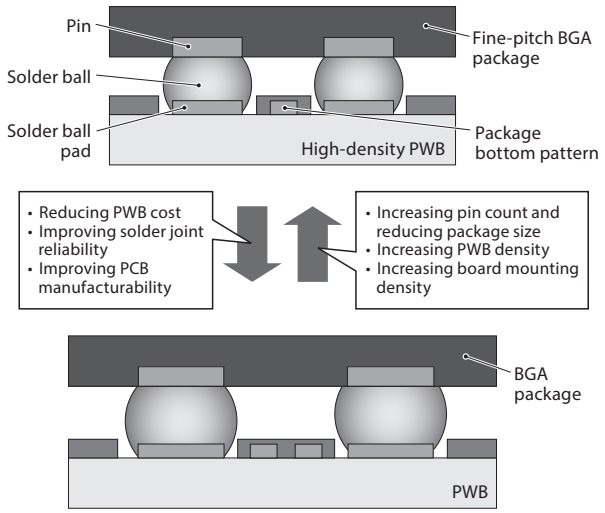


Figure 3. PWB design in accordance with package specifications

In addition to the finalization of package specifications, the final specification for a PWB is estimated according to its application in order to verify its reliability and manufacturability.

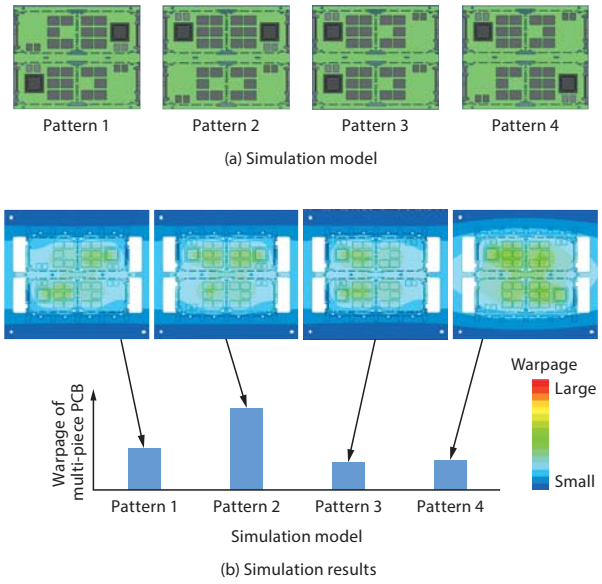


Figure 4. Multi-piece PCBs warpage simulation

Multi-piece PCBs warpage after reflow soldering process was predicted for various different arrangement patterns of single-piece PCBs.

4.1 PCB warpage simulation

The reduction of PCB warpage after reflow soldering process is important to improve the PCB manufacturing quality. PCB warpage simulation, which gives the thermal load emulating the temperature profile of reflow soldering process to the model, is performed using the model of multi-piece PCBs held on the jig. Models of multi-piece PCBs with various arrangement patterns are used in the simulation to select the optimal arrangement patterns for smaller warpage, less cost, and better manufacturability of PCBs. **Figure 4** shows an example of warpage simulation of multi-piece PCBs.

4.2 Thermal fatigue simulation of solder joints

Power cycling causes repetitive fluctuations in temperatures of the solder joints of PCB-mounted parts. This results in thermal fatigue at solder joints derived from the CTE (Coefficient of Thermal Expansion) mismatch between components and PWB. In the product (chassis and PCB) design process, temperature cycling simulation is performed for the entire unit model including the chassis, board, and major components. The simulation result is fed back to product design to optimize the positioning for major parts. **Figure 5** shows an example of the result of a thermal fatigue simulation.

4.3 Drop shock simulation

For data storage products that deal with a huge volume of data, shock resistance is also important. In order to avoid design iterations, it is necessary to predict the deformation of PCB inside the chassis at impact load in the early stage of the design process. Identification of

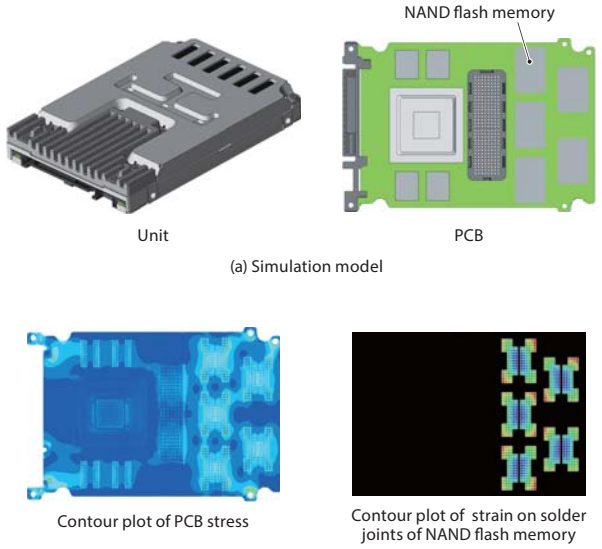


Figure 5. Thermal fatigue simulation of solder joints of BGA package on PCB

Thermal fatigue reliability of solder joints was evaluated through a structural analysis using the entire unit model.

the vulnerable area to impact enables us to provide the appropriate safeguards against impact to the devices. **Figure 6** shows an example of drop shock simulation. This simulation confirms whether there will be any unexpected interference between components and if the board will encounter excessive loads in drop shock conditions. The simulation result is fed back to the design phase process to improve reliability.

4.4 Thermal simulation

Due to the recent increase in the data processing

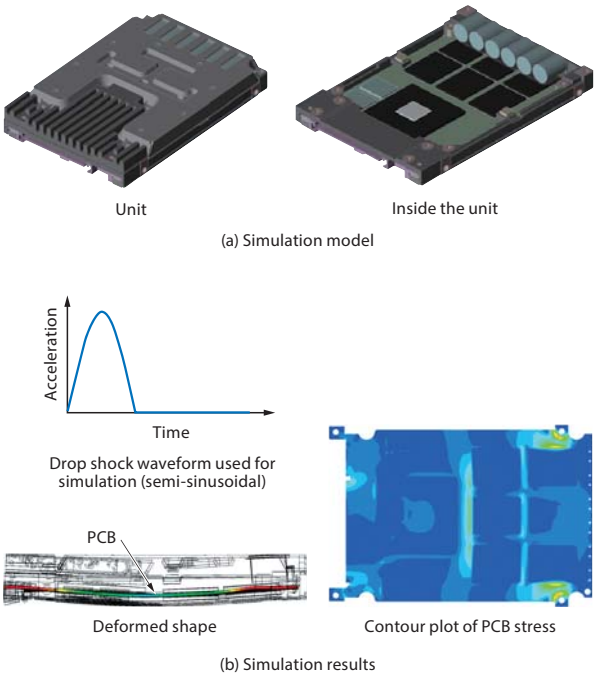


Figure 6. Drop shock simulation of enterprise SSD
Drop shock loads were applied to an entire unit model of an enterprise SSD in order to evaluate the deformation and stress of the PCB.

speeds of enterprise SSDs, their controllers chips now generate significant amount of heat. It is necessary to realize a thermal design which enables the device to keep the package temperatures of NAND flash memories below their maximum operating temperature. Therefore, the simulation is performed for sufficient evaluation of thermal design previous to the detailed product design. A possible temperature rise of components is estimated based on the power consumption under operating conditions of the enterprise SSD and the expected air flow conditions in the server system. The simulation result is fed back to the thermal design of an SSD.

5. Example of a hardware test and manufacturability verification

We test manufacturability and solder joint reliability using actual hardware in order to verify the effects of DFM.

5.1 Manufacturability

It is becoming increasingly important to identify any PCB problems at the prototyping stage and fix them early in order to maintain stable mass-production quality.

Figure 7 shows a board-to-board (BTB) connector used to connect PCBs. The conventional BTB connector was wholly covered by its cap to protect contact pins and to serve as a suction holder at parts mounting process. However, the cap blocks heat transfer from a reflow

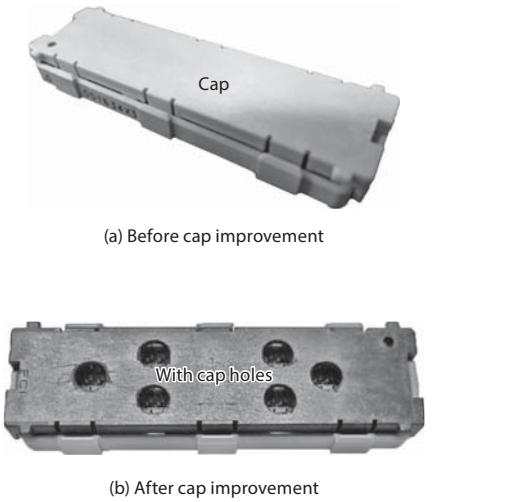


Figure 7. Improvement of solderability of BTB connector
Holes in the BTB connector cap promoted heat transfer from a reflow oven, enabling adequate temperature control for soldering.

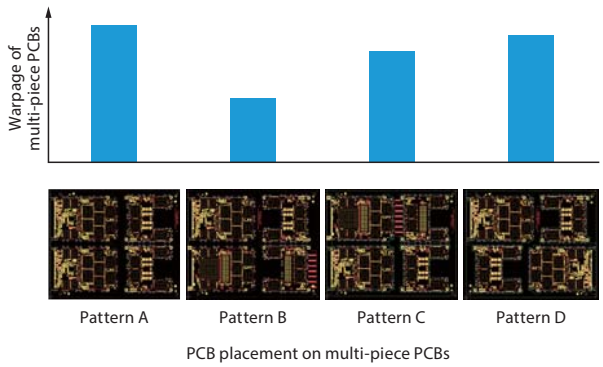


Figure 8. Results of warpage measurements of multi-piece PCBs after reflow soldering process
Multi-piece PCB warpage after reflow soldering varies depending on the arrangement pattern of single-piece PCBs. Smaller warpage of a multi-piece PCB leads to better manufacturability and quality of the board assembly.

oven, causing the solder joints temperature not to rise sufficiently. The newly designed cap with holes could solve this problem by optimizing heat transfer route while protecting contact pins and maintaining manufacturability.

Figure 8 shows the results of warpage measurements of multi-piece PCBs after the reflow soldering process. PCBs with large warpage degrade the manufacturability of subsequent processes, including parts mounting and unit assembly. Therefore, we devise the arrangement patterns of single-piece PCBs for smaller warpage in order to improve the manufacturability of subsequent processes and assembly quality. We also improve simulation accuracy by comparing the simulation results shown in Section 4.1 with actual measurement results.

As a result of the foregoing, the mass-production quality of data storage products is secured.

5.2 Solder joint reliability

In order to evaluate solder joint, temperature cycling tests are performed using test PCBs that imitate the board design of actual products. The wiring of a BGA package used for this evaluation is designed in such a manner that the failure cycle of solder joints can be detected by monitoring their electrical resistance during the test.

Figure 9 shows the cross-sectional image of a solder joint after a temperature cycling test. It was confirmed that no failure occurred after a temperature cycling test and that the solder joints were in good condition without cracks or other damage. For devices requiring high reliability of solder joints, we estimate the thermal fatigue life through detection of the failure cycle, examine the conditions of solder joints in the early stage of development, and provide feedback to the PCB design for mass-production.

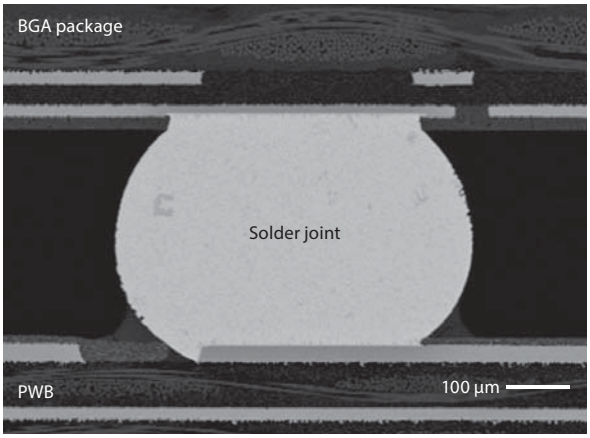


Figure 9. Cross-sectional image of solder joint after temperature cycling test
We confirmed that the solder joints of the BGA package were not damaged by a temperature cycling test.

6. Conclusion

For data storage products, we perform all the development processes in-house from design to manufacturing. By taking advantage of our comprehensive skills and capabilities, we have been endeavoring to optimize our design rules and simulation models through continuous applications of DFM to PCB designs and the verification of their results. We will continue to develop high-quality and low-cost PCBs in order to meet the requirements of storage products with ever-increasing data capacities and becoming higher densities.

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Technology to Form EMI-Shielding Film on Semiconductor Packages Using Sputter Deposition Process

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In order to achieve greater compactness and higher performance of mobile information communication terminals, improvement of the electromagnetic interference (EMI) performance of each electronic device mounted on the high-density printed circuit boards (PCBs) of such terminals is now attracting the attention of electronics manufacturers. The need has therefore arisen for an EMI-shield forming process for semiconductor products that realizes high performance including low noise radiation and high noise resistance at low cost.

Toshiba has developed a mass-production technology for semiconductor packages with an EMI-shielding film on the surface, referred to as EMI-shielded packages, using a sputter deposition process capable of forming a metal thin film more stably compared with the screen printing process using a metal paste. Newly developed special tools are incorporated into the sputtering equipment generally used for the front-end process, so as to prevent overflow of the shielding film to the backside of the package without the need for costly protective tape and thereby reduce costs. Experiments on a prototype EMI-shielded package produced by this sputter deposition process have verified that it is effective in suppressing radiation noise.

1. Introduction

As cell phones, smartphones and other electronic devices have become smaller and more versatile in recent years, market demand is growing for high-density assembly of printed circuit boards (PCBs). As a result, noise produced by semiconductor devices is becoming a major obstacle to electromagnetic interference (EMI). In order to reduce EMI on a PCB, it is necessary to decouple the source of noise from its propagation path and thereby reduce interference between electronic parts.

In conventional mobile devices, electronic parts on a PCB are often covered with a metal shield in order to block EMI radiation. The metal shield makes it difficult to reduce the size and thickness of electronic devices. Since packages housing large-capacity NAND flash memory (NAND packages) are thicker than other electronic parts, their thickness determines the height of a metal shield and therefore restricts the physical dimensions of electronic devices.

In these circumstances, we had been receiving repeated requests from electronics manufacturers that an EMI solution be embedded in semiconductor packages so as to be able to dispense with an external metal shield.

In response, we developed a technology to form an EMI-shielding film in semiconductor packages with silver (Ag) paste using a screen printing technique[1]. However, Ag paste is expensive. Since an Ag film with a thickness of 30 to 50 μm was necessary to obtain a sufficient EMI-shielding effect, the film thickness was a limiting factor in reducing manufacturing cost.

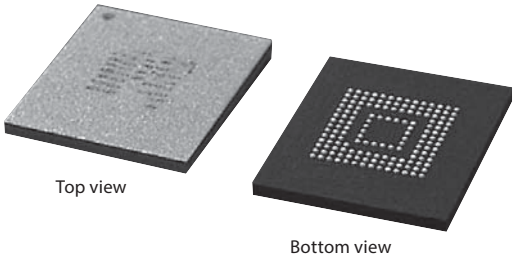

Figure 1. EMI-shielded package.
We have developed a technology to form an EMI-shielding film by using a sputter deposition process instead of the conventional screen printing method.

To solve this problem, we have developed a mass-production technology for EMI-shielded packages using a sputter deposition process (**Figure 1**). This report provides an overview and describes the features of the newly developed technology.

2. Structure of an EMI-shielded package

As shown in **Figure 2**, a metal film is formed on the package encapsulant for EMI-shielding.

In order to produce a positive effect, the EMI-shield-

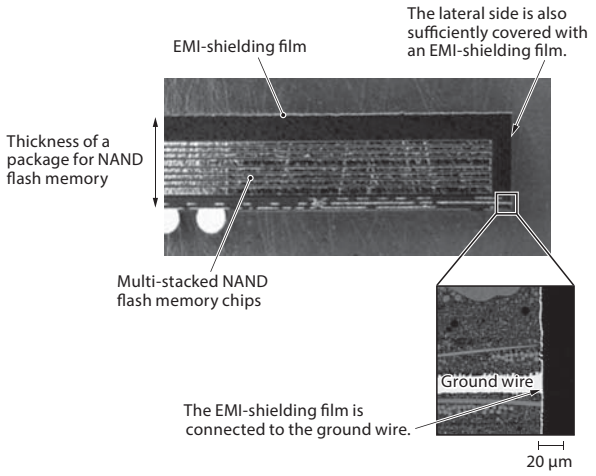

Figure 2. Cross-sectional structure of EMI-shielded package produced by sputter deposition process.
The outermost EMI-shielding film extends to the side of a package and is connected to the ground wire to achieve a remarkable EMI-shielding effect.

ing film must be electrically connected to the ground wire exposed on the side of a package. To fulfill this requirement, it is necessary to form an EMI-shielding film on not only the top but also the side of a package and to reduce the resistance between the EMI-shielding film and the ground wire.

It is known that the lower the sheet resistance of the metal film, the better the EMI-shielding performance it exhibits. The conventional screen printing method cannot reduce specific resistance since it leaves a large amount of impurities in the fired film of Ag paste. In contrast, a sputter deposition process is capable of forming a uniform metal film at a high purity on the surface of a semiconductor package, making it suitable for the mass-production of packages with high EMI-shielding performance.

Since the external dimensions of semiconductor packages are stipulated in international standards, the film thickness necessary for EMI-shielding must be taken into consideration in designing semiconductor packages. In the case of a NAND package, NAND flash memory chips must be made thinner to accommodate an EMI-shielding film in it. This incurs an increase in the cost of NAND package assembly. To reduce this cost increase and achieve mass-production of EMI-shielded packages, it is essential to form a high-performance metal EMI-shielding film with a sputter deposition process.

3. Sputter deposition process

The process of forming an EMI-shielding film in semiconductor packages using a sputter deposition process (hereinafter referred to as a package sputter process) is performed at the last stage after semiconductor devices are singulated for packaging. For the package

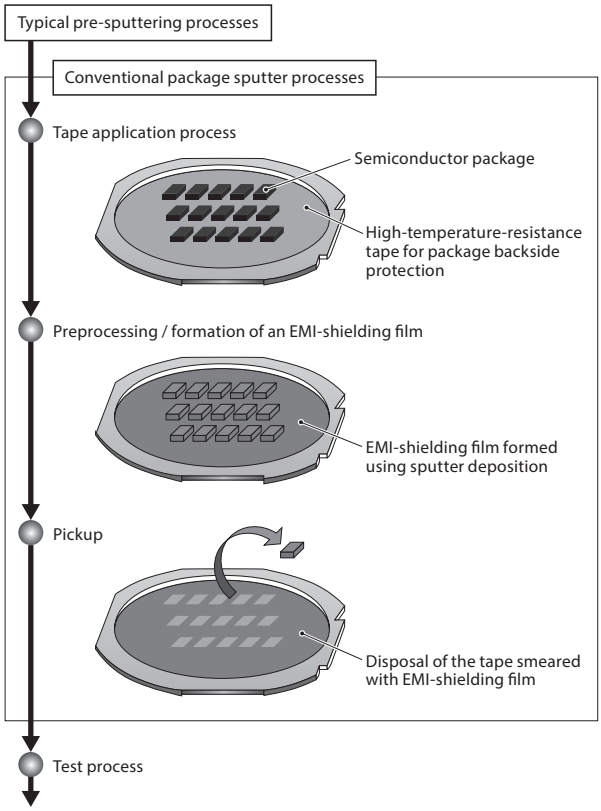

Figure 3. Flow of package sputtering processes using conventional sputtering equipment.
When sputtering equipment for the front-end process is utilized, the backside of semiconductor packages is protected using tape. However, tape has drawbacks such as bursting in vacuum and one-time-only disposal of expensive tape.

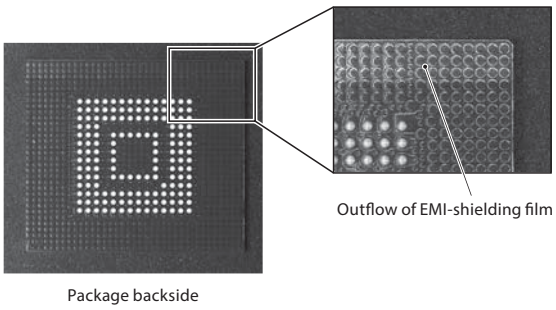

Figure 4. Overflow of shielding film to backside of package.
The tape for backside protection can come off the package. A defect occurs if shielding overflows to the backside.

sputter process, we employed sputtering equipment used at the front-end of semiconductor device fabrication (**Figure 3**).

In the package sputter process, an EMI-shielding film could also be formed on the backside of a semiconductor package (**Figure 4**). This occurs when a semiconductor package floats off a transport tray because of the handling of packages, vibrations of transport equipment, or vacuuming the chamber of sputtering equipment.

Affixing protective tape on the backside of the package is effective in preventing the overflow of an EMI-shielding film to the backside of a semiconductor package. However, if air bubbles are locked between protective tape and a semiconductor package, they burst when air is sucked out into a vacuum chamber, causing the protective tape to locally come off from the package.

During a sputter deposition process, a film is also formed in areas where semiconductor packages are not located. Therefore, protective tape cannot be reused. In addition, since ball grid arrays (BGAs) have solder balls on the backside side, the tape needs thicker adhesive for the protection of solder balls. Furthermore, expensive heat-resistant tape is necessary because the temperature of semiconductor packages rises above 150°C during a package sputter process.

As described above, tape-based protection is unreliable and increase the sputter process cost.

In order to solve these problems, we developed a dedicated tool designed to protect the backside of packages without interfering with the formation of an EMI-shielding film (**Figure 5**). This dedicated tool, if shaped optimally, prevents semiconductor packages from floating off a transport tray and can be used repeatedly. We also developed a handler for transporting the dedicated tool to the sputtering equipment so that the equipment for front-end device fabrication can be utilized for the package sputter process.

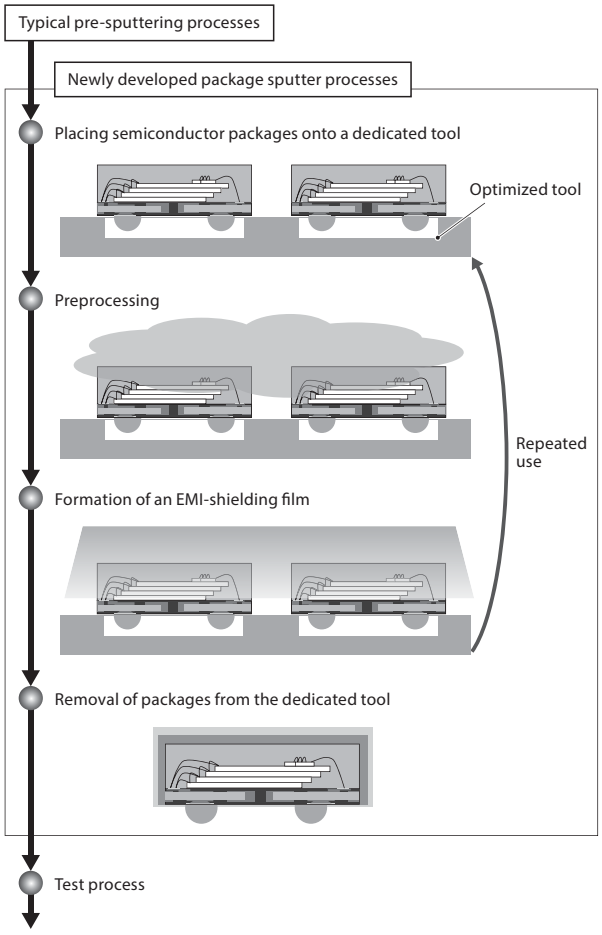

Figure 5. Flow of package sputtering processes using newly developed tools.
To overcome the drawbacks of tape, we developed a dedicated tool and a handler for transportation to the front-end sputtering equipment.

4. Result of a measurement of radiation noise from an EMI-shielded package

We created a prototype EMI-shielded BGA package housing NAND flash memories and a controller and measured the amount of radiation noise coming out of it.

We prepared BGA packages with and without an EMI-shield using a sputter deposition process, and measured radiation noise with a near magnetic field instrument. A magnetic field probe was scanned at a pitch of 1 mm at 1 mm above the package surface to map the amount of radiation noise. The radiation noise in the frequency range of 10–3 200 MHz was measured. **Figure 6** compares the strength of radiation noise from the two BGA packages at frequencies above and below 1 500 MHz.

It was confirmed that the EMI-shielded package using a sputter deposition process provides a shielding of -23 dB for frequencies in the range of 10–1 500 MHz and a shielding of -16 dB for frequencies in the range of 1 500–3 200 MHz. Figure 6 shows that radiation noise comes out of the top surface of the package without EMI-shielding and that the EMI-shielded package suppresses this radiation noise.

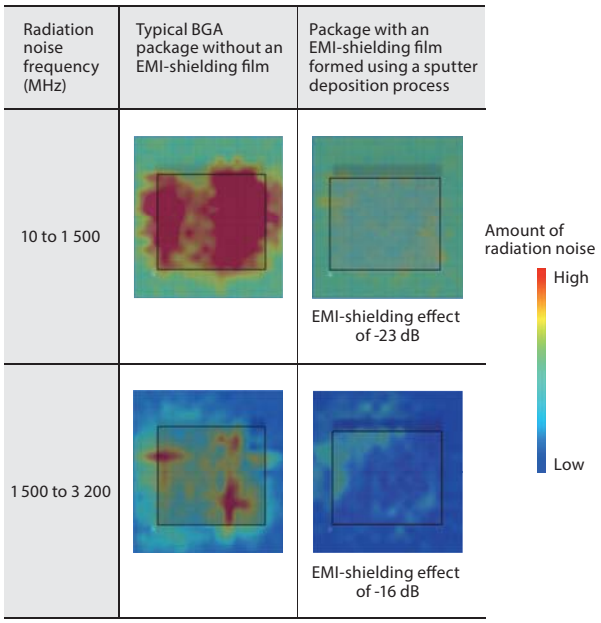

Figure 6. Results of noise measurements of packages with and without EMI-shielding film.
A measurement of a near magnetic field using a magnetic field probe shows good EMI-shielding.

5. Features of EMI-shielded packages using a sputter deposition process

EMI-shielded packages using a sputter deposition process described in the following features:

(1) The use of a sputter deposition process instead of screen printing using Ag paste made it possible to reduce the thickness of an EMI-shielding film from 30–50 μm to a few micrometers, achieving a significant reduction in manufacturing cost (**Figure 7**).

(2) The development of a dedicated tool for protecting the package backside during a package sputter process helps maintain process stability and eliminates the need for the conventional protective tape, significantly reducing material cost.

(3) The prototype EMI-shielded package using a sputter deposition process exhibited a shielding of -23 dB in the frequency range of 10–1 500 MHz and a shielding of -16 dB in the frequency range of 1 500–3 200 MHz.

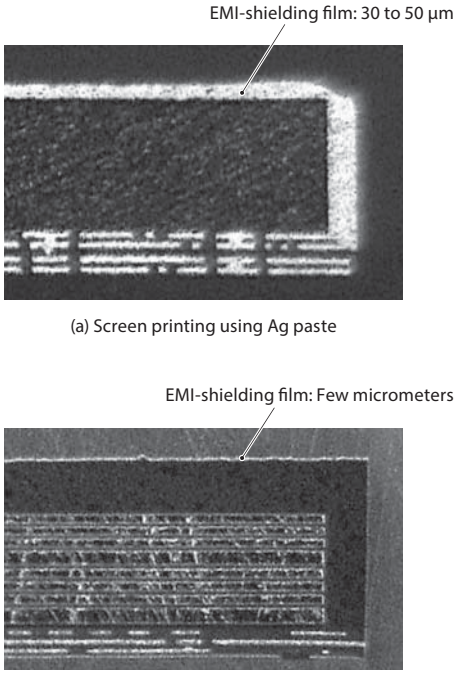

Figure 7. Comparison of cross-sectional structure of EMI-shielded packages produced by screen printing and sputter deposition processes.
A sputter deposition process can reduce the thickness of an EMI-shielding film compared with a screen printing method using Ag paste and therefore provides a significant reduction in manufacturing cost.

6. Conclusion

In order to meet electronics manufacturers' need for an EMI solution, we have developed a mass-production technology for EMI-shielded packages by using a sputter deposition process capable of forming a high-quality EMI-shielding film at low cost.

As a result, we have succeeded in creating value-added EMI-shielded packages by employing to back-end a technology used at the front-end of semiconductor device fabrication.

We will continually promote the development of semiconductor devices that provide higher functionality at lower cost, transcending front-end and back-end technological borders.

Reference

(1) Ishida M. et al. 2012. "Electromagnetic Shielding Technologies for Semiconductor Packages (in Japanese)." *Toshiba Review* 67(2): 7–10.

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TB9150FNG Opto-Isolated IGBT Gate Pre-Driver IC for In-Vehicle Inverters Offering Greater Compactness and Higher Insulation Performance

● KISHI Hiroaki ● HORI Masahiko

Accompanying the expansion of the hybrid electric vehicle (HEV) and electric vehicle (EV) markets, the roles of inverter systems used to drive electric motors have become diversified. This has led to demand for the miniaturization and multifunctionality of such inverter systems incorporating power modules equipped with motor driving devices including insulated-gate bipolar transistor (IGBTs), isolation devices, and IGBT driver circuits.

In response to this situation, Toshiba began shipping samples of the TB9150FNG opto-isolated IGBT gate pre-driver integrated circuit (IC) for in-vehicle inverter systems in April 2016. The TB9150FNG integrates photocouplers as isolation devices, a pre-driver as a controller for the IGBT driver circuit, and other devices into one package, making it possible to downsize inverter systems.

1. Introduction

Nowadays, increased environmental performance is required for automobiles as it is crucial to reduce carbon dioxide (CO_2) emissions from automobiles. Accompanying the expansion of the markets for environmentally friendly HEVs and EVs, the IGBT driver market is also expected to grow (**Figure 1**).

Electric motors, batteries and the related motorized and electronic components comprise major portions of HEVs and EVs. In particular, the roles of inverter systems used to control electric motors have become more diverse than ever before, need the miniaturization and multifunction of inverter systems.

Inverter systems consist of power modules incorporating IGBTs and other motor drivers, isolation devices, IGBT drivers and other components.

Photocouplers, a type of opto-coupled devices, are primarily used as isolation devices. A photocoupler transfers electrical signals between isolated terminals by using light. A light-emitting element such as a light-emitting diode (LED) converts an electric input signal into light, and a light-receiving element such as a photodiode, which detects the incoming light, converts it back into an electric signal. In other words, a photocoupler transfers a signal from the input side to the output side while maintaining electric isolation between them.

Toshiba has been manufacturing photocouplers since the 1980s, including those for power transistors. We take pride in our extensive expertise built up through many years of experience.

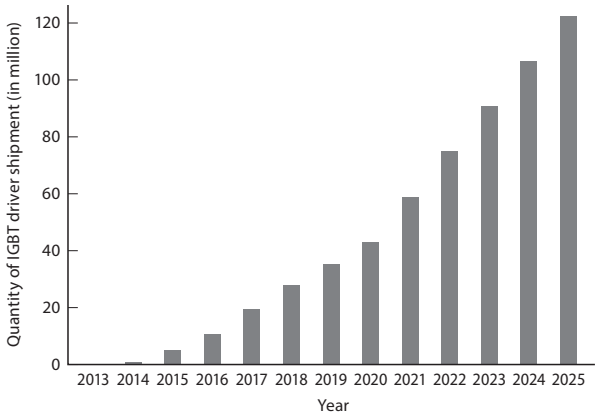

Figure 1. Forecasts of IGBT driver circuit market
According to Toshiba's survey, the IGBT driver market is expected to grow, accompanying the expansion of the HEV and EV markets.

This report describes the TB9150FNG, a newly developed opto-isolated IGBT gate pre-driver for automotive inverter applications. Incorporating photocouplers and control circuitry for IGBT drivers in a single package, the TB9150FNG simultaneously becomes the miniaturization and multifunction of inverter systems.

2. Features of the TB9150FNG

In inverter systems for HEV and EV applications, the domain that handles signals from a microcontroller unit (MCU) (hereinafter, the "control function") and the domain that includes a motor controller/driver (hereinafter, the "drive function") operate at different voltages.

Since the high-voltage domain generates much electrical noise, a high level of isolation is required between the control and drive function. In addition, the multifunction are often required for a controller in the high-voltage domain, such as protection circuits necessary to drive IGBTs efficiently.

The TB9150FNG integrates, in one package, an integrated circuit (IC) in the control function, an IC in the drive function, and photocouplers that provide electrical isolation between the two ICs. The TB9150FNG provides not only the miniaturization and multifunction but also high isolation between the two functions. Since photocouplers provide complete electrical isolation signal transmission method, they are also expected to have an excellent immunity to external noise, including a high electromagnetic susceptibility (EMS) immunity.

Furthermore, the TB9150FNG incorporates multifunctions such as a constant-current source and an analog-digital (AD) converter for temperature-sense diodes. Therefore, the TB9150FNG is capable of measuring the temperatures of the driven IGBTs if they integrate a temperature-sense diode. Monitoring the IGBT temperatures at high accuracy helps to improve the efficiency of a power module and therefore contributes to improving the fuel efficiency of HEVs and the electricity efficiency of EVs.

The TB9150FNG also contains a flyback controller, a current sensor, and a short-circuit detector using a desaturation (DESAT) voltage monitor (**Figure 2**). These on-chip features also help to reduce the size of an inverter system.

3. Package design

The insulation performance is important for the protection of a human body, printed circuit boards, and an overall system. Therefore, safety standards of many countries have statutory regulations for the design of electronic devices based on the International Electrotechnical Commission (IEC).

Although the most important function of photocouplers is to provide electrical isolation, the safety standards also stipulate the minimum physical distance between the isolated domains. Therefore, in designing photocoupler packages, the isolation voltage, creepage distance(*1) and clearance distance(*2) must be carefully considered.

3.1 Isolation voltage

The TB9150FNG consists of four types of devices: a control function IC and a drive function IC as well as light-emitting elements that transmit light and light-receiving elements integrated in the ICs. To increase integration, increase the density and reduce the size of the TB9150FNG, it is housed in a multi-chip package. It is imperative to provide an isolation voltage of at least 2.5 kV between the control and drive function ICs integrated in the same package.

To meet this requirement, the package of the TB9150FNG has a chip-on-chip (COC) structure in which photocouplers have an insulator between the input (light-emitting element) and output (light-receiving element) sides.

The materials used for the insulator and adhesive were selected to provide not only a high dielectric strength but also sufficient optical characteristics such as high transparency and low refractive index to let a light signal pass. In addition, the selected materials meet the reliability requirements including heat and humidity resistance.

3.2 Creepage distance and clearance distance

In order to provide an external creepage distance (i.e., a creepage distance along the package surface) of more than 5 mm and a clearance distance of more than 8 mm in accordance with the safety standards mentioned above, the TB9150FNG is housed in a 48-pin shrink small-outline package (SSOP) measuring 8 mm (width) × 12.5 mm (length) as shown in **Figure 3**. In addition, the die pads for the control and drive function ICs are separated so that their lead frames are sufficiently apart from each other. Furthermore, in order to provide a sufficient external creepage distance, the package was designed in such a manner that metal items are not exposed except external pins such as suspension pins.

4. Issues concerning the package structure and solutions

Figure 4 lists the characteristics that must be veri-

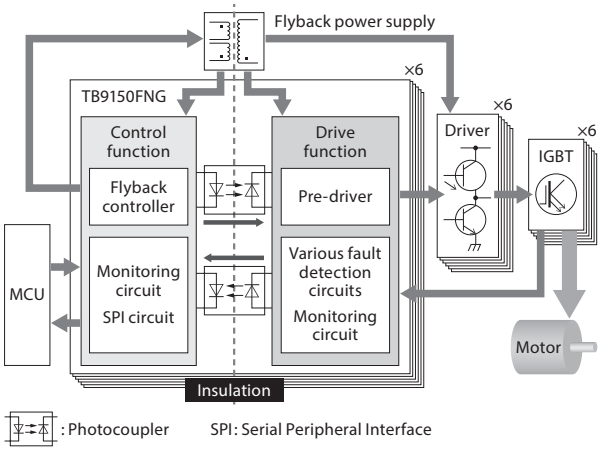

Figure 2. Example of inverter system
Optically coupled photocouplers are integrated to provide high electrical isolation and reduce the overall system size.

(*1) the shortest distance between two conductors (i.e., input and output pins) over an insulator's surface

(*2) the shortest distance between two conductors (i.e., input and output pins) through air

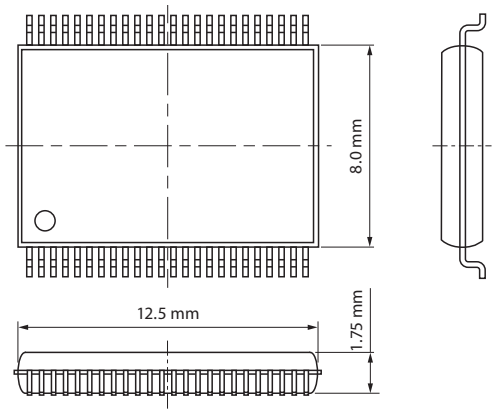

Figure 3. Outline of SSOP package for TB9150FNG
Measuring 8 mm (width) × 12.5 mm (length), the SSOP provides an external creepage distance of 5.0 mm or greater in accordance with the IEC safety standard.

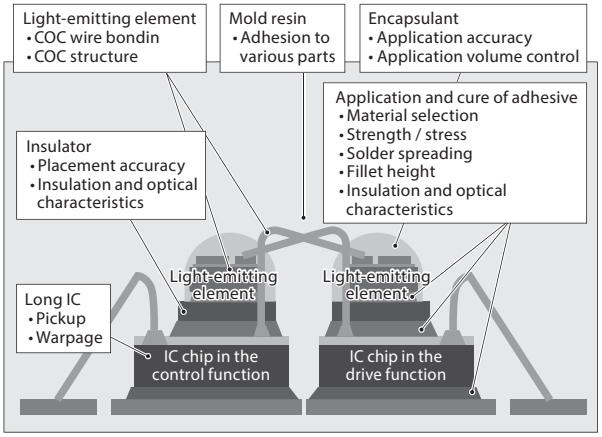

Figure 4. Cross-sectional structure and verification items of SSOP package for TB9150FNG
Various characteristics were verified to realize a multi-chip package that integrates four devices.

fied concerning the cross-sectional structure and packaging of the TB9150FNG. The following subsections exemplify packaging technologies used to fulfill these requirements.

4.1 Die bonding technology

As described above, the SSOP package for the TB9150FNG has two die pads side by side with spacing necessary to isolate the control function and drive function domains. These die pads have an aspect ratio of 1:2, and the control function and drive function IC chips are bonded on each of them. After die bonding, adhesive is cured. During this process, shear stress is applied to the adhered surface because of a difference in a coefficient of linear expansion between the lead frame and the adhesive. Consequently, a bending moment is induced on the IC chips, causing them to be warped along the length with lower rigidity. Large warpage of an IC could

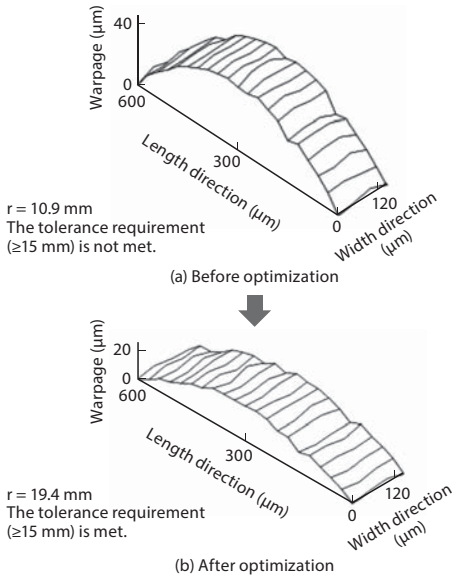

Figure 5. Results of chip warpage measurements after die bonding
Warpage was measured with a three-dimensional (3D) shape measurement system.

degrade the adhesiveness between the insulator and the light-emitting element in it. In the worst-case scenario, the insulator could be delaminated, For example, assuming that a laminated insulator on a chip is 600 μm long, warpage must be kept below 3 μm even when the thickness of mount paste is taken into consideration. In the case of this insulator, it is equivalent to a radius of curvature, r, of 15 mm or greater. We have optimized the physical properties of adhesive and the die bonding process in order to achieve an r of 15 mm or greater (**Figure 5**).

4.2 Wire bonding technology

Light-emitting elements sit at the top of the COC structure. It is therefore necessary to connect bonding wires to elements that are not only placed high but also are unstable since three devices are vertically stacked.

For wire bonding, an ultrasound thermocompression bonding machine is employed. Key parameters for ultrasound thermocompression include temperature, time, load, ultrasound frequency, power and amplitude. If these parameters are set excessively high in an attempt to assure bonding reliability, the light-emitting elements could be physically damaged or even cracked. In order to accommodate fragile structures, we adopted bonding capillaries(*3) and wires and optimized bonding parameters with the result that both improve bonding reliability (increased bonding strength) and low-damage bonding have been achieved (**Figure 6**).

(*3) Expendable tools used by wire bonding machines. Bonding capillaries are precision tools designed according to devices to be bonded.

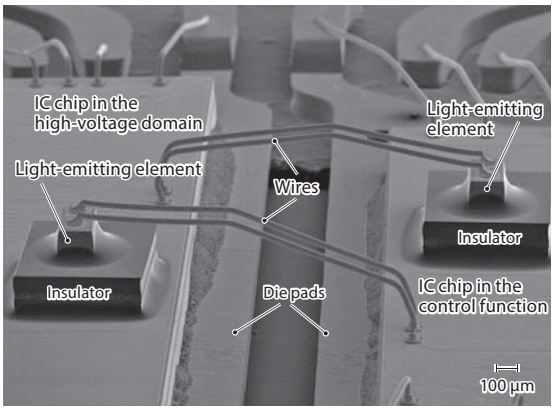

Figure 6. Scanning electron microscope (SEM) image of wires bonding between light-emitting elements with COC structure and IC chips
The materials and bonding parameters were optimized to improve bonding reliability and realize low-damage bonding.

5. Reliability evaluation results

As described above, the TB9150FNG contains photocouplers in a COC structure consisting of a light-emitting element, a light-receiving element, and an insulator between them. We performed a reliability test of the TB9150FNG to evaluate the current conduction characteristics (open/short: O/S) and the performance of the light-receiving element, I_{FHL}, of the photocouplers.

For this evaluation sample, we utilized the same 48-pin SSOP as the one used for actual products as well as the same wiring process as for actual IC chips. Regarding the encapsulant and die-attach materials, we used materials that had shown good results in a prior process evaluation and a Moisture Sensitivity Level (MSL)(*4) evaluation.

An IC chip incorporating a light-receiving element, an insulator, and a light-emitting element were stacked on the die pad of a lead frame. **Table 1** lists the reliability tests performed and their results.

Table 1. Results of reliability tests of sample packages

Test	Conditions	Evaluation item	Result (Number of failures / number of samples)
Precondition (MSL3)	30°C, 60%, 192 hours 260°C reflow, 3 passes	O/S	0/10
		I_{FHL}	0/10
TCT	–65 to 150°C, 2 000 cycles	O/S	0/10
		I_{FHL}	0/10
PCT	121°C, 100%, 200 hours	O/S	0/10
		I_{FHL}	0/10

PCT: pressure cooker test

(*4) A rating that indicates a device's susceptibility to damage due to moisture absorbed during reflow soldering stipulated by a standard of the JEDEC Solid State Technology Association.

The O/S and I_{FHL} characteristics were evaluated before and after reliability tests to check the changes of values. In addition, we checked for abnormalities with visual inspection, ultrasound inspection, and cross-sectional observation.

The reliability evaluation showed that no sample had a significant change in O/S and that all samples met the standard requirements. The I_{FHL} values and the percentage of their changes were also within the range of the standard requirements.

Furthermore, in temperature cycling test (TCT), the chip surfaces and the proximity of adhesive of the samples were examined through ultrasound inspection and cross-sectional observation after 2 000 cycles of temperature cycling. As a result of TCT, no delamination from the encapsulant was found.

It was confirmed that the SSOP package has satisfactory reliability when made of the prototype materials and with the structure described above.

6. Conclusion

In recent years, higher environmental performance has been required for automobiles. Accordingly, demand for HEVs and EVs powered by an electric motor using an IGBT inverter is expected to continue to grow. Accompanying this trend, demand for the miniaturization and multifunction of IGBT inverter systems is expected to increase. As IGBT inverter systems become more miniaturization and multifunction, their applications may spread to other industries.

In order to meet the miniaturization and multifunction requirements for IGBT inverter systems, we developed the TB9150FNG, drawing on our photocoupler and driver/controller IC design technologies. Sampling began in April 2016, with mass production slated for 2018.

We will continue to develop the package lineup to apply TB9150FNG structure in which the miniaturization and multifunction can be expected.

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Small and Lightweight Packaging Technology for Four-Channel Power Amplifier ICs Applied to Car Audio Systems

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A car audio system typically has four speakers located at the front, back, left, and right of the car interior. These speakers are separately activated by individual amplifier circuits in the car audio set. As a result, four-channel power amplifier integrated circuits (ICs), in which four amplifiers are embedded in one package, are the mainstream products in this field. Toshiba has been expanding its lineup of four-channel power amplifier ICs incorporating its proprietary advanced core technologies, and leads the market with a high share. In recent years, demand has been increasing for smaller, thinner profile, and lighter weight car audio sets to secure a wide interior space and improve fuel consumption.

To fulfill these requirements, we have developed a small and lightweight four-channel power amplifier IC applying a shrink small outline package with heat sink (HSSOP) with an exposed pad (e-pad) structure for the first time in the industry(*1).

1. Introduction

Music, news and navigation, and other audio information come from in-vehicle speakers. An audio power amplifier IC is used to drive the speakers and output sound. A car audio system typically has four speakers, which are separately activated by individual amplifier circuits. Therefore, four-channel power amplifier ICs that incorporate four amplifiers in one package are commonly used for car audio applications.

Toshiba has been manufacturing power amplifier ICs for car audio applications since the 1970s. In 1991, we released a four-channel power amplifier IC housed in a thermally enhanced HZIP package (a zigzag in-line package with a heat sink).

We have since expanded our portfolio of power amplifier ICs to meet market needs. Our main products are high-efficiency and high-reliability four-channel amplifier ICs fabricated using 0.13-μm processes with the industry's lowest-class on-resistance that deliver 45 W to 50 W per channel(*2). Additionally, we have been accelerating the development of power amplifier ICs that provide high sound quality through reduced noise and enhanced high-frequency performance, as well as reduced power consumption through the use of a Class-KB(*3) topology, and self-diagnostic functions (**Figure 1**). Car audio head units are expected to continue to become smaller, thinner and lighter in order to allow wider interior space and improve fuel efficiency. Accordingly, semiconductor devices need to be optimized to meet the requirements of their applications.

In response, we have developed the industry's first small and lightweight four-channel amplifier IC housed in an HSSOP package with an e-pad structure.

This report provides overviews of the HZIP and HSSOP packages and describes the packaging technologies used for the development of the HSSOP package.

2. Market requirements and challenges

Our four-channel amplifier ICs for car audio applications maintain a high market share due to advanced core technologies supporting their high reliability and high withstand voltage. At present, our mainstream products are power amplifier ICs in a thermally enhanced through-hole HZIP package. In addition to single DIN (50 mm-high) and double DIN (100 mm-high) car audio head units(*4), low-profile head units with a height of a half DIN (25 mm) are now appearing on the market. This trend is driving the need for semiconductor packages that help to reduce the size and thickness of audio head units.

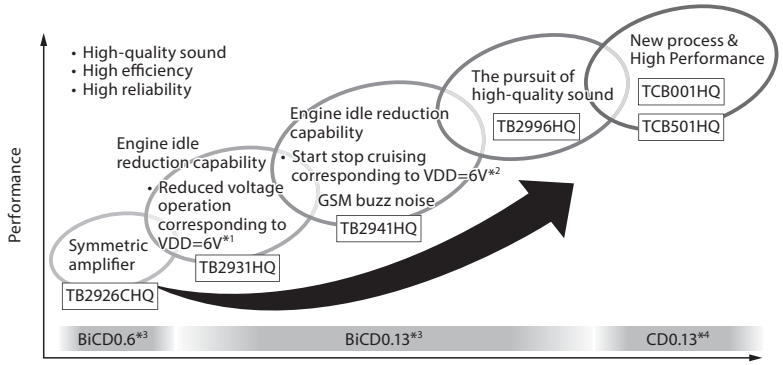
In addition, a reduction in weight of automotive elec-

(*1) As of March 2016 for four-channel power amplifier ICs (as researched by Toshiba)

(*2) As of March 2016 for four-channel power amplifier ICs (as researched by Toshiba)

(*3) Toshiba's proprietary high-efficiency power amplifier class that generates less heat and provides a reduced loss in high-amplitude mode

(*4) Standard size for car audio head units originally established by the German standards body Deutsches Institut für Normung as DIN 75490 and later standardized as the International Organization for Standardization (ISO) 7736 standard in 1984. The term "the DIN size" is still used.



GSM: Global System for Mobile Communication

*1: The minimum operating voltage was reduced to improve tolerance for radio noise.

*2: This device incorporates a feature for reducing noise and intermittent sound dropout due to sudden rise and fall in battery voltage caused by the shutdown and restart of the engine.

*3: A mixed process that combines a 0.6/0.13 µm complementary metal-oxide semiconductor (CMOS) devices with lateral double-diffused MOS (LDMOS) devices, bipolar transistors, and various analog devices

*4: A process made more cost-competitive by removing bipolar transistors from the BiCD 0.13 process

Source: "Power Amplifier ICs" on Toshiba's website

Figure 1. Trends in performance of Toshiba four-channel power amplifier ICs[1].
We have employed successive 0.13 µm processes to reduce on-resistance and improve reliability.

tronics has always been required to improve fuel efficiency.

Figure 2 shows the structure of an audio head unit and the use of an HSSOP package to reduce its size and thickness. In contrast to the through-hole HZIP package that needs to have a certain thickness and depth to attach a heat sink on the backside, the HSSOP package is mounted on the surface of a printed circuit board (PCB) and helps to reduce the size, thickness and weight of an audio head unit. Furthermore, the HSSOP package simplifies reflow soldering onto a PCB.

The market of four-channel power amplifier ICs will remain strong as it is expanding to emerging countries and digital amplifiers are becoming more common. In the future, roughly half of the current high-efficiency amplifiers in a through-hole HZIP package are predicted to be replaced by those in a surface-mount HSSOP package.

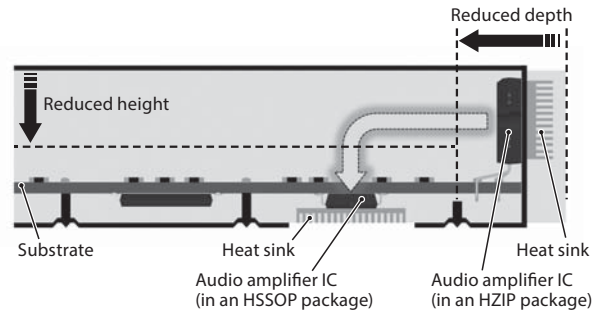


Figure 2. Structure of car audio head unit showing downsizing and thinner profile.
Replacing a through-hole HZIP package with a surface-mount HSSOP package helps to reduce the size and thickness of a car audio head unit.

3. Comparisons of package designs

3.1 Existing HZIP package design

Due to a high current output, four-channel power amplifier ICs must be housed in a package with high heat dissipation. In the case of an HZIP package, a chip is mounted on one side of a heat sink, the other side of which is exposed to the ambient. Heat generated by the chip can be dissipated efficiently by bonding it to a board-level heat sink.

Figure 3 shows the external outline and the internal structure of the existing HZIP package, HZIP25-P-1.00F. In order to provide high heat dissipation performance, HZIP25-P-1.00F has a double-layered structure consisting of a copper alloy leadframe with high thermal conductivity and a heat sink on which a chip is mounted. The leadframe and the heat sink are joined by caulking.

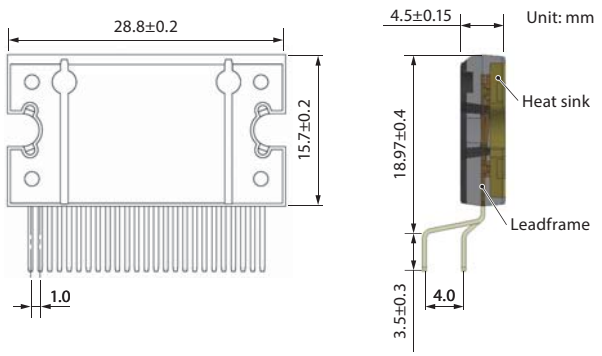


Figure 3. Dimensions and internal structure of HZIP package.
A heat sink is exposed on the back of the package to enhance heat dissipation performance.

3.2 Package design

We developed a new HSSOP package for four-channel power amplifier ICs to reduce the size and weight. Taking market trends into consideration, its external dimensions were determined based on the 36-pin shrink small-outline package (SSOP) with MO-166 dimensions (body size: 11.0 ×15.9 mm, height: 3.15 mm) registered with the Joint Electronic Devices Engineering Council (JEDEC) Solid State Technology Association. This package is hereinafter referred to as HSSOP36.

Figure 4 shows the external outline of the HSSOP36 package. Although bonding a heat sink onto a leadframe as in the HZIP package is effective in dissipating heat, this double-layered structure makes it difficult to reduce the size and weight of a package. Instead of a heat sink, we adopted an e-pad structure for the HSSOP36 package in which die pads on a leadframe are exposed to the ambient. In order to minimize degradation of heat dissipation performance due to the heat sink-less structure, e-pads were designed to be as large as possible (7.8×6.4 mm). In order to realize large e-pads, we changed the ratio of thickness of mold resin (thermosetting epoxy resin containing silica) upper and lower the leadframe to 3:1. The reasons for this change are described below. Figure 4 shows the internal structure of the HSSOP36 package. In general, it is desirable that the upper and lower molds should have a thickness ratio of 1:1. However, since the mold resin of the HSSOP36 package is 3.15 mm thick, the ratio of 1:1 causes the vertical distance between a chip and the inner leads of the package to be long. Long bonding wires could have higher on-resistance, melt due to high electric current, or come into contact with each other during molding. In order to prevent these problems, the thickness ratio of the upper and lower molds was changed to 3:1.

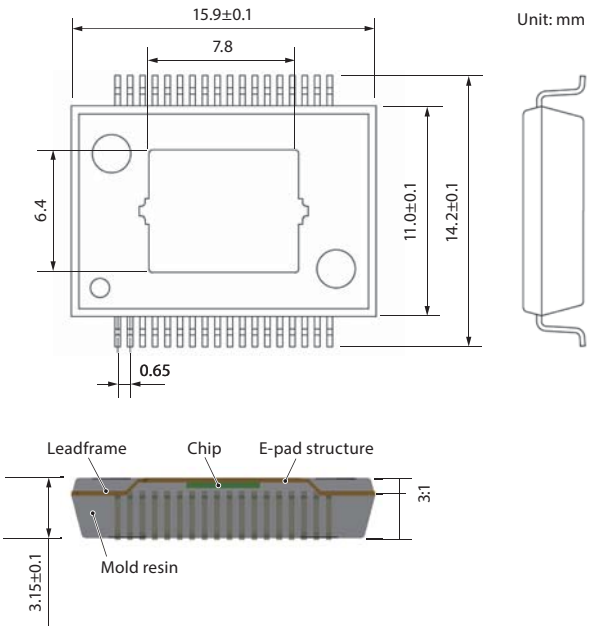


Figure 4. Dimensions and internal structure of HSSOP36.
The HSSOP36 package has an e-pad structure to provide enhanced heat dissipation performance. The upper and lower molds have a thickness ratio of 3:1.

4. Packaging technologies

It was necessary to apply various existing technologies to realize the design of the HSSOP36 package. Among them, this section focuses on multi-tier high-loop wire bonding and mold resin flow simulation.

4.1 Multi-tier high-loop wire bonding

Wire bonding is the process of making electrical interconnections between a chip and a leadframe. Since four-channel power amplifier ICs deliver a high current, the interconnections in the package are made using many thick bonding wires. In addition, the downscaling of the package causes the wire bonding density to increase. Taking account of these factors, we considered the optimal loop shape for bonding wires.

Figure 5 shows the result of the bonding wire layout using a three-dimensional (3D) computer-aided design (CAD) system. Wires are connected from the bonding pads on a chip to the inner leads of a package higher than the chip surface. It is important to allow for sufficient spacing between wires to prevent interference between them. For the development of the HSSOP36 package, we needed to consider not only lateral but also vertical interferences between adjacent wires. Based on the results of 3D CAD analyses from various perspectives, we experimented with loop heights in incremental steps to work out a design free from wire-to-wire interference.

Figure 6 shows the bonded wires. The use of a 3D CAD system made it possible to allow for sufficient spacing between bonding wires.

4.2 Simulation of resin flow for molding

The wire-bonded chip is encapsulated and sealed in resin. Since the upper and lower molds are designed to have a thickness ratio of 3:1 as described above, it is difficult to flow resin uniformly into the upper and lower

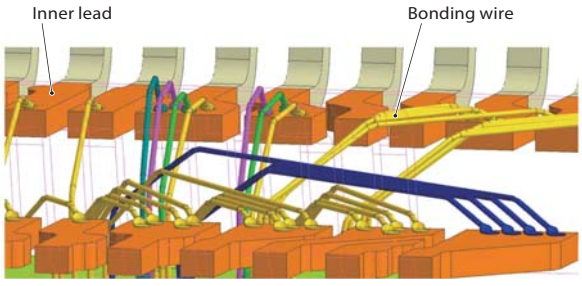


Figure 5. Confirmation of bonding layout using 3D CAD.
We experimented with multiple loop heights in incremental steps to create a design free from interference between adjacent wires.

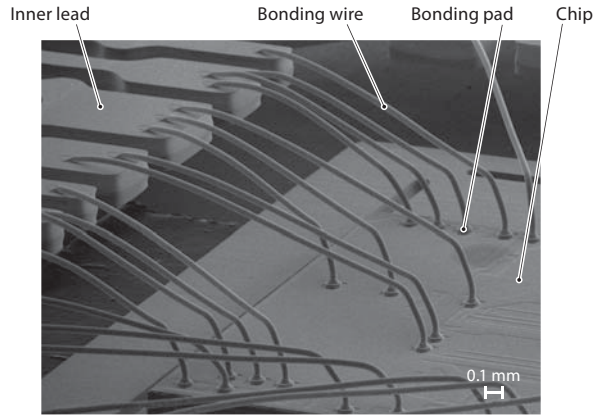
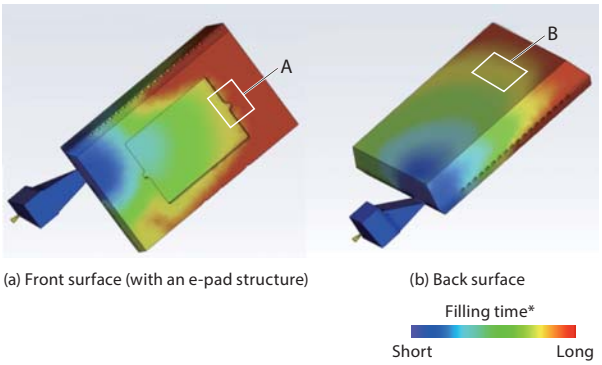


Figure 6. Wire bonding with high loop shape.
A 3D CAD tool was utilized to create a design free of wire-to-wire interference.



* Time taken for the injected mold resin to reach the designated level

Figure 7. Simulation of resin flow for molding of HSSOP36.
The front and back sides of the package are filled at different rates due to a difference in the width of the mold resin gates.

cavities. A difference in resin flows could create defects such as empty space and voids. For the development of the HSSOP36 package, we simulated resin flows to visualize how resin fills the mold cavities in order to optimize a mold design and forming conditions.

Figure 7 shows an example of a result of this simulation. The comparison of A and B in Figure 7 shows that the flow rate of mold resin is slower on the front side (i.e., e-pad side) than on the back side. This occurs because, due to the difference in mold thickness above and below the leadframe, the cavity on the back side of the package is wider, making it easier for resin to flow into.

Based on the results of simulation, we optimized the runner for injecting molten resin into the cavities of the mold, the gate shapes, and mold forming conditions in order to minimize the difference in the resin flow rate between the front and back sides.

4.3 Summary of the HSSOP packaging technologies

By utilizing packaging technologies such as multi-tier high-loop bonding and mold resin flow simulation, we realized the HSSOP36 package that has approximately 60% smaller footprint area and approximately 80% less weight than the conventional HZIP package.

5. Conclusion

We developed a surface-mount HSSOP package with an e-pad structure (i.e., with die pads exposed to the ambient) for four-channel power amplifier ICs for car audio applications for the first time in the industry. We will continue to develop packages that will contribute to application differentiation according to market trends.

Reference

(1) Toshiba. "Power Amplifier ICs." Toshiba homepage. Accessed August 22, 2016. https://toshiba.semicon-storage.com/ap-en/product/automotive/power-amp.html.

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Technologies to Reduce Manufacturing Cost of Super-Small Package for Semiconductor Devices

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With the increase in the number of parts installed in tablets and wearable devices accompanying the progress of telecommunication technologies and expanding multifunctionality, demand has been growing in recent years for higher density packages to reduce the size and thickness of such products. Toshiba released the SC2 super-small package for semiconductor devices, with dimensions of 0.62 mm in width, 0.32 mm in length, and 0.3 mm in height, in 2004 to cater to this demand.

Going to a step further, we developed the SL2 package, a new low-cost super-small package with the same dimensions as the SC2, in September 2014. Through the application of a stamped lead frame to the SL2 based on our accumulated technologies in addition to newly developed technologies, the SL2 package realizes a 33% reduction in manufacturing cost compared with the SC2.

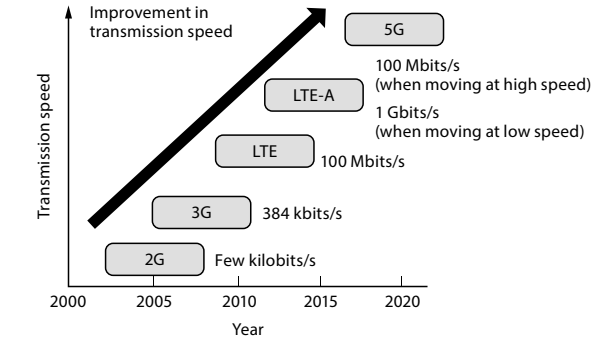
1. Introduction

Semiconductor packages are used in home appliances, PCs, automotive electronics and many other electronic devices. Demand for small-signal semiconductor devices for tablet and wearable applications has been expanding. The market for small-signal devices for these applications alone is expected to reach 100 billion yen worldwide.

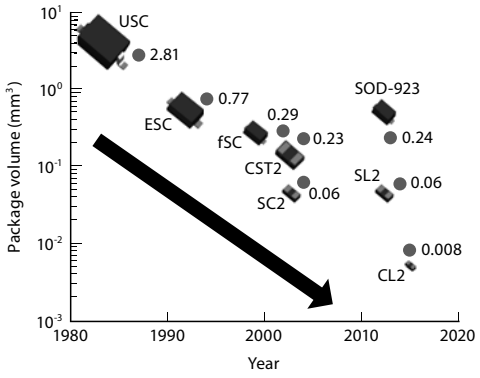
Due to continuous progress in telecommunication technologies in recent years, electronic devices provide ever-higher communication speeds, and more sophisticated and multifunction. As a result, the number of parts used in electronic devices is increasing. There is also demand for longer battery operation time, increasing the capacity, and therefore the size, of a battery pack, and thus leaving less space for electronic parts. In these circumstances, printed circuit boards (PCBs) have been becoming ever smaller, making semiconductor packages smaller and thinner (**Figure 1**).

While packages measuring 1.0 mm wide by 0.6 mm long are most commonly used in the market, a transition to a 0603 package with dimensions of 0.6 mm wide by 0.3 mm long has been accelerating so as to enable higher-density PCB assembly. In response, Toshiba began mass production of the SC2 package in 2004.

In order to meet a market requirement for further size reduction, we developed the SL2 super-small, low-cost package and started its mass production in September 2014. This report describes the enabling technologies for SL2.



(a) Progress of communication technology



(b) Trends in package size and thickness

2G: second generation 3G: third generation LTE: Long Term Evolution
LTE-A: LTE-Advanced 5G: fifth generation

∗ USC, ESC, CST2, fSC, SOD-923, SC2, SL2, and CL2 are package names.

Figure 1. Trends in transmission speed and package size.
In recent years, the transmission speed of telecommunication equipment has been increasing, and semiconductor packages have been becoming ever smaller and thinner.

2. SL2 overview

The new super-small, low-cost SL2 package was designed as a cost-competitive variant of the SC2 package. Its target cost was set 33% below that of the SC2 package, considering the results of benchmarking of other companies' packages and price decline predictions. In order to achieve this target, we chose to replace the electroformed substrate that accounted for the highest percentage of the total direct material cost with a stamped lead frame.

The SC2 package utilizes an electroformed substrate with thin electrodes in order to house a chip and a bonding wire in a body as thin as 0.3 mm. In addition, in order to improve material utilization, the SC2 package is assembled using a batch forming process like the one for molded array packages (MAPs). Semiconductor devices in the SC2 package are singulated into finished products during a dicing process. In contrast, for the low-cost SL2 package with a stamped lead frame, semiconductor chips are encapsulated in a single mold cavity format.

Figure 2 compares the previous SC2 and newly developed SL2 packages.

Both the body and the electrodes of the SL2 package must be sized so as to allow the use of the same PCB land pattern as for the SC2 package. Due to the use of a stamped lead frame, the electrodes of the SL2 package are three times as thick as those of the SC2 package. The thickness of a chip to be bonded on an electrode has not changed. Therefore, in order to keep the highest point of the bonding wire below a certain height, low-loop bonding is employed for the bonding wire of the SL2 package that connects between the top surface of the chip and the adjacent electrode. Furthermore, whereas the SC2 package is formed by MAP molding during the dicing process, the SL2 package is encapsulated in a single cavity mold format. This makes the longer sides of the SL2 package slanted. The slanted sides reduce the interior space of the SL2 package, making it necessary to assemble it at a higher precision.

Accompanying the replacement of an electroformed substrate by a stamped lead frame, the assembly process flow for the SL2 package has been changed. **Figure 3** compares the assembly process flows for the SC2 and SL2 packages. The SL2 assembly process flow was developed based on our conventional packages using a stamped lead frame.

The following assembly technologies were utilized to overcome many challenges we faced in developing an assembly process flow for the SL2 package:

(1) Lead frame stamping for super-small packages
(2) Narrow-pitch wire bonding
(3) Low-loop wire bonding
(4) Single-cavity molding
(5) Mold filling for super-small packages
(6) High-precision die bonding
(7) Conveyance, measurement and packing of super-small packages

Among these technologies, lead frame stamping, low-loop wire bonding, single-cavity molding and high-precision die bonding are particularly important. These technologies are described below.

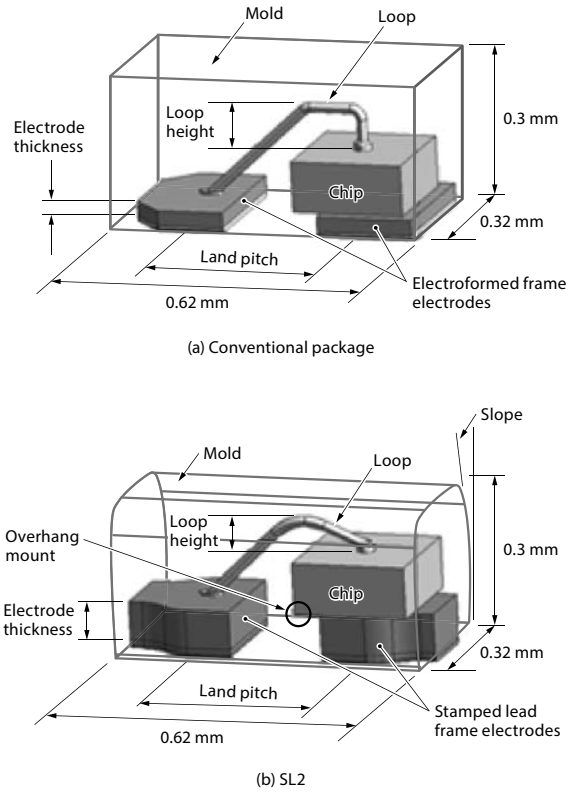


Figure 2. Comparison of previous SC2 and newly developed SL2 packages.
In order to reduce cost, the electroformed substrate was replaced with a stamped lead frame.

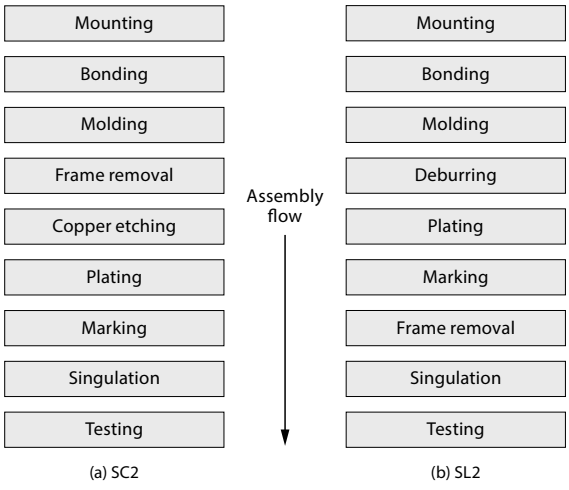


Figure 3. Comparison of assembly processes of SC2 and SL2.
The assembly process has been modified according to the SL2 package with a stamped lead frame.

3. Low-cost packaging technologies

3.1 Lead frame stamping technology

Lead frames are classified into two types: stamped lead frames formed using a stamping metalworking process and chemically etched lead frames. We adopted a stamped lead frame for the SL2 package since stamping was more likely to help reduce cost. This was our first attempt to use a stamped lead frame for a package as small as 0603. However, we had utilized a stamped lead frame for many surface-mount packages before. Drawing on accumulated and new technologies, we succeeded in using a stamped lead frame in a super-small package.

Since stamped lead frames are formed with a stamping metalworking process, they are more susceptible to deformation than electroformed substrates. Since small packages have thin leads and do not provide sufficient space for holding them down during stamping, leads can easily be twisted. Twisted leads make it difficult for die bonding and wire bonding machines to recognize the images of leads and thus degrade the precision of die and wire bonding necessary for super-small packages. In order to reduce variations of deformation and thus an adverse impact on subsequent processes, we reviewed the structure of the metal stamping die and optimized the metalworking process.

In addition, since a chip is mounted with an overhang as shown in Figure 2, burrs produced by stamping can cause die bonding defects. To prevent this problem, burrs must be flattened. However, we found that a burr flattening process causes entire package leads from the seating plane to their tips (i.e., chip mounting area) to lift. Lifted leads affect the molding process and cause a large amount of resin to overflow to the back of the package. Leads were lifted because of a springback caused by the burr flattening process and insufficient lead strength. To address this problem, we utilized a flattening punch, taking the amount of lifting into consideration.

3.2 Low-loop wire bonding technology

The use of a stamped lead frame causes electrodes to become thicker, imposing a restriction for the loop of the bonding wire that connects the chip surface to the adjacent electrode. Therefore, low-loop wire bonding is necessary. However, using the conventional loop forming method for low-loop wire bonding causes excessive stress to be applied to the upright section of the wire and damages it. To prevent this problem, we flattened the upright section of the bonding wire (**Figure 4**). As an alternative means, we also considered using bump bonding that forms low-loop from the electrode side. However, since bump bonding reduces throughput, we opted for low-loop bonding without an upright section, in SL2.

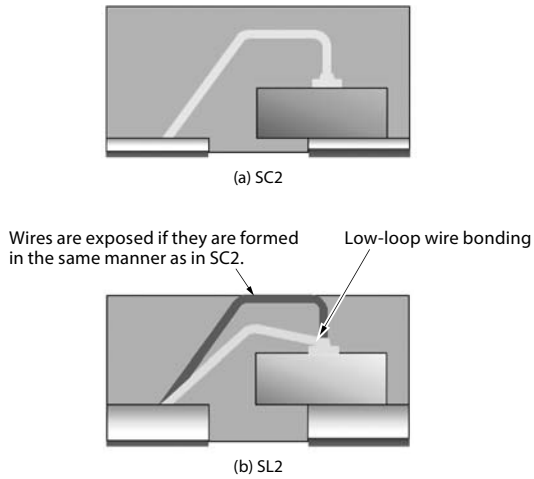


Figure 4. Comparison of loop profile of SC2 and SL2.
The use of the conventional bonding wire design causes it to be exposed to the ambient. Therefore, low-loop wire bonding without an upright section is used for the SL2 package.

Furthermore, there was a concern that, because of a low loop, the bonding wire could be short-circuited to the edge of the chip in the field when used in various conditions. In order to prevent this problem, we identified factors that could potentially cause variations in the loop height and predicted variations due to each factor. Based on the result of evaluation on the limit concerning short-circuiting, we performed material tolerance management and set the ranges of parameters for manufacturing equipment. In addition, for abnormality detection, we defined acceptance criteria for the highest point of the bonding wire to be the same level as the chip edge. The loop height is adjusted as part of product quality control in order to ascertain the distance between the chip edge and the bonding wire.

3.3 Single-cavity molding technology

The SC2 package is encapsulated by combining an electroformed substrate and MAP molding. After molding, the backside of the substrate is peeled off to expose the electrodes on the backside of the package. Therefore, MAP molding requires the use of a substrate that does not cause mold resin to overflow to the back of the package. In contrast, the SL2 package has a through-hole section through which resin drips onto the stamped lead frame. Generally, the backside of the lead frame is covered with a polyimide sheet before the molding process in order to prevent an overflow of resin to the backside. However, the use of a polyimide sheet causes the indirect material cost to increase.

Instead, we employed a single mold cavity format in which the mold cavities for individual packages are linked with a continuous gate. In this method, one-sided mold consisting an upper block forming a single cavity and a flat-shaped lower block was adopted. In addition,

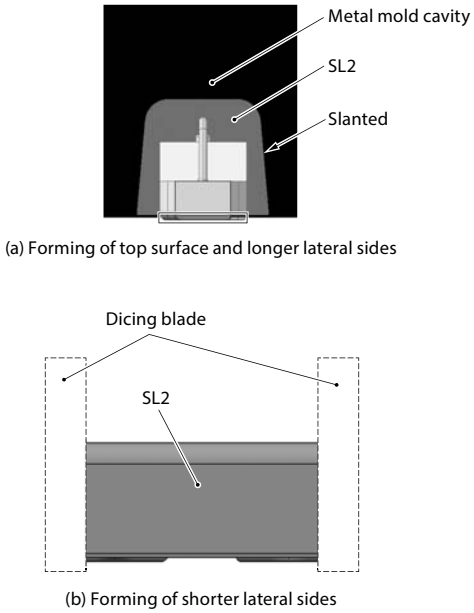


Figure 5. Molding method of SL2.
The top side and the longer lateral sides of the SL2 package are formed by molding, and the shorter lateral sides are formed during a dicing process.

the SL2 package has slanted sides in order to improve mold release. Whereas the top side and the longer lateral sides of the SL2 package are formed by molding, the final shape of the shorter lateral sides is formed during a dicing process (**Figure 5**).

Because of single-cavity molding, sufficient space is unavailable for holding down the mold frame to prevent it from lifting. Therefore, resin burrs are produced. In order to prevent burrs, we designed a mold in such a manner that it can be held down. In addition, we reviewed the flatness of mold closure to reduce the amount of frame deformation caused by an excessive mold clamping force.

As a result of the foregoing, we succeeded in exposing the electrodes without using a polyimide sheet, making it possible to adopt single-cavity molding.

3.4 High-precision die bonding technology

Since the chip area is wider than the chip mount area in the SL2 package, the die bonding process mounts a chip with an overhang. One of the problems of a chip overhang is that a chip can tilt when its position shifts during assembly. If this happens, stress concentrates on the backside of the chip at the edge of the lead frame; a die bonding defect occurs due to the surface property of the lead frame; and reliability degrades due to bonding metal dangling. In order to prevent these problems, we have worked out the optimal conditions for the selection of machines and materials. As described in Section 3.3, the SL2 package has slanted sides in order to improve mold release. This reduces tolerance for the precision of

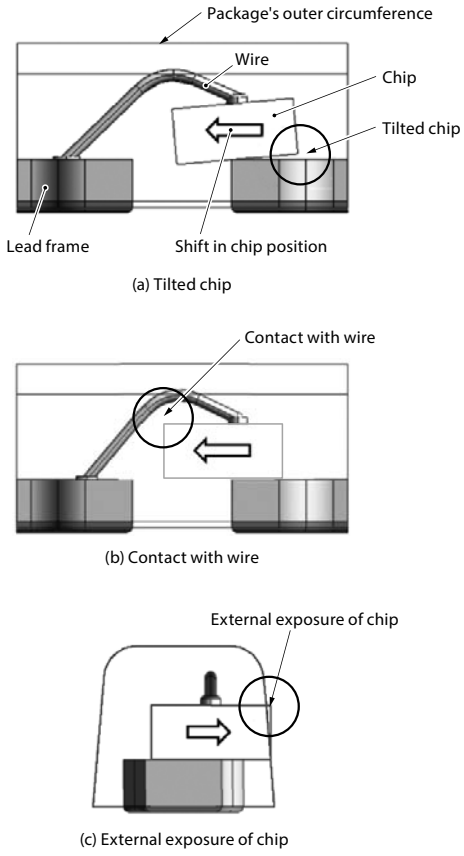


Figure 6. Examples of defects caused by chip position shift.
A chip could tilt, a bonding wire could get into contact with an edge of the chip, and the chip could be exposed to the ambient. To prevent these problems, higher positioning precision is required for die bonding.

chip positioning.

Figure 6 shows examples of defects caused by a chip position shift. Contact of the bonding wire with an edge of the chip and exposure of the chip to the ambient could cause a serious problem concerning product quality. Therefore, the die bonding process of the SL2 package requires higher chip mounting precision than that of the SC2 package.

The die bonding machine for the SL2 package uses a direct pickup method to achieve high throughput. However, the assembly precision requirement for the SL2 package was more stringent than that achievable with this machine. Therefore, we endeavored to develop a solution that provides both high throughput and high positioning precision. First, we examined the motion of the direct-pickup transfer nozzle when it moves and stops using a displacement sensor and a high-speed camera. Based on its result, we have optimized the trajectory of the transfer nozzle. Next, in order to reduce variations in the chip position caused by an impact upon the pickup and drop-off of the chip, we have added a soft-touch sequence to the die bonding machine. The die bonding machine is equipped with a

heater unit and an inert gas system to conduct eutectic metal bonding. It was found that the resulting heat haze obscures the images from image recognition cameras, degrading their accuracy. To address this problem, we have improved the haze removal function to enhance the image recognition accuracy. In addition, we have improved the calibration functions for the transfer nozzle and the work detection camera and optimized the operating conditions of chip pickup needles. As a result of the foregoing, we have successfully fulfilled the positioning precision requirement for the assembly of the SL2 package.

4. Conclusion

The technologies developed to reduce the manufacturing cost of the super-small SL2 package are described herein. In order to achieve the cost target, we replaced an electroformed substrate with a stamped lead frame and developed an assembly process that suits the requirements of the stamped lead frame.

To fulfill rapidly changing market needs, we will continue to develop further cost-competitive and high-pin-count packages, drawing on the newly developed technologies.

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"Environment Sensing Logger" Equipped with ApP Lite Processor Providing IoT Solution

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In the logistics business field, demand has recently been increasing for improvement of transportation quality through the monitoring of freight transportation conditions, as well as for enhancement of product quality through the elucidation of product storage environments.

In response to these diverse requirements, Toshiba developed an "environment sensing logger" for business-to-business (B2B) services in June 2015. This environment sensing logger incorporates the following features: (1) an all-in-one sensor capable of sensing of five types of environmental data (temperature, humidity, pressure, illuminance, and shock); (2) the ApP Lite TZ1001 processor, which provides an Internet of Things (IoT) solution and realizes a long battery life allowing continuous operation for about two months on a full charge; and (3) a waterproof and dustproof construction compliant with the IP67(*1) ratings for dust and water ingress stipulated by Japanese Industrial Standard (JIS) C 0920 and the U.S. military standard drop tolerance requirements (MIL-STD(*2)-810). These features make it possible to apply the environment sensing logger to a broad range of applications.

1. Introduction

The global market for the transportation and logistics industry amounts to more than 150 trillion yen per year. In this market, more than four trillion yen worth of goods are damaged per year. Therefore, improving transportation quality is a significant issue. One of the solutions is to include an electronic logger for monitoring transportation conditions in freight containers. Loggers are attracting great interest in the field of transportation and logistics as they help manage and improve transportation quality.

In addition, there is a need to monitor manufacturing equipment to determine whether it is operating properly, in order to increase its availability. Services that address this demand by monitoring the operating conditions of machines with loggers and replacing machine parts before they fail, thereby improving productivity, are also attracting attention.

Nowadays, there are new services for building users that are designed to maintain a comfortable environment based on the recording and analysis of environmental data inside buildings.

This report provides an overview of, and describes the functionality of, an environment sensing logger developed by Toshiba to meet these market needs (**Figure 1**).

(*1) Degrees of protection provided by enclosures stipulated by Japanese Industrial Standard (JIS) C 0920

(*2) United States Military Standard

Figure 1. Environment sensing logger.
This unit incorporates an all-in-one sensor capable of sensing five types of environmental data and provides water and dust ingress protection as well as shock resistance.

2. Hardware structure and main specifications

The newly developed environment sensing logger incorporates five sensors for temperature, humidity, air pressure, illuminance, and shock. This environment sensing logger measures 100 (width) × 36 (depth) × 31 (height) mm including the cover casing and weighs approximately 110 g. The internal lithium-ion battery can be charged via a Universal Serial Bus (USB) interface. The battery lasts for roughly two months on a full charge (operating sensors every five minutes for 55 days). The environment sensing logger combines the sensing of five types of environmental data and a long battery time. It incorporates a nonvolatile memory to record environmental data, which can easily be exported to a PC via a USB interface. Then, the environmental data can be converted into the Comma Separated Values

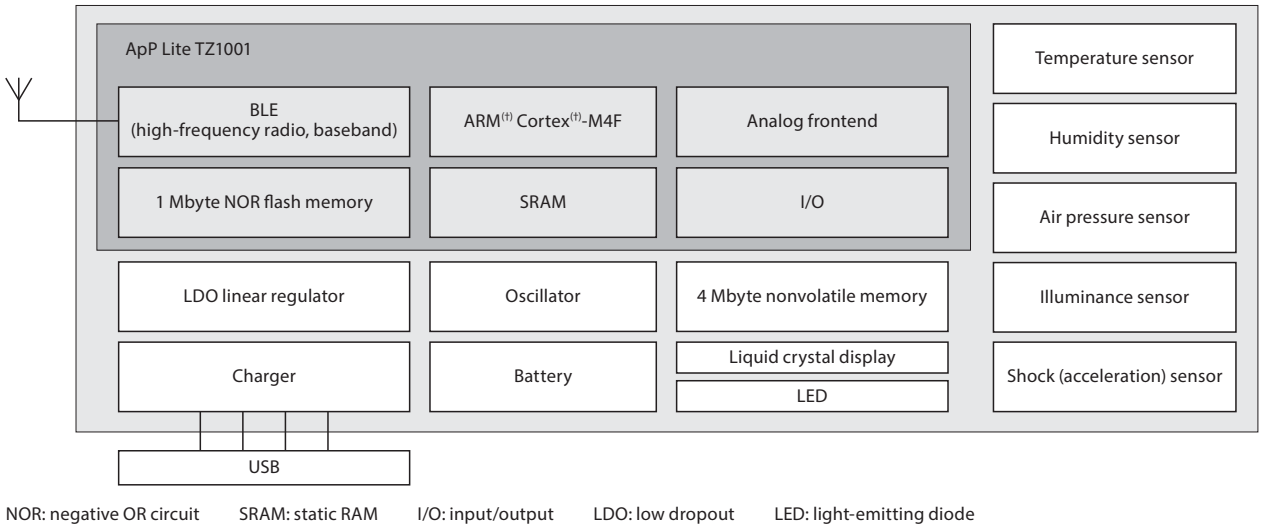

Figure 2. Block diagram of environment sensing logger.
The environment sensing logger contains five sensors for temperature, humidity, air pressure, illuminance, and shock measurement, and the ApP Lite TZ1001 processor designed for IoT applications.

(CSV) format, which can be turned into graphs, saved and printed.

Furthermore, the environment sensing logger incorporates a wireless communication device using Bluetooth(†) low energy (BLE). The BLE connection allows users to turn on and off individual sensors and set the sensing interval using a smartphone. Also, the BLE connection allows users to transmit the sensing results to a cloud server in real time, making it possible to build a system in combination with gateways. These features are realized by a BLE transceiver embedded in ApP Lite TZ1001, various sensors, and a 4 Mbyte nonvolatile memory. **Figure 2** shows the block diagram of the environment sensing logger.

With the cover casing removed, the environment sensing logger complies with the IP67 water and dust ingress requirements, making it usable in a wide range of environments. When housed in the cover casing, it also meets the drop and shock resistance requirements of the MIL-STD-810 standard. **Table 1** shows the main specifications of the environment sensing logger.

Table 1. Main specifications of environment sensing logger.

Characteristic			Specification
Dimensions (WDH) (with cover casing)			100 × 36 × 31 mm
Weight (with cover casing)			Approx. 110 g
Power supply			840 mAh lithium-ion battery
Charging			USB power delivery: 4.75 to 5.25 V, 500 mA max.
Operating temperature			-20 to 70°C
Features	Sensors	Temperature	Measurement range: -20 to 70°C
		Humidity	Measurement range: 0 to 100%
		Air pressure	Measurement range: 300 to 1 100 hPa
		Illuminance	Measurement range: 0 to 65 000 lx
		Shock	Notification upon detection of shock
	Communication		USB, BLE
Continuous operation			55 days (when sensors are configured to operate every 5 minutes) *At ambient temperature of 0°C
Environmental conditions			IP67 (water and dust ingress protection), MIL-STD-810 (shock resistance)

3. Method of operation

The environment sensing logger has four operating modes: OFF, BLE, Record, and USB. Transitions between these operating modes occur when a button on the unit is pushed or when it is inserted into or removed from a USB port. **Figure 3** shows the transitions among the four operating modes.

The environment sensing logger is in OFF mode when sensing is off. In this mode, it detects a button push and USB insertion.

In BLE mode, the environment sensing logger allows an external Bluetooth device to configure its operation. In this mode, the sensing interval and the sensors to be activated can be selected using an external device such as a smartphone. In addition, the BLE mode allows users to turn on and off the recording of shock events and change the acceleration threshold for the record-

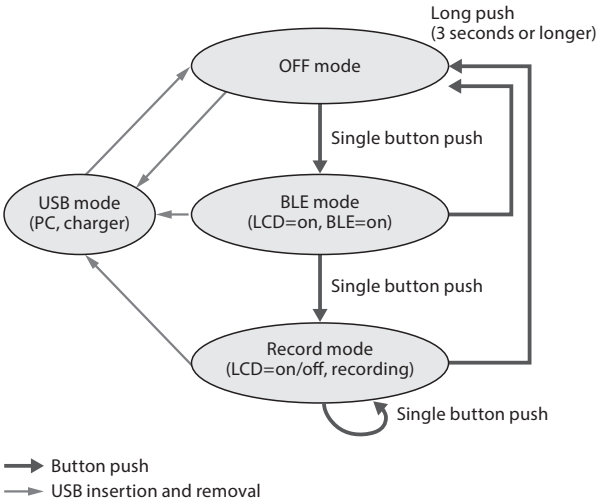

Figure 3. Transitions among four operating modes.
Transition from one operating mode to another occurs upon a button push and USB insertion.

ing of shock events. The environment sensing logger records information on shock events when it detects a change in the acceleration rate exceeding a threshold.

In Record mode, the environment sensing logger performs a sensing operation according to the settings configured in BLE mode. The sensed environmental data are stored in the integrated nonvolatile memory along with timestamps that show the time at which sensing was performed.

In USB mode, environmental data are exported to a PC via a USB interface. In this mode, no sensing is performed, and environmental data accumulated in Record mode can be viewed as a computer file on a PC. In this mode, the environment sensing logger is also charged via the USB cable.

Figure 4 shows an example of an application of the environment sensing logger. This figure shows the changes in environmental conditions of an air cargo in which the environment sensing logger was placed. These data make it easy to see the environmental conditions and shock events to which the cargo was exposed.

4. Functions

The environment sensing logger incorporates five sensors, and meets the IP67 water and dust ingress requirements as well as the MIL-STD-810 shock resistance requirements. The following subsections describe the consideration given to each constituent part of the environment sensing logger.

4.1 Temperature, humidity, and air pressure sensors

The requirements for the temperature, humidity, and air pressure sensors for environment sensing include accuracy, tracking performance, and IP67 compliance.

In order to improve the accuracy of temperature, humidity, and pressure measurement, high-accuracy parts are indispensable. To obtain the best performance from these parts and track varying environments, it is also necessary to increase their exposure to the ambient air and create paths through which air circulates. Therefore, the layout of an electric circuit board and the design of a casing are important. In addition, the temperature and humidity sensors should not be placed in the vicinity of a heat source inside the casing, in order to ensure they are unaffected by the generated heat.

Furthermore, since compliance with the IP67 water and dust ingress requirements and the MIL-STD-810 shock resistance requirements is required, it is necessary to meet multiple contradictory requirements. To satisfy all the requirements, we repeated desktop calculations and, through a process of trial and error, finalized specifications by determining the board layout, the shapes of the compartments within the casing, materials, etc.

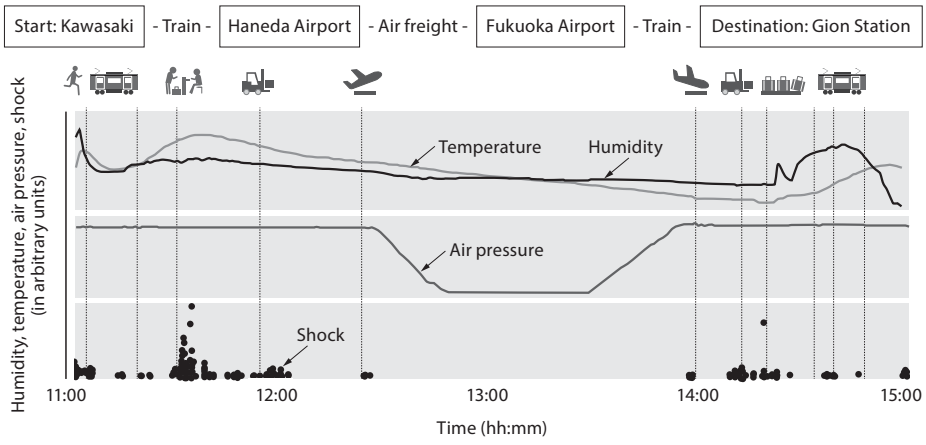

Figure 4. Example of log data of cargo shipped from Haneda to Fukuoka.
This figure shows a log of shock events that occurred when the cargo was transferred from one means of transportation to another as well as drops in air pressure in the airplane cargo hold.

4.2 Shock sensor

We decided to combine an acceleration sensor and software in order to realize the sensing of shock events. There are two reasons why we adopted this approach. One reason was that it was important to detect the occurrence of shock events exceeding a certain threshold rather than the accuracy of shock strength. The other reason was that a shock sensor consumes much more power than the other sensors.

The environment sensing logger needs to continue operating for roughly two months on a full charge, considering its application for ship cargo that does not allow for recharging during transportation. Therefore, we opted to use an acceleration sensor and experimented with it to find the optimal sampling frequency and other conditions in order to obtain the required shock detection and battery life performance. The use of an acceleration sensor also led to cost reduction.

4.3 Illuminance sensor

In addition to temperature, humidity, and air pressure, the environment sensing logger records illuminance at a regular interval. This function is designed to detect the opening and closing of a cargo during transportation. The illuminance sensor provides an event notification signal. When illuminance exceeds a threshold for open/close detection (selectable from three levels), an event time is recorded in the nonvolatile memory.

As described above, the lithium-ion battery of the environment sensing logger needs to last for approximately two months. It would have been difficult to meet this requirement if the output of the illuminance sensor were continually read out.

To resolve this issue, we decided to use an interrupt signal from the illuminance sensor. Since equations for calculating illuminance must be modified according to the wavelength components of a light source, one problem was the inability to select a threshold in use cases in which a light source cannot be identified until a cargo is opened and closed. To address this problem, we used software to adjust a threshold for the illuminance sensor according to the situation.

Many environment sensing loggers available in the market have a condensing lens to collect the light from a light source toward an illuminance sensor. However, we chose not to add a condensing lens to our environment sensing logger because of its susceptibility to shock. Instead, we selected a material for the light-collecting cover of the illuminance sensor, striking a balance between shock resistance and light transmittance.

4.4 BLE

The main purpose of the BLE transceiver embedded in the environment sensing logger is to allow users to set sensing conditions with a smartphone. Since the environment sensing logger is intended to be packed with air cargo as well as with ship cargo, it must be certified under the Radio Technical Commission for Aeronautics (RTCA) DO-160 standard, environmental condition and test procedure for airborne equipment.

In Record mode, the BLE transceiver of the environment sensing logger is off. However, its operating mode transitions from BLE mode to Record mode when a user pushes a unit button. Therefore, there was a possibility that the environment sensing logger would be left in BLE mode on an airplane if the user failed to push a button. To avoid this situation, the BLE transceiver of the environment sensing logger is automatically turned off if it does not establish a BLE connection with another device such as a smartphone for a period of 30 minutes. This period is user-selectable.

Furthermore, the environment sensing logger records transportation data using BLE advertising data. A straightforward application of BLE advertising data is its use in combination with beacons. If beacons are installed along a cargo transportation route, the logger in the cargo can record beacon information each time it detects a beacon signal. This makes it possible to acquire additional information about a transportation route based on the logged beacon information and timestamps.

Beacons are just an example. The environment sensing logger provides a universal function, which we named Advertising Data Structure Detection (ADSD).

For example, the environment sensing logger can be combined with an external sensing device capable of broadcasting the sensed results. This enables the environment sensing logger to collect environmental data that is not supported by the sensors incorporated in it.

4.5 Compliance with statutory regulations

The environment sensing logger is certified for compliance with electromagnetic compatibility (EMC) requirements according to the Conformité Européenne (CE) marking in the European Union (EU), the Federal Communications Commission (FCC) mark in the U.S.A. and Canada, the Voluntary Control Council for Interference by Information Technology Equipment (VCCI) mark in Japan, and the Underwriters Laboratories (UL) mark in the U.S.A. and Canada. In addition, we have obtained a Certificate of Construction Type of Japan and the Telecom Engineering Center (TELEC) conformity certification necessary to use BLE. We had acquired all these certificates necessary for commercial use and later obtained additional certificates in other countries in response to user requests. **Figure 5** shows examples of symbols of certifications obtained by the environment sensing logger.

The cover casing of the environment sensing logger is green as shown in Figure 1. There is a reason for this.

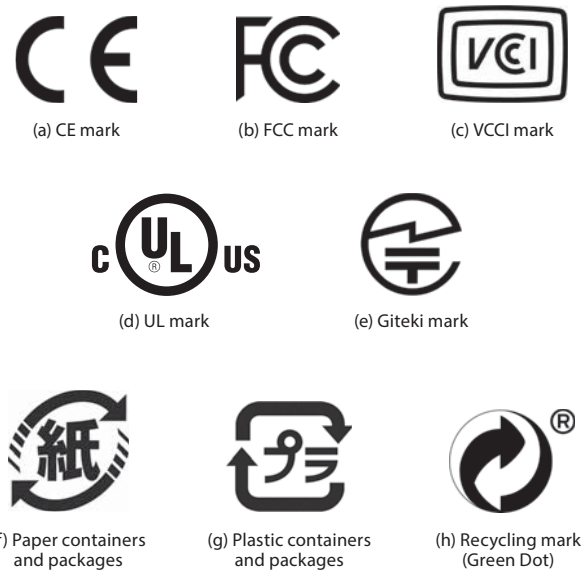

Figure 5. Examples of law, regulation, and certification symbols approver for use.
The environment sensing logger is certified for various standards so that it can be used in many countries and for many applications.

We considered that a bright color should be used in order to make the environment sensing logger conspicuous among air cargos. At first, we considered using red or yellow, but red generally signifies danger, and yellow indicates the need for caution. Adoption of red or yellow would have involved a risk of misinterpretation. Therefore, we selected green for the cover casing.

5. Conclusion

In order to meet the needs for management based on the sensing of environmental conditions, we have developed an environment sensing logger that incorporates the ApP Lite TZ1001 processor designed for IoT applications. Although, at present, the environment sensing logger is mainly used in the logistics field, we will expand its application to other fields requiring real-time processing.

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