

Superjunction MOSFETs and SiC diodes optimise power conversion performance



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The latest advances in superjunction MOSFETs and silicon-carbide rectifiers give designers extra freedom to optimise performance and efficiency in cost-sensitive power-conversion applications.

Introduction

In the drive to continue increasing energy efficiency in switching power-conversion systems such as PFC and switching power supplies, superjunction MOSFETs and wide-bandgap silicon-carbide (SiC) diodes have become favoured solutions for energy-conscious designers. Both technologies have allowed smaller die sizes in relation to key parameters such as MOSFET on-resistance and diode reverse voltage, enabling designers also to reduce circuit size and increase current density. As market adoption of these device technologies continues to grow, new demands are coming to the fore, such as improved noise performance.

Reducing electromagnetic noise emission is desirable in high-end power supplies for equipment such as LCD TVs, LED lighting, medical power supplies, notebook power adapters and power supplies for tablets. Resonant switching topologies, such as the LLC converter with zero-voltage switching, are popular for these types of applications for their inherently low electromagnetic emissions. Primary-side switching in an LLC circuit as shown in figure 1 (MOSFETs Q1 and Q2), is often now handled by superjunction transistors to achieve a compact and energy-efficient power supply.

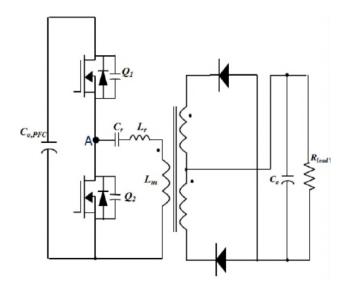


Figure 1. Primary-side superjunction transistors boost the efficiency of high-end LLC-resonant PSUs.

Superjunction Transistor Progress

The superjunction MOSFET has enabled power supply designers to benefit from significantly lower conduction loss for a given die size than is achievable using conventional planar silicon MOSFETs. Because the device architecture also allows low gate charge and capacitance, superjunction MOSFETs also exhibit lower switching losses than conventional silicon transistors.

Figure 2a shows the structure of early superjunction devices, which have traditionally been fabricated using a multi-epitaxial process. Rich doping of the N-region illustrated allows much lower on-resistance than is achievable in conventional planar transistors. The P-type regions bounding the N channel are architected to achieve the desired breakdown voltage.

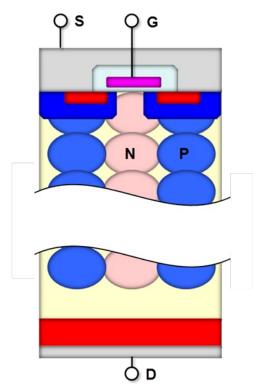


Figure 2a. Multi-epitaxial superjunction MOSFET.

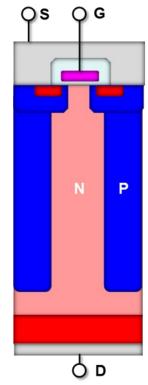


Figure 2b. Single-epitaxial MOSFET.

The N- and P-type structures of these devices have been fabricated using multi-epitaxial processes that have resulted in dimensions that are larger than ideal and have an associated impact on overall device size. The nature of the multi-epitaxial fabrication also restricts engineering of the N-channel to minimise on-resistance.

Improved fabrication processes, such as deep trench filling that enables single-epitaxial fabrication, now give designers greater freedom to optimise the aspect ratio of N- and P-channels and so further minimise on-resistance while also reducing MOSFET size. Figure 2b illustrates Toshiba's fourth-generation DTMOS IV family, which takes advantage of single epitaxy to achieve a 27% reduction in device pitch at the same time as reducing on-resistance per die area by 30%. Also DTMOS V is based on the deep trench process, with further improvements at cell structure level.

The single-epitaxial process also enables superjunction MOSFETs to deliver more stable performance in relation to temperature change. Ultimately, this helps to counter the typical reduction of efficiency experienced in power converters at higher operating temperatures. Figure 3 shows how the temperature-related change in normalised on-resistance is significantly reduced in devices using the latest-generation technologies, resulting in 12% lower on-resistance ($R_{DS(ON)}$) at 150°C.

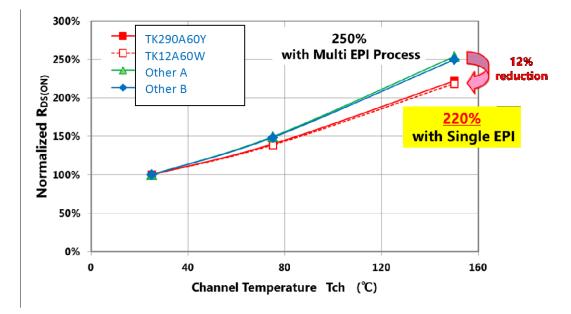


Figure 3. Single-epitaxial fabrication has enabled a flatter on-resistance/temperature characteristic. The TK12A60W represents DTMOS IV and TK290A60Y DTMOS V generation.

DTMOS V FETs Meet Demands for Lower EMI

With the arrival of fifth-generation DTMOS V devices, designers can now choose superjunction MOSFETs that deliver lownoise performance suitable for use in power converters. DTMOS V FETs also display a well-balanced ratio of lower noise performance and switching performance. This is achieved through a modified gate structure and patterning, which results in increased reverse transfer capacitance seen between the gate and drain (C_{rss} or C_{gd}).

Emitted noise is comparable to that experienced with competing low-EMI devices, while at the same time the devices deliver the superior on-resistance that characterises superjunction technology. Figure 4 compares the level of EMI emitted by fourth- and fifth-generation N-channel, $0.38m\Omega$ -class 600V devices used in the PFC circuit of a television power supply, showing a significant reduction interference from the later technology.

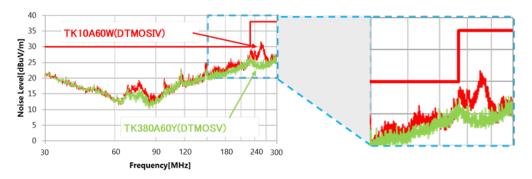


Figure 4. Improved noise performance displayed by fifth-generation superjunction technology.

Further advantages of DTMOS Technology

The superjunction process itself, and DTMOS technology in particular bring other substantial benefits to designers of power electronics. The fundamental figure-of-merit (FOM) of resistance x chip size shows a 30% improvement over DTMOS III, leading to smaller $R_{DS(ON)}$ chips in the same package.

By applying the new, single epitaxial process to DTMOS, the effects of temperature on R_{DS(ON)} are reduced, thus ensuring better and more consistent performance in power applications. When compared to competitive devices and the previous generation of DTMOS, R_{DS(ON)} is some 15% lower at maximum operating temperature. This saves costs by allowing for less stringent heat management requirements.

The fast body diode built in to DTMOS IV achieves fast recovery times in the region of 140ns, even at high temperature. This results in lower power losses, less heat generation and a more thermally efficient design.

The superjunction process also reduces the output capacitance, C_{oss}, by 12%, leading to a reduction in the waste energy being stored in the device (that has to be dissipated during each and every switching cycle). This makes DTMOS IV ideal for the fast-switching and resonant topologies commonly found in power designs.

Hard-switching applications such as Power Factor Correction (PFC) benefit in terms of increased efficiency from the 45% reduction in gate-drain charge (Q_{gd}) found in the X-Series.

Within the DTMOS IV range there are a total of four series covering a wide variety of applications.

> DTMOS IV - SERIES	> APPLICATIONS
W-Series: Standard type	For general switching
W5-Series: With high speed body diode	For bridge circuitry, like UPS or server SMPS
X-Series: High speed type	For PFC circuit
X5-Series: High speed type with high speed body diode	For bridge circuitry, like UPS or server SMPS

Figure 5: The DTMOS IV range offers performance benefits across a wide range of applications

DTMOS product range

The fifth-generation of Toshiba's DTMOS range, DTMOS V, was announced in December 2016, adding further performance improvements to the DTMOSIV range, including a further 17% improvement in $R_{DS(ON)}$ and greater optimization of the trade-off between switching performance and EMI noise.

The DTMOS range encompasses a wide variety of package type options offering both pin-in-hole and surface mount options, giving convenience and compatibility with a wide variety of manufacturing processes. The range includes industry-standard options such as D-PAK, TO-220 and TO-247 as well as other types.

DTMOS IN	V 650V ST	ANDARD"	W"-SERIES	6				
PKG	D-PAK	I-PAK	D2-PAK	I2-PAK	DFN 8x8mm	TO-220	TO-220SIS	TO-247
Outline			P			M		A
(1.2/1.22)Ω	TK5P65W	TK5Q65W	20				TK5A65W	
(1.0/1.05)Ω	TK6P65W	TK6Q65W					TK6A65W	
(0.78/0.8)Ω	TK7P65W	TK7Q65W					TK7A65W	
(0.65/0.67)Ω	TK8P65W	TK8Q65W					TK8A65W	
(0.5/0.56)Ω	TK9P65W	TK9Q65W					TK9A65W	
(0.39/0.44)Ω	TK11P65W	TK11Q65W					TK11A65W	
(0.25/0.28)Ω	0.44	0.44	TK14G65W	TK14C65W	TK14V65W	TK14E65W	TK14A65W	TK14N65V
(0.20/0.21)Ω				TK17C65W	TK17V65W	TK17E65W	TK17A65W	TK17N65V
(0.11/0.12)Ω					TK28V65W	TK28E65W	TK28A65W	TK28N65V
80mΩ					0.12		TK35A65W	TK35N65V
55mΩ								TK49N65\

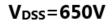
Figure 6: The DTMOS range offers many package options including several industry-standard types

The DTMOS IV series offers V_{DSS} options from 500 to 650V with 800V versions currently under development. Current handling capability extends to 100A in the high-performance TK100L60W, available in a TO-3P(L) package, allowing for Po approaching 800W. Unsurprisingly, the TK100L60W also offers the best $R_{DS(ON)}$ value in the range - an ultra-low 0.018 Ω . The trade-off in this device is the relatively high output capacitance (C_{OSS}) and gate charge (Q_g) of 320pF and 360nC, respectively.

However, many devices in the series offer far lower switching loss performance with the TK5Q60W standing out with C_{oss} and gate charge (Q_g) values of 10pF and 10.5nC.

The recently announced DTMOS V series offers a more focused range, initially packaged in the highly popular TO-252 (DPAK) and TO-220SIS formats. In moving to the latest series, the product naming conventions have changed and the $R_{DS(ON)}$ value now replaces the drain current (I_D) in the part number. While, at one level, this is a detail, it also communicates the importance Toshiba places on continually reducing this critical parameter for future, high-performance, power systems.

V _{DSS} =600V					
	DPAK (TO-252)	TO-220SIS			
Rds(on) MAX (Ω)					
0.56	TK560P60Y ES : OK CS : OK MP : Jan. '17	TK560A60Y ES : OK CS : OK MP : Jan. '17			
0.38	TK380P60Y ES : OK CS : OK MP : Jan. '17	TK380A60Y ES : OK CS : OK MP : Jan. '17			
0.29	TK290P60Y ES: OK CS:OK MP:Jan.'17	TK290A60Y ES : OK CS : OK MP : Jan. '17			



	DPAK (TO-252)	TO-220SIS
Rds(on) MAX (Ω)		
0.56	TK560P65Y ES: OK CS:OK MP:Jan.'17	TK560A65Y ES : OK CS : OK MP : Jan. '17
0.38	TK380P65Y ES: OK CS:OK MP:Jan.'17	TK380A65Y ES : OK CS : OK MP : Jan. '17
0.29	TK290P65Y ES : OK CS : OK MP : Jan. '17	TK290A65Y ES : OK CS : OK MP : Jan. '17

Figure 7: Initial variants available in fifth-generation DTMOS superjunction technology

Rectifier Diodes Toughen Up with SiC Advances

Complementing the high efficiency and current density of deep-trench superjunction power switches, new generations of silicon carbide (SiC) diodes combine inherently superior energy efficiency compared to standard silicon devices with increased current density, higher current ratings and greater robustness, and enhanced cost-performance ratio.

Recap on SiC Advantages

The properties of SiC enable SiC Schottky Barrier Diodes (SBDs) to deliver fast and temperature-stable reverse-recovery comparable to that of conventional silicon diodes. The latter can result in thermal instability if reverse-voltage derating is not applied. In addition, the wide-bandgap property of SiC allows the device to have a higher voltage rating in relation to die size, enabling 650V and 1200V devices to be housed in industry-standard surface-mount and through-hole packages. This combination of characteristics makes SiC diodes ideal for applications such as power-factor correction when used as shown in figure 8, in conjunction with a high-speed superjunction MOSFET such as a DTMOS IV X-type device.

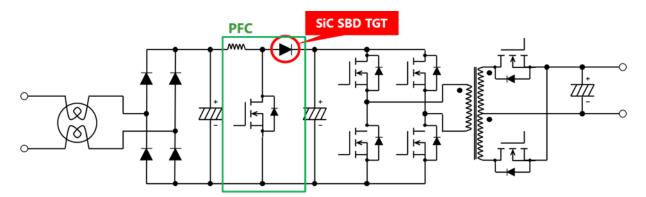
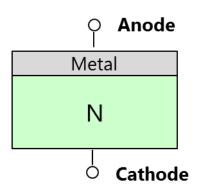


Figure 8. The latest SiC diode technology can be used in conjunction with a high-speed superjunction MOSFET, to boost the efficiency of PFC circuitry.

Figures 9a and 9b illustrate the enhanced architecture of the SiC SBD in comparison with the standard silicon SBD architecture.



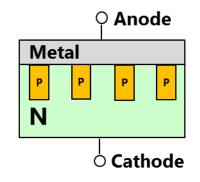


Figure 9a. Basic architecture of standard silicon SBD.



The Emerging Generation

The key targets for the latest generation of 650V SiC SBDs have been to increase performance in relation to device cost, and to raise the maximum forward-current surge capability and thus deliver more robust devices that are capable of surviving harsh exception conditions.

As with LSI semiconductors, power semiconductor die size is a key determinant of device cost. Development of the second-generation SiC SBD architecture has focused on reducing the die thickness. The result has been to reduce thickness by two-thirds, bringing an attendant cost saving, while also raising current density by a factor of up to 1.5.

To increase the surge-current capability and hence deliver more robust devices for power switching applications, the firstgeneration architecture has been modified to minimise modulation of the conductivity (as measured using the diode forward-voltage, V_F) thereby allowing higher maximum forward surge current, I_{FSM} . Figure 10 shows how this has been achieved by optimising the area of the P+ region.

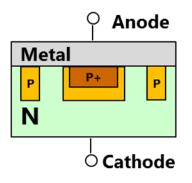


Figure 10. Optimising the SiC P+ region in the second-generation 650V SiC SBD.

Changes to the diode architecture have modified the I_{FSM} , as shown in figure 11. As a result, the second-generation architecture permits I_{FSM} to be increased above the reach of first-generation devices.

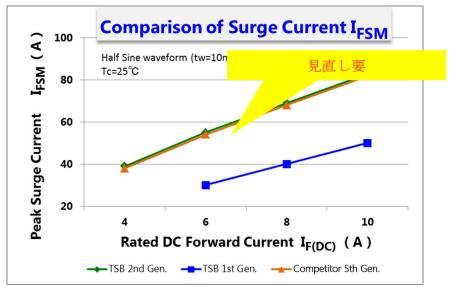


Figure 11. IFSM capability comparison between 1st gen and 2nd gen

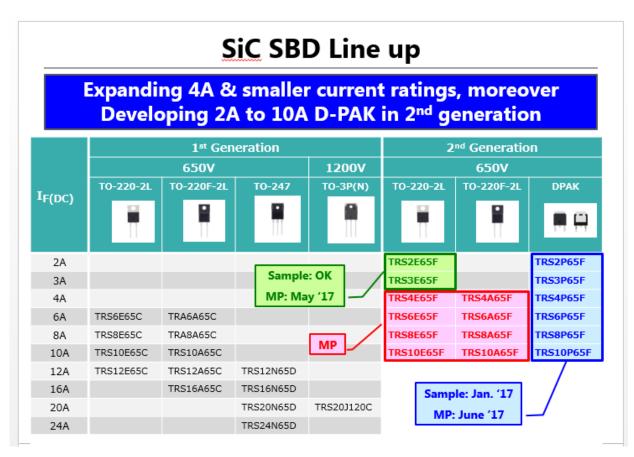


Figure 12: Comparison of 1st and 2nd generation SiC SBD Diodes

The second generation of SiC SBD diodes from Toshiba offers designers performance benefits based upon the new technology as well as additional current ratings and package types. While the second generation retains the two TO-220 packages, including the TO-220-2L with metal tab and TO-220F-2L with full plastic encapsulation, for pin-in-hole applications, the new range includes SMD options for the first time.

The industry-standard DPAK package offers benefits in automated manufacturing environments across the full current range from 2A to 10A, while the 4A to 10A devices have the added option of an 8x8DFN package. Both packages are available in tape-and-reel packaging for convenience and include a metal pad for excellent thermal conductivity.

Summary

Power supply designers are under pressure to satisfy unrelenting demands for greater energy efficiency, reliability and miniaturisation, within increasingly tight cost constraints. Moreover, there is less time available to look at EMI suppression during the design process.

Success depends on taking advantage of the latest power-semiconductor technologies that deliver lower on-resistance and noise performance in the case of power MOSFETs, and reverse recovery loss with greater temperature stability in the case of rectifier diodes. The latest-generation superjunction MOSFETs and SiC diodes deliver these advances, as well as improved switching performance, greater robustness and reliability, and increased current density, at a price that can make economic sense for cost-sensitive applications.



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