TOSHIBA

Isolating the I^2C bus with optocouplers for industrial applications

Achieving 5kV isolation for industrial, test and measurement, and metrology applications

Introduction

Introduced to the market 40 years ago, the Inter-Integrated Circuit (I^2C) interface was designed to provide a serial bus system for short-distance communication between microcontrollers and on-board peripherals. Over the decades, almost every semiconductor manufacturer has brought I^2C devices to market. As a result, applications are simplified significantly. Temperature sensing is a classic example. The complete sensing and post-processing are integrated into a single device with additional features such as alert signals. This replaces a complex analogue circuit made up of operational amplifiers, a host of passive components, and an analogue-to-digital converter (ADC). Such has been the success of this serial protocol that it has become the basis of other busses such as SMBus (System Management Bus) targeting computer motherboards, and PMBus (Power Management Bus) for communication between the components of power systems.

Because of the broad range of support, from peripheral devices to microcontrollers (MCU), along with its versatility, I^2C is useful when communicating with electrically isolated sections of application implementations. With just two signals, a data line marked SDA and a clock line marked SCL, this single-ended synchronous interfacing technology only requires two wires. However, there is a challenge in that the signals use bi-directional communication. This demands a little ingenuity on behalf of the development engineer when implementing any isolation circuitry.

Basics of I^2C Communication

I^2C is typically used with a single controller, normally an MCU or system-on-chip (SoC), and one or more target devices. Provision is, however, made to support a second controller (Figure 1). At the hardware level, the controller's I^2C pins are implemented as open drain. This means they can pull the SDA and SCL signals low but a suitably dimensioned resistor is required to pull the signals high. Bus contention is thus avoided in the case of two controllers.

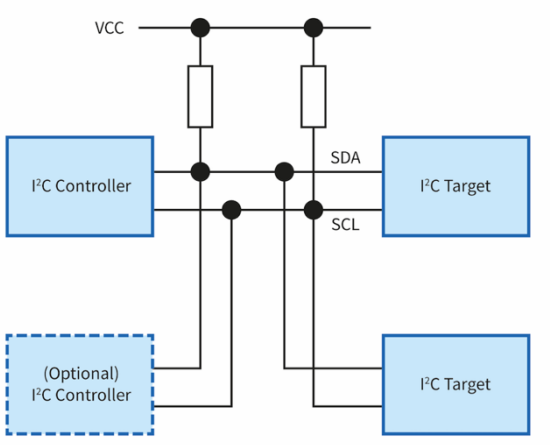

Figure 1: Systems utilising I^2C implement the bus 'controller' in a microcontroller. This communicates with one or more 'targets'. In some cases, the bus may implement a second 'controller'.

The SDA signal is bi-directional. When implemented, the controller places its data on the SDA line to first select the target to be addressed. It is then used to select the register to access within that target. Once complete, the target returns the requested data over the SDA line. Targets also use the SDA line to acknowledge correct reception of the request (ACK) by holding SDA low or deny correct reception (NACK) by letting SDA be pulled high.

The SCL line is controlled by the controller, dictating the speed with which data is communicated over the bus. The original specification was limited to 100 kHz but, over the years, supported signalling rates were increased to 400 kHz, 1 MHz, and then up to 5 MHz. Most of the time, this signal is uni-directional. However, in the event a target requires more time to respond to a request, it may hold the SCL signal low together with the SDA that is providing the ACK. This feature is known as clock stretching. When developing circuitry for an isolated I²C interface it is therefore essential that both lines support bi-directional communication.

Isolating I²C Communication Circuits

I²C was never intended to be used anywhere other than for board-level communication. This means that any latencies added by the isolation circuitry have to be considered. One aspect is the ACK/NACK response of the target to the controller. According to the specification (Figure 2), the ACK/NACK signal must be valid after a setup time ($t_{VD;ACK}$) of between 3.45µs in standard-mode (100kHz) operation and 0.45µs in fast-mode plus operation (1MHz).

Additionally, there is timing defined for data setup times. For example, in standard-mode a target is expected to set up the SDA signal within 250ns ($t_{HD;DAT} + t_{SU;DAT}$ – Table 11 I²C Specification[1]) after the falling edge of the previous clock bit. For fast-mode plus, this drops to just 50ns.

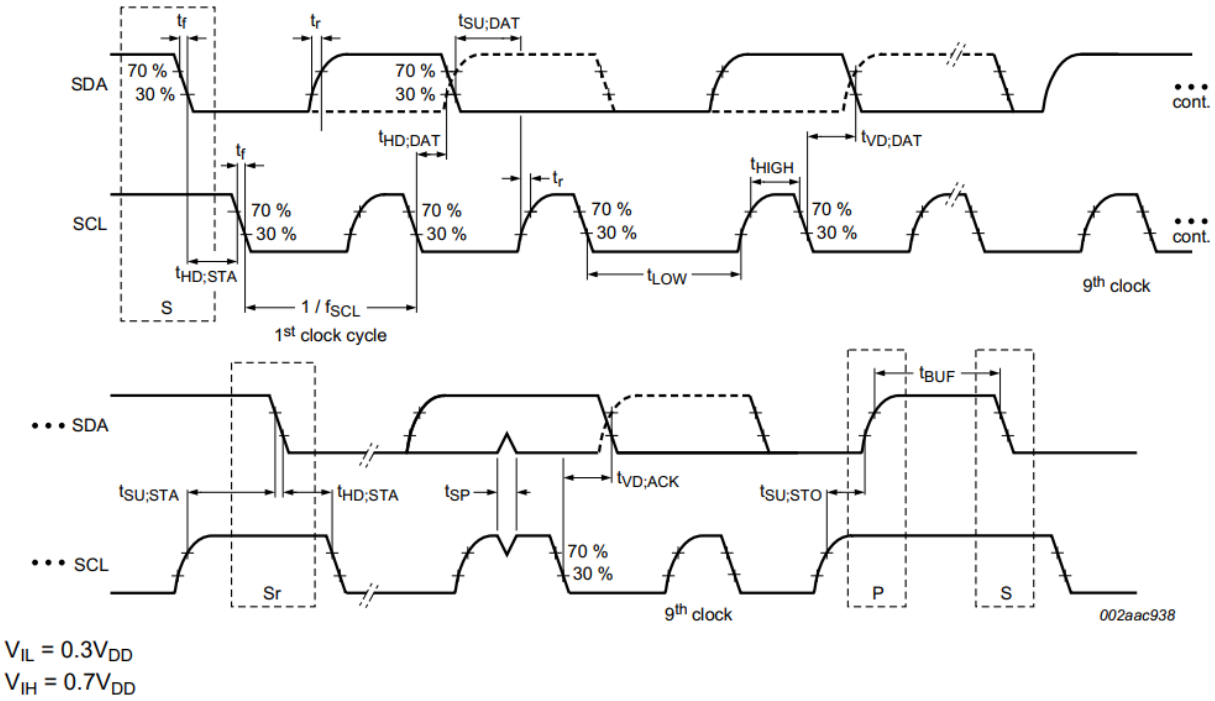

Figure 2: The I²C specification defines the timing on the bus. An optocoupler can add delays when a target responds with data (Source: Figure 38. Definition of timing for F/S-mode devices on the I²C-bus[1]).

In both cases, latency through an isolation circuit could cause problems in fulfilling the timing specified in the standard. Furthermore, added latency causes a drop in throughput, as the extra time caused by latency through the isolator is seen as an implicit clock stretch from the perspective of the master. As a result, the circuit design should keep the latency as low as possible to ensure reliable operation, especially at the fastest SCL speeds.

Optocoupler-Based I²C Isolator

Selecting an optocoupler as the basis of an I²C isolator circuit is no easy task. Firstly, as highlighted, the propagation delay from input to output should be as low as possible to avoid impacting normal bus operation. Secondly, the device needs to support the voltage used by the controller. Finally, the optoisolator needs to have an open-drain output so that the target can be interfaced correctly. Other aspects will also need to be examined, such as board real estate, component count, and cost.

A solution is available from Toshiba with the TLP2362 optoisolator (Figure 3) that uses a high-output infrared LED coupled with a high-gain, high-speed photodetector. Operating from 2.7V to 5.5V, it is ideal for most embedded application power supply implementations requiring isolation of up to 3750kV. Its internal Faraday cage protects against common-mode transient signals of up to ±25kV/µs, ensuring robust I²C communication even in noisy, industrial applications. Furthermore, this optocoupler is UL and cUL recognised and VDE and CQE approved. Its operating temperature range extends from -40°C to 125°C.

The device is housed in an SO6 package (3.7 × 7mm) with five pins and provides an inverted output. A ceramic 1 µF bypass capacitor is required between pins 6 (V_{CC}) and 4 (GND) to stabilise the operation of the output logic. Without this, the photocoupler may not switch correctly. This component should be placed within 10mm of the TLP2362 pins. Propagation time delay is just 35ns (max. 100ns) for high-to-low signal transitions and 26ns (max. 100ns) for low-to-high transitions. The device-to-device skew is only ±40ns, ensuring good consistency between manufactured boards.

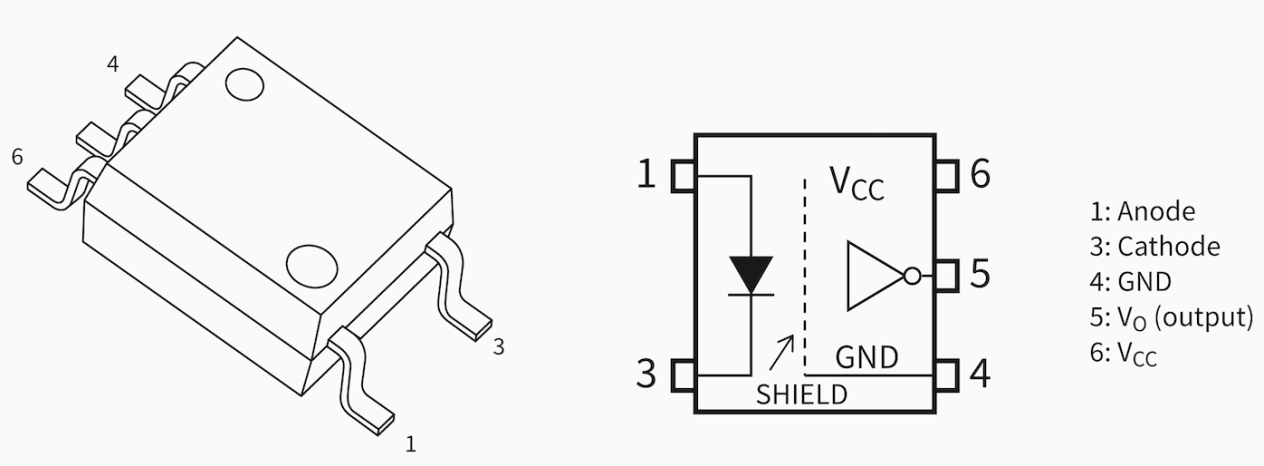

Figure 3: The TLP2362 provides isolation of up to 3750kV. Its output is open-drain, making it ideal for implementing isolated I²C communication.

The complete I²C optoisolator circuit requires four TLP2362 devices, two for SDA and two for SCL (Figure 4). As the design is identical for both channels, only the operation of the SDA path of the circuit will be covered.

The SDA signal from the non-isolated side (NIS) is pulled up to the supply via R1, while SDA on the isolated side (IS) is pulled-up by R8. These resistors must be dimensioned according to the supply voltage used, the capacitive loading seen by the controller or target, and the equations supplied in the I²C specification (Chapter 7.1). The maximum pull-up resistance is defined as:

$$R_{p(\max)} = \frac{t_r}{0.8473 \times C_b}$$

where t_r is the maximum allowable rise time for the operating mode selected, and C_b is the estimated bus capacitance.

The minimum resistance is defined as:

$$R_{p(\min)} = \frac{V_{DD} - V_{OL(max)}}{I_{OL}}$$

When SDA on both sides is high, the circuit is in its default state. When the NIS SDA signal is pulled low, current flows through R4 and the LED of optocoupler IC2. This results in the zero state being passed to the IS SDA signal as it is pulled low by the output of IC2 and D2, a small-signal barrier diode. This zero state is not returned to the NIS side due to the reverse pole implementation of the LED in IC1, thus avoiding that the circuit causes a permanent zero state.

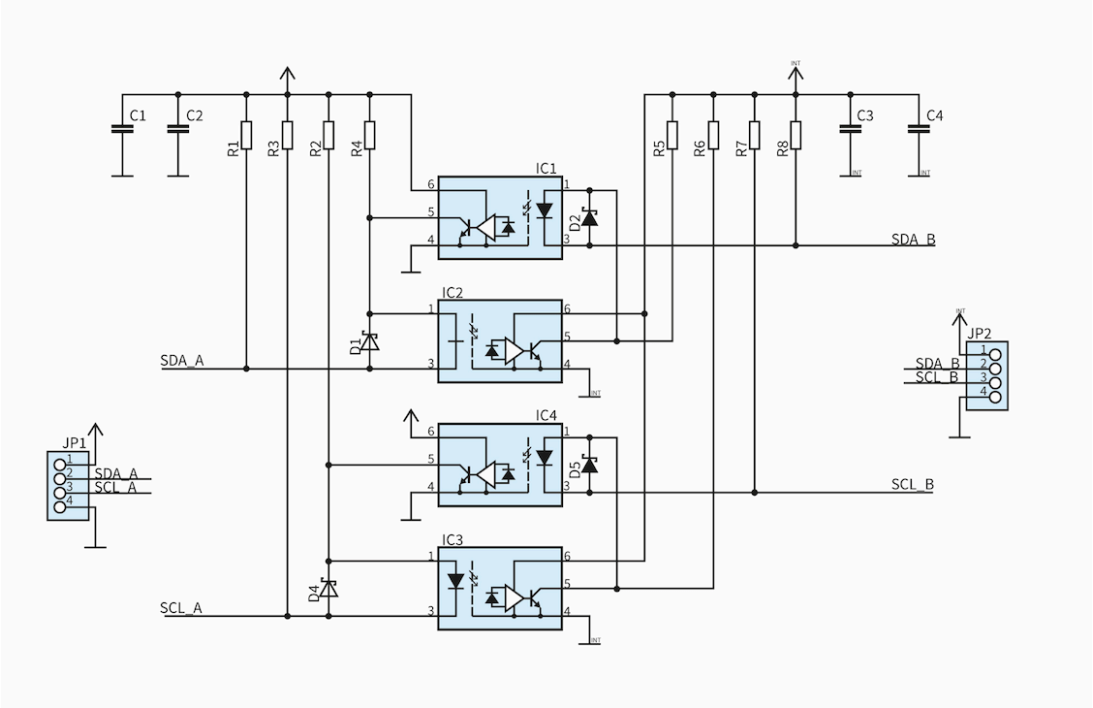

Figure 4: The full I²C bus isolator circuit requires just 20 components, four of which are the optocouplers, and another four are diodes. The rest are passives.

As the circuit is symmetrical, a zero state generated at SDA on the IS is passed to the NIS in the same manner.

The diodes separate the sending signal from the returning signal in the bi-directional paths of SDA and SCL, and their selection requires a certain amount of care. Firstly, it should be noted that this circuit only functions with open-collector

photocouplers, as used here. Secondly, the diodes should be small signal types and low capacity, such as Schottky barrier diodes (SBD), to ensure low noise and distortion, especially at the fastest signalling speeds. They should also offer a low forward voltage to ensure that the low signal level of I²C communication meets the specification (V_{IL} = 0.3V_{DD}). Bearing in mind that the maximum V_{OL} of the TLP2362 is 0.6 V (typical is 0.2 V), an SBD with a V_F of 0.3 V ensures V_{IL} is in spec even for a V_{DD} of 3.3 V. Suitable diodes include the DSF01S30L or the DSR01S30SL.

Simple I²C Isolator Design

In total, this approach requires just 20 components, eight of which are the four optocouplers and four diodes. The rest can be implemented using space-saving 0402 components, leading to a total footprint of just 116 mm² (Figure 5).

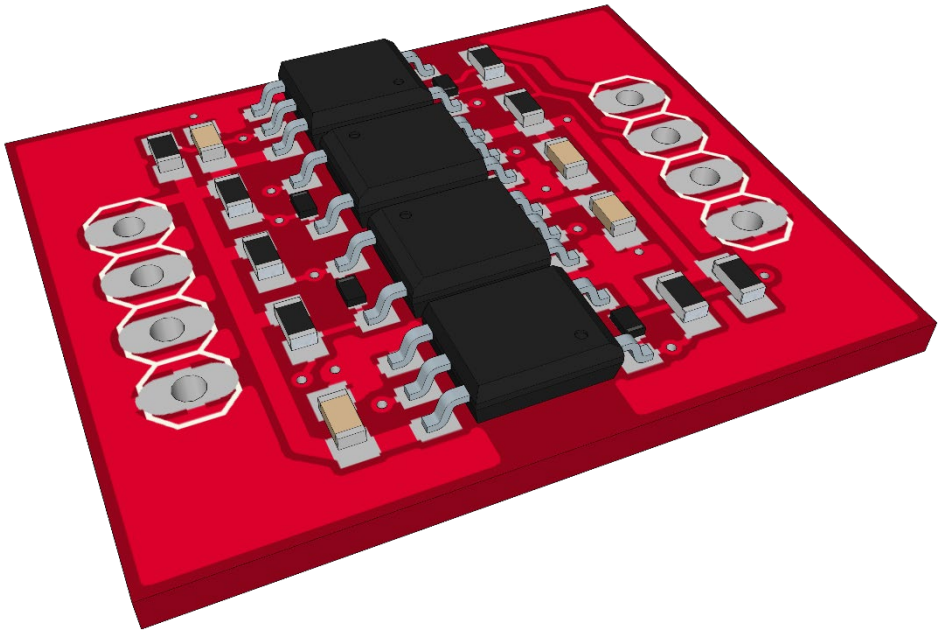

Figure 5: The I²C isolator design is very compact, making it simple to integrate into a design.

To increase the level of isolation, the same design can be modified to use the TLP2768, which offers 5kV. Should clock speed be an issue, the TLP2368 can be considered offering up to 50MHz clock speeds. Higher supply voltages of 3V to 30V can be covered using the TLP2309. And an automotive implementation for I²C or even LIN can be undertaken using the AEC-Q101 qualified TLX9309.

In work undertaken to validate the design, the waveform passing through the optocoupler demonstrated a clean shape with an almost symmetric delay of around 60ns (Figure 6). This should be more than suitable for fast-mode (400 kHz) I²C operation.

Figure 6: Analysis of the prototype displayed a symmetrical delay of around 60 ns, making the design suitable for use in fast-mode, 400 kHz I²C applications.

I²C peripherals can vary greatly, so it is worth checking that the devices used in conjunction with this isolator are capable of driving the necessary current required by the internal LED. For the TLP2362, the input threshold current I_{FHL} is a maximum of 5.0 mA (typical 1.0mA). Should this be too high, the TLP2363 operating at 3.3 V could be a suitable alternative with an I_{FHL} maximum of 2.4 mA (typical 0.9mA).

Summary

As a board-level, chip-to-chip communication protocol, I²C is simple and effective. This has resulted in its use in various applications for the past 40 years. However, when it comes to isolating this two-wire interface, challenges arise due to the bi-directional nature of the signals passing between the controller and targets on both the data and clock lines. The most significant cause for concern is the latency introduced by an isolation circuit, as this has the potential to push the communication timings outside the limits defined in the specification.

The design provided here offers an optocoupler-based solution that offers up to 3750kV of isolation for a fast-mode, 400kHz interface. Alternative optocouplers from Toshiba provide support for a range of input/output voltages, higher levels of isolation, and even higher clock rates if needed. Furthermore, considering the current pressures on component sourcing, purchasers and designers can easily employ a dual-sourcing strategy for the optoisolators, offering peace of mind for long-term deployment.

Reference:

[1] UM10204 – I²C-bus specification and user manual, Rev. 7.0, October 2021

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