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Efficient field-oriented control of BLDC motors in automotive applications

Introduction

Brushless direct current (BLDC) motors are a critical component in many automotive subsystems including pumps and fans, sunroofs, power doors, tailgates, window wipers and lifters (Figure 1). Making a BLDC motor rotate is a relatively straightforward task but making it run optimally presents a greater challenge. Vector or Field-Oriented Control (FOC) enables smooth motor operation over the whole speed range but places significant overhead on the subsystem microcontroller unit (MCU). This can make it difficult for it to schedule other tasks, meaning an MCU with a dedicated hardware accelerator is preferable. This white paper reviews the concept of FOC and the advantages of using the Toshiba vector engine co-processor in automotive motor control applications. Next, it explores the features and benefits of a new and highly integrated TB9M003FG Smart Motor Control Driver (SmartMCD™) IC from Toshiba, which not only integrates an Arm® Cortex® M0 based MCU with a fourth-generation vector engine co-processor, but also includes pre-drivers to control external B6 N-channel MOSFETs. Finally, it considers the extensive range of supporting hardware and software development tools for the TB9M003FG, which can be used to accelerate the design of smaller, simpler and lower-cost 30 – below 1000 Watt BLDC motors in automotive subsystems.

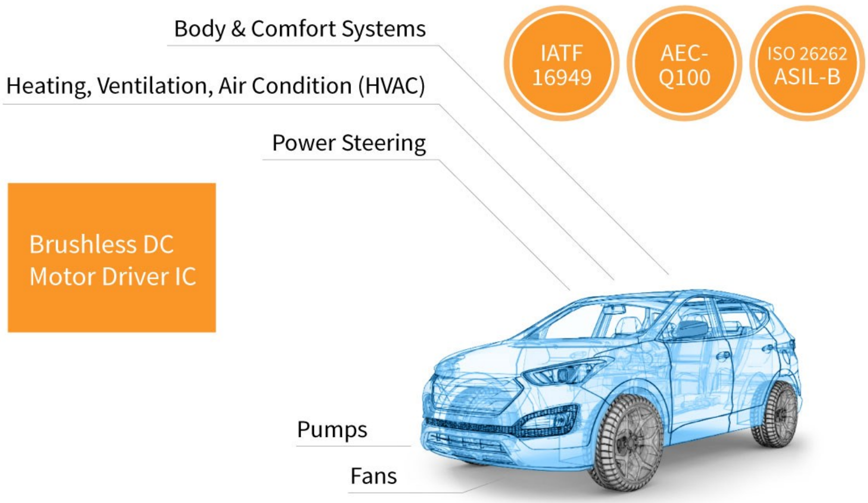

Figure 1: BLDC motors are critical components in many automotive subsystems

Field-oriented control

Switching to electronically commutated brushless DC (BLDC) motors has led to significant improvements in energy efficiency, better power/size ratio, wider speed range, lower inertia, and electrically and mechanically quieter operation. However, this change presents some challenges. Traditional brushed DC motors use brushes and a slip-ring to time the motor's commutation and to know the rotor's position. This is not the case with BLDC motors, which can cause issues, such as mechanical stress or damage, if the coils are energised incorrectly.

To solve this, thanks to Faraday's law of induction, we know that the magnets of the rotor passing through the stator coil generate an electromotive force (EMF) in the stator windings. This Back-EMF effect can be measured by a microcontroller (MCU) via an analog-to-digital converter (ADC) used to determine the rotor angle mathematically. These calculations are made using field-oriented control (FOC) algorithms, also known as vector control.

There are two common approaches to measuring the Back-EMF: using three separate shunt resistors for each motor phase (known as a 3-shunt method), or using a single shunt resistor for all phases (a 1-shunt method). The 1-shunt method is more cost-effective but necessitates more complex FOC algorithms. However, both of these methods have limitations, especially when the motor is at a standstill or running at low speeds – this is because the signal-to-noise ratio (SNR) of the generated Back-EMF does not allow for precise estimation.

One way to overcome this is to start the motor in a controlled way until a speed is reached, where enough EMF is generated. A common method is the 6-step commutation, but it can cause power inefficiency and noise, which is unsuitable for many applications, including automotive. This torque ripple arises due to the inability to maintain a consistent 90° electrical angle between the stator and rotor magnetic fields. The angle fluctuation leads to non-uniform acceleration and deceleration of the rotor, which manifests as mechanical vibration and audible noise, compromising its reliability.

Those looking to achieve higher reliability and lower levels of audible noise will use various sensing techniques to accurately determine the position of the rotor, particularly at low speeds. Rotor position sensing can be achieved through incremental encoders, which offer high accuracy but at a higher cost and with potential integration challenges. Alternatively, resolvers or Hall sensors provide a compromise between cost and accuracy. Sensor-less control methods eliminate the need for physical sensors or encoders on the motor, while still maintaining adequate precision for most FOC applications.

The FOC control strategy produces a rotating stator magnetic field that is dynamically regulated to sustain a constant 90° lead angle relative to the rotor's magnetic field. It does so by generating three sinusoidal control signals, phase-shifted by 120°, that align with the desired revolutions per minute (RPM) set-point for the motor.

Controlling the sinusoidal three-phase currents with a proportional-integral (PI) regulator in a typical microcontroller (MCU) is complex. FOC algorithms simplify this by transforming the three-phase currents into a two-dimensional reference frame, using Clarke and Park transformations, which align with the moving rotor. This frame consists of direct (d-axis) and quadrature (q-axis) currents, Id and Iq, respectively.

By regulating Id towards zero and Iq towards the required torque value with two PI controllers, the desired 90° phase lead is maintained. The two-dimensional control signals are then converted back into three-phase currents using inverse Clarke/Park transformations to generate the stator field necessary for maintaining the constant lead angle.

To produce the sine control signals, the MCU modulates the duty cycle of its pulse-width modulated (PWM) outputs, which, through the motor inverter, results in three sinusoidal outputs at a frequency corresponding to the desired motor RPM. The entire FOC control loop, including signal generation, is illustrated in Figure 2.

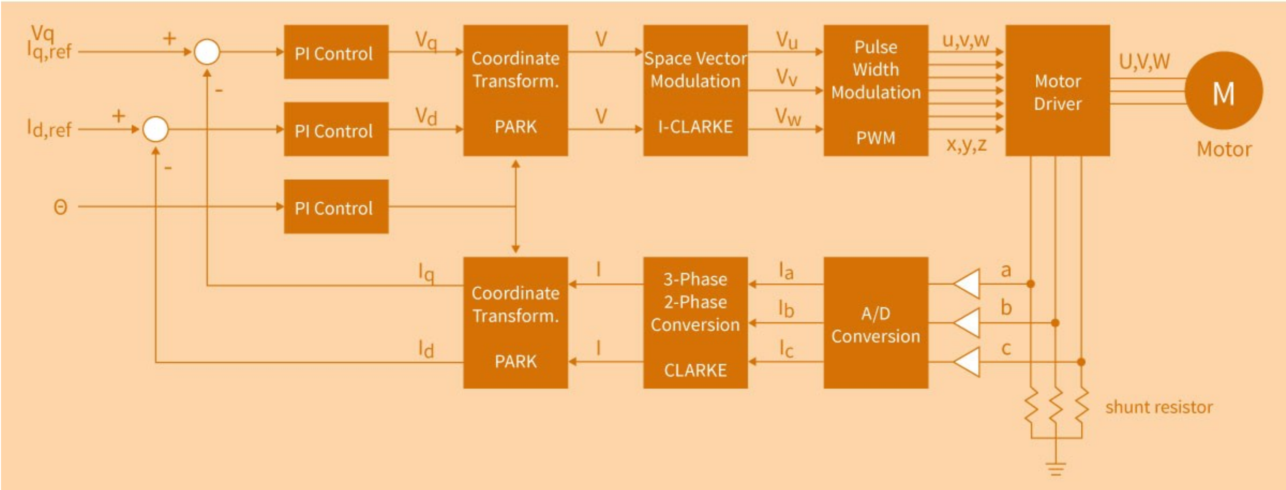

Figure 2: FOC block diagram with transformations from the time-variant three-phase motor currents into the time-invariant Id and Iq reference frame

As previously discussed, implementing FOC for a BLDC motor application using a standard MCU is not trivial. It requires appropriately dimensioned ADCs, a processor that can handle vector mathematics for the Park and Clarke (forward and reverse) transformations, a software implementation of proportional and integral (PI) control, and a pulse width modulator (PWM) of sufficient resolution. Moreover, programming the controller for the Park and Clarke transformations and PI control is a complex task for optimizing motor operation.

As system performance demands increase and systems form factors shrink, a dedicated FOC controller, like the Toshiba vector engine co-processor, is an attractive alternative. A vector engine co-processor handles the current control and the complex transformations between two-dimensional rotational coordinates, rotation angle estimation, and the three-phase motor current system. It also reduces motor control processing time by executing typical calculations for vector control of BLDC motors, thereby freeing up valuable CPU resources and thus improving the overall system performance. This allows CPU resources to be used for various non-motor control application tasks such as Man Machine Interface (MMI), communication with other nodes, real-time data logging and pre-analysis (Figure 3).

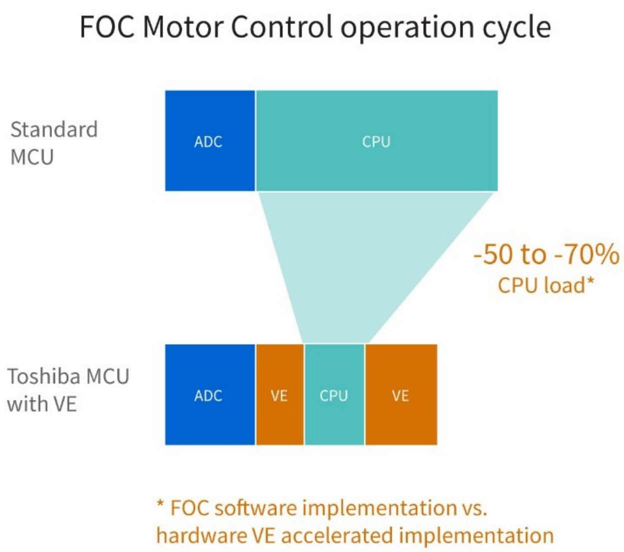

Figure 3: Toshiba's vector engine co-processor significantly reduces CPU overhead

Toshiba's fourth-generation Advanced-Vector Engine alpha (A-VEα) is an evolution of earlier iterations of its vector engine co-processors, which were denoted VE, VE+ and A-VE. Compared to these, the A-VEα offers improved functions for a 1-shunt solution, including enhanced current detection, improved "shift PWM-2", enhanced non-interference control, as well as motor rotation angle estimation in addition to flexible task scheduling.

Highly integrated SmartMCD™ delivers exceptional FOC performance

The SmartMCD™ TB9M003FG motor control driver is manufactured using Toshiba's advanced mixed-signal process technology and combines an Arm® Cortex® CPU with a vector engine co-processor and gate drivers to control external B6 N-channel MOSFETs. This IC can be connected directly to the battery and local interconnect network (LIN) bus in an automobile to deliver high levels of performance and integration. The functional blocks in the TB9M003FG are shown in Figure 4.

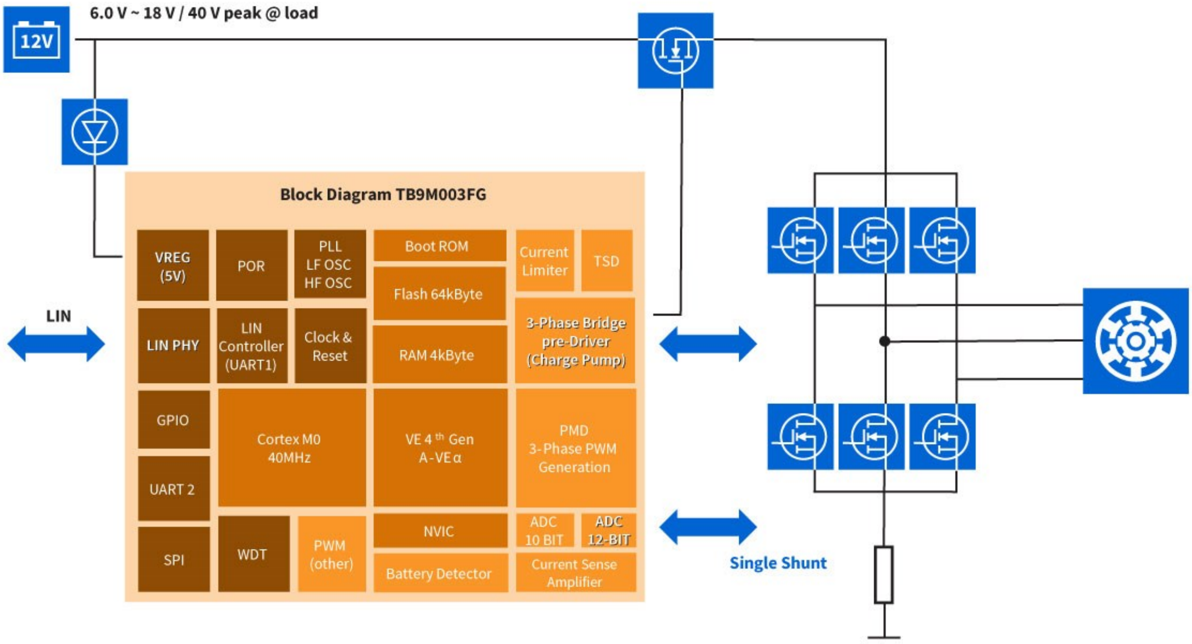

Figure 4: TB9M003FG system diagram for FOC of BLDC motors in automotive applications

CPU core and on-chip memory

The CPU system on the TB9M003FG (Figure 5) is based on an ARM® Cortex®-M0 processor running on a 40MHz clock.

The AHB-Lite interface provides simple integration to all system peripherals and memory. The range of on-chip memory includes 12 Kbytes ROM (Boot Loader, Flash API), 64 Kbytes Code Flash and 4 Kbytes SRAM. All memories feature error correction code (ECC) for single (1-bit error) correction and double (2-bit) error detection. The TB9M003FG also features multiple operating modes, including normal mode, debug mode, and BOOT loader mode (via UART).

The processor also includes a nested vector interface controller (NVIC) component, which features a wake-up interrupt controller (WIC) that provides ultra-low power sleep mode support.

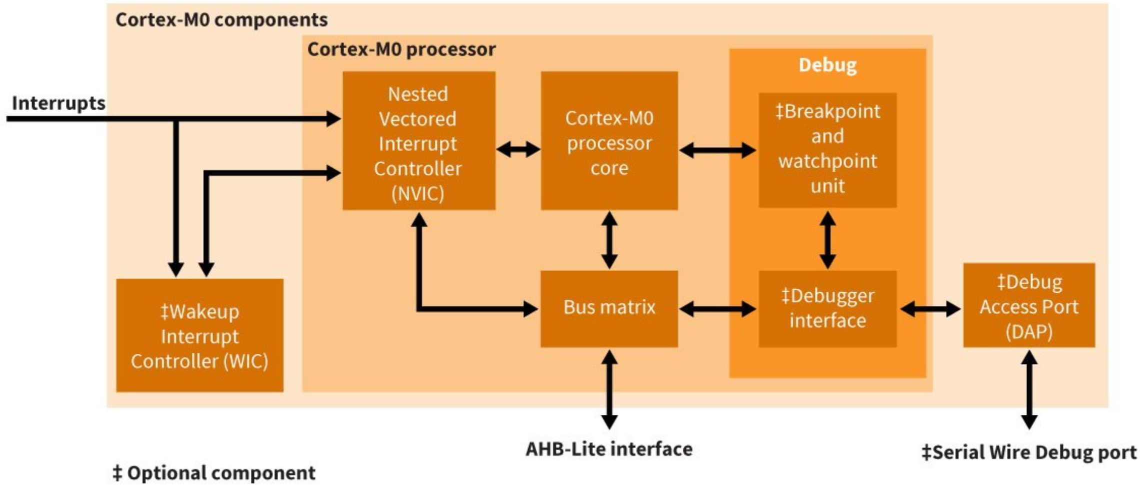

Figure 5: TB9M003FG CPU Core / Subsystem

Vector Engine A-VEα

The vector engine on TB9M003FG (Figure 6) supports PI for current control (d-/q-axis), Park and inverse Park coordinate transformation as well as Clarke and inverse Clarke phase transformations. It also supports space vector modulation (SVM) and enables sine and cosine calculation of the phase angle (θ) as well as rotation angle estimation. The engine also includes a scheduler, allowing flexible task execution. It also supports a 1-shunt sensor, with 2-phase or 3-phase modulation and has a PWM shift function (automatic PWM modification for 1-shunt measurement). Other features include auto-trigger generation of current detection with a wait function for minimising the switching noise impact, a phase timer for performing automatic theta (θ) compensation for schedule repetition and synchronised interaction between the vector engine, programmable motor driver (PMD) unit and the ADC.

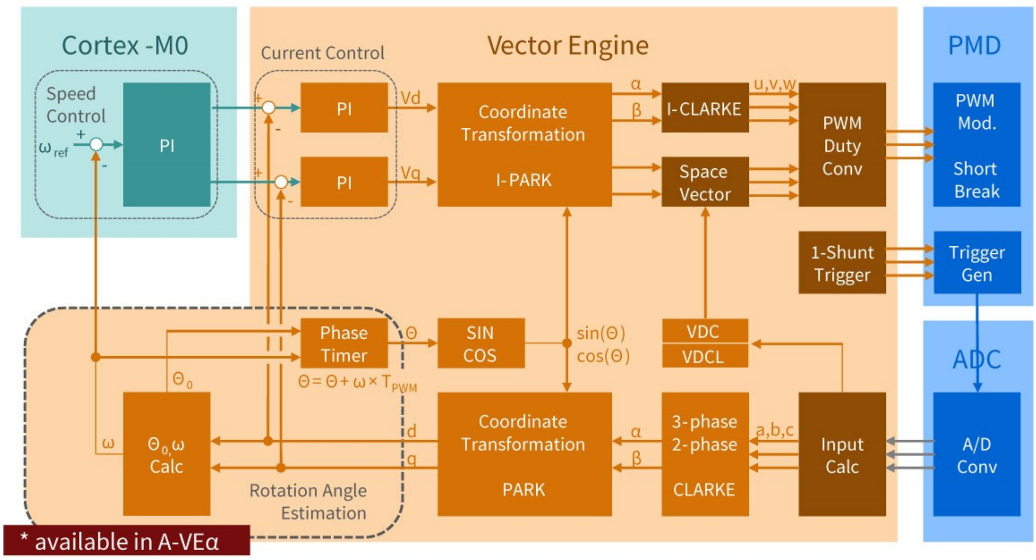

Figure 6: Smart co-processor for sensor-less vector control

Programmable motor driver unit

The PMD unit (Figure 7) enables PWM carrier generation (triangular, inverse triangular, saw-tooth or inverse saw-tooth) with individually selectable waveforms for each phase. It also features a user-configurable phase shift between the carrier and each phase. The PWM carrier frequency is between 0.06 kHz and 117 kHz, while the vector engine runs at 60 MHz. Complementary 3-Phase PWM generation is performed by comparing the PWM carrier with the individually adjustable duty cycle setting. This unit also features conduction control with U/X, V/Y and W/Z phase outputs individually configurable as PWM or as high/low output and to be active-high or active-low. A/D conversion trigger generation function has adjustable timing and is synchronised to the PWM carrier, while buffer function settings can be changed during normal operation. For added robustness, the unit also features a protection control circuit that supports the EMG and OVV inputs, while a dead-time control circuit prevents short-circuiting when switching between upper and lower phases (U/X, V/Y, W/Z).

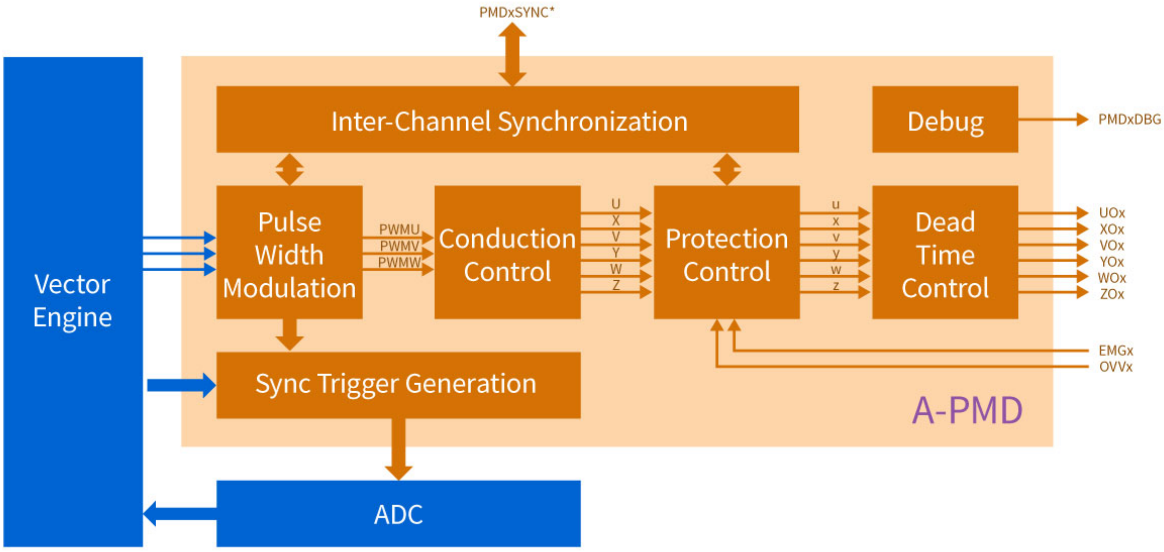

Figure 7: PMD unit block diagram

Encoder input circuit

The TB9M003FG enables precise motor position acquisition for systems that use incremental encoders and Hall sensor ICs (Figure 8). The encoder mode supports AB- and ABZ-type incremental encoders, while the sensor mode supports 2-phase and 3-phase Hall sensors. There are three sensor operating modes available - event counter, timer counter, and phase counter. It also supports zero-crossing detection for BLDC motors with square wave commutation using Back EMF (BEMF) detection control. Other features of the encoder input circuit include rotation edge and direction detection, a 32-bit up-/down counter (controlled by rotation direction), a division pulse output, an Interrupt (generated by edge detection or counter values), and an abnormal state detection flag.

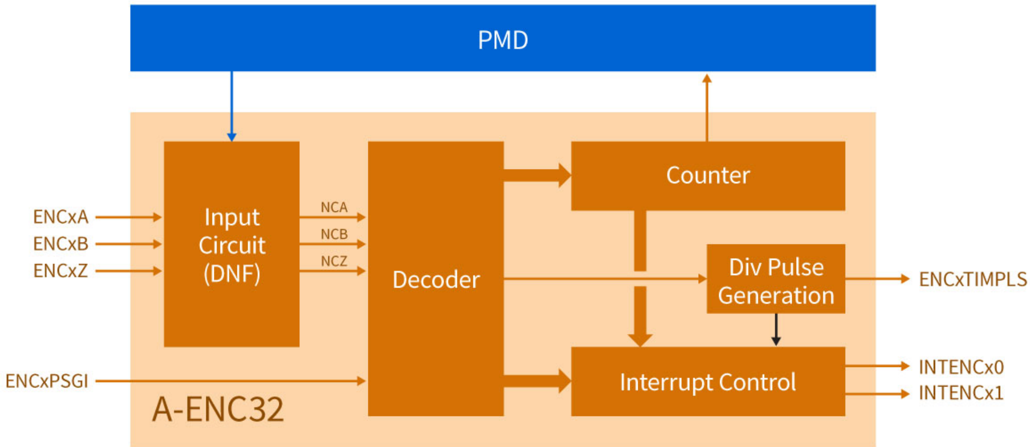

Figure 8: Encoder input circuit on the TB9M003FG supports incremental encoders and Hall sensor ICs

Bridge driver

The TB9M003FG integrates a 6-channel gate driver to control external B6 N-channel MOSFETs, and includes a broad range of features to ensure system-level robustness and reliability. These include MOSFET charging and discharging drive capability as well as MOSFET open circuit and short circuit detection and programmable VDS level detection (Figure 9). A built-in charge pump has a typical output level of VBat +12 V and 50 % duty cycle range. The bridge driver also includes slew rate control (SRC), which provides programmable three timing selectable phases - up to 120mA in the first phase (Phase 1) and up to 48mA in the second phase (Phase 2).

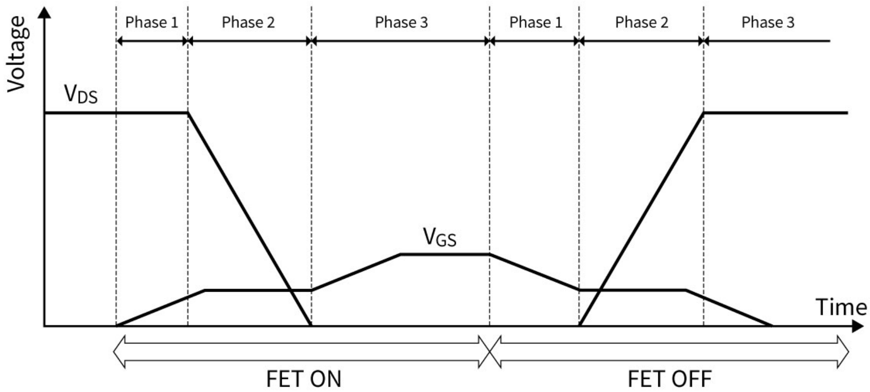

Figure 9: Bridge driver features voltage level detection

Communication interfaces

For maximum flexibility, the TB9M003FG offers various communication interfaces. To achieve this, the 12 GPIOs can be multiplexed with other interfaces, including LIN, UART2, and SPI. The LIN UART is based on the ARM PrimeCell® PL011 and includes an ISO17987/SAEJ2602 Phy+ Controller. It enables baud rate auto trimming and features built-in wake-up control. UART2 is also ARM PrimeCell® PL011 based and has 8-bit data length with a maximum baud rate of 1Mbit/s. The SPI interface using ARM PrimeCell® PL022 operates at up to 4MHz/1MHz in master and slave. Finally, the TB9M003FG features three Hall sensor inputs for position sensing.

Analog peripherals

The TB9M003FG features a diverse set of analog peripherals. These include an internal voltage regulator (LDO), which can provide up to 100mA driving current for external circuitry, and a power-on-reset (POR) function. Other features include a 10-bit ADC (16us conversion @ 40 MHz clock) to perform automatic limit checking for up to four channels, including up to two external analog inputs, Vcc (5V), voltage monitoring (VMON) and chip temperature readings. A 12-bit ADC (1.33µs conversion @ 30MHz clock) is exclusively dedicated to motor control voltage (VM) and current measurement. Other peripherals include a current sense amplifier with programmable gain settings (5/10/15/20/40/60 V/V) and an ADC settling time of 1µs in addition to various comparators for BEMF, overcurrent and short circuit detection.

Clock controller

The clock controller on the TB9M003FG includes two on-chip oscillators - HOSC at 20MHz (±5%) and LOSC at 32kHz (±25%). A PLL can be set to multiply the clock oscillation frequency by either a factor of 12 or 15. An internal clock has a maximum frequency of 120MHz but, as an alternative, it is also possible to connect an external crystal oscillator (16MHz/20MHz). Clock gearing is available for peripheral timing. The standby current consumption of the clock controller in sleep mode with all blocks disabled but supporting LIN wake-up) is less than 3µA (max). Current consumption in standby mode (cyclic wake-up) is below 90µA (max).

Safety

Safety features on the TB9M003FG help to provide extra system reliability. These include error correcting code (ECC) for RAM, ROM and flash memory. Other features include battery over- and undervoltage detection as well as configurable MOSFET overcurrent protection for the LDO as well as the low side and high side drivers. It also features a temperature sensor and the MCU has an internal watchdog-timer. Finally, there is PLL loss-of-lock detection function.

Software architecture and development support

With its scalable, extendible and portable multilayered structure, the provided software encapsulates the underlying hardware and functionality, introducing levels of modularity, and further improves the maintenance and testability.

A top-level view of the firmware architecture is presented in Figure 10.

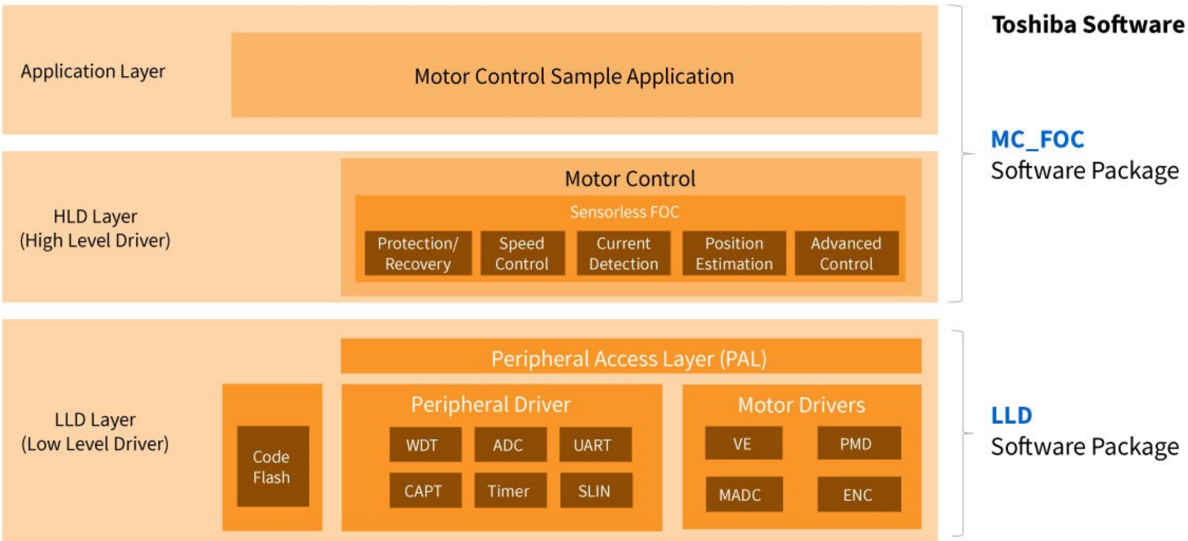

Figure 10: Software architecture for a sensor-less FOC BLDC motor application

The MC-FOC software package includes a sample motor control application, a high-level (HLD) and a low-level (LLD) device drivers with abstraction layer for the underlying periphery and motor control specific hardware accelerators. API specifications and extensive documentation round the delivery. The software packages are provided by Toshiba under a range of attractive and flexible licensing conditions., including free evaluation versions as well as commercial use licenses for mass production.

SmartMCD evaluation kit
The SmartMCD evaluation kit is fully supported by Toshiba's software developed with the Arm® Keil® microcontroller development kit (MDK) and the TB9M003FG evaluation board, which round the solution (Figure 11). The evaluation kit also offers four (optional) inverter boards featuring automotive-grade power N-channel MOSFETs from Toshiba, including:

- TK100S04N1L 40V/100A 2.30mΩ DPAK+
- TPWR7904PB 40V/120A 1.14mΩ DSOP Advance(WF)L
- XPH1R104PS 40V/90A 2.40mΩ SOP Advance(WF)
- XPN3R804NC 40V/40A 3.80mΩ TSON Advance(WF)

In addition, Debug interface access is provided via J-link or on-board CMISIS-DAP.

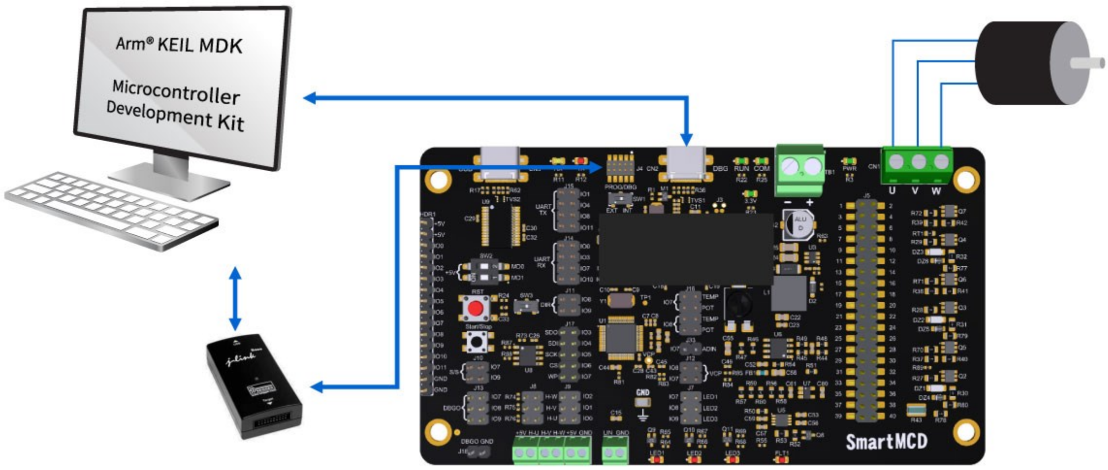

Figure 11: TB9M003FG development kit and evaluation board

Motor Studio
Motor Studio is an easy-to-use, well-structured, and versatile PC tool that complements Toshiba's solution. Built for Windows 10, it features parameter configuration, drive control, and real-time logging of various motor parameters and diagnostics via a high-speed UART. Together with the TB9M003FG evaluation board, it allows quick and easy system evaluation as well as BLDC motor application development and prototyping. The tool's Digital Storage Oscilloscope (DSO) module makes possible the graphical tracking of up to 4 parameters - target/actual speed, torque, current on a scalable and zoomable chart (Figure 12). It also provides detailed error state indication as well as real-time monitoring of temperature and DC link voltage levels.

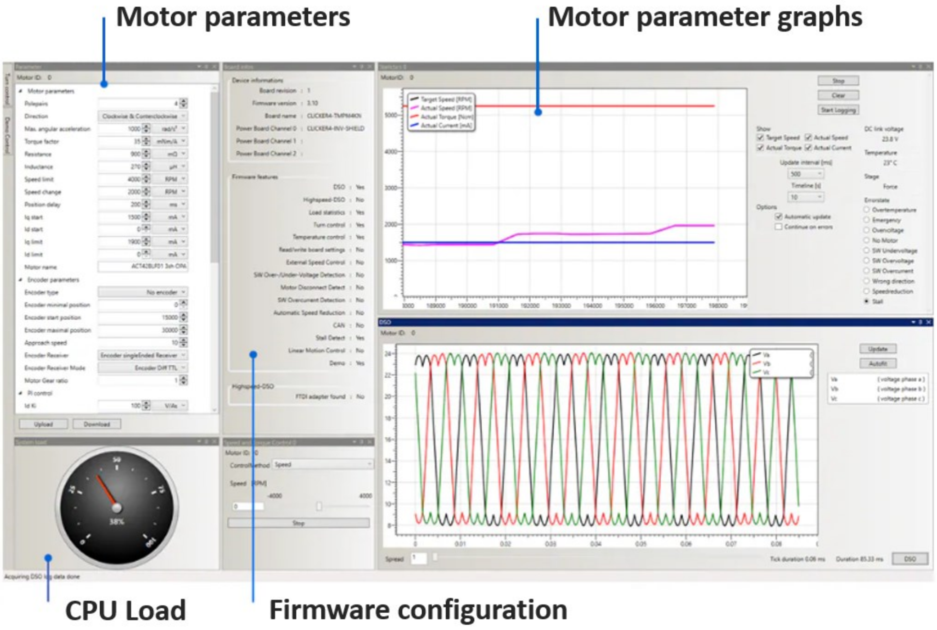

Figure 12: Motor studio accelerates BLDC application development and prototyping

Conclusion

FOC offers many advantages for BLDC motor operation in automotive subsystems, including smooth operation over the full speed range and superior dynamic performance with fast acceleration and deceleration. However, it is complex and demanding to implement and can easily overwhelm standard MCUs. This white paper explored the features and benefits of theTB9M003FG, the first IC out of Toshiba's Smart Motor Control Driver (SmartMCD™) family which not only integrates an Arm® Cortex® M0 based MCU with the fourth-generation vector engine co-processor, but also includes a 3-phase motor control gate driver to enable smaller, simpler and lower cost 30 – below 1000 Watt BLDC motor designs in automotive applications.

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