TOSHIBA

Innovative packaging and thermal design boost the density of power supplies for AI, telecom, and e-mobility

Introduction

Multiple industries are looking for a step change in power density. The pressures are different in each market. But they lead to the need to deliver higher energy levels from smaller packages. Circuit topology and component technology have helped to make great strides at increasing watts per cubic centimetre. But further improvements demand that manufacturers examine novel mechanical design options. Engaging the assistance of power specialists in combining these design changes to improve power density is more important than ever.

Artificial intelligence (AI) provides one example of the demand for increasing power density. AI servers need the combined performance of graphics processing units (GPUs) and neural processing units (NPUs) to deliver the performance that operators need to support highly complex language models and agentic AI systems. For the highly parallelised workloads GPUs and NPUs require high DC current levels supplied to each point of load by multiple 48V rails distributed throughout the racks. Operators do not want to sacrifice space to the power subsystems more than is necessary. That demands converters that are able to sustain outputs of several kilowatts, with full power-factor correction (PFC) support without increasing the space needed inside the rack.

The telecom sector needs more efficient solutions to meet the increasingly complex power needs of cellular base stations. More compact converters that can support kilowatt power outputs allow for higher channel densities and more sophisticated multiple-antenna designs.

In the mobility sector, users want to charge e-scooters quickly and take advantage of the longer range made possible by high-capacity battery packs without increasing weight and bulk. Being able to deliver several kilowatts of power from an AC source to a fast charger is becoming a key requirement. That includes the need for PFC to ensure the power is drawn in a way that is compatible with grid requirements.

The densification of these power converters requires innovative design approaches that go beyond improvements in individual device performance. Changes in technology allow for modified topologies. With PFC, for example, bridgeless conversion has allowed the use of fewer components by eliminating the bridge rectifier circuit of older designs. Migration to silicon carbide (SiC) has helped this by supporting faster switching and reduced losses compared to silicon MOSFETs in these types of circuits. The higher efficiency and thermal capability of silicon carbide also allow for alternative packaging choices, including surface-mount options.

This is where reference designs developed by semiconductor suppliers are invaluable. Providing customers with practical insights into innovative design choices, reference designs illustrate how changes in component selection can open previously unexplored design possibilities without the need for customers to embark on extensive prototyping programmes. One example of this approach is an isolated 3kW AC/DC converter developed by Toshiba engineers, combining a PFC stage with a phase-shifted full-bridge (PSFB) architecture to support higher power density. This converter design builds on an existing 1.6kW architecture and uses a surface-mount packaging approach enabled by wide-bandgap (SiC) semiconductors, together with changes in PCB layout, to nearly double the output power with only a small increase in overall volume.

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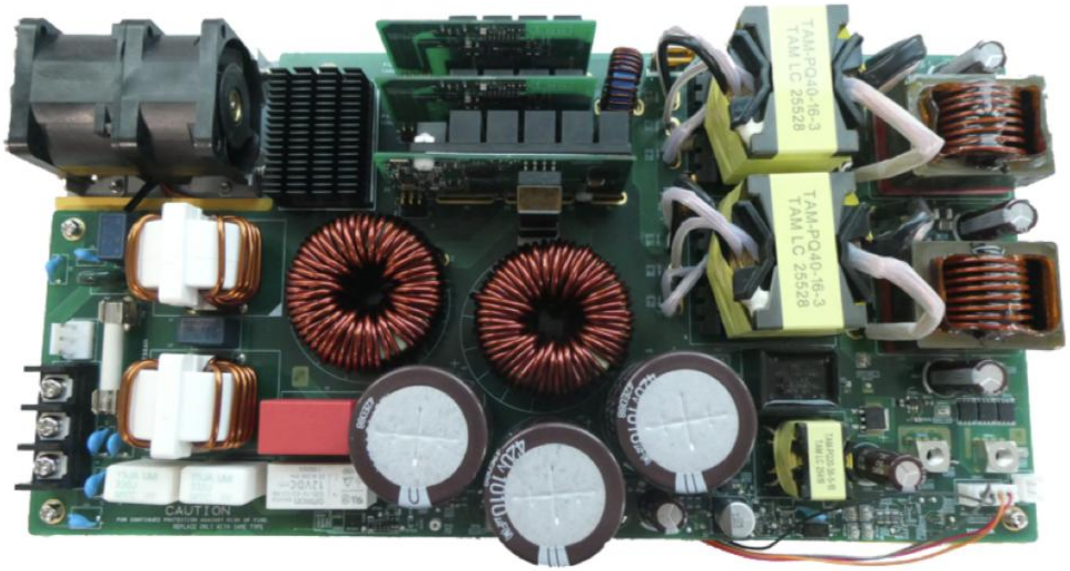

Figure 1— Innovative 3D design enables a 3kW AC/DC power converter with a density of 1.25W/cm³

Overcoming the limitations of a planar design

Frequently, power-converter designs are designed assuming a 2D layout. The components will be arranged on a single printed circuit board (PCB). The height of the overall subsystem will be governed primarily by large passive components such as capacitors and transformers.

Within these designs, the popular TO224 and TO247 packages provide good trade-offs between thermal performance and footprint. The metal tag bonded to one end of these packages allows for product designs that employ a vertical heatsink to be attached and conduct excess thermal energy away from the die inside. Normally, the thermal connection is to the drain of a MOSFET, where the most heat develops during operation.

In the context of a planar design surrounded by tall passive components, this type of packaging represents a good choice. The vertical heatsink allows for a small PCB footprint. But it limits the number of mechanical design options that designers could use to improve density. One possibility explored and developed into a full reference design by engineers at Toshiba was to separate the converter into sub-modules that could be mounted on daughterboards. However, the use of daughterboards brings constraints in terms of component height. The design needs to consider the spacing between daughterboards needed to accommodate the power devices and their heatsinks. If the resulting structures are too tall, the advantage of using vertical daughterboards disappears because of the need to increase the horizontal spacing between boards.

Once separated into daughterboards, the use of low-profile packaging allows for situations where they are deployed using a vertical orientation. This reduces the footprint needed on the main PCB. At the same time, sufficiently compact daughterboards need not extend much further in terms of height than capacitors and other larger passives on the main board. Such a design also allows for improved heat dissipation with proper thermal design. It is possible to arrange the

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daughterboards in a similar way to the heatsinks that would be used with TO220 or TO247 devices. In doing so, forced-air cooling from a single fan can pass over both surfaces of each sub-board.

With conventional silicon devices, such a design might continue to need to use TO224 or TO247 packaging and the space overheads they bring. SiC delivers improved thermal behaviour and efficiency. That combination makes it possible to explore new packaging choices for high-power switching devices. The high efficiency, coupled with the ability of SiC to operate at high junction temperatures, enables the use of surface-mount packaging. The switch to this packaging then opens possibilities in power-converter 3D design. Using surface-mount package options allows small boards to sit closer together, with the practical density governed by thermal considerations.

Topology choices

For the reference design conceived to show the advantages of using compact switching devices on daughterboards, Toshiba engineers considered several circuit-topology options for the PFC and AC/DC conversion elements. A semi-bridgeless topology offered the best tradeoffs of density and functionality. Fully bridgeless designs reduce the total number of discrete components by removing the front-end diodes of a rectifier bridge. But they can suffer from noise and inrush current issues. A dual-boost, semi-bridgeless topology uses several additional diodes, D_{aa} to D_{dd} in Figure 2, to reduce these issues. However, the diodes are placed in such a way that D_{cc} and D_{dd} do not contribute to the circuit's behaviour after start-up.

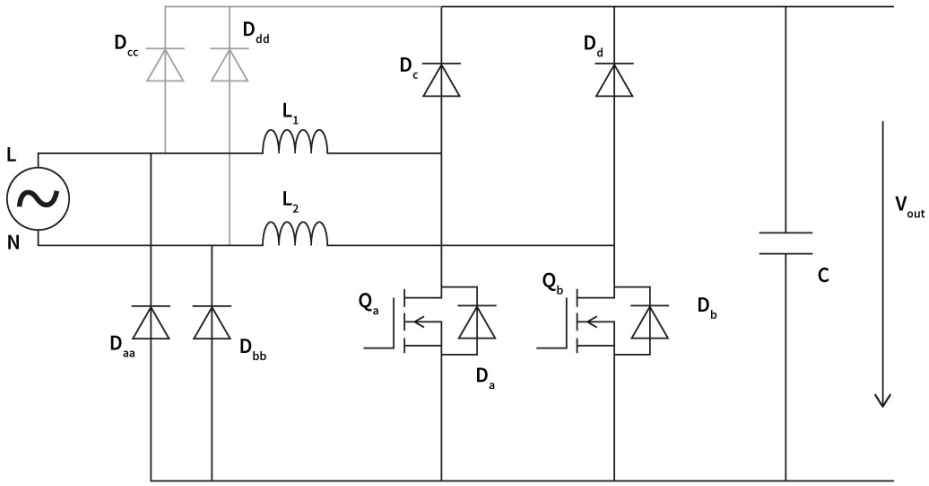

Figure 2 — Semi-bridgeless PFC circuit operation

For the components in the PFC sections, Toshiba engineers selected two key SiC devices. One is the TW092V65C MOSFET. This is a 650V enhancement-mode device using Toshiba's third-generation SiC technology with dedicated integrated Schottky barrier diode. In this device, drain-source on-resistance is less than 100mΩ, and it can be supplied packaged in a compact DFN8x8. This package employs a large metal heat pad on the underside. The other key SiC device is the TRS12V65H Schottky barrier diode, also packaged in a DFN8x8.

Output current from the PFC daughterboard flows to a phase-shifted full-bridge (PSFB) that is used to step the incoming voltage down to 50V, using a transformer stage that delivers DC through a smoothing stage at the output that incorporates several power MOSFETs. The PSFB circuit deploys on the primary side four MOSFETs with antiparallel

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Schottky diodes to implement a full bridge. Such a design can handle high power levels because losses are significantly reduced by the use of zero-voltage switching (ZVS) control. The PSFB in the reference design employs the TW027U65C SiC MOSFET with an integrated Schottky barrier diode. The device comes in a TOLL package, with a metal surface-mount tab acting as the drain-to-heatsink contact.

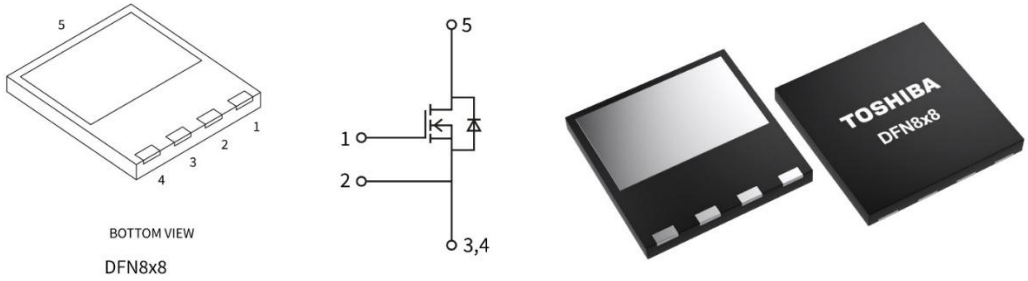

Figure 3 — DFN8x8 package showing the heat pad

The circuit elements most in need of high thermal performance are the power semiconductors used for high-frequency switching. In an AC/DC power converter designed for AI servers, these components will primarily be used in PFC and the primary side of the PSFB sections because of blocking voltage requirements. With this architecture, it is possible to place the key switching devices and their control circuitry functionally structured on individual daughterboards. The transformer and post-transformer stage that follow the PSFB, which require physically larger passive components, can remain on the main board. The same is true for the inductors and other passive devices that feed into the PFC section.

There is no efficiency penalty for moving the switching elements to daughterboards. Soldered connections to large copper areas on each of the daughterboards allow for high-conductivity paths between the main board and the daughterboards.

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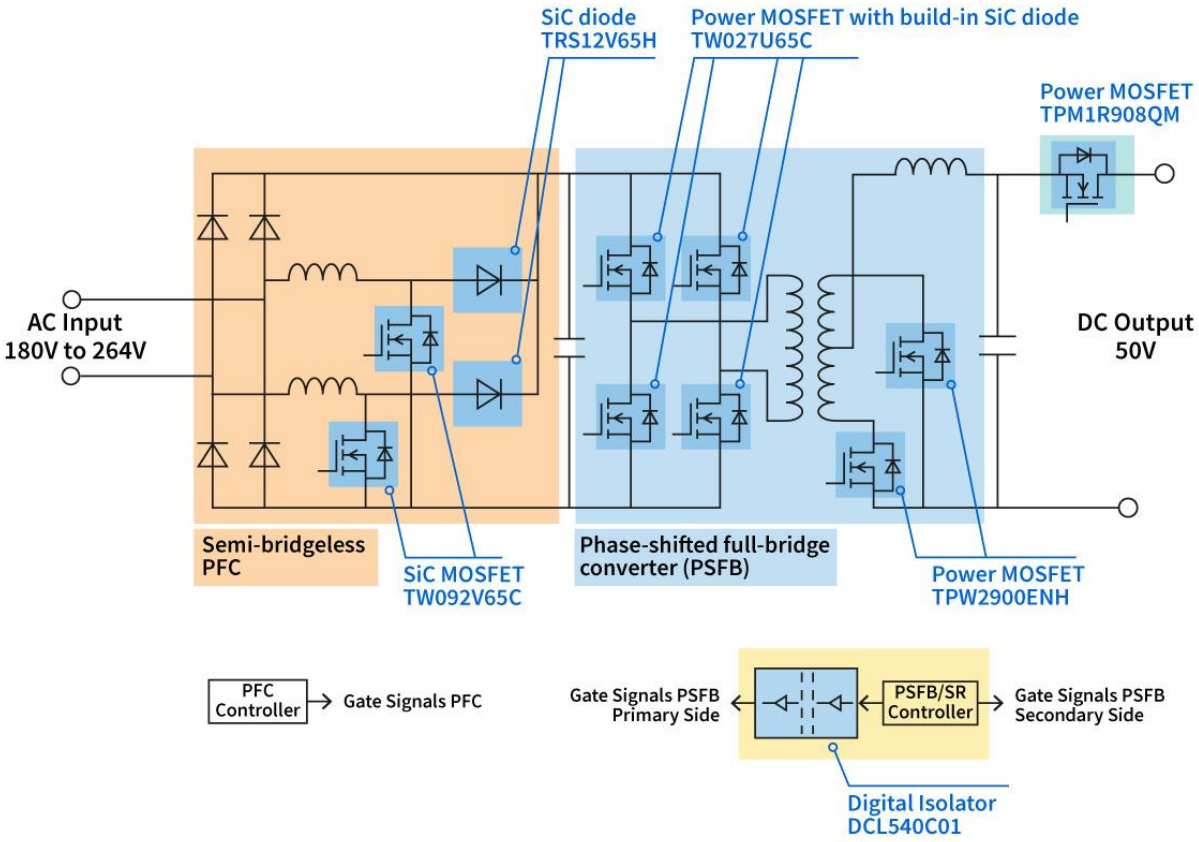

Figure 4 — Power supply unit design showing the PFC and PSFB sections

In principle, the improvements offered by the new generation of SiC devices would enable a near doubling in output power to 3kW from the 1.6kW achieved with the earlier RD240 reference design, which also employs a semi-bridgeless PFC topology feeding into a PSFB. Because of the significantly higher power capability, such a power converter would demand the use of larger electrolytic capacitors for power smoothing. This resulted in a minor change to the form factor to accommodate these larger passive components. The revised approach resulted in a 34% improvement in power density by moving to a multi-board design.

Thermal optimisation

With such a large increase in power density, thermal behaviour becomes a key concern. Insufficient heat flow from the switching circuits will compromise performance. Though the thermal conductivity of the DFN and TOLL packages through the bottom surface is relatively high, thermal design required additional optimisation to deliver the full benefit of the innovative partitioning and layout.

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Evaluation of the first prototype showed hot spots forming around two of the power semiconductors on the PFC daughterboard. If left unaddressed, the heat cycle (ΔTc) caused by switching activity could reach up to three times the internal criteria of 60°C. To remain within this limit, the output power would need to be limited to 1.4kW. The image below shows the measurement results for the PFC board.

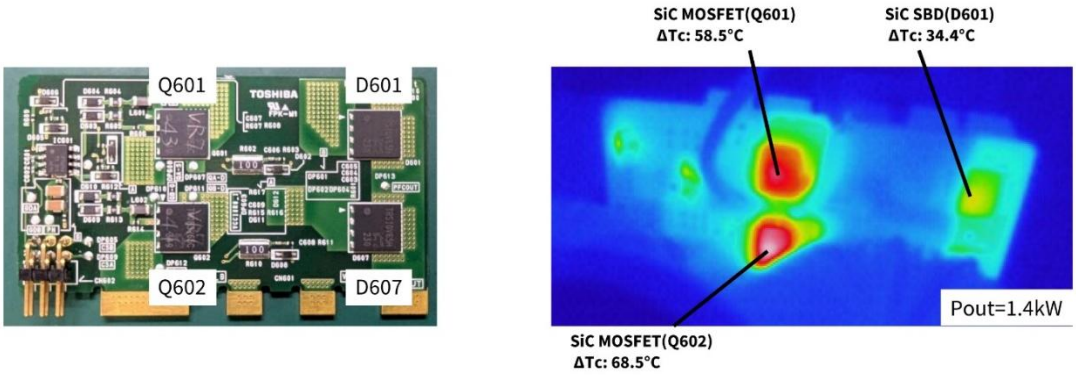

Figure 5 — The layout of the first iteration of the PFC sub board and its thermal analysis

The design team identified several options for improving thermal performance in a way that allowed increasing the power output to the maximum. To improve heat delivery to a heatsink mounted on the backside of each daughterboard and take full advantage of forced-air cooling, the first change involved improving the heat transfer of vias under the packages' thermal pads.

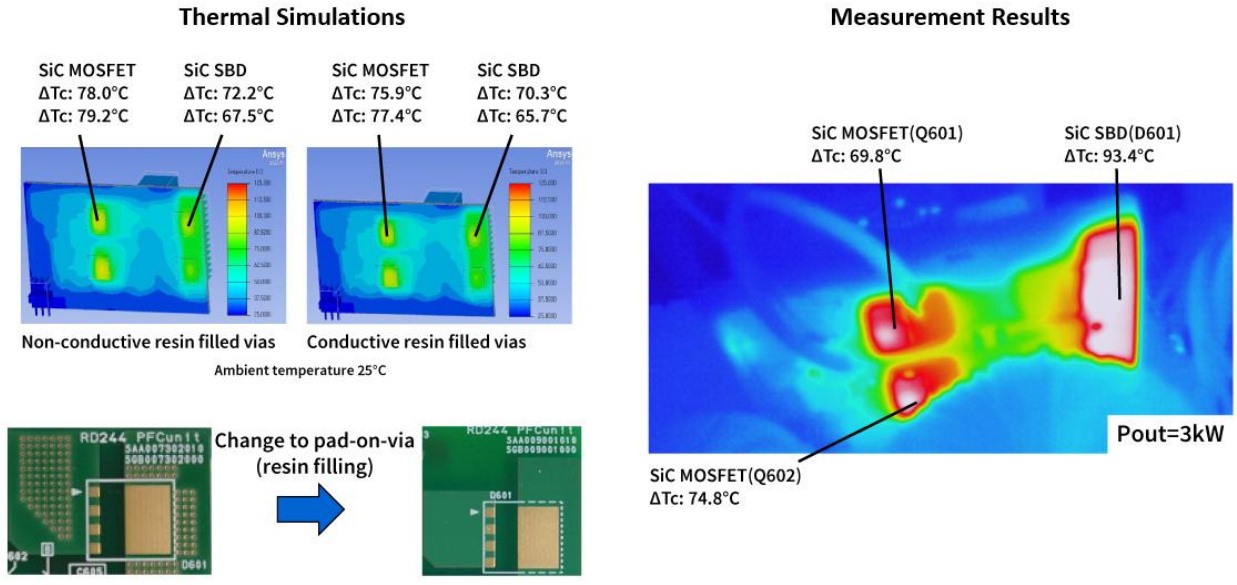

Figure 6 — Changing conductive vias on the second PFC sub board to non-conductive filled vias helped improve heat flow and reduce ΔTc around the power switches

Thermal simulations (upper left corner of Figure 6) showed that filling these vias would significantly increase thermal conductivity. With the change, the measured ΔTc of the hottest devices would decrease by more than 50% (Figure 6 – image on the right).

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Simulations (Figure 7 – image on the left) showed that further improvement would come from changing the fill material inside the vias to one that is electrically conductive. A layout change that relocated two small transformers to the front side of the daughterboard allowed for the use of a larger, single heatsink instead of two separate heatsinks. This alteration, coupled with an increase in board thickness, showed that the ΔTc value should fall well below the critical value of 60°C. Physical tests (Figure 7 – image on the right) showed that the revised design could easily support an output power as high as 3.1kW. However, thermal imaging showed that one of the MOSFETs on the PFC daughterboard was significantly hotter than the other. That suggested further optimisation of the thermal design was advisable.

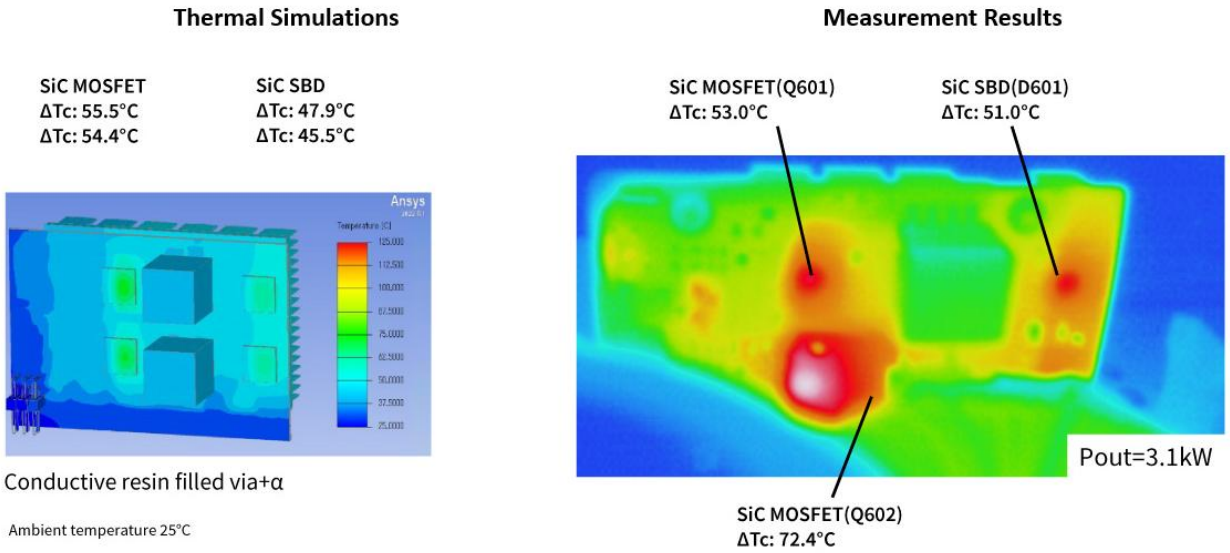

Figure 7 — The third iteration of the PFC daughterboard, showing further decreases in ΔTc

The heatsink, which used a crimp connection secured at three points by screws, did not attach sufficiently well to the backside of the PCB beneath the transistor found to be running hot.

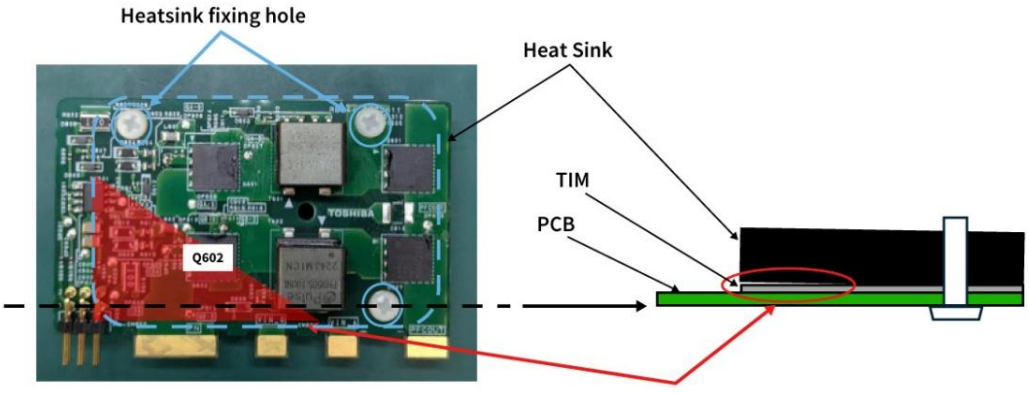

Figure 8 — The use of three screw points to attach the heatsink to the PFC daughterboard resulted in poor heat transfer away from one of the key power transistors

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A small design revision introducing two connection points along a diagonal resulted in better alignment. For production, the team opted for a design with four screws close to the corners of the heatsink to ensure high overall compression during operation. Following these changes, the ΔTc fell to below 50°C for all the power semiconductors on the PFC daughterboard.

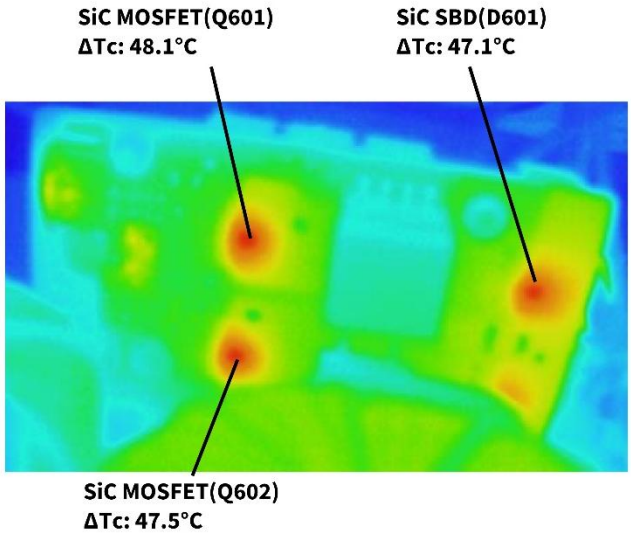

Figure 9 — Thermal image of the final interaction showing ΔTc well within design limits

Summary

The changes in packaging, circuit topology optimisation, layout, and thermal engineering, supported by simulation-driven optimisation, resulted in a design that increased power density by over 30%. This created the basis for a power converter capable of sustaining 3kW in a volume of 2400cm^3, achieving a power density of 1.25W/cm^3. The project also highlighted the importance of building reference designs to demonstrate how customers can quickly adapt these novel techniques to optimise their own power subsystems for capacity and efficiency. Comparatively minor changes to the topologies and component selection can enable the development of power converters for a range of markets, from telecom to e-mobility. Together, they demonstrate the combined potential of SiC and packaging innovation.

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