TOSHIBA

e-Learning

Basics of Op-amps

Chapter3 Electrical characteristics

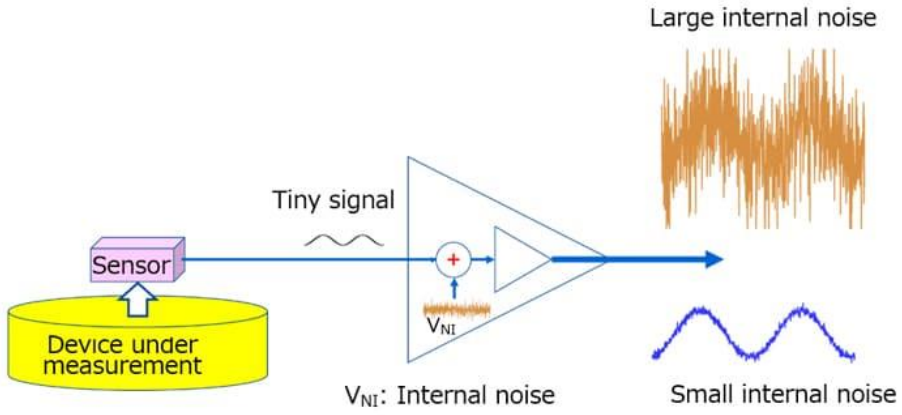
Toshiba Electronic Devices & Storage Corporation

Chapter3 Electrical characteristics

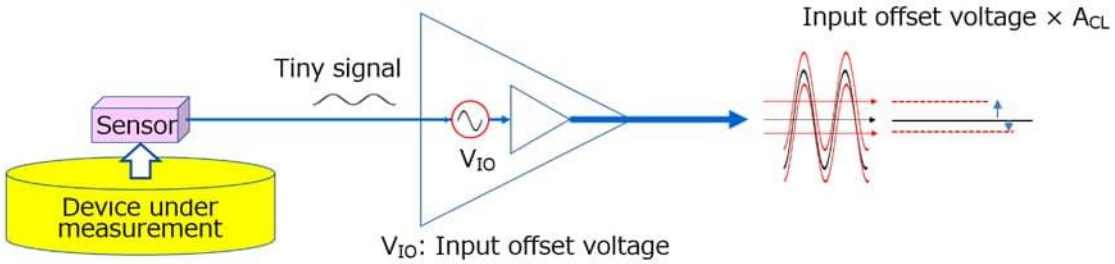
Electrical characteristics

This section describes the electrical characteristics specific to op-amps.
When an op-amp is used as an amplifier, the common-mode input voltage range indicates the input voltage range in which it operates properly. When an op-amp is used to amplify a tiny signal from a sensor or other device, what the sensor resolution is to a sensor is what the input offset voltage or the common-mode input signal rejection ratio (CMRR) is to an op-amp. The minimum resolution is determined by the amount of noise.
This section describes the following:

1. Input offset voltage, V_{IO}
2. Common-mode input voltage range (CMV_{IN}), common-mode input signal rejection ratio (CMRR)
3. Op-amp noise
4. Noise gain and signal gain



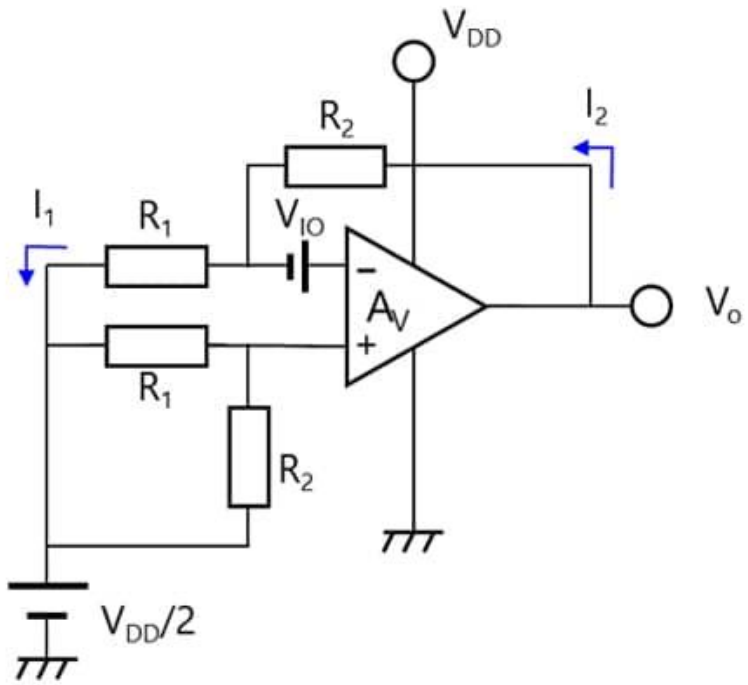
Op-amp with large internal noise



Effect of input offset voltage

1. Input offset voltage (V_{IO})

Figure shows the ideal op-amp without an offset voltage source (V_{IO}). When a common-mode input voltage is applied to $V_{IN(+)}$ and $V_{IN(-)}$ simultaneously, the output (V_o) voltage theoretically becomes $V_{DD}/2$. In reality, however, it has a small error from $V_{DD}/2$. The input offset voltage (V_{IO}) is the voltage applied between $V_{IN(+)}$ and $V_{IN(-)}$ required to reduce the V_o error to zero. The definition of the input offset voltage is similar to that of the common-mode input signal rejection ratio (CMRR) detailed in the next section.
In real-world applications, the input offset voltage multiplied by the closed-loop gain (A_{CL}) is added to the output voltage. Therefore, in the case of a sensor circuit, the maximum input offset voltage must be lower than its minimum sensitivity.



Test circuit for the input offset voltage

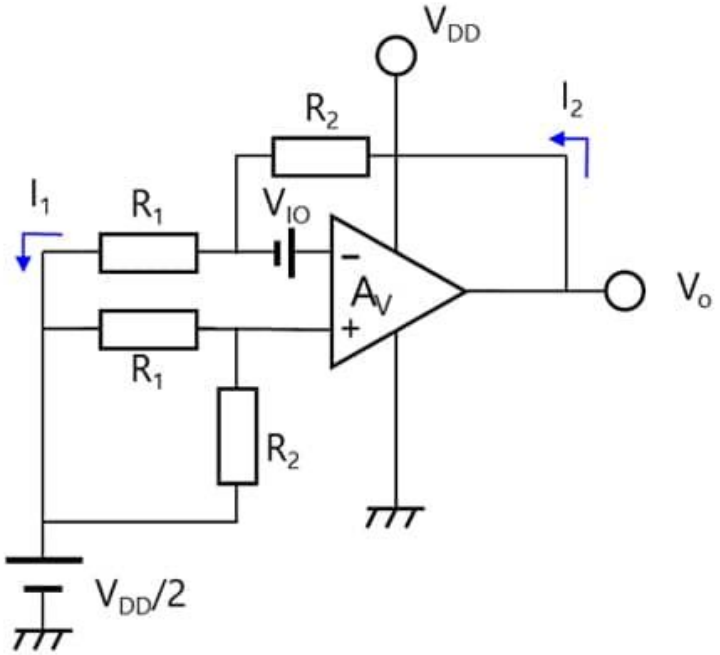
1. Input offset voltage (V_{IO})

Let's consider an op-amp with an input offset voltage of V_{IO}. As shown in the test circuit for the input offset voltage shown in Figure, this op-amp can be regarded as the ideal op-amp with an external V_{Io} voltage source connected to $V_{IN(-)}$.
The $V_{IN(+)}$ voltage becomes $V_{DD}/2$. From the concept of a virtual short, the $V_{IN(-)}$ voltage also becomes $V_{DD}/2$.
Therefore, the voltage at the intersection of R_1 and R_2 becomes $V_{DD}/2 - V_{IO}$. In the case of the ideal op-amp, $I_1 = I_2$.

$$I_1 = (V_{DD}/2 - V_{IO} - V_{DD}/2) / R_1 = - V_{IO} / R_1 = I_2$$
$$V_O = V_{DD}/2 - V_{IO} + (-V_{IO} / R_1) \times R_2$$
$$= V_{DD}/2 - V_{IO} \times (R_1 + R_2) / R_2$$

This can be rewritten as follows to calculate V_{IO}:

$$V_{IO} = (V_{DD}/2 - V_O) \times R_1 / (R_1 + R_2)$$



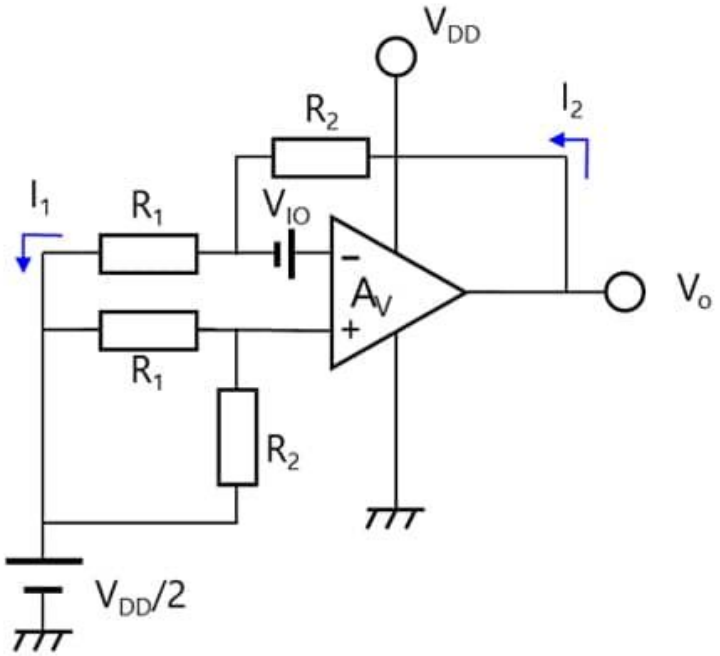
Test circuit for the input offset voltage

1. Input offset voltage (V_{IO})

$$V_{IO} = (V_{DD}/2 - V_O) \times R_1 / (R_1 + R_2)$$

Note that resistors have some tolerance. For actual measurement, the measured resistance values should be used.

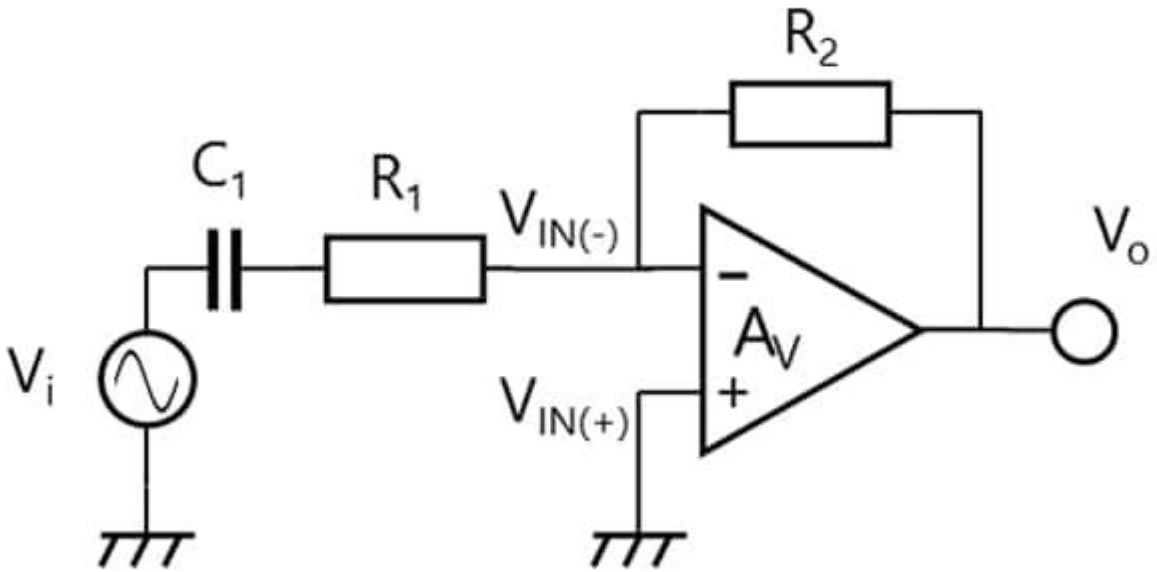
V_{IO} is a differential voltage between $V_{IN(-)}$ and $V_{IN(+)}$. Therefore, when an op-amp is used with a closed loop, the voltage obtained by multiplying this input offset voltage (V_{IO}) by the closed loop-gain is added to the ideal output voltage. Since the V_O voltage varies from device to device, it is necessary to consider the maximum offset voltage when creating a circuit design. If it exceeds a system's tolerance, it is necessary to modify the circuit configuration in such a manner as to reduce the effect of the input offset voltage or select an op-amp with a lower input offset voltage.



Test circuit for the input offset voltage

1. Input offset voltage (V_{IO})

The AC-coupled circuit is the simplest form of circuit to reduce the effect of the input offset voltage. Figure shows an AC-coupled inverting amplifier. When capacitor C_1 is connected in this way, current due to the input offset voltage does not flow through R_1. Therefore, the input offset voltage has a DC gain of 1 and thus has less effect on V_O.



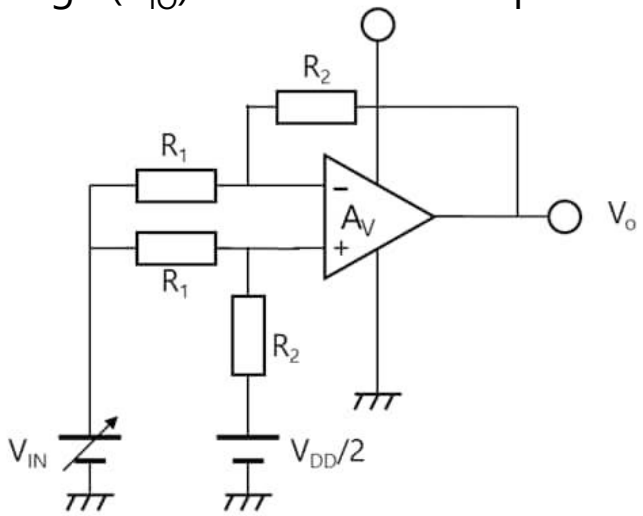
AC-coupled inverting amplifier

2. Common-mode input voltage range (CMV_{IN}) and common-mode input signal rejection ratio (CMRR)

The common-mode input signal rejection ratio (CMRR) of a differential amplifier is a metric used to indicate its ability to reject two signals or noises (common-mode noise) that have the same amplitude and phase at $V_{IN(-)}$ and $V_{IN(+)}$. It is expressed by the following equation. Figure shows a test circuit for the common-mode input signal rejection ratio.
The common-mode input voltage range (CMV_{IN}) is defined as the input voltage range in which the prescribed CMRR is satisfied under the prescribed conditions. The datasheets for Toshiba's op-amps specify the CMRR value under DC conditions.

$$CMRR = 20\log\left(\left|\frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}}\right| \times \frac{R_F + R_S}{R_S}\right)$$

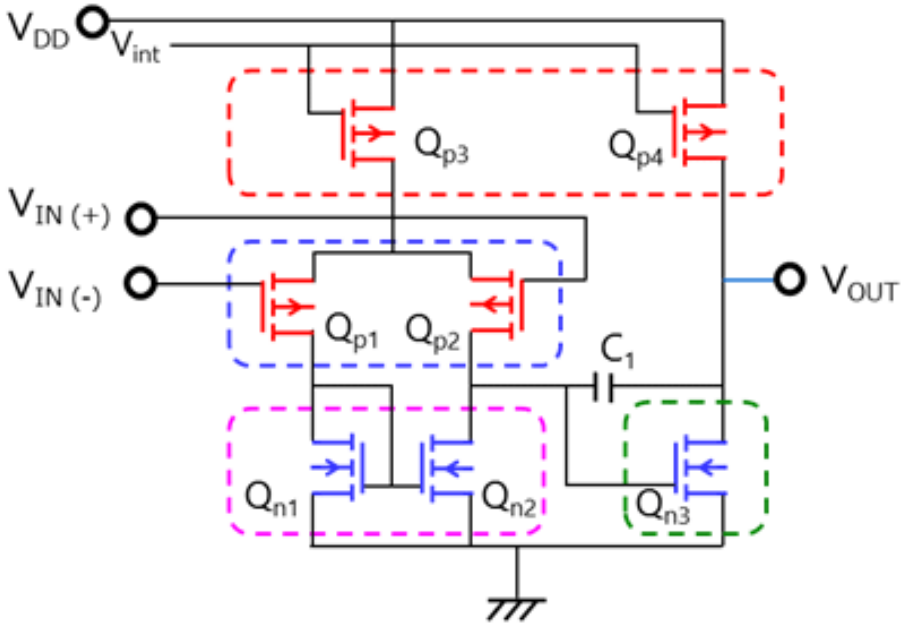
where V_{IN1} and V_{IN2} are the maximum and minimum CMV_{IN} values, respectively, and V_{OUT1} and V_{OUT2} are the output (V_O) voltages at V_{IN1} and V_{IN2}, respectively.
As can be seen from Figure, the input offset voltage (V_{IO}) discussed in the previous section is the CMRR value under a special condition ($V_{IN} = V_{DD}/2$).



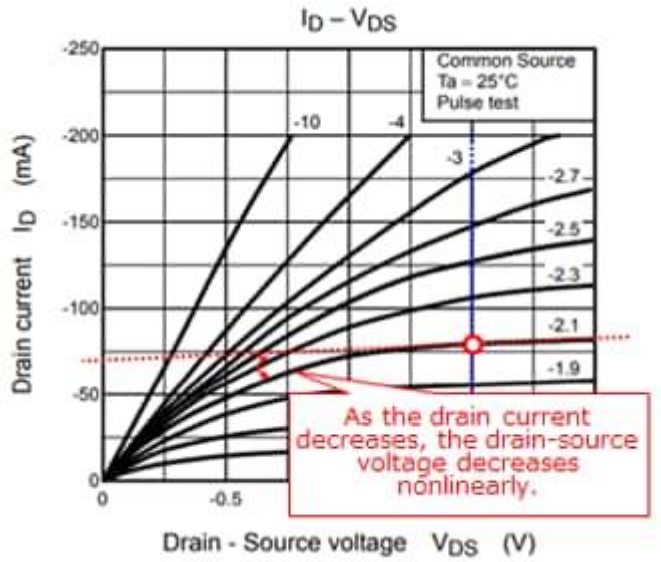
Test circuit for CMRR and CMV_{IN}

2. Common-mode input voltage range (CMV_{IN}) and common-mode input signal rejection ratio (CMRR)

The differential input pair of a typical op-amp is composed of P-channel MOSFETs as shown in left Figure. As the $V_{IN(+)}$ and $V_{IN(-)}$ voltages increase, the drain-source voltage of Q_{p3} in the current source decreases, causing the current flowing to the differential input pair and the current mirror to decrease slightly. Right Figure shows an example of I_D-V_{DS} curves for a discrete P-channel MOSFET. Suppose, for example, that V_{DS} = -1.5 V and I_D = 80 mA initially. As the drain current of the MOSFET decreases, its drain-source voltage changes nonlinearly in the saturation region.



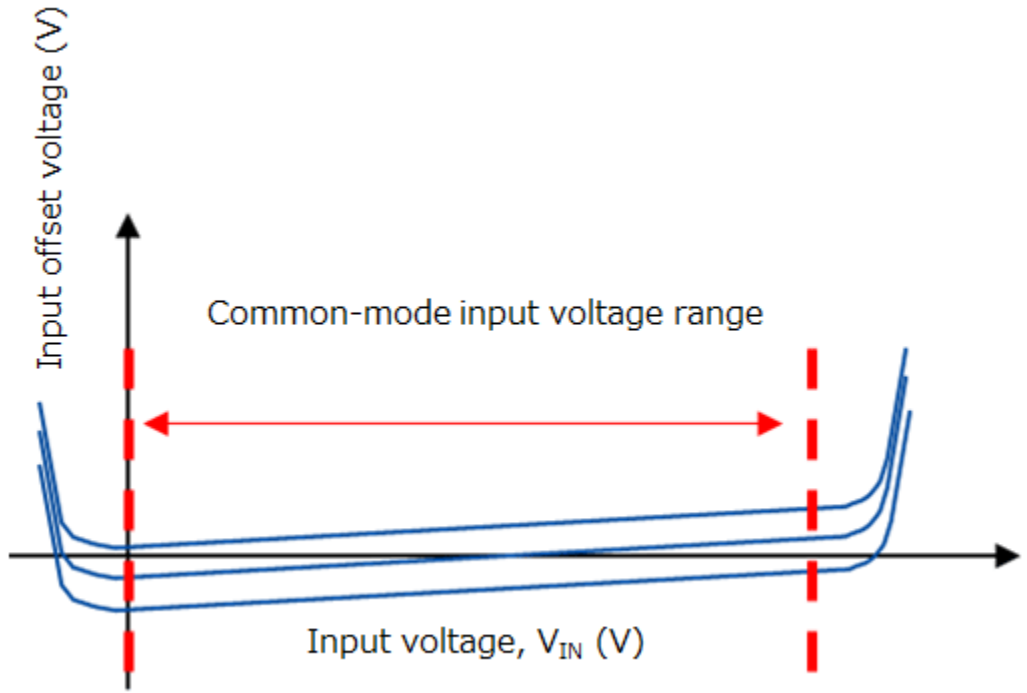
Simplified equivalent circuit for an op-amp



Example of I_D-V_{DS} curves of a P-channel MOSFET

2. Common-mode input voltage range (CMV_{IN}) and common-mode input signal rejection ratio (CMRR)

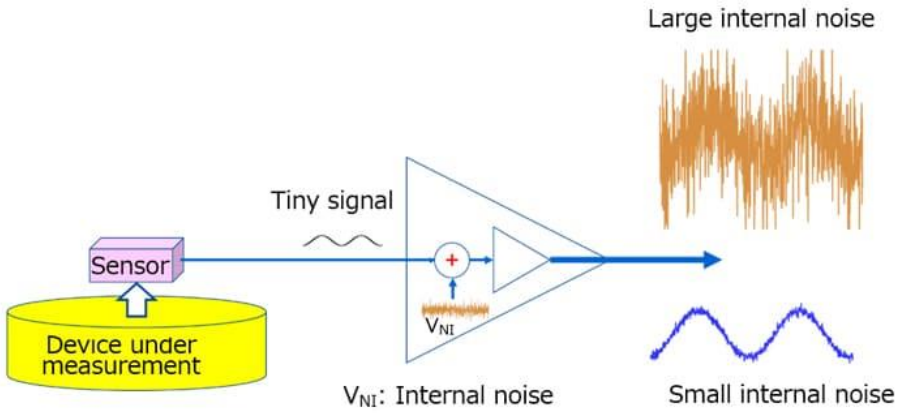
Although the internal devices of an op-amp IC are placed and fabricated in such a manner as to make the MOSFETs uniform, they are not perfectly symmetrical at the micro level. In addition, semiconductor chips are mounted on a metal frame in a package and soldered onto a printed circuit board. Therefore, the mechanical stress applied to each element of an op-amp IC differs slightly. These factors cause a slight difference in threshold voltage among the P-channel MOSFETs of the differential input pair. Therefore, a decrease in drain current causes different nonlinear changes in their drain-source voltage. As a result, the input offset voltage has a slope with respect to the input voltage (V_{IN}) in the common-mode input voltage range as shown in Figure. Therefore, the CMRR values are calculated at the maximum and minimum common-mode input voltages.



Input offset voltage vs input voltage (V_{IN})

3. Internal noise of an op-amp

Op-amps are used to amplify a tiny signal from a sensor or other device. Noise is added to this tiny signal and amplified by an op-amp. Therefore, noise contributes to a reduction in the sensitivity and accuracy of a sensor.
The noise related to an op-amp is divided into external noise caused by electromagnetic interference and external parts and internal noise. This section focuses on the internal noise of an op-amp.



Op-amp with large internal noise

3. Internal noise of an op-amp

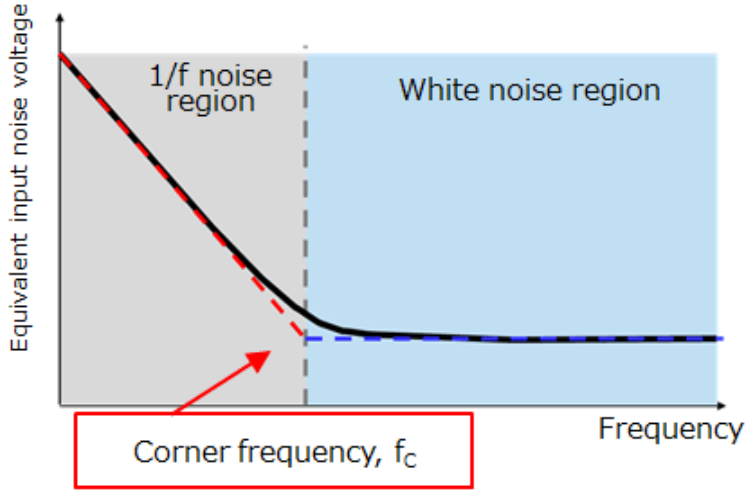
Two types of internal noise are defined as equivalent input noise:

- Frequency-dependent 1/f noise: Thermal noise generated by resistors and shot noise generated by free-moving carriers in a semiconductor
- Frequency-independent white noise: Flicker noise caused by crystal defects and burst noise

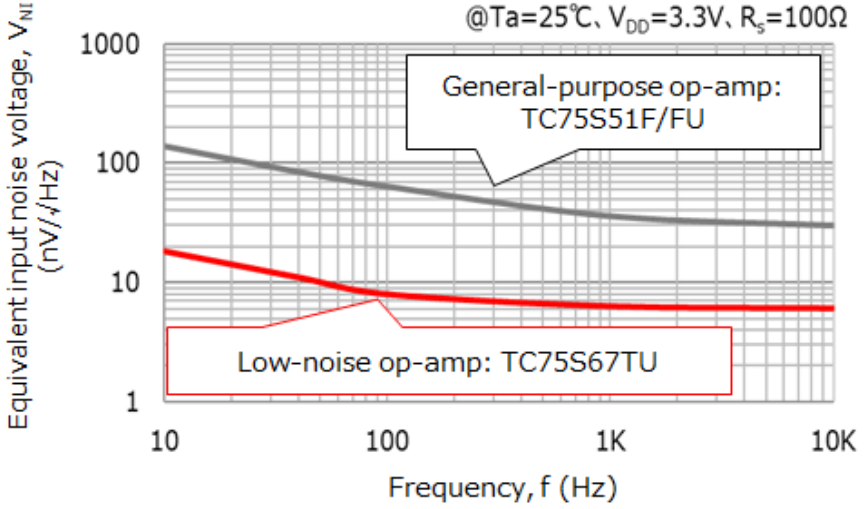
Left Figure shows the noise frequency characteristics of the op-amp, and right Figure shows an example of the measured equivalent input noise voltage. The Figure compares Toshiba's TC75S51 general-purpose op-amp and TC75S67 low-noise op-amp.

The general-purpose op-amp has a white noise of roughly 30 nV/√Hz and a corner frequency of 300 Hz whereas the low-noise op-amp has a white noise of roughly 6 nV/√Hz and a corner frequency of 100 Hz.

Both 1/f noise and white noise appear at the inputs of an op-amp and are defined as equivalent input noise voltage. The equivalent input noise is amplified by a gain and appears at the output. In particular, care is required as to low-frequency noise because its voltage is dependent on frequency.



Comparison of general-purpose and low-noise op-amps

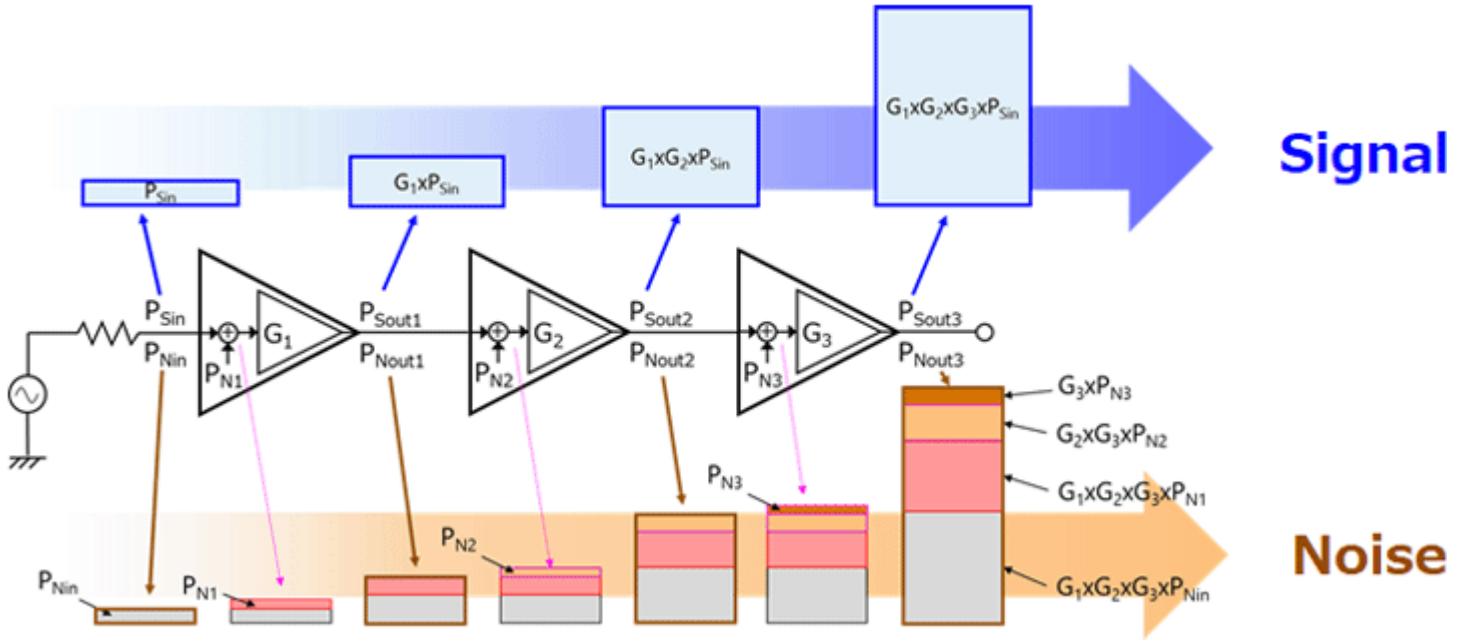


Noise frequency characteristics of an op-amp

3. Internal noise of an op-amp

To amplify a tiny signal, multiple amplifiers are sometimes connected in a cascade in order to prevent abnormal oscillation.
Let's consider how each amplifier stage affects the noise that appears at the output of the cascade amplifier.
Figure shows a three-stage cascade amplifier.
As shown in Figure, the output signal power (P_{Sout3}) and the output noise power (P_{Nout3}) can be calculated as follows.
As you see, the input noise (P_{Nin}) and the equivalent input noise (P_{N1}) of the first-stage amplifier have the greatest impact on the output noise.
The output signal power (P_{Sout3}) and the output noise power (P_{Nout3}) are expressed by the following equations:

$$P_{Sout3} = G_1 \times G_2 \times G_3 \times P_{Sin}$$
$$P_{Nout3} = G_1 \times G_2 \times G_3 \times (P_{Nin}+P_{N1}) + G_2 \times G_3 \times P_{N2} + G_3 \times P_{N3}$$



3. Internal noise of an op-amp

Therefore, the noise factor (F), a measure of noise, is calculated as follows:

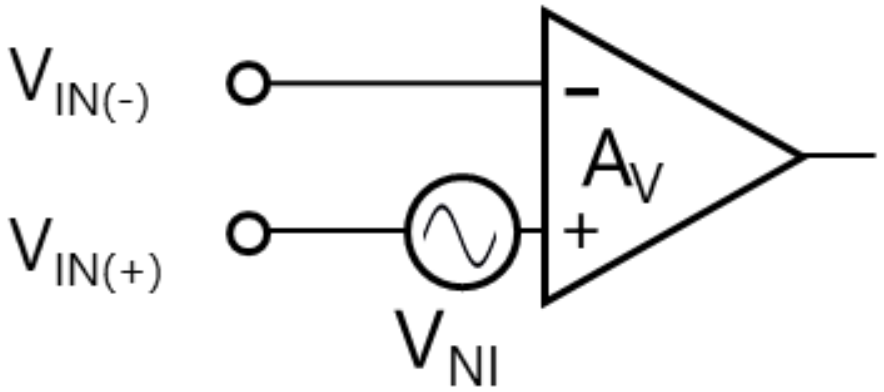
$$F = \frac{P_{Sin}}{P_{Nin}} \Bigg/ \frac{G_1 \times G_2 \times G_3 \times P_{Sin}}{G_1 \times G_2 \times G_3 \times \left(P_{Nin} + P_{N1}\right) + G_2 \times G_3 \times P_{N2} + G_3 \times P_{N3}}$$

$$= 1 + \frac{P_{N1}}{P_{Nin}} + \frac{P_{N2}}{G_1 \times P_{Nin}} + \frac{P_{N3}}{G_1 \times G_2 \times P_{Nin}}$$

The equivalent input noise of the second-stage amplifier (P_{N2}) is divided by the first-stage gain (G_1) whereas the equivalent input noise of the third-stage amplifier (P_{N3}) is divided by the first-stage and second-stage gains (G_1 and G_2). Therefore, the input noise of the successive stages of amplifiers has progressively less impact on the output P_{Nout3}.
As indicated by this example, a low-noise amplifier should be used at the first stage to reduce the effect of its noise.

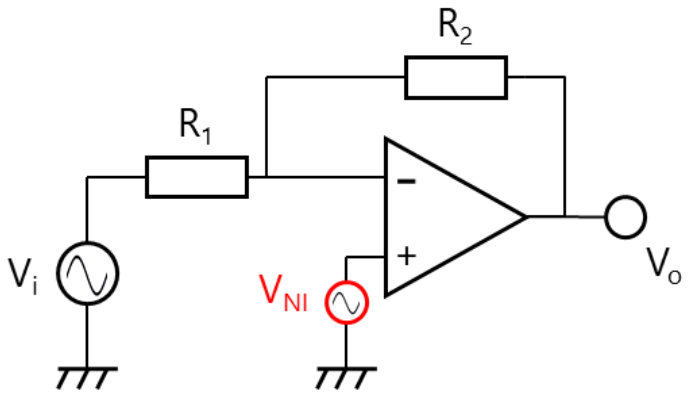
4. Noise gain and signal gain

The previous section described different types of noise generated by the op-amp. As discussed, the internal noise of an op-amp is defined as equivalent input noise voltage. Figure shows a simplified equivalent circuit. The op-amp represented by the triangle is the ideal one. Since Figure expresses the equivalent input noise voltage (V_{NI}) as a difference in voltage between $V_{IN(+)}$ and $V_{IN(-)}$, it is not significant whether V_{NI} is inserted in series with $V_{IN(+)}$ or $V_{IN(-)}$.



4. Noise gain and signal gain

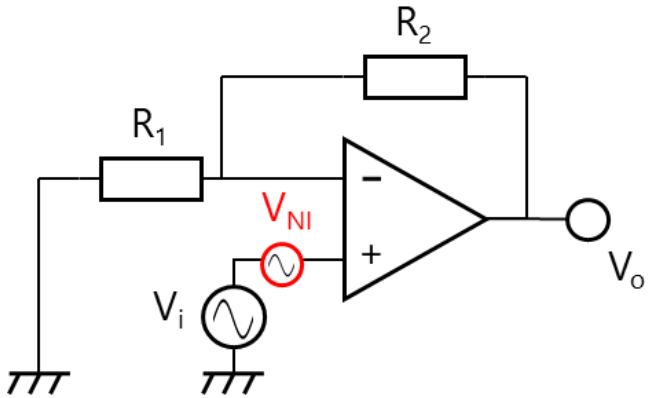
Next, let's consider noninverting and inverting amplifiers using this model.
Left Figure shows an inverting amplifier, and right Figure shows a noninverting amplifier. Both the inverting and noninverting amplifiers have an equivalent input noise source (V_{NI}) inserted in series with the $V_{in(-)}$ input of the ideal op-amp. These amplifiers have a signal gain of A_V as discussed in chapter 2.



$$A_V = -\frac{R_2}{R_1} \qquad A_n = \frac{R_1 + R_2}{R_1}$$

Signal gain Noise gain

Inverting amplifier



$$A_V = \frac{R_1 + R_2}{R_1} \qquad A_n = \frac{R_1 + R_2}{R_1}$$

Signal gain Noise gain

Noninverting amplifier

4. Noise gain and signal gain

Using the principle of superposition, signal and noise sources can be considered separately. Let's calculate the gain for the noise source.

In the Figure, the gain of the noise source of the op-amp is obtained in the same way as the non-inverting amplifier circuit. The noise voltage V_{NO} of V_O is as follows:

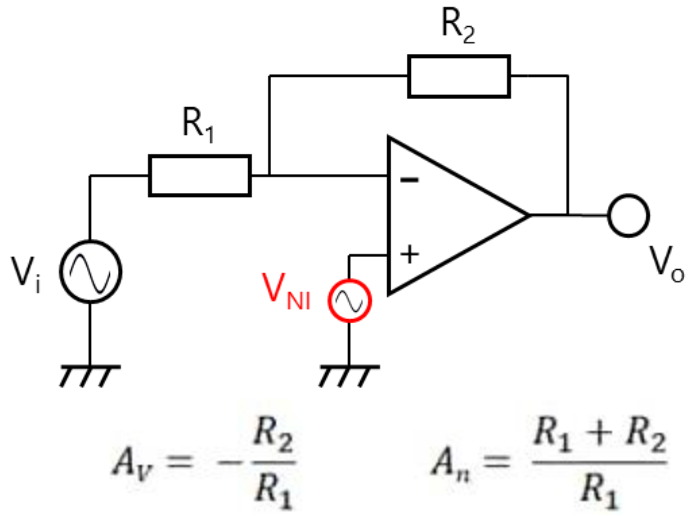
$$V_{NO} = V_{NI} \times (1 + R_2 / R_1)$$

Since the noise gain (A_N) is equal to V_{NO}/V_{NI},

$$A_N = 1 + R_2 / R_1$$

Here, the signal gain A_V of inverting amplifier circuit is as follows.

$$A_V = -R_2 / R_1$$



Inverting amplifier

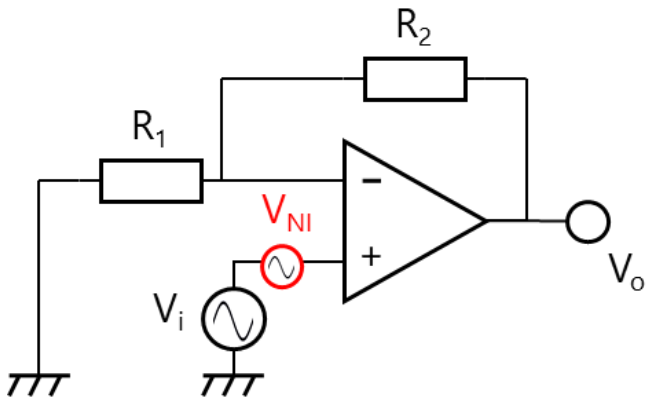
In this way, the gain of the noise generated in an op-amp might be different from that of the signal gain.
This gain is called a noise gain.

4. Noise gain and signal gain

This concept of noise gain can be used as follows:

- Converting the equivalent input noise into output noise
- Calculating the effect of the input offset voltage on the output
- Calculating the oscillation margin

As described above, the concept of noise gain is important for circuits using an op-amp.



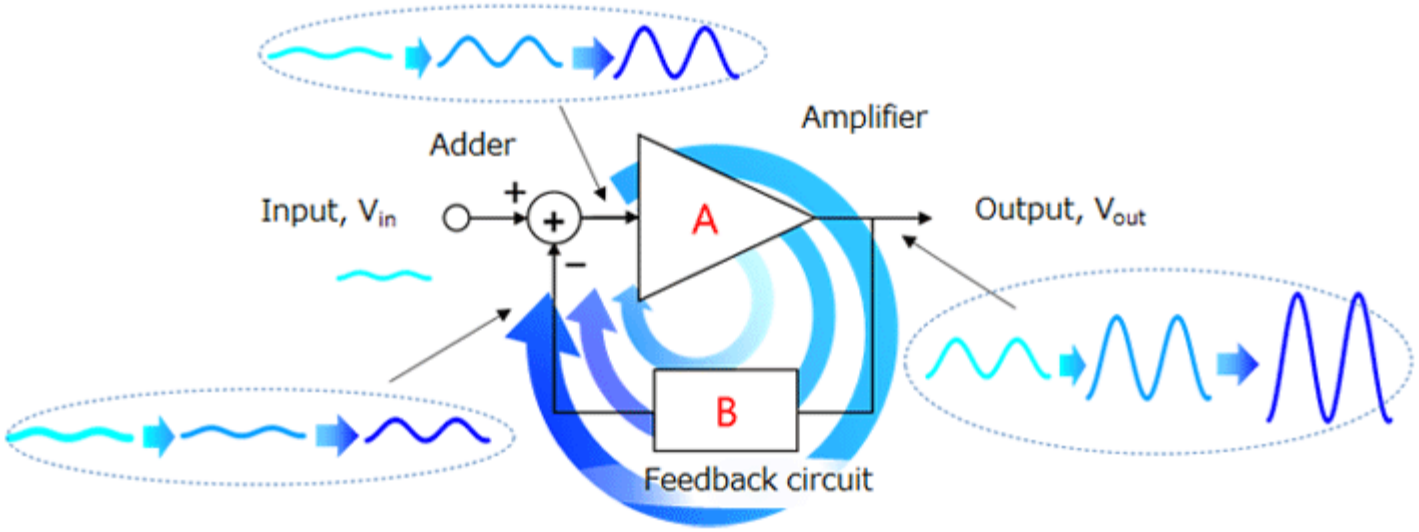
$$A_V = \frac{R_1 + R_2}{R_1}$$ Signal gain

$$A_n = \frac{R_1 + R_2}{R_1}$$ Noise gain

Noninverting amplifier

4. Noise gain and signal gain

Next, the following paragraphs briefly describe the oscillation margin.
Except for oscillators, oscillation means an unwanted fluctuation of a signal at an unintended frequency. A source of oscillation such as unwanted noise circulates through a feedback loop, developing into oscillation, as described in Chapter 2.



Growth of an unwanted signal through a feedback circuit

The source of oscillation is random noise. It is applied as a difference in voltage between the $V_{IN(+)}$ and $V_{IN(-)}$ inputs of an op-amp. In other words, it is the equivalent input noise voltage (V_{NI}) discussed above.
It is important to determine the oscillation immunity based on the noise gain. As described above, the noise gain of typical inverting and noninverting amplifiers can be calculated using the signal gain equation for noninverting amplifiers.
The concept of the noise gain can be used to provide a margin for oscillation (i.e., increase the noise gain).

4. Noise gain and signal gain

Figure shows an example of increasing the oscillation margin without changing the signal gain with an inverting amplifier.
Let's consider V_i and V_{NI} separately using the principle of superposition.
(V_{NI} is regarded as being short-circuited when considering V_i whereas V_i is regarded as being short-circuited when considering V_{NI}.)

From the concept of a virtual short, both the $V_{IN(-)}$ and $V_{IN(+)}$ inputs are regarded as being grounded.
Therefore, since the voltage across R_3 is equal to the GND potential at a signal gain of A_V (= V_o/V_i), no current flows through R_3. Hence, $A_V = -R_2/R_1$, which is identical to the equation for a basic inverting amplifier.
Since V_i is short-circuited at a noise gain of A_N (= V_o/V_{NI}), $V_i = R_1 // R_3$. Hence, $A_N = 1 + R_2 / (R_1 // R_3)$, which is higher than the noise gain for basic inverting amplifiers, $A_N = 1 + R_2 / R_1$. This means that this circuit provides a larger oscillation margin than a basic inverting amplifier.
However, since the concept of the noise gain is exactly the same as that of the input offset voltage, the oscillation margin increases at the expense of an increase in input offset voltage.