TOSHIBA

e-Learning

Usage Considerations of CMOS Logic ICs

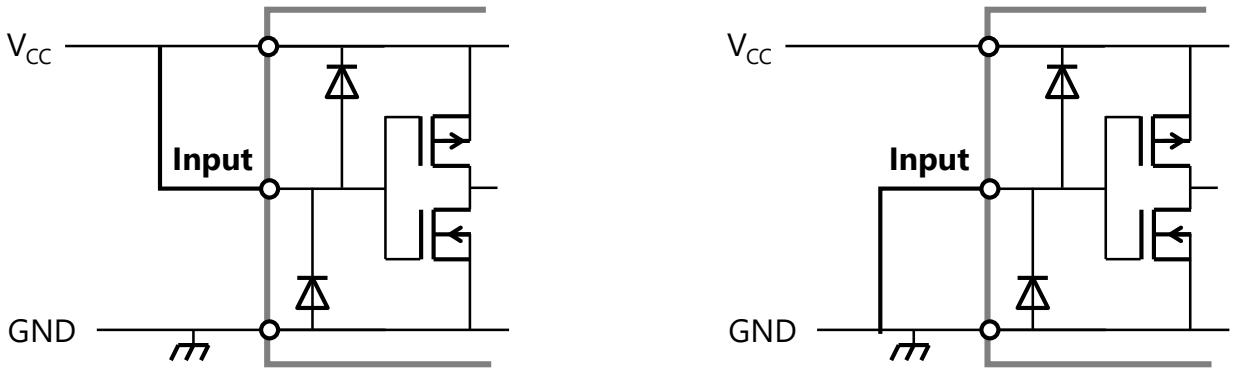
Toshiba Electronic Devices & Storage Corporation

Contents

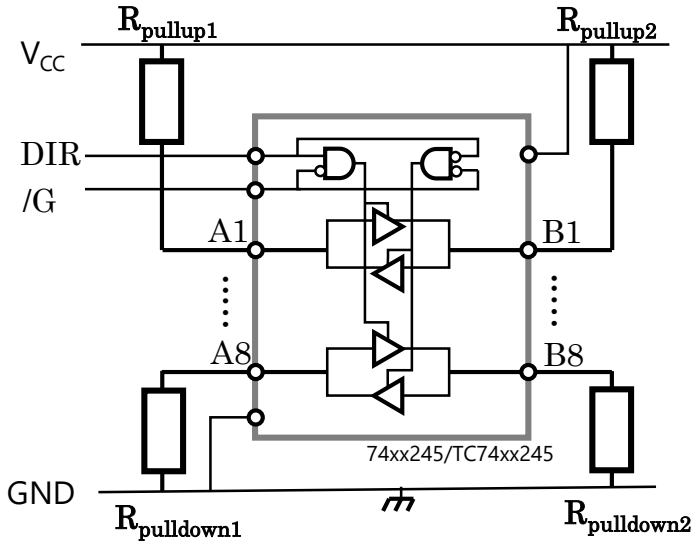
1. Handling of unused input pins

Generally, all unused inputs should be tied to either V_{CC} or GND.
However, any pins of bidirectional bus buffers (e.g., Function 245) that can be configured as an output (e.g., bus pins) should be tied to V_{CC} via a pull-up resistor or to GND via a pull-down resistor. It is recommended that both ends of the buffer be pulled up or down to the same potential to avoid unnecessary current flow. However, leave the input pins with bushold, such as those of the ICs of the TC74VCXHxxx Series, open. Large inrush current due to parasitic capacitance (in the order of a few milliamperes) can be a problem even with typical CMOS logic ICs when their power supply is on. In order to improve system reliability against device destruction and other failures, their inputs can be tied to V_{CC} via a pull-up resistor or to GND via a pull-down resistor.

Because CMOS logic has a very high input impedance, any open input might result in a false output value due to the influence of a surrounding electric field. In addition, shoot-through current might flow at the midpoint of V_{CC} and GND, causing an increase in supply current and leading to device destruction in the worst-case scenario.
Be sure to apply these considerations to all inputs without a bushold capability unless otherwise instructed in the datasheet.



Unused inputs of CMOS logic ICs tied to V_{CC} or GND



Unused bidirectional pins of a bidirectional bus buffer pulled up to V_{CC} or down to GND

2. Input rise and fall time specifications

In the datasheet, the input rise and fall times of general-purpose CMOS logic ICs are specified in the operating ranges in which their functional operation is guaranteed.
Use CMOS logic ICs within the operating ranges to prevent a malfunction due to output oscillation etc.
If a slowly rising or falling signal (a low slew rate signal) is applied to an input, a current spike occurs during switching, causing V_{CC} and GND bounce, which might result in output oscillation or a malfunction.

Use ICs with a Schmitt-trigger input for slowly changing inputs. However, in the case of excessively slowly changing inputs, even ICs with a Schmitt-trigger input might not be able to suppress noise on power supply or signal lines, resulting in output oscillation or instability.

The following table shows the rise and fall times of a typical IC[*1] in each series.

2. Input rise and fall time specifications

By family input rise and fall times in each series

Type	Series Name	Series No.	One-Gate Logic (L-MOS) Equivalents	Operating Voltage Range (V)	Propagation Delay Times*1, t_{pLH} and t_{pHL} (ns)	Output Current*2, I_{OUT} (mA)	Rise and Fall Times at 3.3 V	Rise and Fall Times at 5 V
For 5-V Systems	Standard	TC40xxB TC45xxB	TC4S TC4W	3 to 18	200 (at 5.0 V)	±0.51 (at 5.0 V)	0 to 10000 ns*6	0 to 5000 ns*6
	High Speed	TC74HC	TC7S TC7W	2 to 6	23 (at 4.5 V)	±4.0 or 6.0 (at 4.5 V) (±2.0 in the case of TC7S)	0 to 1000 ns at 2 V	0 to 500 ns at 4.5 V
		TC74HCT	TC7WT	4.5 to 5.5	28 (at 4.5 V)			0 to 500 ns
	Advanced	TC74AC		2 to 5.5	8.5 (at 4.5 V)	±24 (at 4.5 V)	0 to 100 ns/V	0 to 20 ns/V
		TC74ACT		4.5 to 5.5	9.0 (at 5.0 V)			0 to 10 ns/V
	Very High Speed	TC74VHC 74VHC	TC7SH TC7WH	2 to 5.5	8.5 (at 5.0 V)	±8.0 (at 4.5 V)	0 to 100 ns/V	0 to 20 ns/V
		TC74VHC9 74VHC9			10 (at 5.0 V)		– *5	– *5
		TC74VHCT 74VHCT	TC7SET	4.5 to 5.5	9.5 (at 5.0 V)			0 to 20 ns/V
		TC74VHCV 74VHCV		1.8 to 5.5	8.5 (at 5.0 V)	± 16 (at 4.5 V)	0 to 20 ms/V	0 to 1 ms/V
For low-voltage systems	Medium Speed	TC74LCX 74LCX	TC7SZ TC7PZ TC7WZ	1.65 to 3.6 (1.65 to 5.5 in the case of TC7SZ/PZ/WZ)	6.5 (at 5.0 V)	± 24 (at 3.0 V)	0 to 10 ns/V	
	High Speed	TC74VCX	7UL	1.2 to 3.6 (0.9 to 3.6 in the case of 7UL)	4.2 (at 2.3 V)	± 24 (at 3.0 V) (±8.0 in the case of 7UL)	0 to 10 ns/V	

*1: Maximum propagation delay time of typical ICs (TC4001, TC74HC244, TC74AC244, TC74VHC244, TC74LCX244, and TC74VCX244) at 85°C, except for the TC4001 for which the maximum propagation delay time at 25°C is shown

*2: Output current values are specified in the DC Characteristics table shown in the datasheet. Absolute maximum rated output current is specified separately.

*3: The TC7SET series does not have an output power-down protection function.

*4: The ICs of the TC7SZ series in the fSV package do not have an output power-down protection function except those with an open-drain output.

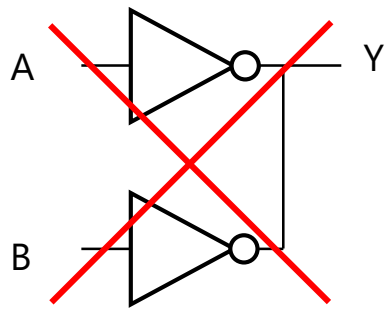
*5: Rise and fall times are not specified because the TC74VHC9 and 74VHC9 series provide Schmitt-trigger inputs.

*6: Rise and fall times are not specified in the datasheet. The values shown above should be considered only as a guide for creating a design.

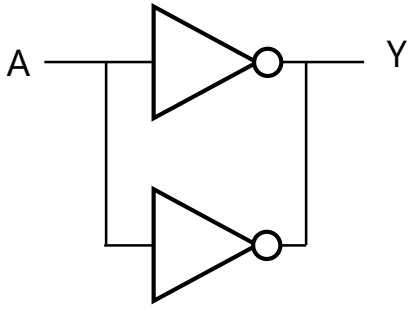
3. Multiple outputs from a general-purpose CMOS logic IC come into conflict (Short-circuiting)

Unlike diodes, the outputs of typical CMOS logic ICs cannot be wired-ORed together, except those with three-state outputs. Even in the case of CMOS logic ICs with three-state outputs, unintended current might flow, causing IC degradation, if they are enabled simultaneously. When creating a circuit design, ensure that multiple outputs will not be enabled at any given time. Also, the outputs of CMOS logic ICs without bushold become unstable if all of them are disabled (i.e., assume the High-Z state) without being pulled up to V_{CC} or down to GND. For a description of logic transitions of three-state bus buffers, see the FAQ entry "Do bidirectional bus buffers have any constraints on the timing of the direction (DIR) and other input signals?" For a description of bushold, see the FAQ entry "What is bushold?"

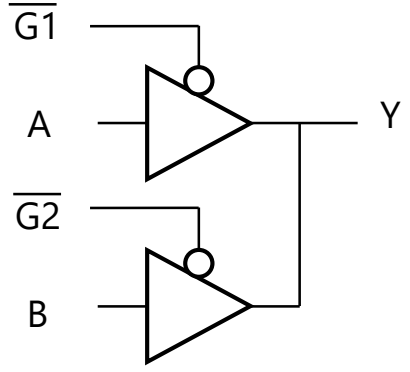
Only the gates in the same package may be wired-ANDed to increase the drive capability (i.e., output current). However, it is recommended to use high-drive ICs (with an I_O of ±24 mA) instead. For a description of high-drive CMOS logic ICs, see the DC Characteristics table shown in the FAQ entry "How many amperes of current can an output pin drive?"

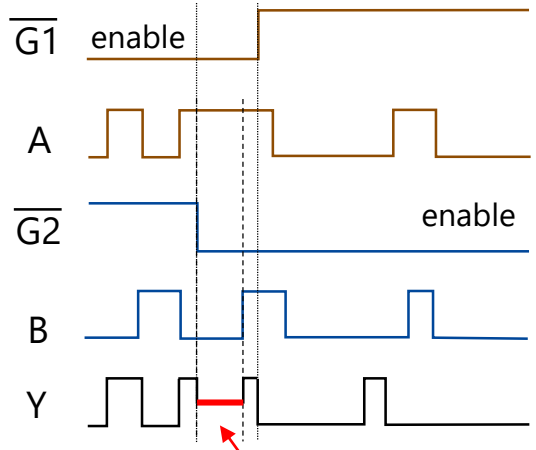


Do not use multiple wired-OR gates.



Example of a parallel connection to increase drive capability
(Only gates in the same package may be paralleled.)





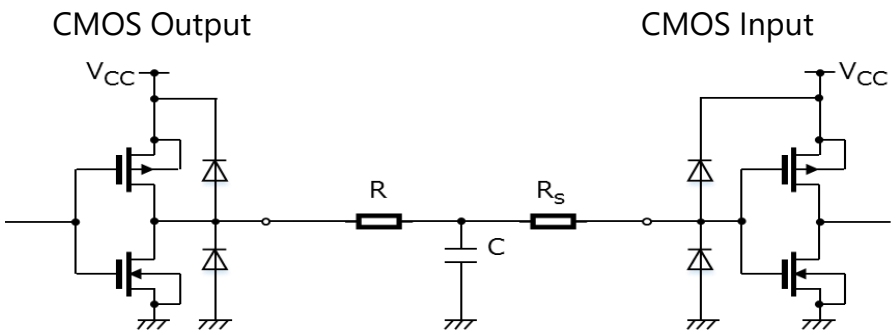
Conflict of three-state outputs

When both /G1 and /G2 are Low, the A input is High, and the B input is Low (or the A input is Low and the B input is High), connecting the outputs together results in a short-circuit and therefore excessive current.

4. Connecting a load capacitance to a CMOS output pin

When an output pin of a CMOS IC is connected directly to a large load capacitance, its propagation delay increases. In addition, the increased charge/discharge current into or out of the capacitor might cause noise or a bonding wire burnout. Since current flows to the output parasitic diode at power-down, a CMOS IC should not be connected directly to a large load capacitance.
If it is necessary to connect a capacitor directly to the output of a CMOS IC in order to increase its delay time or filter out noise, its capacitance should be 500 pF or less. When a larger capacitor is required, a current-limiting resistor (R) should be connected between the IC output and a capacitor as shown below. CMOS ICs with an output-tolerant function do not need a current-limiting resistor (R) for power-down. However, a current-limiting resistor (R) might be necessary to limit the charge current into the capacitor.

When a capacitor is discharged as a result of power-down, current flows to an internal protection diode returned to V_{CC} via the input pin.
In the case of an input pin, current flows to an internal protection diode returned to V_{CC} when a capacitor is discharged as a result of power-down.
Therefore, a large load capacitance should not also be connected directly to an input pin. A capacitor of up to 500 pF may be connected directly to the input of a CMOS IC, but when a larger capacitor is required, a current-limiting resistor (R_s) should be connected between the IC input and a capacitor as shown below.



Connecting a large load capacitance

5. Calculating the operating supply current and power dissipation

Calculating the power dissipation of a CMOS logic IC

https://toshiba.semicon-storage.com/ap-en/semiconductor/knowledge/faq/logic_common/logic_common_17.html

Power dissipation should be calculated from both of the following:

- Static supply current
- Dynamic supply current

Power can be obtained by multiplying current by the voltage applied to an IC.

Static power dissipation: P_S

While CMOS logic is in a static state (i.e., while its input voltage remains almost unchanged), little current flows in it except tiny leakage current that flows across the internal reverse-biased pn junction (known as static supply current, I_{CC}). Static power dissipation is I_{CC} multiplied by the supply voltage.

$P_S = V_{CC} \times I_{CC}$

V_{CC}: Voltage applied to a logic IC

I_{CC}: Static supply current shown in the datasheet

Dynamic power dissipation: P_L+P_{PD}

Dynamic supply current is the current that flows in CMOS logic ICs while its input transitions between High and Low. This current flows during the charging and discharging of capacitance. It is necessary to consider both parasitic capacitance (internal equivalent capacitance) and load capacitance.

Dynamic power dissipation is dynamic supply current multiplied by the voltage applied to the p-channel or n-channel MOSFET.

For the sake of simplicity, the following calculation assumes that this voltage is equal to V_{CC} at which dynamic supply current becomes the maximum.

5. Calculating the operating supply current and power dissipation

Dynamic power dissipation due to load capacitance (C_L): P_L

P_L means power dissipation when an external load is charged and discharged as shown by the right-hand figure.

The amount of charge (Q_L) stored on the load capacitance is calculated as follows:

$Q_L = C_L * V_{CC}$

C_L: Load capacitance

Let the output signal frequency be f_{OUT} (= $1/T_{OUT}$). Then, the average current (I_L) is expressed as follows:

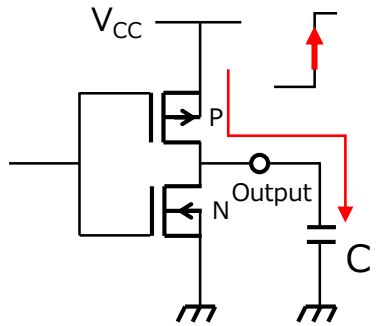
$I_L = Q_L / T = C_L * V_{CC} * f_{OUT}$

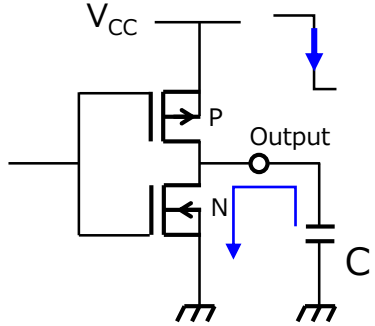
Hence, dynamic power dissipation (P_L) is:

$P_L = V_{CC} * I_L = C_L * V_{CC}\text{^}2 * f_{OUT}$

If an IC has multiple outputs, its dynamic power dissipation can be calculated as follows:

$P_L = V_{CC}\text{^}2 * \Sigma\ (C_{Ln} * f_{OUTn})$





Dynamic power dissipation due to C_L

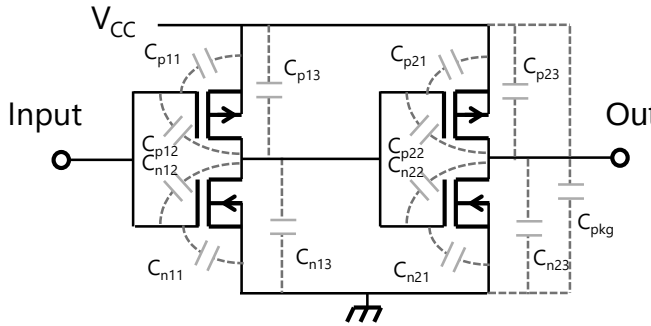
Dynamic power dissipation due to internal equivalent capacitance (C_{PD}): P_{PD}

CMOS logic ICs have various parasitic capacitances as shown by the right-hand figure. These capacitances are equivalently expressed as C_{PD}. (Actually, C_{PD} is calculated from power dissipation at relatively high frequency (1 MHz) under a zero-load condition.)

P_{PD} is the power dissipated by the equivalent capacitance of an IC and can be considered in the same manner as P_L.

Note, however, that P_{PD} is calculated at input frequency (f_{IN}):

$P_{PD} = V_{CC} * I_L = C_{PD} * V_{CC}\text{^}2 * f_{IN}$



Dynamic power dissipation due to C_{PD}

Total power dissipation (P_{TTL}) can be obtained as the sum of static power dissipation (P_S) and dynamic power dissipation ($P_L + P_{PD}$):

$P_{TTL} = P_S + P_L + P_{PD}$

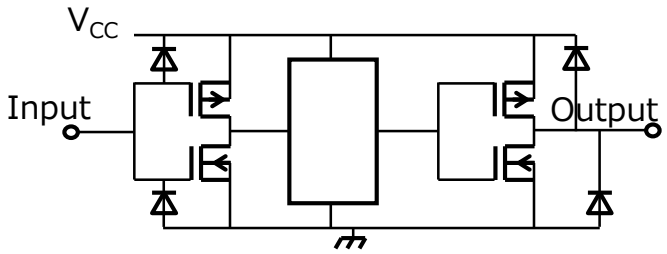
6. Level shifting using an input-tolerant function

An input-tolerant function can be used for level shifting.

The input-tolerant function allows a voltage of up to the maximum operating voltage to be applied to an input while the power supply is active or at 0 V. The input-tolerant function allows level shifting from a higher voltage to a lower voltage.

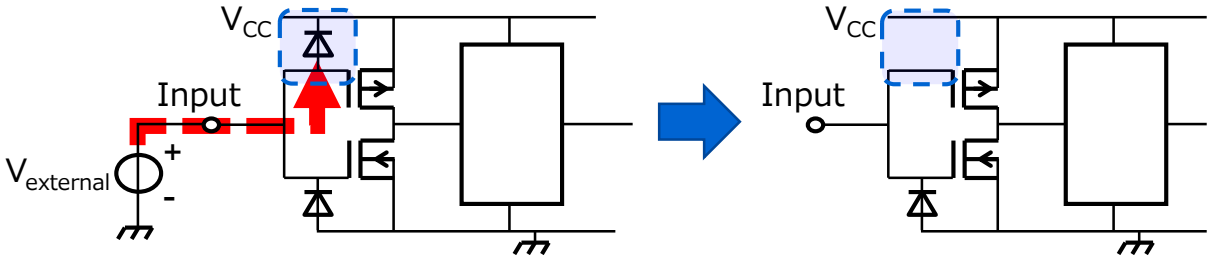
Product selection options:
The 74VHC and 74LCX series can be used for conversion from 5 V to 3 V.
The 74VCX series can be used for conversion from 3 V to 1.2 V.

The following shows an equivalent circuit for a typical CMOS logic IC.



Equivalent input/output circuit for a CMOS logic IC without input-tolerant and power-down protection functions

The diodes on the input side are inserted for the purpose of ESD protection.
The diode between the input and the power supply might turn on if a voltage higher than V_{CC} is applied or voltage is applied when the IC is off. In this case, the IC might be destroyed by the resulting large current. Device destruction can be prevented by using an IC with an input-tolerant function, i.e., an IC without a diode between the input and power supply.



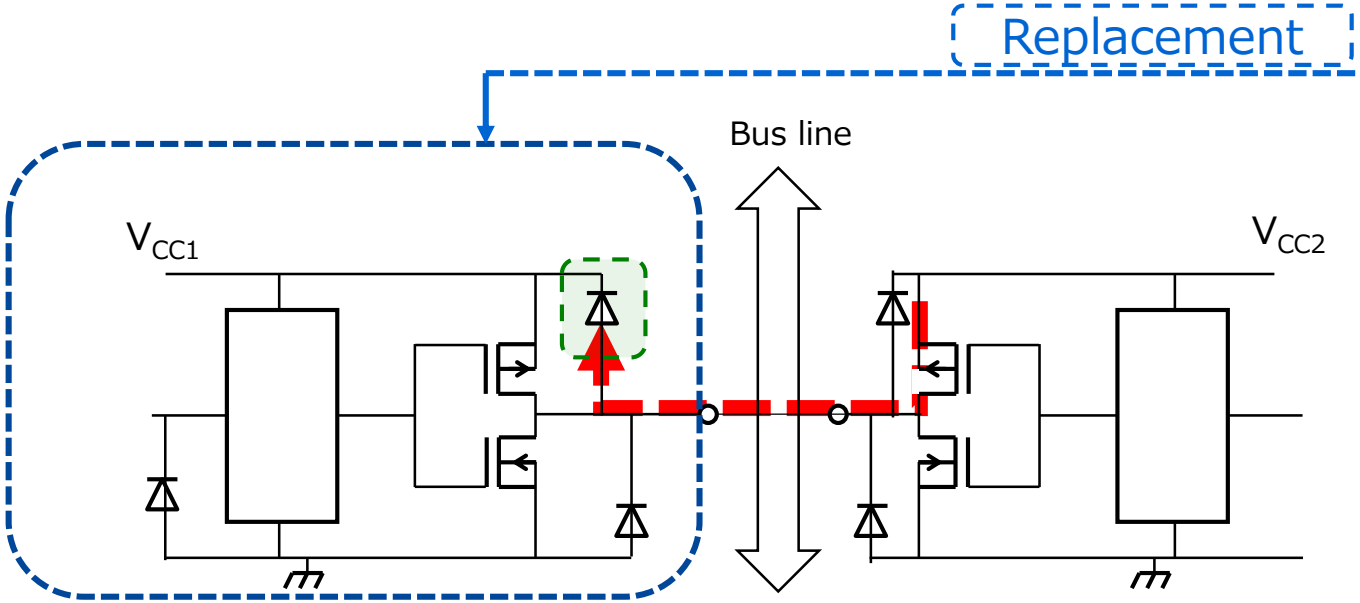
Without an input-tolerance function:
$V_{external} > V_{CC}$

Equivalent input circuit for a CMOS logic IC with an input-tolerant function

7. Example of application of the power-down protection function (partial power-down)

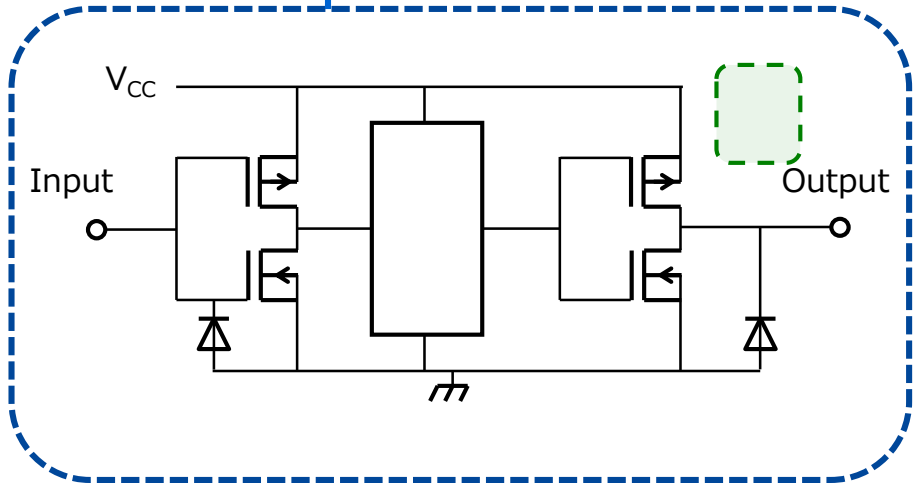
Partial power-down is possible if an IC with a power-down protection function is used.

To reduce power consumption, a system with two voltage domains (V_{CC1} and V_{CC2}) might provide **partial power-down mode** in which the subsystem operating from V_{CC1} is shut down. Suppose, for example, that the 74VHC Series is used in the V_{CC1} domain. The 74VHC Series has an unintended parasitic diode between the output and power supply. Therefore, when $V_{CC2} > V_{CC1}$, this parasitic diode turns on. In this case, the IC might be destroyed by the resulting large current. Device destruction can be prevented by using **an IC with neither an input nor output parasitic diode** (e.g., 74VHCT, 74LCX, and 74VCX Series). **These series provide power-down protection.**



Without an output power-down protection function, current flows into the IC from another IC.
$V_{CC2} > V_{CC1}$

Replacement



Equivalent input/output circuit for a CMOS logic IC with input-tolerant and output power-down protection functions

8. Input-tolerant and output power-down protection functions available with each series

The following table shows whether each CMOS logic IC series provides the input-tolerant and output power-down protection functions.

Series	Part Number	Operating voltage range (V)	Input-tolerant function	Output power-down protection
Standard CMOS	TC4000B TC4500B	3 to 18	- *1	-
High-Speed	TC74HC	2 to 6	- *1	-
	TC74HCT	4.5 to 5.5		
Advanced	TC74AC	2 to 5.5	-	-
	TC74ACT	4.5 to 5.5		
Very-High-Speed	74VHC 74VHC9	2 to 5.5	✓	-
	74VHCT	4.5 to 5.5	✓	✓
	74VHCV	1.8 to 5.5	✓	✓
Low-Voltage	74LCX	1.65 to 3.6	✓	✓
Very-Low-Voltage	TC74VCX	1.2 to 3.6	✓	✓

*1 : TC4049BF/BP, TC4050BF/BP, TC74HC4049BP/BF/BFT, 74HC4049D, TC74HC4050BP/BF/BFT and 74HC4050D have the input-tolerant function that allows level shifting from a higher voltage to a lower voltage.

9. Types of noise to be noted

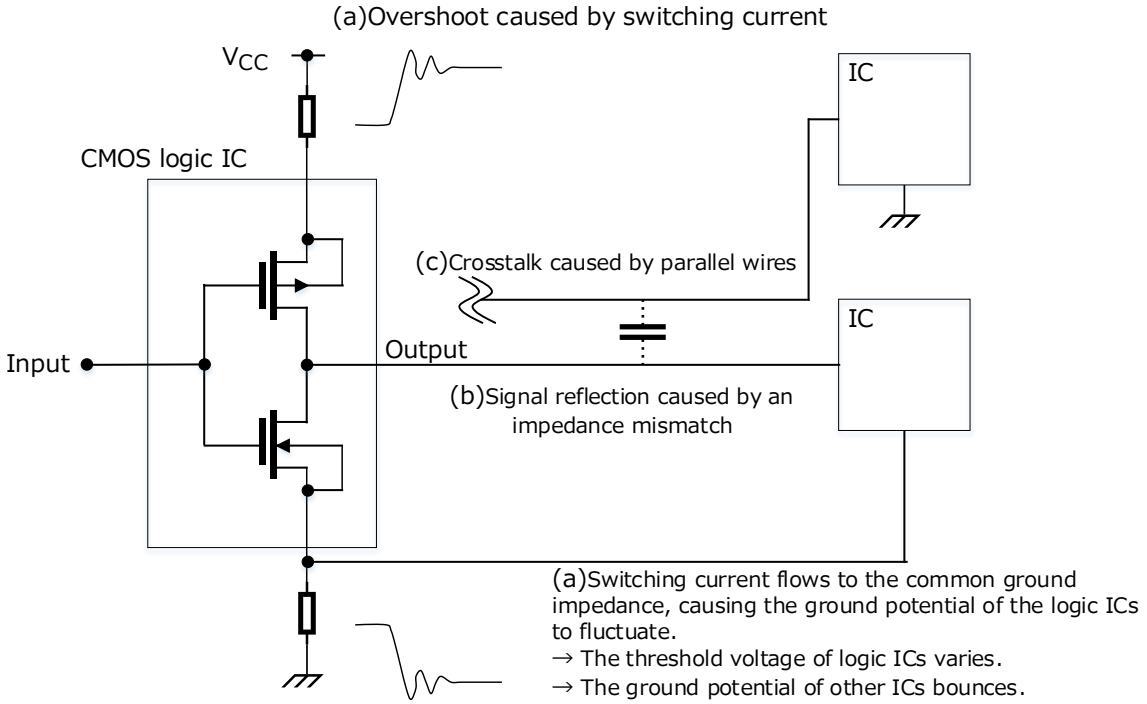
Care should be exercised as to switching noise when using CMOS logic ICs. Major types of noise include:

(a) Switching noise (overshoot, undershoot, ground bounces)

(b) Signal reflection

(c) Crosstalk noise

See the figure below. Each type of noise is detailed in the following subsections. These types of noise are caused by the output slew rate (di/dt or dv/dt) and the output trace. Care should also be taken as to electromagnetic interference (EMI) noise generated under multiple combined conditions and electromagnetic susceptibility (EMS) noise emitted by nearby electronic devices.

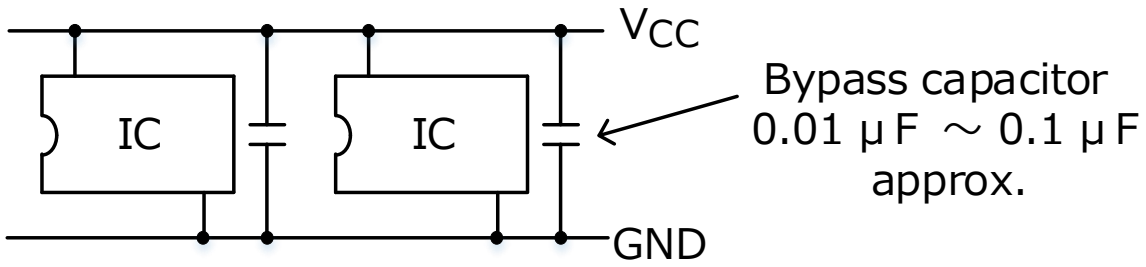


9-1. Countermeasures #1 for reducing switching noise

The MOSFETs in a CMOS logic IC make switching transitions while charging and discharging internal and external load capacitances. The trace impedance during switching can be regarded as an LCR circuit. Since the switching current (i) flows through inductance (L), a spike voltage (=L(di/dt)) appears on the V_{CC} and GND lines of the CMOS logic IC. This noise is called switching noise.
Multiple simultaneously switching outputs draw a large charge/discharge current and therefore cause a large switching noise (called simultaneous switching noise). The following lists the measures for the reduction of switching noise.

Countermeasures to reduce switching noise:

(1) Increase the width and reduce the length of V_{CC} and GND lines to reduce their inductance.
(2) Place a bypass capacitor between and as close as possible to the V_{CC} and GND pins of the CMOS logic IC (See below figure).



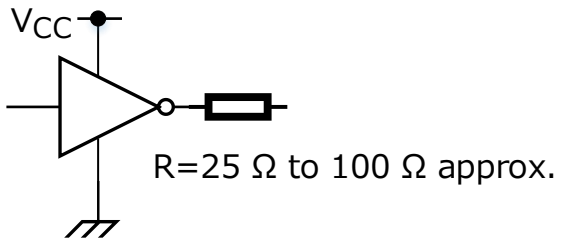
9-1. Countermeasure #2 for reducing switching noise

Countermeasures to reduce switching noise:

(3) Exercise care as to clock and reset signals. Unused inputs of gates such as drivers should be connected to either V_{CC} or GND. Connect a low-pass filter to the output of used gates to remove noise.

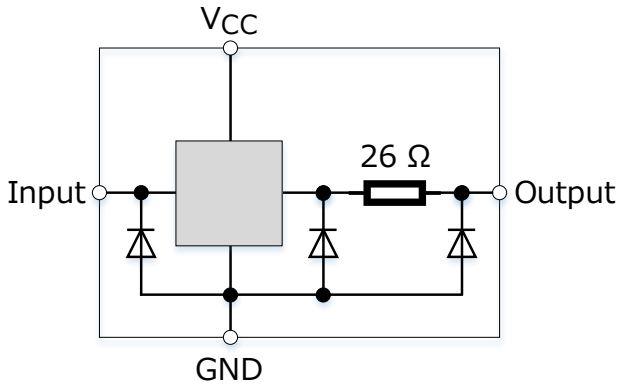
(4) Select low-noise ICs.

(5) Add a damping resistor to the output of used gates (See below figure). It is necessary to adjust the value of the damping resistor by checking the output waveform.



* Toshiba provides CMOS ICs with an internal damping resistor (See below figure), which help reduce not only switching noise but also parts count.)

I/O equivalent circuit



Product lineup

The TC74VVCX series contains 8-bit and 16-bit bus buffers with a damping resistor.

Example: TC74VCX2244FT

↳ The "2" in this digit represents an internal damping resistor.

9-2. Countermeasures for signal reflection

In the case of high-speed CMOS logic ICs, reflections cause an increase in the signal delay, ringing, overshoot, and undershoot. Reflections in transmission lines:

Typical traces have a characteristic impedance(*1) of 50 to 150 Ω. However, the I/O impedance of high-speed CMOS logic ICs differs from the typical characteristic impedance of traces. This impedance mismatch causes part of the transmitted signal to be reflected to both the transmitting and receiving ends of a transmission line.
Signal reflection does not affect a slowly rising output because its rise period overlaps that of the reflected signal. Signal reflection causes a problem when the reflected signal returns to the output after it rises, i.e., when the following equation is true:

$t_r < 2T$

t_r: Rise time of the output signal

T: Propagation delay time from the transmitting end to the receiving end of a transmission line

Suppose that the output rise time is 3 ns and that the propagation delay time along a transmission line is 5 ns/m. Then, signal reflection has a significant impact when the transmission line is 30 cm or longer.

*1 Characteristic impedance

The characteristic impedance is one of the characteristics of a transmission line (e.g., board trace, coaxial cable).

The general expression of the characteristic impedance of a transmission line is $Z_0 = \sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. The unit of characteristic impedance is ohm (Ω). When a termination resistor of 50 Ω is connected to the end of a transmission line with a characteristic impedance of 50 Ω, signal reflection does not occur at the connection point. However, if the characteristic impedance does not match the resistor value, signal reflection occurs at the connection point.

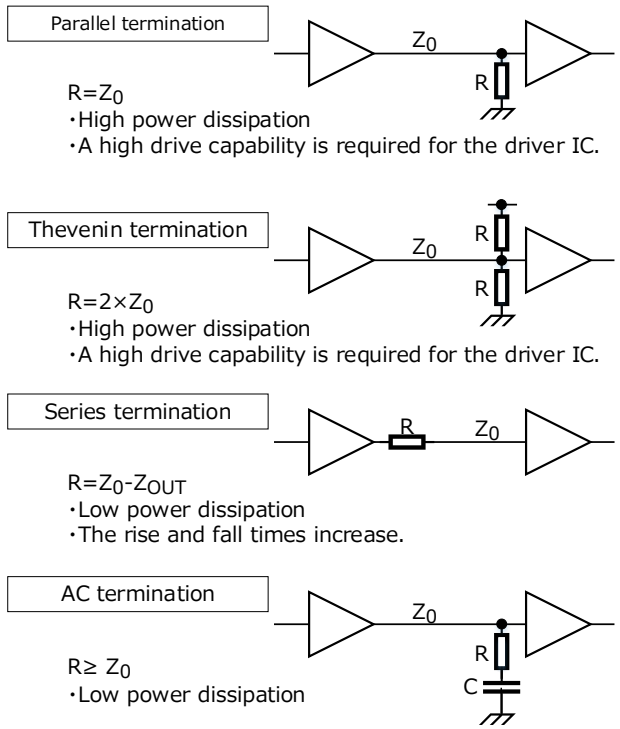
9-2. Countermeasures for signal reflection

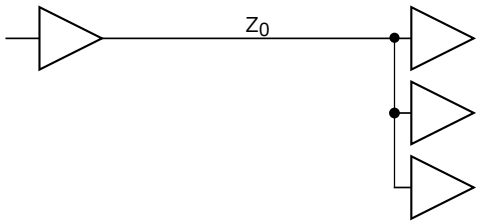
Countermeasures to reduce Signal Reflection

(1) Increase the board assembly density and reduce the length of board traces to reduce their inductance and capacitance. In this case, however, care is required as to crosstalk between adjacent traces. (See Section 9.3)

(2) Do not use ICs with an output current higher than necessary.

(3) Provide electrical termination so that the I/O impedance of a CMOS logic IC matches the characteristic impedance of the transmission line (See blow figure).





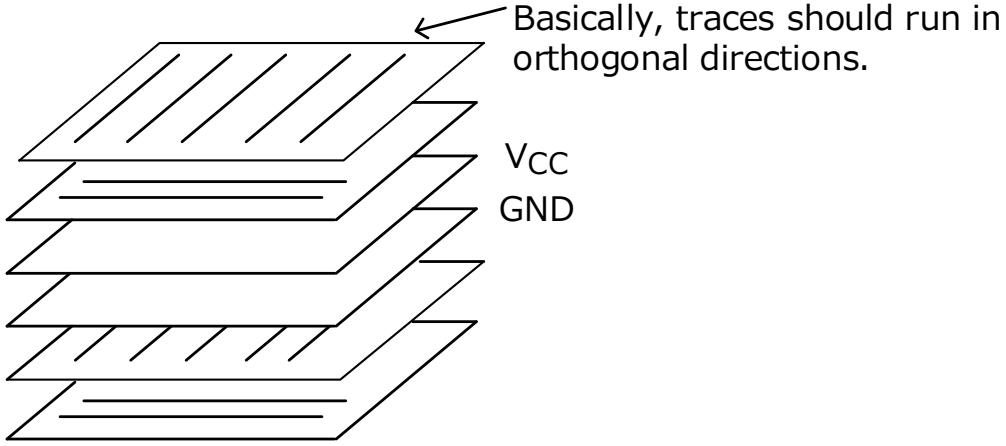
(4) When the output of a CMOS logic IC drives multiple CMOS logic ICs the output trace should be fanned out close to the driven ICs. (Right hand side figure).

9-3. Countermeasures for crosstalk

Crosstalk noise is induced by capacitive or inductive coupling between two adjacent transmission lines that run in parallel (called an aggressor and a victim). Regarding crosstalk, care should be exercised as to rapidly rising or falling signals. When such a signal travels through a transmission line, crosstalk noise is induced in an adjacent line (victim) and propagates in both directions: in the same direction as for the aggressor signal and in the direction opposite to it.
Since the speed of crosstalk propagation is equal to that of the aggressor signal, the crosstalk noise that travels in the same direction as the aggressor signal (called far-end crosstalk) appears as pulse-like noise.
On the other hand, the crosstalk noise that travels in the opposite direction (called near-end crosstalk) maintains a constant level while the aggressor signal propagates along the line.
Crosstalk noise also propagates along the aggressor line and then returns to the victim line.
Generally, you can prevent crosstalk as follows.

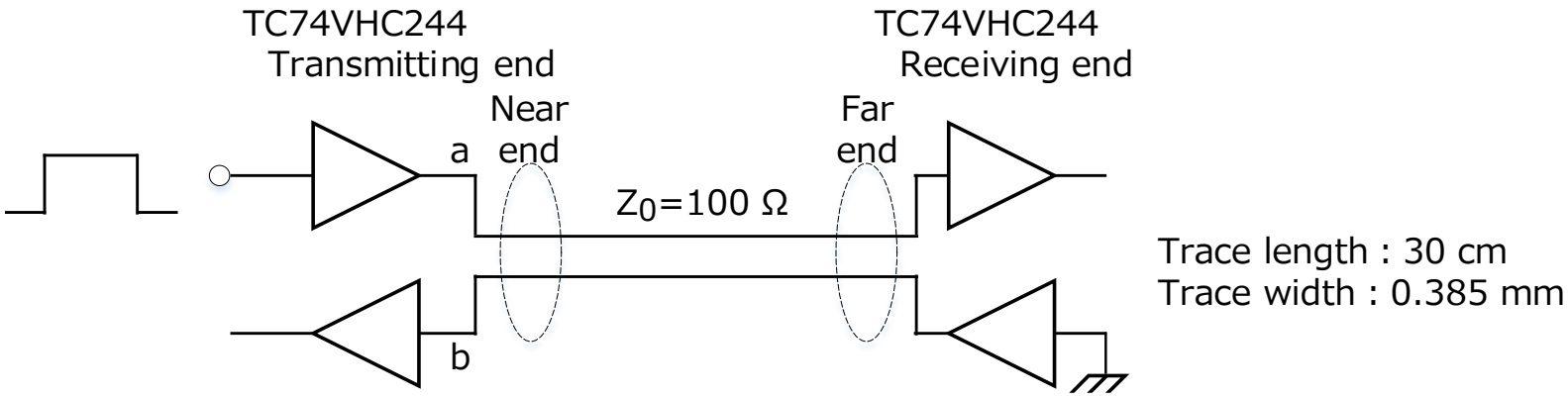
Measures for Crosstalk:

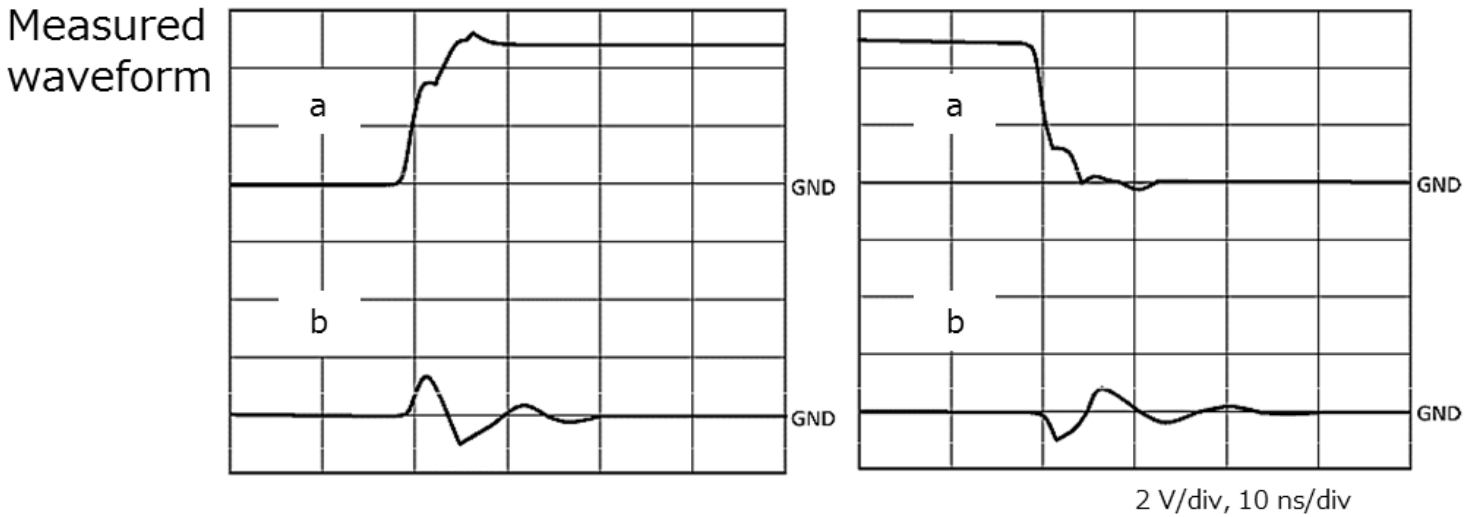
- Add earth traces between parallel traces.
  (Alternatively, use a multi-layer board in which a low-impedance layer (e.g., V_{CC} or GND layer) lies between signal layers.)
- Reduce the length of traces that run in parallel.
- In the case of a multi-layer board, run traces on alternate layers orthogonally to each other (See the right hand side figure).
- Increase the spacing between traces.



9-3. Countermeasures for crosstalk

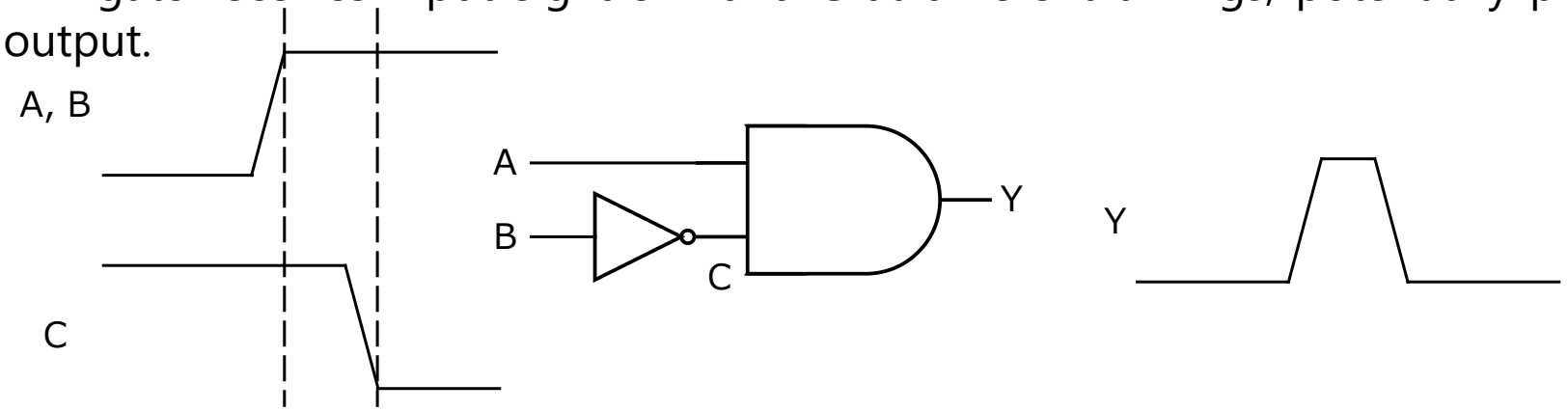
The below figure shows a typical level of crosstalk noise traveling along 30-cm traces. This example shows near-end crosstalk. When the near end of the victim trace is the receiving end, it is susceptible to the effect of crosstalk.





10. Countermeasures for hazards

In the case of multiple-input combinational logic consisting of OR, AND and other gates, a slight difference in the timing of input signal changes causes a brief whisker-like pulse called a hazard.
Using the circuit shown in below figure, let's see how a hazard occurs because of a difference in signal delays. Suppose that a rising signal transition occurs simultaneously at A and B. The signal applied to B reaches the AND gate via an inverter. Since the signal that enters the AND gate from B is delayed by an inverter, the AND gate receives input signals A and C at different timings, potentially producing a High pulse at the Y output.



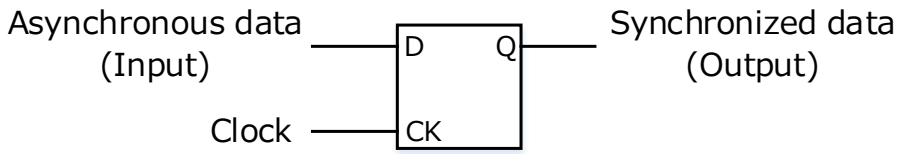
Countermeasures for hazards

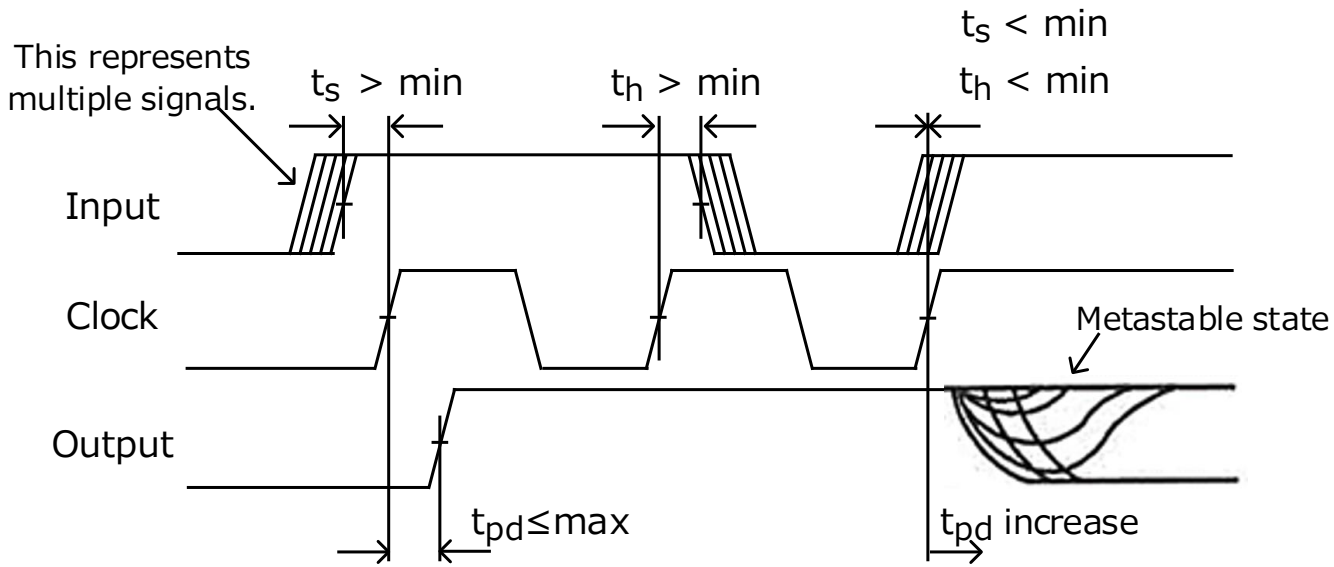
combinational logic should not be designed to produce a desired output value from simultaneous changes in its inputs. Using a flip-flop to adjust the output timing also helps eliminate a hazard.

In addition to a signal timing difference, a slowly changing input can be a cause of a hazard.
Hazards due to a slowly changing input can be prevented by using a logic gate with a Schmitt-trigger input.

11. Countermeasures for metastability

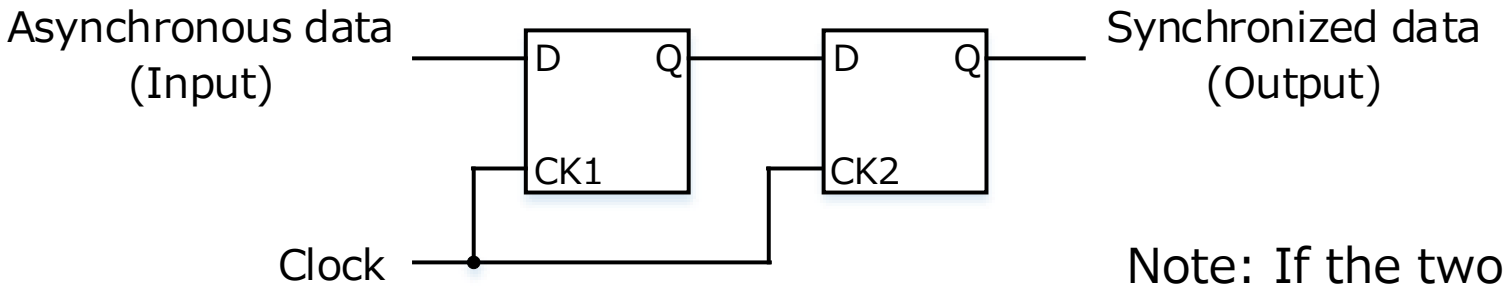
The output of a synchronous sequential circuit can potentially persist in an unstable equilibrium called a metastable state, depending on the timing of a data signal to be latched relative to the clock signal. A sequential circuit enters a metastable state when its input setup and hold time (t_s and t_h) requirements shown in the datasheet are not satisfied.





11. Countermeasures for metastability

Metastability potentially occurs when an active input (e.g., a clock signal) and a passive input (e.g., a data signal) are asynchronous to each other. To prevent sequential circuits from entering a metastable state, the recommended timing conditions shown in the datasheet must be satisfied.
For example, when the CK and D inputs are asynchronous, they can be synchronized as shown below.
In this case, however, care should be exercised as to the cycle period and propagation delay of CK.
If they are close, the data signal might not propagate to the second flip-flop.
The synchronizer shown in Figure 5.3 consists of two flip-flops. The first flip-flop prevents an increase in t_{pd} and a hazard from being transferred to the output of the second flip-flop.
Even in this case, care is needed when the phase difference between CK1 and CK2 is close to the CK-to-Q delay (t_{pd}) of the first flip-flop.



Note: If the two flip-flops cannot operate from the same clock, metastability is avoidable by creating an inverted clock synchronous to CK1 and using it as CK2 (e.g., CK2 = /CK1).

12. Countermeasures for latch-up

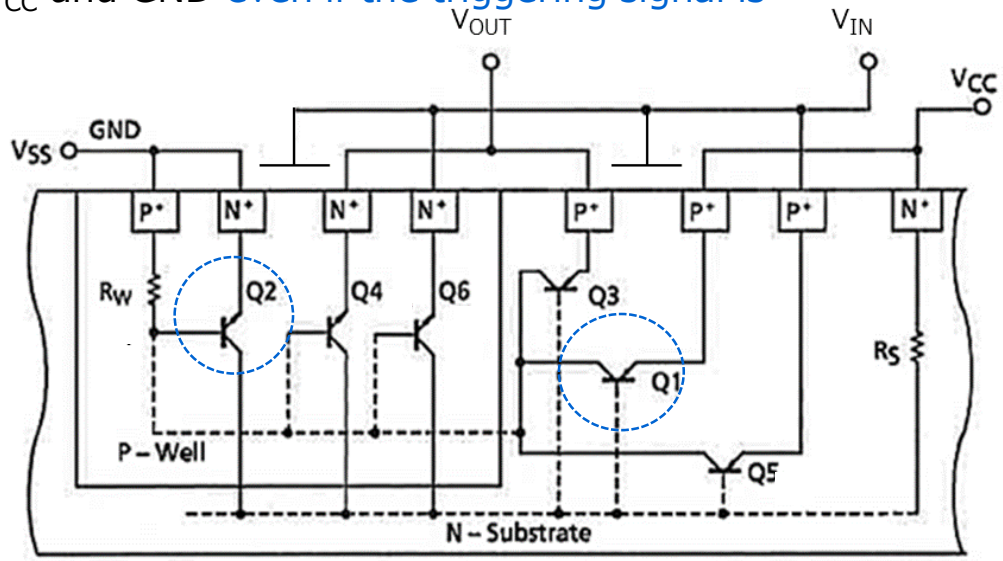
A latch-up is a phenomenon specific to CMOS integrated circuits that is caused by SCR (Silicon Controlled Rectifier) generation.

Let's consider a CMOS logic IC formed on an n-substrate. A CMOS logic IC has various parasitic bipolar transistors (Q1 to Q6), internally forming a triac circuit. A common cause of a latch-up is excessive noise, surge voltage, or surge current on an input or output pin of a CMOS IC. Another cause is a sharp change in the supply voltage. In such cases, the internal triac circuit turns on, causing an excessive current to continue flowing between V_{CC} and GND even if the triggering signal is disconnected, and eventually leading to the destruction of the IC.

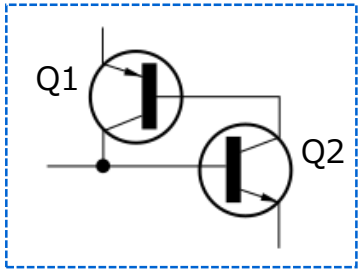
The following briefly describes the process leading to a latch-up.

The right-hand figure shows an equivalent circuit of a CMOS circuit, including its parasitic structure. An NPN transistor (Q2) is formed in the p-well on the n-channel MOSFET side while a PNP transistor (Q1) is formed in the n-substrate on the p-channel MOSFET side. Parasitic resistances (R_S and R_W) also exist between IC pins. **Parasitic elements (Q1 and Q2) form a thyristor.**

For example, if current flows into the n-substrate because of an external cause, a voltage drop occurs across resistor R_s in the n-substrate. As a result, Q1 turns on, causing current to flow from V_{CC} to GND via resistor R_W in the p-well. The current flowing through R_W produces a voltage difference across R_W, which turns on Q2, causing supply current to flow via R_s. Since this further increases the voltage difference across R_s, Q1 and Q2 remain on. Consequently, the supply current continues increasing. As described above, CMOS ICs suffer from a latch-up problem when voltage differences occur across R_W in the p-well and R_s in the n-substrate.

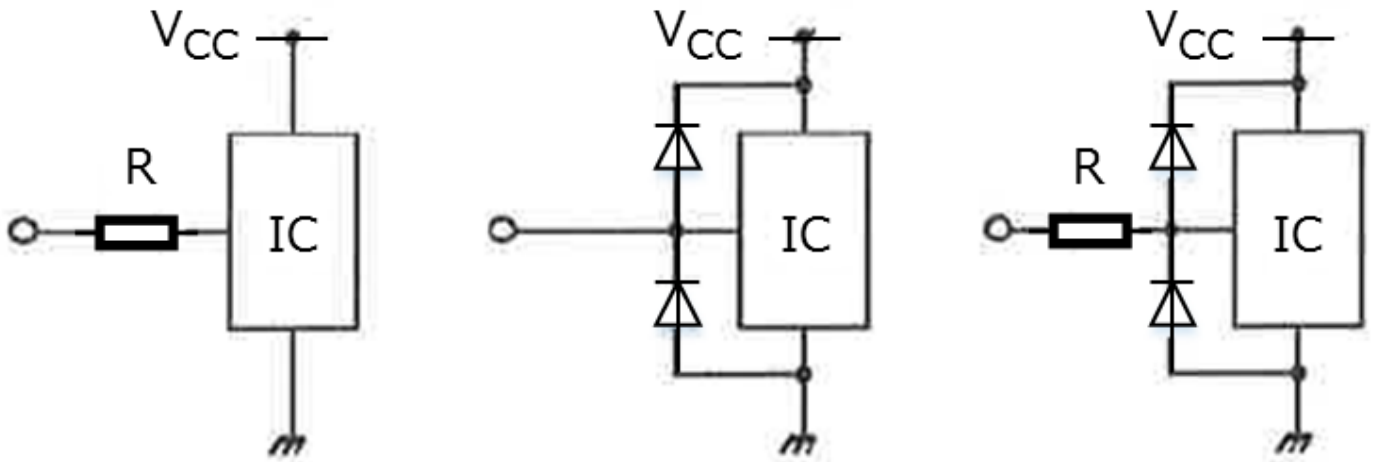


Equivalent circuit for a typical CMOS logic IC with parasitic elements



12. Countermeasures for latch-up

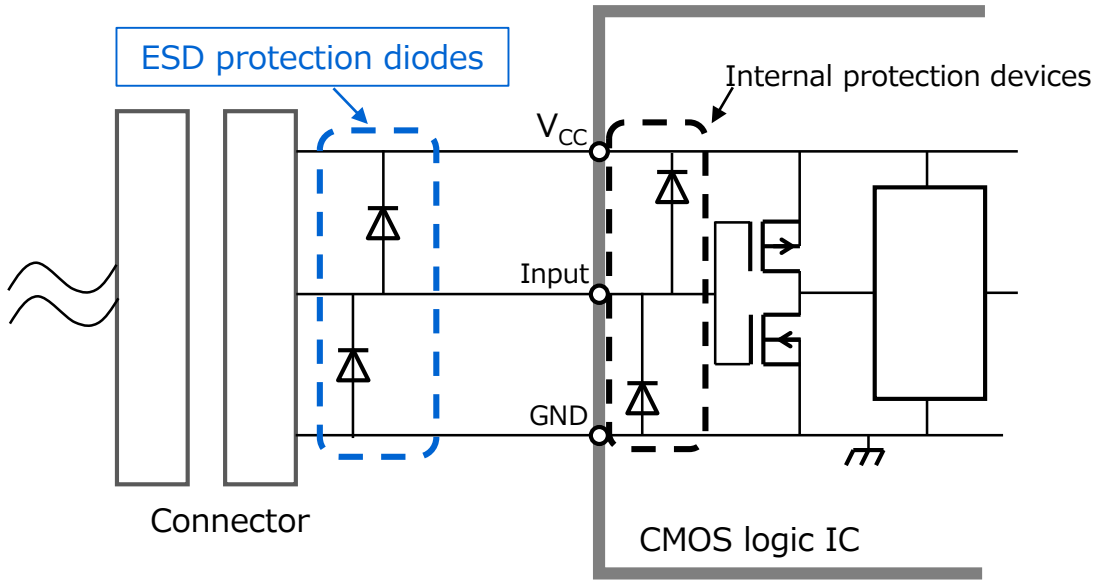
Countermeasure for latch-up
Use under the rated conditions.
But it is recommended to add a protection circuit to the IC interface as shown in below figure.
if an excessive surge might be applied to the IC.



13. Countermeasures for ESD protection

CMOS logic ICs provide electrostatic discharge (ESD) immunity compliant with international standards. Exposure to higher ESD might cause a malfunction or permanent damage to a CMOS logic IC. Because the oxide film at the input gate of a CMOS logic IC is very thin (hundreds to thousands of angstroms), it could be damaged by an ESD of hundreds to thousands of volts.

To prevent this, each input pin generally provides ESD protection circuitry. However, there is a limit to this protection. Insert external ESD protection diodes for the inputs that might be exposed to excessive ESD (e.g., inputs connected to a board's external interface).



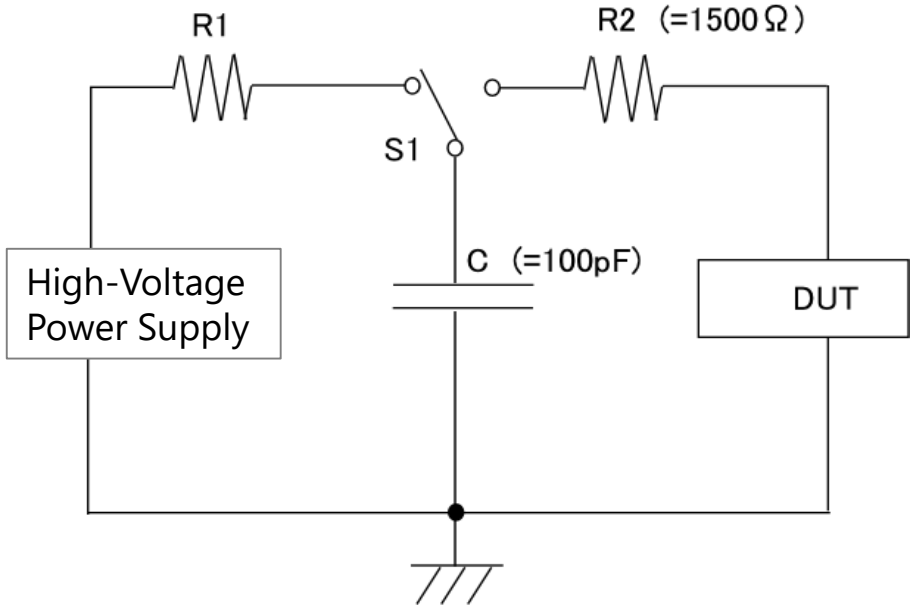
Example of external interface protection against electrostatic discharge

13. Countermeasures for ESD protection

There are various ESD models. The following describes one of the major ESD models.

Human body model (HBM)
This model characterizes the susceptibility of a semiconductor device to damage from ESD that might be generated from a human body.
There are numerous discussions on the human body capacitance. For ESD immunity testing, the charged human body is modeled by a **100-pF** capacitor and a **1500-Ω** discharging resistor. During testing, the capacitor is fully charged and then discharged through a resistor.

The HBM test circuit is shown below.



HBM test circuit

TOSHIBA