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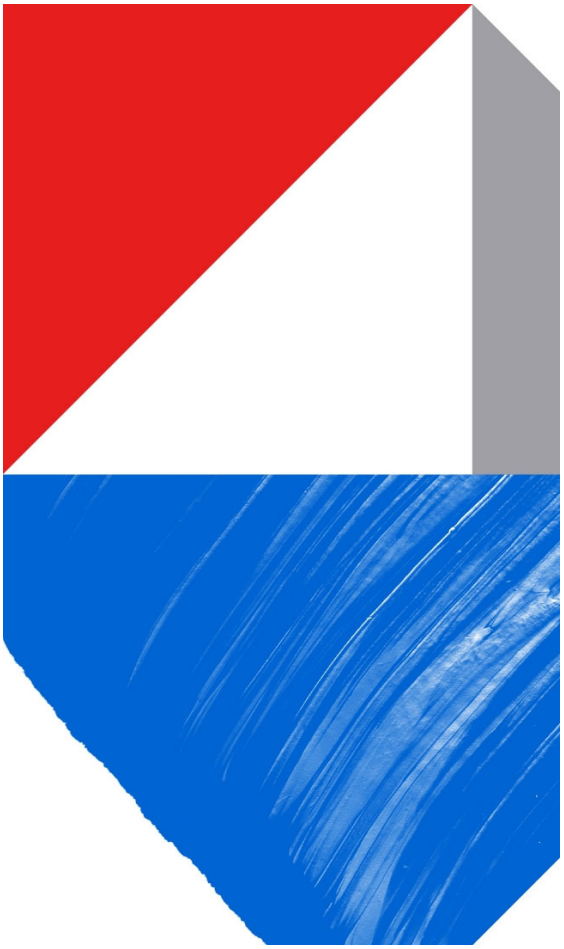

Reliability Handbook

Toshiba Electronic Devices & Storage Corporation

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Chapter 1 Semiconductor Reliability

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As functionality and performance have improved in recent years in equipment and systems that use semiconductor products, demand for functionality and reliability improvements in semiconductor products has also increased. Also, to satisfy demand for higher functionality, miniaturization and high integration of semiconductor products has progressed, which require further reliability.

In this chapter, we will explain the concept of reliability and the factors affecting the reliability of semiconductors.

1-1. Reliability Concept

1-1-1. Defining and Quantifying Reliability

From the beginning of industrial production, reliability, defined in terms of durability, long lifespan, safety, and serviceability, has been adopted as a measure of product quality. However, reliability has been more systematically adopted since the 1950s. Along with the sophistication and complexity of devices and the progress of systemization for complex systems such as chemical plants and electric power grids, public demand for reliability and awareness of the damage caused by breakdowns have increased, and reliability has become an important quality characteristic. For this reason, movement from the abstract concept of reliability to developing more quantitative ways to achieve and to measure, improve, and manage the reliability of actual systems and products has become active.

In JIS-Z8115:2000 Glossary of terms used in dependability, “Reliability” is defined as “the ability for an item to perform its required function for a given period under given conditions.”

Here, we define “item” as “any part, component, device, equipment, functional unit, instrument, subsystem, system, etc. that is subject to dependability.”

It is important to note that reliability is defined as a characteristic of a product and is expressed as a probability which includes three independent concepts: [1] time, [2] spatial factors such as operating and environmental conditions, and [3] evaluation parameters for determining whether or not the product performs as specified (i.e., the definition of failure).

1-1-2. Reliability and Time

Of the three items (time, spatial factors, and the definition of failure) mentioned in Defining and Quantifying Reliability, spatial conditions and the definition of failure for each device are constant. Therefore, reliability can generally be defined as a function of time (t). Reliability concerns the normal functioning of a product over time, while quality mainly concerns the normal functioning of a product initial stage (at time 0).

Reliability, as described above, is expressed as a probability value with time as a variable. Depending on whether the product is a component or system and depending on its purpose and application, the following functions can be used as measures of reliability quantification.

1-1-2-1. Reliability (or Reliability Function) R(t)

This function defines reliability as the ratio of non-defective units after *t* hours of use to the total number of units at the start of use, i.e., the product survival rate. It is expressed as:

$$R(t) = \frac{N_0 - C(t)}{N_0}$$

where N_0 = Number of non-defective units at time 0(zero), $C(t)$ = Number of units that have failed by time t

1-1-2-2. Non-Reliability (or Cumulative Failure Distribution) F(t)

This equation calculates the Cumulative Failure Rate from time 0 to time t.

Its distribution complements that of R(t), as shown in Figure 1-1-2-1.

$$F(t) = \frac{C(t)}{N_0} = 1 - R(t)$$

N_0=Number of non-defective units at time 0(zero)

$C(t)$=Number of units that have failed by time t

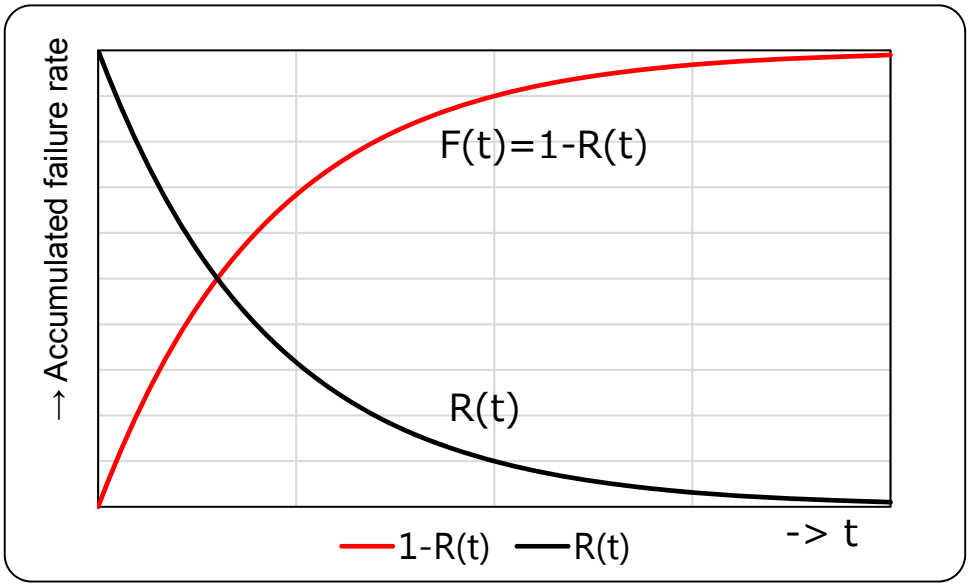


Figure 1-1-2-1 Relationship Between Reliability and Non-Reliability

1-1-2-3. Failure Density Function $f(t)$

This is the differential of the cumulative failure rate F(t) with respect to time.
It shows the rate of failure increase at time t.

$$f(t) = \frac{dF(t)}{dt} = -\frac{dR(t)}{dt}$$

$$R(t) = \int_t^{\infty} f(t)dt$$

$$F(t) = \int_0^t f(t)dt$$

1-1-2-4. (Instantaneous) Failure Rate (or Hazard Rate) $\lambda(t)$

This represents the rate of failure per unit time at time t.

$$\lambda(t) = \frac{f(t)}{R(t)} = -\frac{dR(t)}{dt} \cdot \frac{1}{R(t)} = -\frac{d \ln R(t)}{dt}$$

Reliability can be expressed in terms of $\lambda(t)$ as follows:

$$R(t) = \exp\left(-\int_0^t \lambda(t) dt \right)$$

According to the MIL standard, failure rate is expressed as "%/1000h" using 1000h as the unit of time. For semiconductor products, however, failure rate is expressed using the unit FIT, where 1 FIT = 10^{-9} (failures/hour) = 10^{-4} (%/1000h), because the failure rate is very low.

1-1-2-5. Product Life

Product life can be expressed in many ways. Mean Time to Failure (MTTF) is used with non-repairable devices and parts, and Mean Time Between Failures (MTBF), which shows the mean lifetime, and Useful Life, which shows the length of time until the failure rate will remain below a specified value, is used with repairable devices and parts. For devices and parts that cannot be repaired, MTTF is found as follows:

$$MTTF = \int_0^\infty t f(t) dt$$

1-1-2-6. Distributions in Reliability Analysis

The evaluation and quantification of product reliability are prerequisites for selecting appropriate technical and control techniques for reliability improvement, and are necessary for determining trade-offs between reliability improvement and cost during designing as well as for assuring products.

The following is an example of an evaluation procedure in graph form.

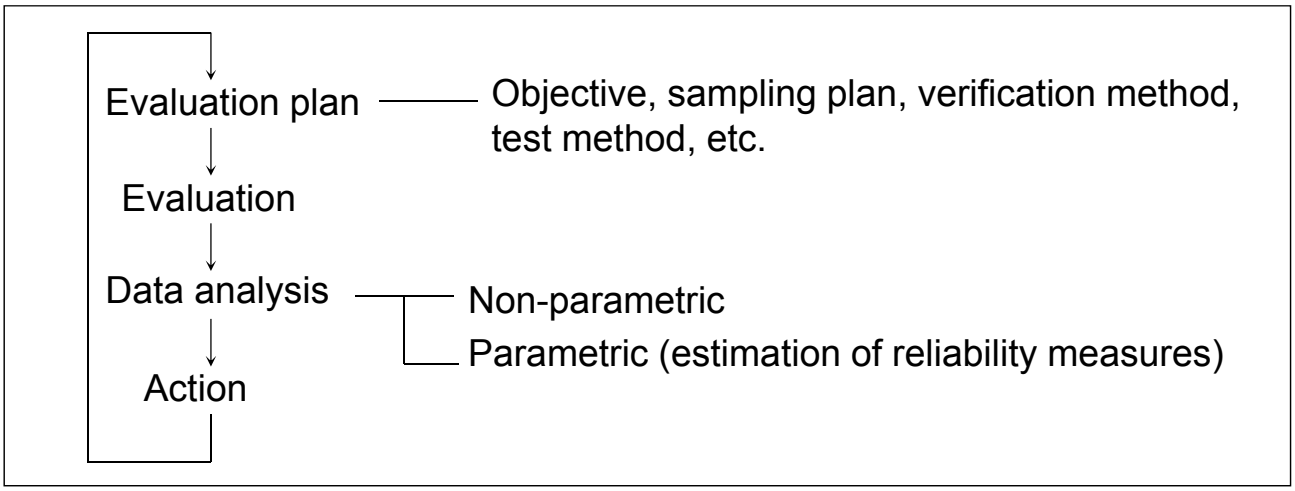


Figure 1-1-2-2 Example of Evaluation Procedure

This section describes the fundamental mathematics required for data analysis. Data analysis is used to estimate the reliability measures (such as reliability, mean life and failure rate) previously described. The two estimation methods are the non-parametric method, which does not assume a distribution form, and the parametric method, which does assume a distribution form.

The parametric method is widely used, because it is more precise and less costly, as described later. Continuous distributions (the exponential, Weibull, log-normal, normal and gamma distributions) and discrete distributions (the geometric, binomial, Poisson and negative binomial distributions) are used.

1-1-2-7. Continuous Distributions

(a). Exponential Distribution

The exponential distribution expresses the failure density function $f(t)$ as:

$f(t) = \lambda e^{-\lambda t}$ λ: Failure rate (constant)

The reliability R(t) is expressed as:

$R(t) = e^{-\lambda t}$

The failure rate (λ) is a constant, independent of time.
The mean life μ is:

$\mu = 1/\lambda$

In other words, the reciprocal of the failure rate is the mean life. The exponential distribution is characterized by the fact that the mean life and MTBF are equal and by the fact that the reliability of the surviving product after a certain time has elapsed is equal to the initial reliability of the product.

(b). Weibull Distribution

The failure density function $f(t)$ is given as:

$$f(t) = \frac{m(t-\gamma)^{m-1}}{t_o} \cdot \exp\left\{-\frac{(t-\gamma)^m}{t_o}\right\}$$

and the failure rate λ (t), the mean life μ, reliability or survival rate R(t) at time t, and cumulative failure rate F(t) at time t are expressed as follows:

$$\lambda(t) = \frac{m(t-\gamma)^{m-1}}{t_0}$$

$$\mu = t_0^{\frac{1}{m}}\Gamma\left(1+\frac{1}{m}\right)$$

Where, Γ = gamma function

$$R(t) = \exp\left\{-\frac{(t-\gamma)^m}{t_0}\right\}$$

$$F(t) = 1 - \exp\left\{-\frac{(t-\gamma)^m}{t_0}\right\}$$

In the above equation, m, t_0 and γ are distribution parameters. The parameter m determines the shape of the distribution and is referred to as the shape parameter. When the value of m is changed, the failure rate changes with time as shown in Figure 1-1-2-3.

The distribution is exponential when m = 1. In other words, the Weibull distribution includes the exponential distribution as a special case.

The failure rate increases with time when m > 1 and decreases with time when m < 1. When m is 3 or 4, the distribution is similar to the normal distribution which is described later.

The parameter t_0 determines the time scale and is referred to as the scale parameter. γ determines the time at which failures start to occur and is referred to as the position parameter.

When time $(t-\gamma) = t_0^{1/m}$ is substituted in the reliability equation, F(t) = 0.632, a constant value independent of m, t_0 and γ. Therefore, $t_0^{1/m}$ is referred to as the characteristic life.

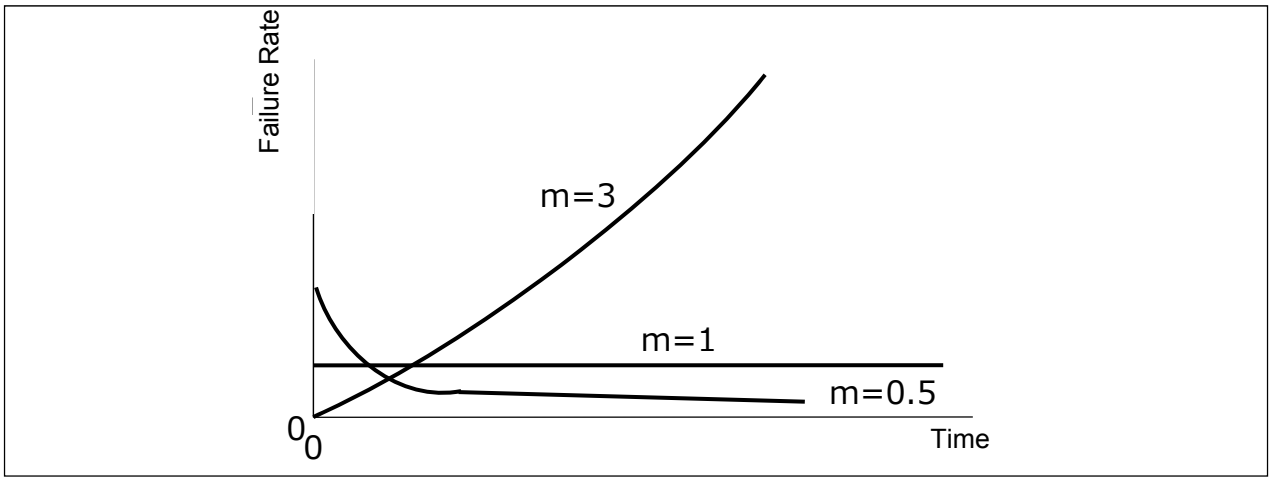


Figure 1-1-2-3 Relationship between Failure Rate and Shape Parameter m

(c). Log-Normal Distribution

In this distribution, the failure density function $f(t)$ is expressed as:

$$f(t) = \frac{1}{\sqrt{2\pi}\sigma t} \exp\left\{ -\frac{(\ln t - m)^2}{2\sigma^2} \right\}$$

This becomes a normal distribution when ln t = y.

The mean life μ and median t_{50} are expressed respectively as:

$$\mu = \exp\left\{ m + \frac{1}{2}\sigma^2 \right\}$$

$$t_{50} = e^{\mu}$$

where m and σ are the median and a parameter showing the variation of the distribution, respectively.

(d). Normal Distribution

In this distribution, the failure density function $f(t)$, mean life μ and failure rate $\lambda(t)$ are expressed respectively as:

$$f(t)=\frac{1}{\sqrt{2\pi}\sigma}\cdot\exp\left\{-\frac{(t-m)^2}{2\sigma^2}\right\}$$

$\mu=m$

$$\lambda(t)=\frac{\exp\left\{-\frac{(t-m)^2}{2\sigma}\right\}}{\int_t^{\infty}\exp\left\{-\frac{(t-m)^2}{2\sigma^2}\right\}dt}$$

where m and σ are the average and standard deviation of the distribution.

(e). Gamma Distribution

In this distribution, the failure density function $f(t)$, mean life μ and failure rate λ (t) are expressed respectively as:

$$f(t)=\frac{m^k}{\Gamma(k)}t^{k-1}\cdot e^{-mt}$$

$\mu=k/m$

$$\lambda(t)=\frac{t^{k-t}e^{-mt}}{\int_t^{\infty}x^{k-1}\cdot e^{-mx}dx}$$

where k is called the shape parameter. When k = 1, this distribution is similar to the exponential distribution; and when $k \geq 4$, it is similar to the normal distribution.

The gamma distribution (Γ distribution) can be considered a distribution of failures occurring for the first time after k harmful shocks have been received. In this case, m is the number of harmful shocks per unit time.

1-1-2-8. Discrete Distributions

When it is physically impossible or inconvenient to inspect a product continuously until it fails, inspections are performed at specific intervals. In this case, time is not continuous and is treated as a discrete variable k (k = 0, 1, 2, . . .). Distributions in which time is discrete are referred to as discrete distributions.

(a). Geometric Distribution

In this distribution, the failure density function $f(k)$ is expressed as:

$$f(k)=p\cdot q^{k-1} \quad (p + q = 1)$$

where p is the probability that a failure will occur (the failure rate) during the interval from time (k – 1) to time k, and is independent of the transition of time.

The mean life μ and reliability R(k) are expressed respectively as:

$$\mu = 1/p$$

$$R(k)=q^k$$

When the time interval is made infinitely small, the result is an exponential distribution.

(b). Negative Binomial Distribution

The negative binomial distribution is a discrete form of the gamma distribution, just as the geometric distribution is a discrete form of the exponential distribution.

The failure density function f(k), mean life μ and reliability R(k) are expressed respectively as:

$$f(k) = \begin{pmatrix} k-1 \\ k-m \end{pmatrix} p^m q^{k-m}$$

m = 1, 2, …

K=m, m+1, …

$$\mu = m \cdot q/p$$

$$R(k) = 1 - \sum_{i=m}^{k} \begin{pmatrix} i \\ k \end{pmatrix} p^i q^{k-1}$$

In the above equations, the parameters p and m can be considered as follows: p is the number of harmful shocks per unit time interval and m is the durability against the shock. In other words, the product fails when harmful shocks are applied to the product m times.

(c). Compound Negative Binomial Distribution

In (a) and (b) above, p was constant and independent of time. If p is expressed as a function of time, as p(k), the failure density function f(k) can be expressed as:

f(k)={1-p(1)}·{1-p(2)}……{1-p(k-1)}·p(k)

k=1, 2 ……

which becomes a continuous Weibull distribution when p(k) is substituted as follows:

$$p(k) = \frac{\gamma}{\beta}\left\{k^{\beta} - (k-1)^{\beta}\right\}$$

(d). Binomial Distribution

While the geometric distribution and negative binomial distribution are used to indicate reliability, the binomial distribution and the Poisson distribution (described below) are discrete distributions mainly for sampling inspections.

The probability $P_B(r)$ of failure occurring r times during n tests is referred to as a binomial distribution, and is expressed by the equation below.

(Assuming that r failures occur when N items of the product are tested by inspecting n samples, if the relationship 10n < N exists, the probability of failure can be approximated by a binomial distribution.)

$$P_B(r) = \begin{pmatrix} n \\ r \end{pmatrix} p^r (1-p)^{n-r}$$

In the above equation, p is the probability of failure occurring in a single test.

(e). Poisson Distribution

When np = λ in the binomial distribution and

$n \to \infty$

$p \to 0$

the binomial distribution becomes a Poisson distribution with parameter λ:

$$P_B(r) = \frac{\lambda^r}{r!} e^{-\lambda}$$

where the parameter λ is equivalent to np in the binomial distribution. If:

$n > 10$

$p < 0.1$

the distribution sufficiently satisfies the Poisson distribution.

1-1-2-9. Bathtub Curve

In general, the failure rate of electronic components displays a certain pattern as shown in Figure 1-1-2-4. We divide this into three periods: the initial failure period, the random failure period, and the wear-out failure period. (We call the behavior in this figure a bathtub curve.)

In the initial failure period, the failure rate can be reduced by screening (so-called burn-in, aging, heat run, etc.) and process improvement.

For semiconductor products, there is a tendency for the failure rate to decrease in the random failure period. Failures that occur in the random failure period are considered to be caused by survivals that have existed for a long time and could not be removed in the initial failure period screening due to minor failures and low acceleration.

Although most semiconductor products do not reach the wear-out failure period, we curb the occurrence of wear-out failure with design measures and preventive maintenance.

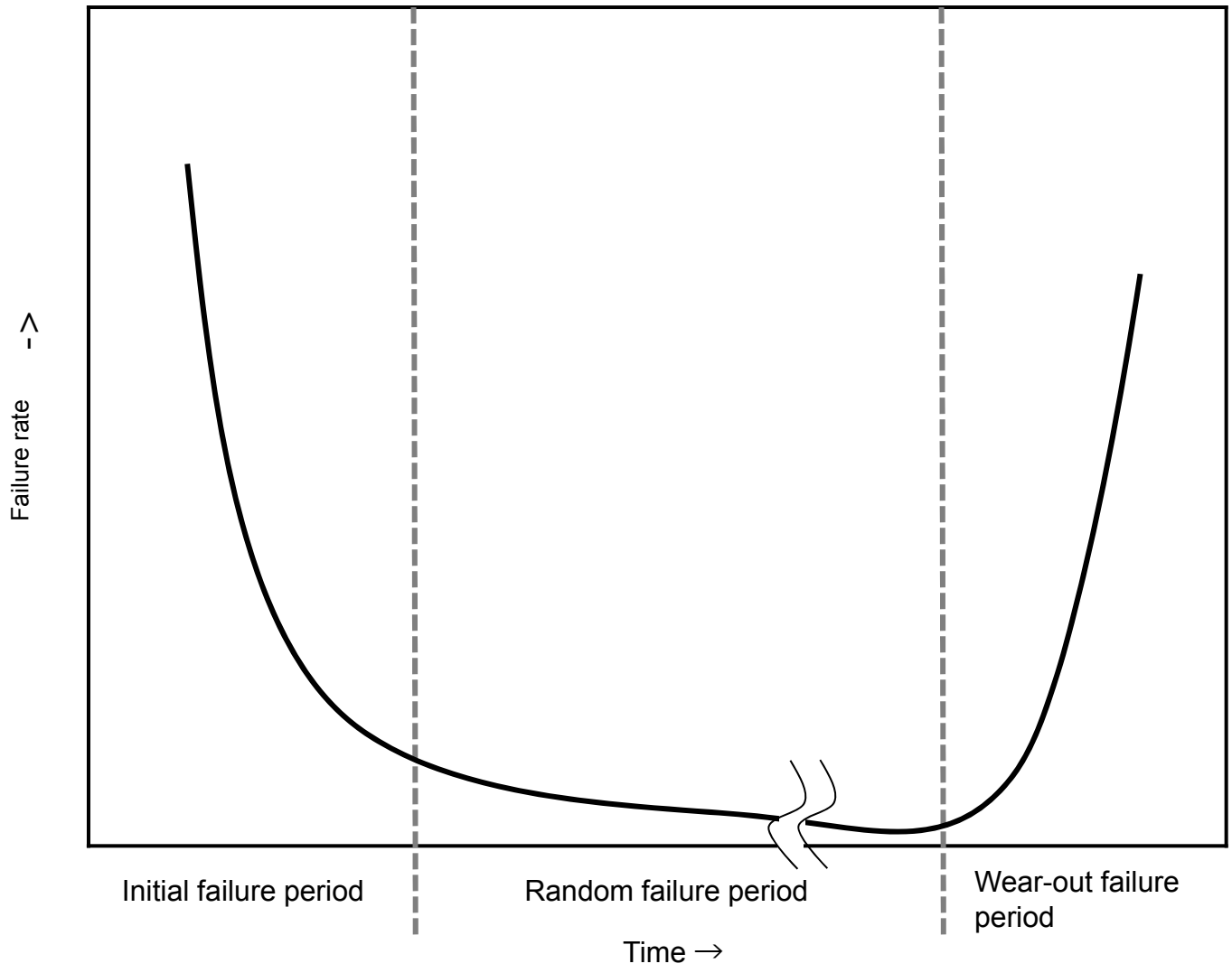


Figure 1-1-2-4 Bathtub Curve Example

1-1-2-10. Concept of Initial Failure Period's Screening

In the early failure period in the bathtub curve, the failure rate is higher than in the random failure period, but failures caused by defects incorporated during the manufacturing process are common and decrease gradually over time.

To reduce the initial failure rate, measures are taken to reduce the defects themselves by improving processes, but it may take time to reduce them. In parallel with defect reduction measures, we may use screening to reduce the failure rate.

Figure 1-1-2-5 shows an example of a screening condition investigation procedure.

We perform Weibull plot analysis using the data acquired in accordance with Figure 1-1-2-5 to determine screening conditions so that the survival rate after screening satisfies the market failure rate of that semiconductor product. The determined screening conditions are verified according to the EFR (Early Failure Rate) after screening.

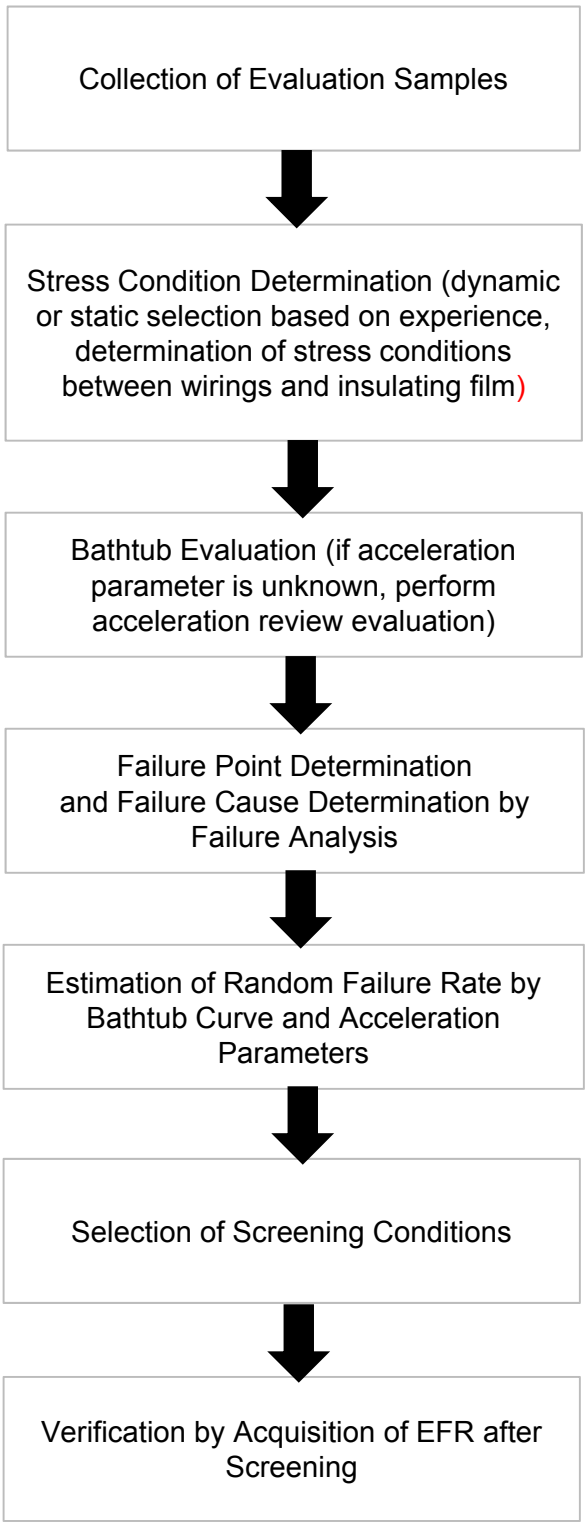


Figure 1-1-2-5 Screening Condition Investigation Procedure Example

1-1-2-11. System LSI Field Failure Mode

(a). Test Coverage

There are various System on Chip (SoC) failure models. A typical failure model is “stuck-at” fault in which a circuit is logically fixed to 0 or 1, regardless of the circuit input status.

In general, fault simulation is used to check the effectiveness of a test pattern at the time of circuit failure detection. For example, let us presume that a faulty node becomes stuck at 0. When a pattern that changes this node to 1 is entered and the output value is compared with that of the normal circuit, the fault is detectable if the values do not match and not detectable if the values match.

In this manner, fault simulation is used to check the integrity of a test program by presuming the failure of a certain node in a circuit and repeating the test program for all possible failure locations to see if the failure is detectable by the test pattern. The term “test coverage” refers to the ratio of detectable failures to the number of presumed failures in a circuit.

For a stuck-at failure, it is difficult to achieve a high fault coverage using conventional function tests alone due to ever increasing SoC scaling. For this reason, the scan method and automatic test pattern generation (ATPG) technology are combined to achieve a high fault coverage. Furthermore, with higher SoC speeds as a result of process miniaturization in recent years, response to stuck-at faults as well as delay faults will be increasingly in demand.

A delay fault is a failure in which the circuit delay does not conform to specifications for some reason or other. Similar to stuck-at faults, it is difficult to achieve a high delay fault coverage using conventional function tests alone. The scan method must therefore be combined with transition delay tests or other techniques to achieve a high fault coverage. Figure 1-1-2-6 provides an overview of the transition test.

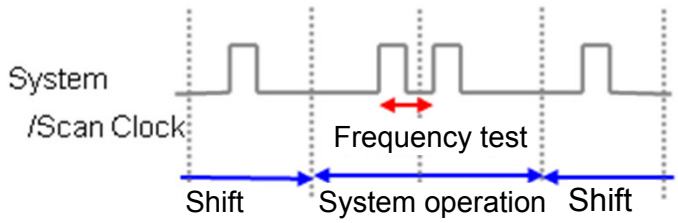


Figure 1-1-2-6 Overview of Transition Delay Test

As shown in Figure 1-1-2-6, the frequency test is conducted with the clock operated at the desired test frequency. The pattern is automatically generated and impressed on SoC based on an ATPG algorithm, enabling delay failure detection.

(b). Zero Time Failure Reduction Method

The term “zero time failure” refers to a defect that occurs after shipment from Toshiba, between customer incoming inspection and product shipment. Zero time failures are estimated based on test coverage and production yield. In general, the relational expression of test coverage and defect level (DL) is as follows:

$$DL = 1-Y^{(1-T)}$$

DL: Defect level, Y: Yield, T: Test pattern failure detection rate

Toshiba indicates zero time failures based on the above-described logical equation and actual field data using the formula below, utilizing the result as an index for measures for yield improvement and reduction of defects caused by test pattern inadequacies.

$$FDL = \alpha \{1-Y^{(1-T)}\} + \beta$$

FDL: Failure defect level

α, β: Coefficients

Y: Yield

T: Test coverage

1-1-3. Operating and Environment Conditions

The reliability of semiconductor products is determined by stresses caused by electrical loads, ambient environmental loads and mechanical loads applied to the exterior of the product (collectively referred to as external stresses), and the product's ability to withstand these external stresses (in a broad sense, the product's strength).

To increase reliability, two things are required: (1) Design products to withstand forces beyond the expected external stress levels, and (2) During use, limit external stress to a level the product can withstand.

External stresses that affect the reliability of semiconductor products are:

1. Electrical loads during use, such as voltage, current, power and surges
2. Ambient environmental loads, such as temperature, humidity, gas, dust and radiation
3. Mechanical loads, such as vibration and shock during installation and transport

In order to increase reliability, Toshiba semiconductor products are designed with a sufficient margin against the normally applied external stresses, such as thermal and mechanical stress. Reducing external stress generally improves the reliability of the equipment in which semiconductors are used.

For details of external stress and derating methods (methods used to minimize to the extent possible operating conditions with respect to maximum ratings and increase reliability), refer to the later sections entitled "Factors Affecting Semiconductor Reliability" and "Use Precautions," and Appendices.

1-1-4. Designing Against External Stress

To increase the reliability of a semiconductor product, the ability of the product to withstand external stress (i.e., the strength of the product) must be improved, and failure factors must be analyzed and countermeasures must be taken.

The reliability of semiconductor products can be greatly affected by the manufacturing process and integrated circuit layout as well as the wiring for electrical connections with external devices. Thus, semiconductor design, that is the design of processes, circuits and packages, is very important. During mass production, manufacturing processes are subject to strict process QC and screening to improve reliability. Various reliability tests and field result analyses are conducted to identify the weak points of the product. This information is then used to make improvements and take reoccurrence preventive measures.

Due to the rapid progress in and frequent use of new technology in semiconductor manufacturing, reliability is improved by physical failure analysis methods.

Failure physics is not a new idea. The concept is based on the idea that failure occurs when certain energies are applied to the product as a result of external stress, such as those related to operating and environmental conditions. The method involves the identification of failure type and failure mechanism by physical and chemical analyses. This information is then fed back to the design process and manufacturing line, and the relationship with product life is subsequently identified and the failure rate and reliability are estimated.

The repeated cycle of design, manufacture, evaluation, analysis and corrective action allows the company to respond to harsh market demands and improve reliability.

1-2. Factors Affecting Reliability

1-2-1. Design Factors

Product reliability is basically determined in the product design phase. Table 1-2-1-1 lists the semiconductor design factors that should be taken into consideration during semiconductor design. The three major design categories are pattern, manufacturing process and package.

With integrated circuit design, for example, the dimensions of the transistor (bipolar or MOS) and other factors that affect performance are determined during the pattern design phase from the functional characteristics required of the device. Transistors are then combined and connected to obtain certain functions. At this time, continuous efforts are made, in order to minimize the lengths of the wiring between transistors and the chip size, to decrease to the extent possible the individual transistor size, resistance, wiring width and wiring interval dimensions. At present, this process is automated by computers and design is performed according to predefined design rules. Related factors listed in Table 1-2-1-1 and so on are incorporated into design rules and checked by computer.

In the manufacturing process design phase, the manufacturing process is designed to realize high efficiency and the expected characteristics based on the designed pattern. The manufacturing process is broadly divided into two processes: (1) the wafer process, which puts the transistors, diodes and resistors on the silicon substrate in accordance with the design pattern, and (2) the assembly process, which consists of dicing of the pattern developed on the wafer, die bonding, wire bonding and sealing to form the final product structure. During the wafer process, various manufacturing techniques are used to accurately reproduce the size and shape of the diffusion layer, oxide film and metal wiring formed on the wafer. Continuous efforts are made to maintain consistency in these characteristics. In addition, processing precision is incorporated into the design rules and fed back to pattern design.

In the package design phase, packages are designed to mechanically and thermally protect components on the diced silicon substrate from the stress of use, making the product into a form that is easy to use. There are two major types of packages: hermetically sealed, with an internal cavity structure, and resin-encapsulated, in which the device is buried in the resin. Materials such as glass, ceramic, metal and resin are used in package construction.

Table 1-2-1-1 Main Design Factors Affecting Reliability (1/2)

Factors That Affect Reliability			Related Items	Main Failure Modes
Pattern Design	Transistor (Bipolar)		Size and Shape (Collector, Base, Emitter) Impurity Concentration, Diffusion Depth	hFE Variation, Short, Open
	Transistor (MOS)		Size and Shape (W/L), Gate Film Thickness	Vth Variation, Breakdown Voltage Degradation, Leakage Current Increase
	Isolation		Width, Diffusion Depth, Impurity Concentration	Parasitic Transistor, Leakage Current Increase, Breakdown Voltage Degradation
	Resistance (Diffusion)		Size and Shape, Diffusion Depth Impurity Concentration	Breakdown Voltage Degradation, Leakage Current Increase, Short, Open, Resistance Variation
	Resistance (Poly Si, W)		Size and Shape, Impurity Concentration, Film Thickness	Open, Short, Resistance Variation
	Internal Wiring (Al/Cu/Si)		Size and Shape, Film Thickness	Open, Short, Resistance Variation
	Internal Wiring (Poly Si, W)		Size and Shape, Film Thickness, Impurity Concentration	Open, Short, Resistance Variation
	Internal Wiring Contact		Size and Shape, Contact Combination (Al/Cu/Si, Al/Cu/poly Si W Embedding, etc.)	Open, Short (Punch-through), Resistance Variation
	Barrier Metal		Size and Shape, Film Thickness	Open, Short
	Bonding Pads		Size and Shape Wire Drawing Shape	Open Bonding, Open Wiring
	Bonding Pads Layout		Bonding Pad Spacing, Package Bonding Position Correlation	Open and Short Defects of Bonding Wire Displacement (Resin Mold) of Bonding Wire
	Bump		Size and Shape	Bump Open
	Input/Output Pin Protection Circuit		Protective Resistance, Protective Diode/Transistor	Static Electricity Breakdown, Surge Breakdown
Manufacturing Process Design	Pattern Forming Process	Resist Coating	Film Thickness, Dust, Foreign Particle Adhesion, Resist	Wiring Open/Short, Resistance Variation, Breakdown Voltage Degradation, Leakage Current Increase, Vth Variation
		Mask Alignment	Alignment Accuracy	Wiring Open/Short, Resistance Variation, Breakdown Voltage Degradation, Leakage Current Increase, Vth Variation
		Exposure	Time, Illumination	Wiring Open/Short, Resistance Variation, Breakdown Voltage Degradation, Leakage Current Increase, Vth Variation
		Development	Time, Developing Solution	Wiring Open/Short, Resistance Variation, Breakdown Voltage Degradation, Leakage Current Increase, Vth Variation
		Etching	Time, Temperature, Etching Solution	Wiring Open/Short, Resistance Variation, Breakdown Voltage Degradation, Leakage Current Increase, Vth Variation
	Oxide Film Formation (Thermal Oxide Film Method)		Temperature, Time, Reaction Gas, Film Thickness	Vth Variation, h_{FE} Variation, Leakage Current Increase, Breakdown Voltage Degradation
	Oxide Film Formation (CVD Method)		Temperature, Time, Reaction Gas, Film Thickness	Vth Variation, h_{FE} Variation, Leakage Current Increase, Breakdown Voltage Degradation
	Diffusion (Thermal Diffusion)		Temperature, Time, Impurity Concentration, Diffusion Depth	Vth Variation, h_{FE} Variation, Leakage Current Increase, Breakdown Voltage Degradation
	Diffusion (Ion Implantation)		Voltage Acceleration, Dose, Ion Source Implantation Depth	Vth Variation, h_{FE} Variation, Leakage Current Increase, Breakdown Voltage Degradation
	Electrode Formation (Al/Cu/Si)		Evaporation Method, Temperature, Film Thickness	Open, Short
	Electrode Formation (Poly Si, W)		Temperature, Time, Reaction Gas, Film Thickness	Open, Short
	Barrier Metal		Temperature, Time, Reaction Gas, Film Thickness	Open, Short
	Back Gliding		Grinding Method, Grinding Pressure, Grinding Rate, Surface Condition	Wafer Crack, Surface Burn (Discoloration, Resistance Increase), Wafer Curve
	Dicing		Dicing Method, Wafer Thickness	Die Crack, Scratch, Open, Short
	Die Bonding		Die Bonding Method, Pickup Method, Temperature, Die Bonding Material (Au-Si, Epoxy, DAF, etc.)	Adhesion Protrusion, Die Crack, Scratch, Open, Short
	Wire Bonding		Wire Bonding Method (Thermocompression Bonding, US, etc.) Wire Material (Au, Al, Cu, Ag), Wire Diameter	Open, Short
	Seal (Sealing Resin)		Casting Method, Temperature, Time Material Characteristics (Thermal Expansion Coefficient, Impurities)	Die crack, Void, Open, Short, Wire Corrosion Breakages, Poor Mounting
	Exterior Lead Forming		Lead Forming Method, Size and Shape	Package Damage, Lead Shape, Defects, Lead Damage
	Exterior Lead Surface Treatment		Treatment Method (Plating, Dipping) Protective Material (Gold, Tin, Solder, etc.)	Rusting, Poor Contact, Poor Soldering, Wire Corrosion Breakages
	Solder Ball Mount		Ball Material, Mount Temperature, Cleaning Method	Ball Separation, Ball Discoloration, Substrate Crack

Table 1-2-1-1 Main Design Factors Affecting Reliability (2/2)

Factors That Affect Reliability		Related Items	Failure Mode
Manufacturing Process Design	Package Dicing	Cutting Method, Cutting Speed	Erroneous Size, Package Crack, Adhesion Degradation
	Laser Marking	Laser Method, Laser Output, Resin Surface Condition	Die Damage (Laser Penetration), Visibility Degradation
	Ink Marking	Temperature, Time, Marking Agent	Mark Erasure, Transfer
	Sealing Method	Glass, Metal Welding, Metal Melting Resin Welding, Seal Condition	Poor Airtightness, Inferior Characteristics Large Leakage Current, Wire Corrosion Breakages
Package Design (Airtight Seal)	Sealing Gas	Chemical Reactivity, Moisture Content	Inferior Characteristics, Increase in Electrical Leakage, Wire Corrosion Breakage
	Package Materials	Glass, Ceramics, Metal, Resin Thermal Expansion Rate, Mechanical Strength	Package Damage, Poor Airtightness, Inferior Characteristics, thermal runaway
	Package Shape and Size	Chip Size Correlation, Seal Dimensional Margin	Poor Airtightness, Inferior Characteristics
	Lead Materials	Electrical Conductivity, Hardness, Thermal Expansion Rate, Corrosion Resistance, Mechanical Strength	Poor Contact, Lead Damage
	Plating Material	Plating Composition, Temperature, Current	Poor Solderability, Whisker
Package Design (Resin Seal)	External Lead Shape and Size	Lead Cross Section Shape, Tensile Strength, Bend Strength	Lead Damage
	Sealing Method	Transfer Mold, Potting, Others	Open, Short (Bonding Wire)
	Sealing Resin Materials	Base Resin, Stiffening Agent, Chemical Resistance, Impurities, Thermal Expansion Rate, Thermal Conductivity	Inferior Characteristics, Open, Short, (Bonding Wire), Wire Corrosion Breakages
	Package Shape and Size	Chip Size Correlation, Seal Dimensional Margin	Missing Exterior Lead, Open, Short, Wire Corrosion Breakages
	Casting Conditions	Temperature, Time, Pressure	Open, Short (Bonding Wire), Displacement of Bonding Wire
	Lead Materials	Electrical Conductivity, Hardness, Thermal Expansion Rate, Corrosion Resistance, Mechanical Strength	Poor Contact, Lead Damage
	Plating Material	Plating Composition, Temperature, Current	Poor Solderability, Whisker

1-2-2. Manufacturing Process Factors

The semiconductor manufacturing process includes various steps, such as heat treatment, chemical treatment, processing, testing and inspection. These steps involve a great number of factors that affect reliability. Factors that degrade reliability include processing variances (dimensions, property values, etc.) that inevitably occur during product manufacturing, defects and damage that occur in the manufacturing process, handling errors due to human error, and equipment operation errors.

The semiconductor manufacturing process is extremely complicated, requiring great precision. In addition, because product characteristics are extremely sensitive, it is essential to fully understand the factors that affect reliability and take corrective actions to prevent each factor from occurring.

Table 1-2-2-1 shows the factors affecting reliability that are related to the semiconductor manufacturing process. The manufacturing process repeats several processes to form the elements of the semiconductor product, such as the transistors, resistors and capacitors that are placed on the silicon substrate, and then interconnects these elements to form a single circuit. These processes are adversely affected by dust and therefore take place in cleanrooms. It is critical that the particle originated from equipment and instruments as well as the dust level inside cleanrooms should be controlled at the submicron level. Such contaminates greatly affect reliability.

Of the factors listed in Table 1-2-2-1, those related to the wafer (silicon substrate) are most fundamental to the product. Factors such as crystal defects, resistivity dispersion, surface contamination and surface flaws directly affect product characteristics.

The assembly process begins with dicing. In this process, the die bonding, wire bonding and sealing processes are particularly critical. Die bonding and wire bonding are the processes used to secure the chip and bond the electrodes to the exterior. Since junctions are formed between different materials, changes in temperature and other physical forces (such as vibration, shock and acceleration) result in die cracks or open faults, either of which can be fatal to the product.

In the case of resin encapsulation, impurities in the sealing resin (such as sodium, potassium or chlorine), moisture adsorption, thermal expansion and mold shrinkage are critical. These can result in failures such as corrosion, characteristic failure, bonding wire breakage and die cracks. In the case of hermetic sealing, critical points include the moisture content and other impurities in the sealing gas, and the presence of conductive foreign matter. These can adhere to the chip surface and cause failures such as increased leakage current or faulty operation.

Table 1-2-2-1 Main Process Factors Affecting Reliability (1/2)

Processes That Affect Reliability			Related Parts in the Device	Related Items	Failure Mode
Wafer Process	Wafer (Silicon Substrate)		Silicon Bulk	Resistivity Distribution, Variation, Crystal Defect, Surface Dirt, Abnormal Cracks, Scratches, Warping, Distortion	Unstable Behavior, Short, Open
	Oxide Film Formation		Field Oxide, Gate Oxide, Interlayer Insulating Film, Surface Protective Film	Pinholes, Cracks, Uneven Thickness, Contamination, Poor Step Coverage	Surface Inversion, Channel Electrical Leakage, Vth Variation, Breakdown Voltage Degradation, hfe Variation, Noise, Unstable Behavior
	Pattern Forming Process	Resist Coating	Transistor, Diode Resistance, Internal Wiring, Size and Shape, Contacts	Film Thickness Defect, Unevenness, Dust, Foreign Particle Adhesion, Residual Resist	Pinholes, Leakage Current Increase, Characteristics Variation
		Mask Alignment		Misalignment, Dust, Foreign Particle Adhesion, Scratches	
		Exposure		Incorrect Exposure Amount	
		Development		Incorrect Development Amount	
		Etching		Incorrect Etching Amount, Etching Temperature, Insufficient Cleaning	
	Diffusion (Thermal Diffusion)		Transistor, Diode, Diffusion Resistance, Isolation, Contacts	Diffusion Failure (Width, Depth), Impurity Settling, Crystal Defects, Incorrect Impurity Concentration	Breakdown Voltage Degradation, Open, Short, Unstable Behavior
	Diffusion (Ion Implantation)		Transistor, Diffusion Resistance, Contacts	Oxide Film, Silicon Bulk Damage, Incorrect Dosage, Incorrect Implantation Depth	Breakdown Voltage Degradation, Open, Short, Unstable Behavior
	Electrode Formation (Metal)		Transistor Electrodes, Internal Wiring, Contacts, MOS Gate Electrodes	Scratches, Void, Step-Disconnection, Poor Contact, Thickness Defects, Fuses, Penetration, Contamination, Electromigration	Open, Short, Wiring Resistance Increase, Wire Corrosion Breakages
	Electrode Formation (Polysilicon)		MOS Gate Electrodes, Resistance, Internal Wiring, Contacts	Scratches, Step-Disconnection, Poor Contact, Thickness Defects, Fuses	Open, Short, Wiring Resistance Increase

Table 1-2-2-1 Main Process Factors Affecting Reliability (2/2)

Processes That Affect Reliability		Related Parts in the Device	Related Items	Failure Mode
Assembly Process	Dicing/Rear Grinding	Chip Proximity	Scratches, Cracks, Contamination	Leakage Current Increase, Breakdown Voltage Degradation, Wire Corrosion Breakages
	Die Bonding	Chip Adhesive	Poor Chip Adhesive, Adhesion Protrusion, Crawl-Out, Adhesion Debris, Degas (Resin Bond Substance)	Unstable Behavior, Leakage Current Increase, Short, Intermittent Inferiority
	Wire Bonding	Bonding Wire Connection	Incorrect Bonding Pressure Amount, Failure of Foundation Bonding, Bonding Loop Shape, Wire Scratches, Contamination, Wire Adhesion	Open, Short, (Package, Substrate) Wire Cutting, Bonding Separation
	Seal (Sealing Resin)	Package	Poor Molding (Bond, Crack), Displacement of Bonding Wire, Poor Lead Frame Adhesion, Molding Shrinkage and Distortion, Moisture Absorption	Bonding Wire Open, Short, Wire Corrosion Breakages (Chip, Metal Wiring) Die Cracks, Inferior Characteristics
	External Lead Forming	Lead Pins	Poor Shape, Damage, Poor Strength of Pins	Open, Poor Contact
	External Lead Surface Treatment	Lead Pins	Oxidation, Rusting, Surface Treatment Liquid Residue (Lack of Cleaning)	Open, Poor Contact, Electrical Leakage Between Pins
	BGA	Solder Ball	Poor Shape, Damage, Ball Loss	Open, Poor Contact
	Marking	Product Display	Error Display, Poor Display	Destruction due to Misuse

1-2-3. Operating Environment Factors

The factors that affect reliability and should be taken into consideration as described above include the above-described failure factors that exist within a product as well as external stresses that can accelerate those factors, i.e., the operating environment. Table 1-2-3-1 shows the operating environment factors that affect reliability.

Some of these factors operate independently. Generally, however, external factors affecting reliability are intricately interrelated. For example, corrosion breakage is caused by a combination of temperature and humidity.

Stresses are broadly divided into those deriving from the natural environment and those related to human factors.

Stresses deriving from the natural environment include temperature, humidity, atmospheric pressure, salinity, overvoltage surges due to lightning, and, for special purposes, radiation by a nuclear reactor or in the space environment. Of these, temperature and humidity are the most critical factors.

In general, a rise in temperature speeds up chemical reactions and accelerates changes in materials. This in turn accelerates failure mechanisms which cause failure. Therefore, temperature must be monitored carefully. During actual use, increases in temperature due to the environment as well as self-generated heat resulting from power consumption must be taken into account.

A change in temperature produces distortion stress on the junction between two materials with different expansion rates. If this occurs repeatedly, material fatigue arises, causing failures such as hermetic seal damage, die bond adhesion damage and bonding wire opens. In addition, if the semiconductor product is used with improper connections, the heat generated from the equipment or element can accelerate the temperature change and affect the product in an accelerated manner.

Humidity primarily causes condensation to adhere to the surface of an object and, consequently, increases the electric conductivity of the material surface. This increases leakage current, which in turn leads to defective characteristics and defective operation. Humidity can also accelerate chemical and electrical reactions, producing metal corrosion.

Resin encapsulated products especially have an inherent moisture permeation problem. However, great strides have been made to improve resin materials, resulting in improved resin capsulation that, when a comparison in actual operating environments is made, is by no way inferior to hermetic sealing.

Atmospheric pressure affects devices used in mountainous regions or in aerospace applications. Low atmospheric pressure induces a corona discharge between electrodes and reduces the package's heat radiation rate. This results in internal thermal generation, accelerating the rise in chip temperature.

Salinity greatly affects devices used in coastal regions, ships and marine applications. Salt adhering to the element surface deteriorates the insulation between electrodes and increases the change of damage caused by metal corrosion.

Lightning readily affects outdoor applications, such as traffic signaling equipment. Special protective measures must be taken to increase the ability of devices to withstand voltage surges caused by lightning.

Other natural environment factors include soft errors caused by the alpha rays of radioactive isotopes in packaging materials which affect high-integration memory, and damage or malfunction caused by radiation in certain applications, such as nuclear reactors and the aerospace.

Human factors affecting reliability include vibration during transport and in vehicle applications (Table 1-2-3-2); shock during handling by industrial robots or caused by dropping (Table 1-2-3-3); heating during printed circuit board soldering; voltage surges during the opening and closing of switches; noise from poor relay contacts or motor devices; electrostatic damage caused by use in low humidity environments; malfunction due to strong electromagnetic waves from a nearby transmitter or communicator; and ultrasonic vibration during printed circuit board cleaning after soldering.

In addition to physical factors caused by the natural environment or human error, operating conditions imposed by semiconductor use in a device or system also affect reliability. This occurs when a product is used irrespective of the maximum ratings defined in specifications.

Examples are device breakdown due to use at a voltage higher than the rated voltage, malfunction due to use at low voltage, breakdown due to excessive loads, and malfunction or breakdown due to use based on an operation timing other than that specified.

Table 1-2-3-1 Operating Environment Stress Factors Affecting Reliability

Environmental Stress Factors		Encounter Locations	Failure Mode
Temperature	High Temperature	Tropics, Desert Regions, Space, Automobiles, Other Special Environments	Unstable Behavior
	Low Temperature	Cold Regions, High Altitudes, Space, Aircraft, Other Special Environments	Unstable Behavior
Temperature Change		Intermittent Use	Die Cracks, Die Bond Degradation, Open, Short, Unstable Behavior
Humidity	High Humidity	Tropical Regions, Tunnels, Automobiles, Other Special Environments	Rusting, Poor Contact, Wire Corrosion Breakages, Open, Short
	Low Humidity	Deserts, Low Humidity Climates	Static Electricity Malfunctions
Atmospheric Pressure	Low Atmospheric Pressure	High Altitude, Mountainous Regions, Aircraft	Corona Discharge, Low Heat Dissipation, Poor Operation
	High Vacuum	Space	Corona Discharge, Low Heat Dissipation, Poor Operation
Saltiness		Coastal Regions, On the Sea, Ships, Marine Facilities	Rusting, Poor Contact, Lead Damage
Vibration		Products Being Transported, Automotive Devices, Machine Tools, Aviation Devices	Bonding Open (Hermetic Sealing Device), Lead Breakage (Circuit Board Mounting), Package Damage
Physical Shock, Dropping		Products Being Transported, Automotive Devices, Machine Tools, Aviation Devices	Package Damage, Lead Deformation
Acceleration		Aviation Devices, Rockets, Other Special-Purpose Devices	Bonding Open (Hermetic Sealing Device), Package Damage
Heating		Construction Processes (Soldering Process, etc.)	Open, Short, Abnormal Package Shape
Overvoltage, Surges		Switch, Relay Switching, Capacitive Load, Motor	Open, Short
Noise		Motor, Poor Contact	Malfunction, Open, Short
Static Electricity		Handling at Low Humidity, High Electric Field Generator Vicinity, Transporting	Open, Short
Strong Electromagnetic Waves		Near a Transmitter or Signal Generator	Malfunction
Ultrasonic Waves		Cleaning Print Circuit Boards After Soldering	Bonding Open (Hermetic Sealing Device), Mark Erasure
Radiation		Nuclear Power Related Facilities, Space (Satellites)	Malfunction, Breakdown Problems, Memory Soft Errors
Misuse	Overvoltage	Power Supply Voltage Mismatch	Breakdown Problems, Breakdown Voltage Degradation, Open, Short
	Overload	Drive Capacity Mismatch	Breakdown Problems, Open, Short
	Others	Operation Timing Mismatches, etc.	Malfunction, Latch-Up

Table 1-2-3-2 Main Environments with Vibration

Type		Description
Land transportation	Road	1 to 3 Hz up to 29.4 m/s^2, 15 to 40 Hz at 9.81 m/s^2
	Rail	14.7 m/s^2, an amplitude of ±0.05 mm at 2 to 100 Hz
Sea		Frequency: 1 to 50 Hz, Amplitude: 2.5 to 0.075 mm
Air		Frequency: 3 to 500 Hz, Amplitude 3 to 0.025 mm

Table 1-2-3-3 Main Environments with Shock

Type		Description
Land transportation	Road	58.9m/s^2 peak, 5 to 40 mm/s shock width
	Rail	When coupling and decoupling rolling stock: 196 m/s^2, Speed change: 5.4 m/s
Sea		-
Air		Shock on arrival and departure: Up to 36.3 m/s^2

1-2-4. Reliability Factor Analysis Techniques

In general, the analysis of reliability factors during product development and design and process design is very effective for improving reliability. The main reliability factor analysis methods are:

Design Review (DR)

Fault Tree Analysis (FTA)

Failure Mode and Effects Analysis (FMEA)

Taguchi method

DR, in the case of semiconductor products, refers to checking for any inconsistencies in the design of such items as shown in “Main Design Factors Affecting Reliability” and correcting any problems so as to yield a more complete product. Normally, a design standard is defined to simplify this process and incorporate corrections in advance. Design thus proceeds in accordance with the standard and is checked against the standard in the DR. If there are any deviations, tests are conducted to confirm compliance to the standard, corrections are incorporated in the design and the standard is updated as necessary.

FTA (Fault Tree Analysis) is used to analyze factors contributing to a failure, such as circuit configuration, pattern design, manufacturing process, package design and method of use.

FMEA (Failure Mode and Effects Analysis) is an analytical method used to confirm that corrective measures have been established for all possible failures in relation to aspects such as design, the manufacturing process and method of use.

The analysis divides aspects such as design, manufacturing process, packaging and methods of use into well-defined detailed smaller functional items. The possible failure modes for each item are then cataloged, and the effect of the failure on the product as well as failure causes are investigated. These items are then weighted so that countermeasure priorities can be defined and established.

Table 1-2-4-1 shows an example of the FMEA method for a resin-package MOS LSI manufacturing process. Using a scale of 1 to 10, the “R.P.N.” (Risk Priority Numbers) section of the table rates failure information in terms of occurrence , severity (on the product, equipment or system) and detection. “R.P.N.” is calculated by multiplying these three rated values together. The larger this value, the more serious the failure. The last column in the table shows the processing and countermeasures for each item.

The Taguchi method is an effective method for minimizing variance to create a robust design. While conventional basic designs required a certain constant identified experimentally and theoretically for incorporating target outputs and characteristics, quality engineering parameter design introduces an S/N ratio (average value to variance ratio) as a measure of stability with respect to variance. A robust design is developed by creating a design that incorporates a standard with a high S/N ratio.

Table 1-2-4-2 shows an example of Taguchi method factors and an S/N ratio cause and effect diagram for mold resin package conditions in the resin-package MOS LSI manufacturing process. The table shows the results of testing based on “smaller-is-better” characteristics, using the L18 orthogonal array table.

Table 1-2-4-1 Manufacturing Process FMEA Example (Resin Molding)

Process Name (Process Function)	Potential Failure Mode	Potential Effect of Failure	Potential Cause of Failure	Failure Index				Countermeasures
				Occurrence	Severity	Detection	R.P.N.	
(1-10) Metallization	Improper thickness, wiring flaws, disconnection	Electromigration, open circuit	Operator error, dirt, foreign particle adhesion, poor adjustment of equipment	2	9	2	36	Improvement and adjustment of work procedures, dust control in clean room, SEM inspection in process
(1-11) Passivation	Lack of passivation film, improper film thickness	Increased leakage current, operation failure	Adherence of dirt and foreign particles, operator error	2	2	4	16	Dust control in clean room, improvement and adjustment of work procedures
(1-12) Visual inspection	Scratch, die crack, contamination, blem, residual photoresist	Open circuit, increased junction leakage current	Mishandling of wafer, erroneous wafer cleaning	2	2	2	8	Improvement and adjustment of work procedures
2. Assembly process								
(2-1) Dicing	Die crack	Increased junction leakage current, operation failure	Improper adjustment of equipment, operator error	1	3	2	6	Equipment control operator corrective action, improvement and adjustment of work procedures
(2-2) Die bonding	Die crack, die floating	Open, increased junction block leakage current, operation failure	Operator error, temperature decrease	1	9	2	18	Equipment control operator corrective action, improvement and adjustment of work procedures, visual inspection
(2-3) Wire bonding	Wire open, wire short, improper bonding position	Open, short	Improper bonding strength, operator error, poor adjustment of equipment, abnormal loop shape	2	10	1	20	Equipment control operator corrective action, improvement and adjustment of work procedures, visual inspection
(2-4) Resin molding	Wire open, wire short, package crack, corrosion	Open, short, defective appearance	Poor adjustment of equipment, insufficient curing	2	10	2	40	Equipment control operator corrective action, improvement and adjustment of work procedures, visual inspection
(2-5) Lead finishing (plating)	Improper plating thickness, dirt	Poor soldering, improper contact	Operator error, poor adjustment of equipment, insufficient cleaning	1	2	3	6	Improvement and adjustment of work procedures, equipment control operator corrective action
(2-6) Lead forming	Abnormal shape, lead damage	Improper printed circuit board insertion, operation failure	Operator error, poor adjustment of equipment	1	2	1	2	Adjustment of work procedures, equipment control operator corrective action
(2-7) Marking	Marking error, illegible marking	Breakage during use	Operator error, insufficient curing	1	1	1	1	Improvement and adjustment of work procedures

Table 1-2-4-2 Taguchi Method Example (Factors)

	Factor	Unit	Parameters		
			Standard 1	Standard 2	Standard 3
A	Mold resin (mold name)	-	A1	A2	-
B	Resin preheating time	s	B1	B2	B3
C	Mold impregnation pressure	Pa	C1	C2	C3
D	Metal mold clamp pressure	t	D1	D2	D3
E	Metal mold temperature	°C	E1	E2	E3
F	Time from molding to bonding	H	F1	F2	F3
G	Mold ambient temperature return time	H	G1	G2	G3
H	Mold service period	H	H1	H2	H3

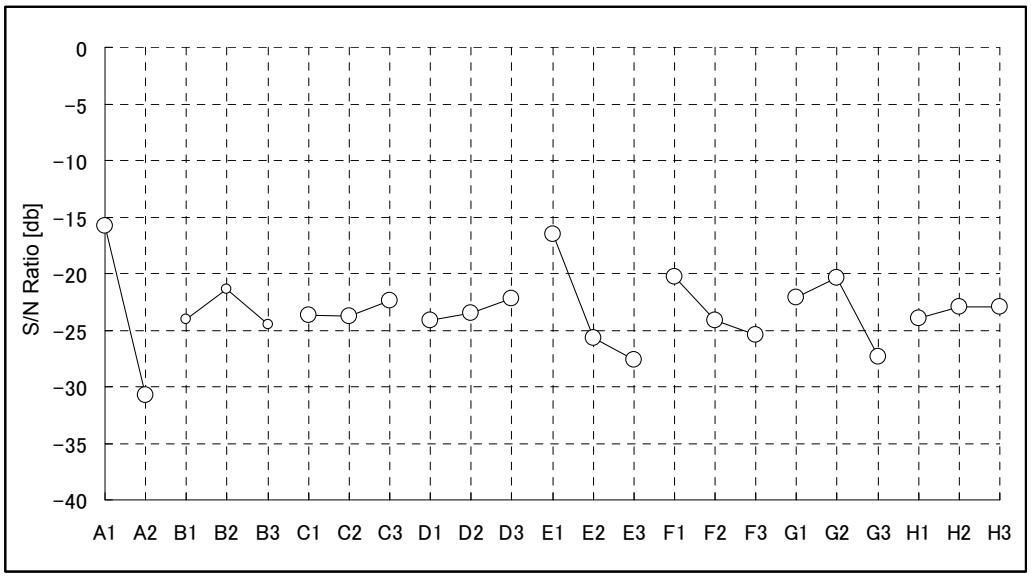


Figure 1-2-4-1 Taguchi Method Example (S/N Ratio Cause and Effect Diagram)

Chapter 2 Failure Mechanisms

Chapter 2 Failure Mechanisms

Semiconductor products have various reliability failure modes, and it is necessary to take measures to deal with them in the design and development stages.

In this section, we will explain the variety of failures with their failure mechanisms.

2-1. Wafer Process

Table 2-1 lists the main reliability failures of the wafer process.

Table 2-1 Main Reliability Failures of Wafer Process

Process	Reliability Failure Modes	Failure Mechanisms
FEOL (Front End Of Line)	Time Dependent Dielectric Breakdown (TDDB)	Even at or below dielectric breakdown voltage, micro-leakage or dielectric breakdown occurs due to time-dependent degradation. The gate insulating film, the interface state to the substrate, the insulating film thickness, etc. impact.
	Hot Carrier Injection (HCI)	Carriers accelerated by the high electric field become hot carriers and are captured in the insulating film, thereby causing characteristic degradation in the transistor.
	Instability Due to Mobile Ions	Mobile ions from the inter-layer film and the passivation film move to the gate insulating film or the interface, which causes characteristics variation.
	Negative Bias Temperature Instability (NBTI)	When a negative bias is applied to a PMOS transistor, hydrogen at the interface between the insulating film and substrate is separated, and fixed charges are generated in the insulating film, which causes characteristic fluctuation.
BEOL (Back End Of Line)	Electromigration (EM)	Metal atoms move due to colliding with electrons in metal wiring, thereby generating voids and resulting in disconnection.
	Stress Migration (SM)	A phenomenon in which a metal atom moves only by temperature stress without applying an electrical current. Metal atoms move due to stress applied to the wiring. This leads to resistance increase or breakage.
	Short Between Wirings, Inter-wiring TDDB	Electrical current passes between the wires due to breakdown of the inter-layer insulating film and due to minute foreign particles. This leads to micro-leakage and dielectric breakdown due to time-dependent degradation.

2-1-1. Time Dependent Dielectric Breakdown (TDDB)

Since the gate insulating film of MOS products is thin, from roughly a few nm to 100 nm, it breaks down when the system applies a voltage higher than the breakdown voltage. For example, it is easy for it to break down from sudden static electricity or surges. Also, in an actual use state, there is a possibility that breakdown of the insulating film that depends on time, called TDDB (Time Dependent Dielectric Breakdown), will occur.[1)]

The distribution of dielectric strength voltage based on defects in the gate insulating film and the potential defect density greatly influence these breakdowns. The parameters that determine the dielectric voltage strength distribution and potential defect density are very complicated and are subject to the influence of the gate electrode material, film thickness, substrate defects, oxidation method, cleaning, contamination, and other factors.

Although degradation is accelerated considerably due to the increase in electric field intensity, and several acceleration models of TDDB have been proposed, none has been established as authoritative. In general, the following four models are proposed.[2)3)4)5)6)]

TTF= $A\exp\left(\frac{E_a}{k}\cdot\frac{1}{T}\right)$ * exp(-βE).... E-model

TTF= $A\exp\left(\frac{E_a}{k}\cdot\frac{1}{T}\right)$ *exp (G/E) 1/E-model

TTF= $A\exp\left(\frac{E_a}{k}\cdot\frac{1}{T}\right)$ * exp(-γV_G) .... V_G-model

TTF= $A\exp\left(\frac{E_a}{k}\cdot\frac{1}{T}\right)$ * V_G^{-n} .... Power-Law model

(TTF: Time To Failure, Ea: Activation energy, k: Boltzmann constant, β･G･γ･n: Acceleration factor, A: Coefficient, E: Electric field, V_G: Voltage)

In addition, due to the miniaturization of devices and three dimensional structuring, the space between metal wires has become narrower, so TDDB under the low κ insulating film between wires is one of the important reliability evaluation items.

For TDDB between wires, E-model, 1/E-model, and the below √E-model are proposed as described in the gate insulating film TDDB. [7)]

$$\text{TTF} = A\exp\left(\frac{E_a}{k}\cdot\frac{1}{T}\right) \quad \text{*exp } (\alpha\sqrt{E}) \text{ .... } \sqrt{E} \text{ –model}$$

(TTF: Time To Failure, E_a : Activation energy, k: Boltzmann constant,

α : Acceleration factor, A: Coefficient, E: Electric field)

Figure 2-1-1-1 shows an example of a gate insulating film TDDB lifetime test acquired by our company.

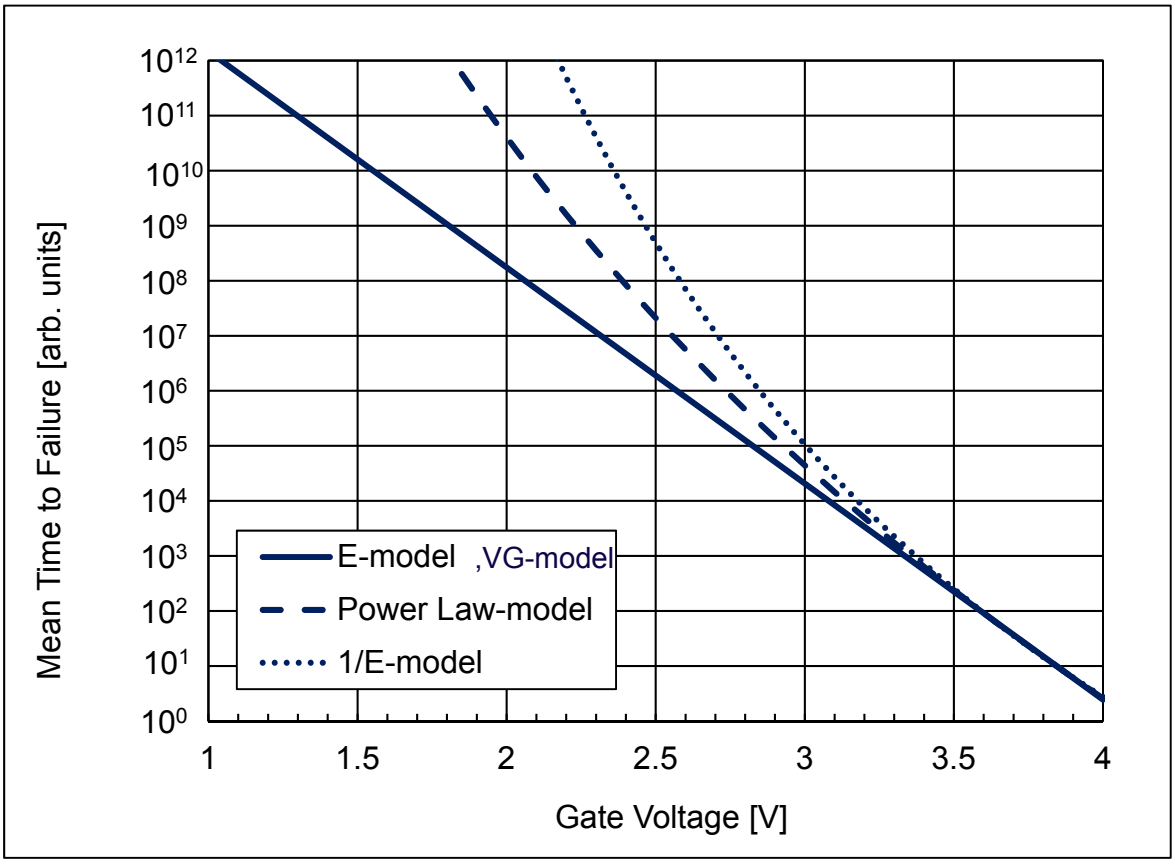


Figure 2-1-1-1 Example of TDDB Voltage Acceleration Life Test Result

2-1-2. Stress Induced Leakage

The leakage conduction mechanisms of oxide film can be broadly divided into two types: the Fowler-Nordheim tunneling current and hard breakdown (HBD) whereby insulation properties are completely lost. However, with the development of increasingly thin gate oxide films, direct tunneling current, stress induced leakage current (SILC) and soft breakdown (SBD) conduction mechanisms have been observed in thin films of 5 nm or less.

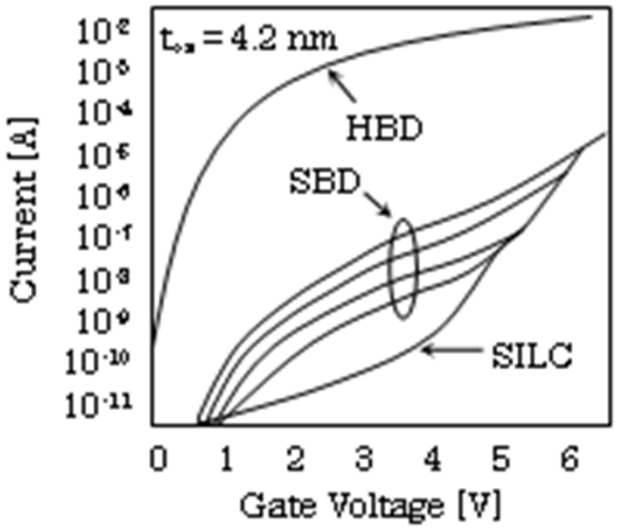


Figure 2-1-3-1 SILC, SBD, HBD I-V Characteristics [11)]

SILC has been observed to gradually increase leakage current from the initial stages of wear-out failure. Soft breakdown exhibits a current increase of an intermediate range, i.e., between that of hard breakdown and SILC, but results in a certain level of insulation rather than a complete short in the oxide film. This type of stress leakage is thought to affect factors such as the reliability of flash memory.

2-1-3. Hot Carrier Injection (HCI) [8)]

When voltage is applied to the drain of a miniaturized N-channel MOS transistor, a large electrical field is generated in the drain region as shown in Figure 2-1-2-1. As carriers flow into this region, they gain energy from the electrical field and become hot carriers. Some of them are scattered by phonons and others lose energy due to impact ionization.

Hot carriers with enough energy to surmount the Si-SiO2 electrical potential barrier are injected into the gate oxide film. This phenomenon, which accelerates with voltage, changes the MOS transistor threshold (Vth) and the mutual conductance (gm).

There are four known gate oxide film carrier injection/capture mechanisms, based on MOS transistor bias conditions: channel hot electrons (CHE), drain avalanche hot carrier injection (DAHC), two-port hot electrons and substrate hot electrons. [9)]

To avoid the effects of hot carriers, countermeasures are taken, such as reducing the circuit's internal operating voltage or forming a gate oxide film which does not readily trap injected hot carriers. Various measures are taken with the transistor structure, especially for semiconductor products with a gate length of 2 μm or less. One such measure is a lightly doped drain (LDD) transistor, as shown in Figure 2-1-2-2. [10)]

This structure exhibits a smaller electrical field around the drain and thus has fewer hot carriers.

Degradation of device characteristics due to hot carriers also occurs in bipolar transistors. This is a well-known phenomenon in which hFE degradation occurs when a reverse bias is applied across the emitter and base. With the advanced shallow junction devices of recent years, there is a tendency towards increased reverse leakage current between the emitter and base, causing device characteristic degradation to readily occur as a result of the hot carrier effect.

Figure 2-1-2-3 shows an example of high-frequency characteristic ft degradation caused by reverse emitter-base bias. This is because the base current increases due to an increased number of recombination centers at the Si-SiO2 interface caused by hot carrier injection during reverse biasing.

Many of the semiconductor product failure modes exhibit higher degradation at higher temperatures. In contrast, hot carriers are characterized by higher degradation at lower temperatures.

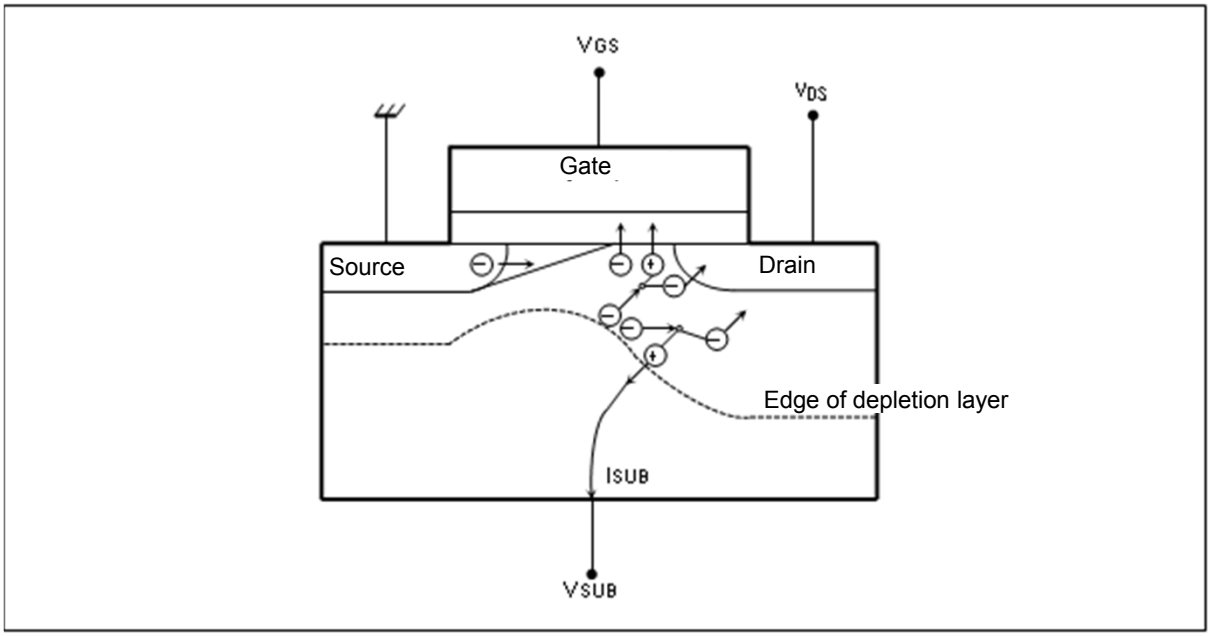


Figure 2-1-2-1 Hot Carrier Injection Model

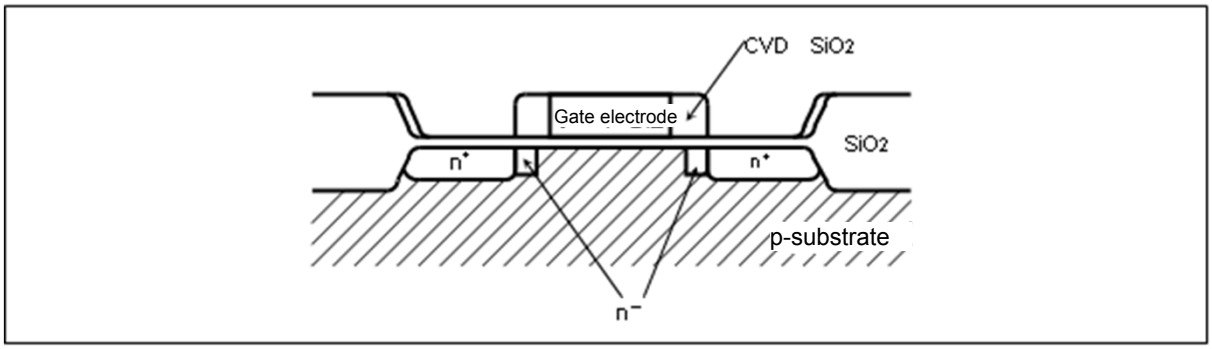


Figure 2-1-2-2 Lightly Doped Drain (LDD) Structure Transistor

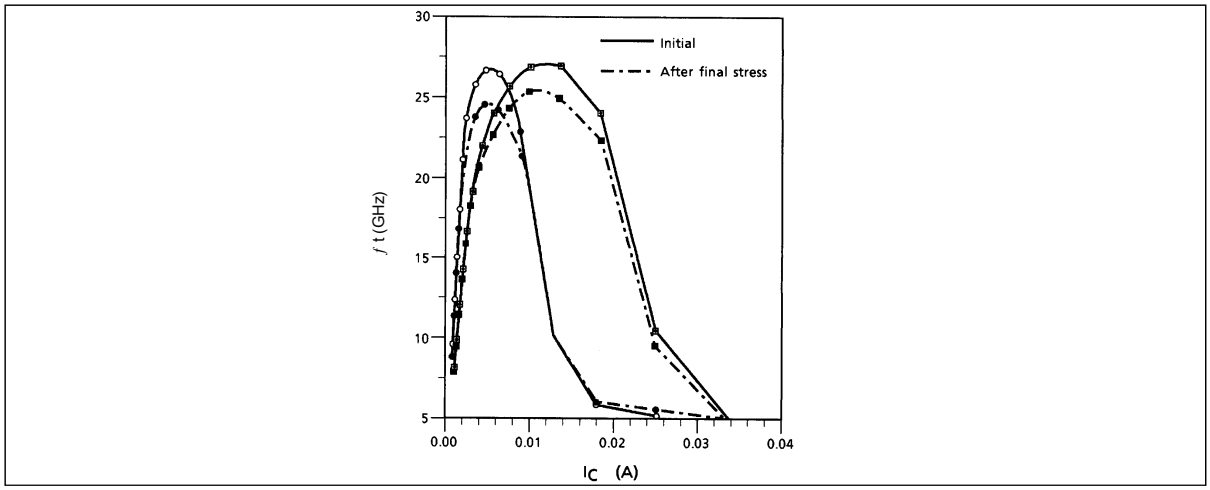


Figure 2-1-2-3 Degradation of RF Characteristics (f_t) Due to Reverse Emitter Bias

2-1-4. Negtive Bias Temperature Instability (NBTI)

NBTI is a phenomenon that causes characteristics variation when negative bias is applied to a PMOS transistor. [12)]

As shown in Figure 2-1-4-1, classified as follows, electron traps exist on the interface between the Si substrate and the gate insulating film, and in the insulating film.

[1] The impurity states of Na+, K+, etc. (mobile ions): Qm

[2] Electron holes in the insulating film (fixed charges): Qf

[3] Oxide-trapped charges: Qot

[4] Interface-trapped charges (interface state): Qit

[5] Trapped charges generated by ionizing radiation

The instability due to mobile ions [1] is considered to be caused primarily by contamination of the passivation film or by external contamination introduced into the process rather than by contamination of the gate oxide film itself. In the past, characteristics variation was observed due to the interposition of impurity states by these mobile ions, but it does not occur now due to the progress of gettering technology for removing impurities.

Charges [2] and [3] do not change state due to surface potential. When these charges are generated within the oxide film, threshold voltage V_{th} fluctuates. Charges generated near the interface between the gate oxide film are referred to as fixed charges, and charges generated within the film are referred to as oxide film trapped charges.

The interfacial state [4] changes in accordance with the surface potential and is referred to as “fast state.” When this state occurs in the oxide film interface, gm is degraded.

Charges [2], [3] and [4] are being introduced in new processing and once again coming to the fore.

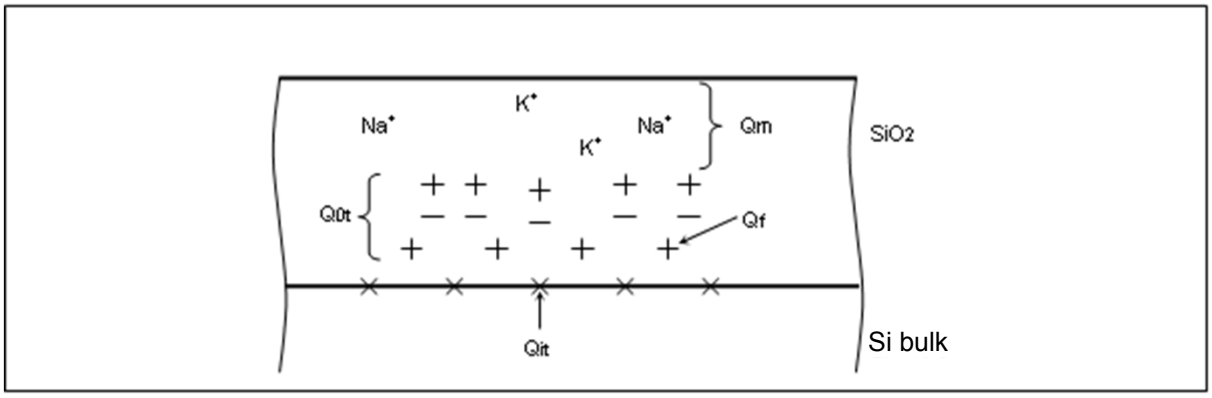
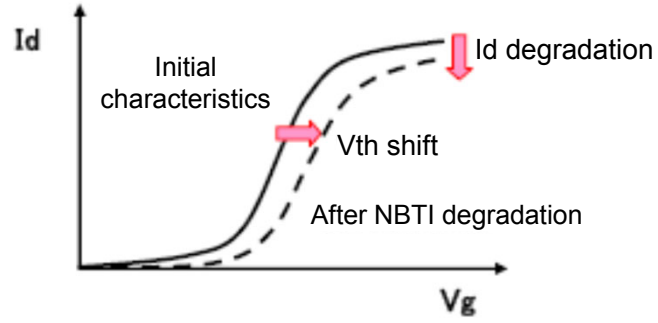
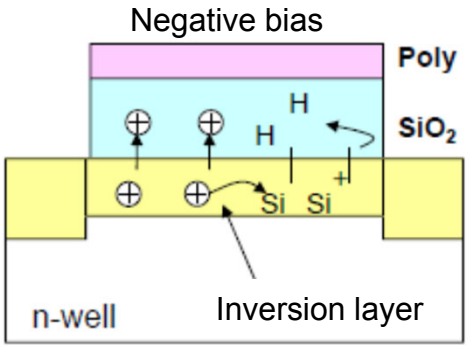


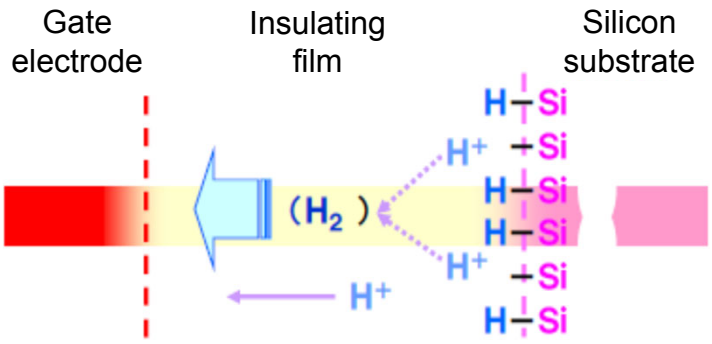
Figure 2-1-4-1 Oxide Film and Interfacial Charges[13)]

It is proposed that the occurrence of interface states is because the combination of Si and Si-H at the gate oxide Si interface disassociates H atoms with holes, resulting in the diffusion of H ions into the oxide film. This results in positive ion conductivity models (upper right figure on the next page). Another model says that ionizing collisions of tunnel electrons generate the interface states.

In reality, the model is not uniformly determined, and it may change depending on process conditions. There are reports of various influences such as the amounts of moisture, hydrogen, deuterium nitrogen, and fluorine. [14)15)16)]





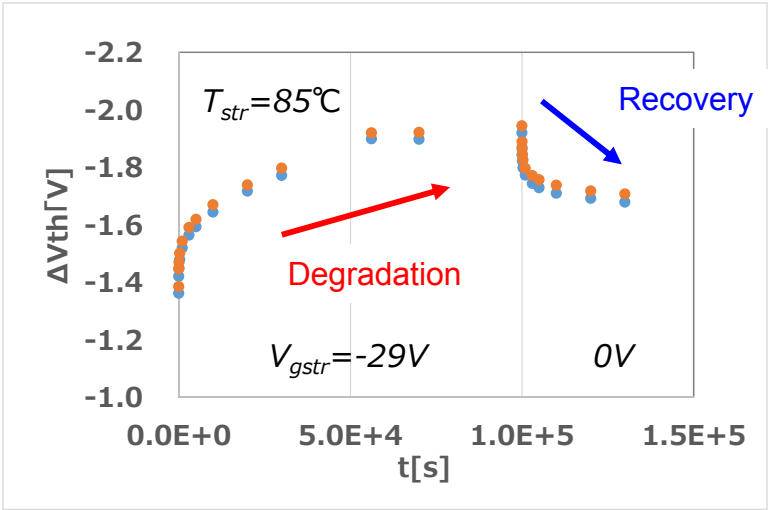


Reaction – Diffusion Model

1. Hole accumulation in channel inversion layer
2. Si-H decomposition to release H
3. Interface state formation
4. NBTI (Vth shift, Id degradation)

Due to H diffusion when a stress is imposed, a trap is formed on the SiO2/Si interface.

Also, several recovery properties (recovery effects) after stress removal have been reported. It is also important to confirm AC effects along with DC test results.



2-1-5. Electromigration (EM)

2-1-5-1. Al Metal Electromigration

It is well-known that introducing a high current to the metal wiring in an semiconductor product can cause an open fault in the metal wiring and subsequent device failure. This phenomenon is called electromigration and is becoming an important failure mechanism as the scaling of ICs gets larger and miniaturization advances, such as the case with VLSI.

The following describes the mechanism of electromigration in thin film. If a large current flows in a thin film, a force is applied to the metal atoms due to the electron wind force. As a result, Al atoms diffuse in the direction of the electron flow (from cathode to anode), forming a void on the cathode side, and a hillock or whisker on the anode side.

An open failure on thin film can occur when the mass transfer in the metal becomes variable. This variable mass transfer is caused by variations in temperature or current density, or by a variable shift in metal ions such as a triple point of Al grain boundaries.

Causes include, for example:

[1] Variable grain size [17)]

[2] Temperature gradient due to heat generation inside the device[18)]

[3] Metal in contact with other material [19)]

The electromigration life of the thin film is generally expressed as the Median Time to Failure (MTF), establishing the following relationship: [20)]

$$MTF = AJ^{-n} \exp\left(\frac{E_a}{kT}\right)$$

where MTF is Median Time to Failure, J is current density, n is a constant related to the current density, E_a is the activation energy, T is the absolute temperature, k is Boltzmann's constant and A is a constant related to the material, structure and size of the metal.

From this expression it can be seen that MTF increases with a decrease in current density or temperature. Also, the life distribution is in accordance with a logarithmic normal distribution with a narrow variation.

Figure 2-1-5-1 shows an example of how to find the activation energy related to Al metal. Activation energy is metal width dependent and as the width thickens the value approaches 0.6. This is believed to be due to the shift from bulk diffusion to grain boundary diffusion by the Al metal.

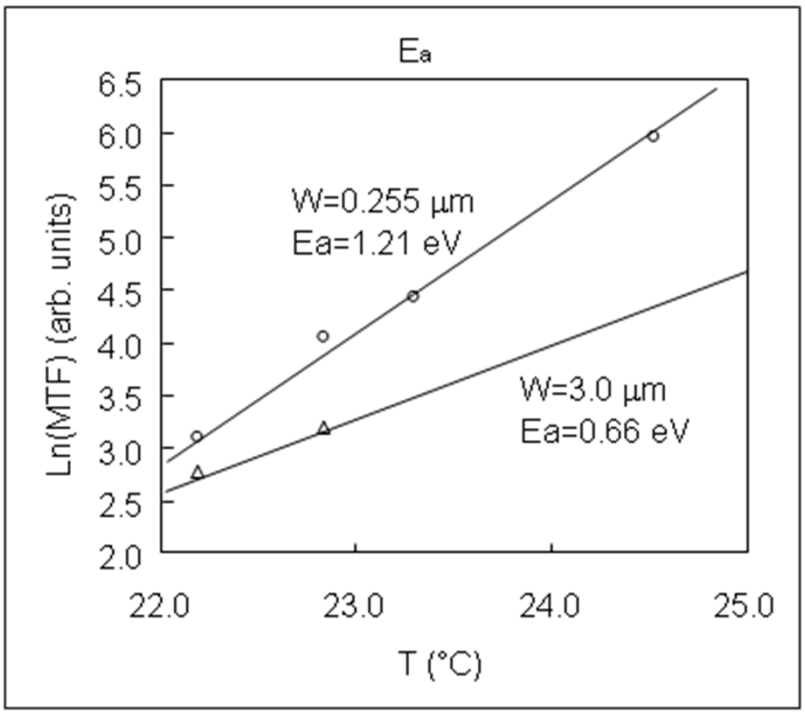
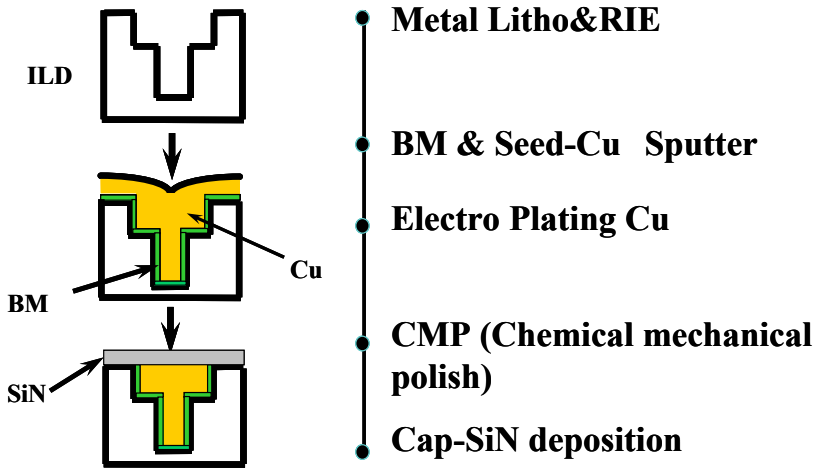


Figure 2-1-5-1 Metal Electromigration Life (Temperature Dependency)

2-1-5-2. Cu Metal Electromigration

With the advances in miniaturization in the silicon process, performance degradation due to increased metal resistance and metal-to-metal capacity has become problematic. To resolve this problem, the Cu metal process has been applied. The Cu metal formation process employs a process called “damascene.” The flow of this process is shown in Figure 2-1-5-2.



* RIE: Reactive Ion Etching, BM: Barrier Metal

Figure 2-1-5-2 Cu Metal Formation Flow (Damascene Process Flow)

In this manner, electromigration failure is a potential failure mechanism for both conventional Al metal and the intrinsically different Cu metal from the standpoints of material and metal formation process. The MTF formula can also be expressed in the same manner as that for the Al metal.

However, because the Cu melting point (1083℃) is higher than the Al melting point (660℃), the Cu metal is believed to exhibit better resistance to electromigration in comparison to the Al metal. Figure 2-1-5-3 shows an example of the results obtained when comparing the differences in electromigration resistance that result from the differences in metal material, using the same design rules for each product. It is evident that the Cu metal exhibits a life that is approximately one digit greater than that of the Al metal at the point of MTF for electromigration failure.

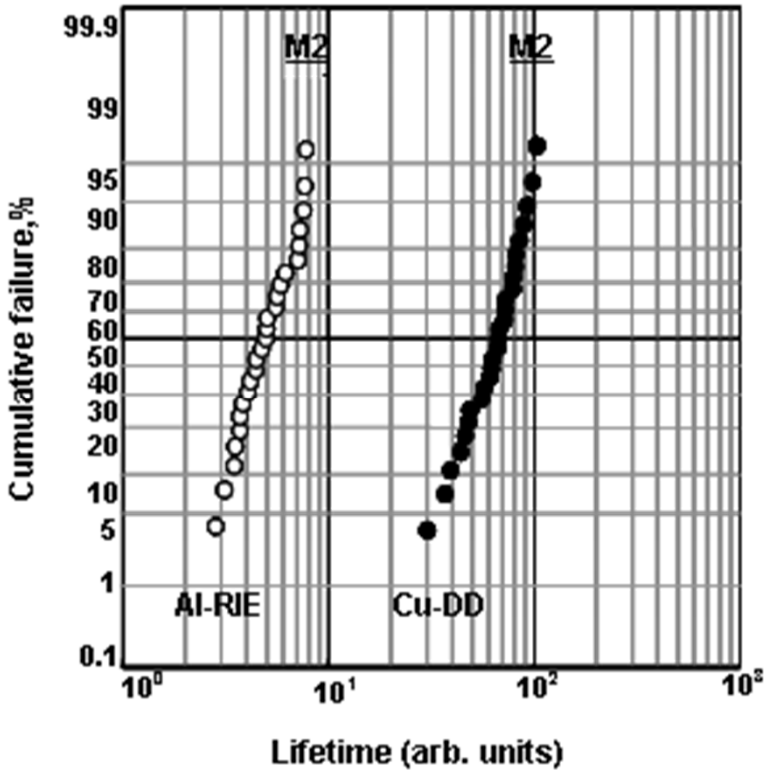


Figure 2-1-5-3 Difference in Al Metal and Cu Metal Electromigration Resistance

The electromigration in Cu metal is characterized by the fact that there are reports indicating that the dominant diffusion route is grain boundary diffusion, like the Al metal, as well as those indicating that it is interface diffusion. A clear explanation of the failure mechanism, therefore, has not yet been concluded. Because Cu metal readily oxidizes, case examples exist in which failure to develop appropriate procedures and optimize conditions in the manufacturing process significantly degraded reliability.

2-1-6. Stress Migration (SM) [21)22)23)]

Stress migration is a failure mechanism where open failures occur simply due to extended exposure to a high-temperature environment. [24)25)] In general, LSI metal is subjected to high-temperature heat treatment during formation of the interlayer insulator after metal formation. Although stress does not occur on the metal during this high-temperature period, stress is generated in the metal after cooling due to the mismatch in thermal expansion coefficients between the metal and interlayer insulator or passivation film. The residual stress and subsequently applied heat cause void generation and diffusion in the metal and, in consequence, metal opens and open faults in vias (through-holes for connections between overlapping geometries on two adjacent routing layers). This event is called stress migration since it is induced by internal stress.

Stress migration countermeasures, such as the addition of Cu to the Al metal, the use of barrier metal under the Al metal, and reducing passivation film stress, are taken to minimize this effect.

Acceleration of stress migration failure due to temperature does not uniformly occur due to a combined mechanism of void diffusion and stress relief. However, the apparent activation energy at 125℃ or below is 0.7 eV for Al-Si and Al-Cu, and 0.9 eV for Al-Si-Cu.

In addition, stress migration tends to occur more readily in processes that use Cu metal in comparison to those that use Al metal since the Cu grain size tends to be smaller than that of Al. This type of stress migration, similar to the Al metal process, can be suppressed by the existence of a barrier metal. However, since structural placement of the barrier metal in the via is not possible, the stress migration that occurs in the via is viewed as problematic.

In general, the via readily becomes the singular point of concentrated mechanical stress, causing voids in the vicinity of the via to readily grow. There are many reported cases of this type of failure. [26)27)28)] Figure 2-1-6-1 shows a case of void observation.

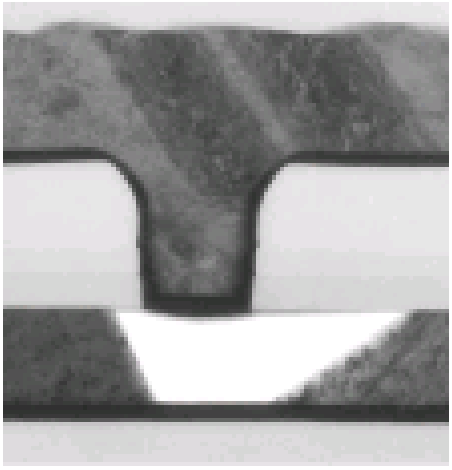


Figure 2-1-6-1 Image of Void that Occurred Under Via in Cu Process

To suppress Cu process stress migration failure, in particular void occurrence and growth, development of a reduced stress process as described for the Al metal process above, application of an interlayer insulator with an expansion coefficient approximate to that of the Cu metal, and use of a barrier metal with a high melting point, such as Ti or Ta, have been confirmed as effective methods.

Countermeasures incorporated at the metal design phase are also effective. It is also possible to suppress void generation by diffusing the stress at locations where stress collects in the metal. For instance, the stress that collects in a via can be alleviated and subsequent stress migration can be suppressed by making the metal volume (metal width and film thickness), which is the void supply source, no larger than necessary or by creating multiple vias in the area of connection with a large surface area metal. [29)]

The speed of progression of stress migration can be expressed by the product of the stress component and diffusion component as follows:

$$R = C \cdot (T_0 - T)^N \cdot \exp\left(-\frac{E_a}{kT}\right)$$

Where, R indicates the speed of stress migration progression, C indicates a coefficient, T_0 indicates the metal formation temperature or interlayer film formation temperature, T indicates the test temperature, N indicates the acceleration coefficient, E_a indicates the activation energy, and k indicates Boltzmann's constant.

Both the stress component and diffusion component depend on test temperature. The stress component increases as the test temperature lowers in comparison with the metal formation temperature, and the diffusion component increases as the test temperature increases. The speed of progression is expressed as the product of these two components, resulting in a peak value at a certain temperature. (Figure 2-1-6-2)

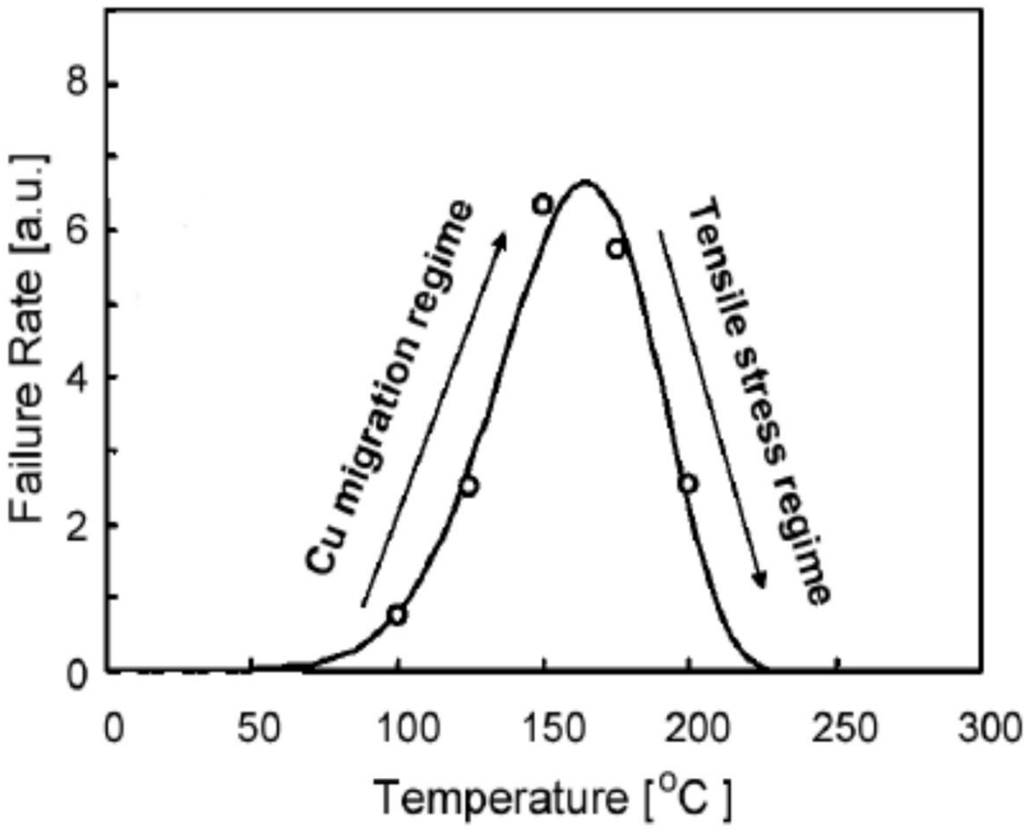


Figure 2-1-6-2 Temperature Dependency in SM Failure Rate

2-1-7. Nonvolatile Memory Failure Mode [30)31)]

Nonvolatile memory (EEPROMs and flash EPROMs) store charge (electrons or holes) in electrically isolated memory cells (floating gates), thereby realizing no data loss even if the power is turned off. Electrical reprogramming operations are performed via a tunnel oxide film. The memory cells are electrically isolated by the formation of a silicon oxide film between the polycrystaline silicon floating gate and substrate silicon, and a polycrystaline oxide film – nitride film – oxide film (ONO) stacked insulating film between the polycrystalline silicon floating gate and control gate. The nonvolatile memory “1” and “0” states are determined by the amount of charge stored in the floating gate. If the insulating film that surrounding the floating gate is defect free, the stored charge will not dissipate at all. If a defect exists in the insulating film or the film degrades, leakage current will flow, causing a change in the charge amount determined by program and erase operations and, consequently, defect detection by the read operation (i.e., when voltage is applied on the control gate).

2-1-7-1. Endurance Failure (Endurance)

Program and erase operations gradually reduce the “1” and “0” read voltage differential, resulting in window closing and operation failure. Causes include oxide charge traps and the interface state charges. With the former, a trap is formed in the tunnel oxide film, capturing electrons and causing degradation of the program speed. With the latter, program/erase cycling increases the density of the interface states, thereby decreasing the read current and causing window closing.

2-1-7-2. Disturb Failure (Disturb）

“Disturb” refers to a change in stored charge due to voltage applied on nodes during memory cell program/erase and read operations.

While in principle this type of failure is possible regardless of operation selection, a representative type is the Read-Disturb failure that occurs during read operations.

A Gate-Disturb failure in particular requires caution since this type of failure introduces a charge simply when gate voltage is applied, and exhibits a maximum disturb time of 10 years. The Gate-Disturb failure prominently appears when program/erase operations are performed repeatedly. The true cause is believed to be the formation of a neutral traps or positive charge traps in the tunnel oxide film due to program/erase cycling operations, as described in Section 2-1-7-3 Retention Failure (Improper Charge Retention), resulting in the conduction of electrons via these traps.

2-1-7-3. Retention Failure (Improper Charge Retention)

Retention time refers to the amount of time until the charge stored in a memory cell either increases or decreases for some reason or other and retention is detected. The main cause of retention failure is leakage of charge through a defect in the film isolating the memory cell. Subsequent defects include neutral traps or positive charge traps formed in the oxide film. These defects have the same origin as SILC described in Section 2-1-2.

The charge stored in a memory cell fluctuates due to the effects of the following:

1) Natural attenuation

2) Charge loss or charge injection associated with material or geometric structural defects

3) Charge migration associated with circuit design

Regularly observed charge loss and charge injection events include events such as the following:

a) The event occurs due to defects in the oxide film or insulating film between the polycrystaline silicon, often resulting in a random 1-bit failure.

b) The stored charges are lost by ionizable contamination, normally resulting in a cluster bits failure.

c) Holes generated from a drain avalanche breakdown are trapped, causing the event and resulting in a single bit failure.

d) The event occurs due to the dissipation of electrons through a defect-less section of the oxide film or insulating film between the polycrystaline silicon, resulting in slow leakage over an extremely long period of time.

Items a) and b) are normally checked and eliminated using the voltage acceleration and temperature acceleration methods.

Item c) is prevented by source/drain junction profile design.

And item d) results in an intrinsic retention life exceeding 100 years since the leakage is one electron or less per day.

Ionic contamination is observed under high temperature environments and is presumably caused by a positively charged alkali ion (Na+ or K+) or water or H+.

Program /erase cycling sometimes results in further degradation of retention characteristics and Gate-Disturb resistance. In particular, when the tunnel oxide film thickness is 8 nm or less:

e) Charge loss and charge injection failure caused by low electric field leakage due to SILC readily occur.

This leakage is believed to occur due to electron conduction via charged traps (hole trap or neutral trap). Because this is mainly determined by tunneling probability, the activation energy is low, necessitating caution during screening by the high-temperature test.

Figure 2-1-7-1 shows the flash memory cell structure and improper retention failure, and Figure 2-1-7-2 shows the band structure and leakage path in response to the representative improper retention modes a) to e).

Mainly to prevent single bit failures, actual LSIs apply redundancy and error correction circuits when mounting larger-scale nonvolatile memories.

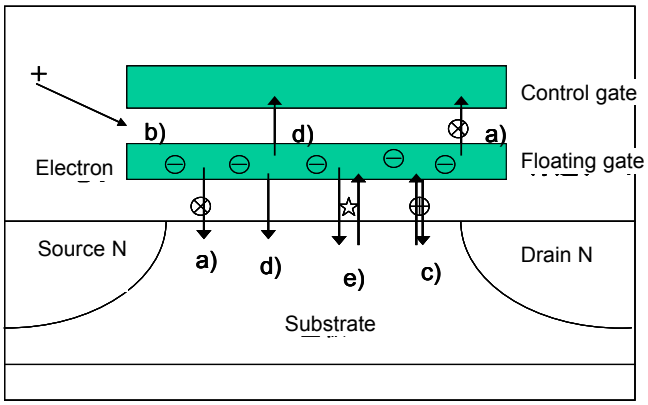


Figure 2-1-7-1 Flash Memory Cell Structure and Improper Retention

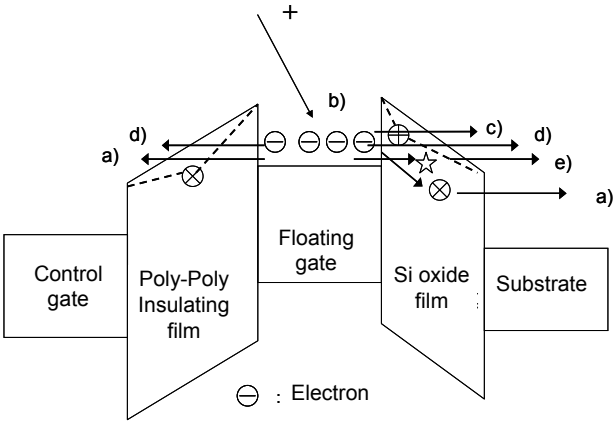


Figure 2-1-7-2 Band Structure and Leakage Path

2-1-8. Other (Alloy Spikes, Metal Corrosion by Ion Contamination, Polarization, Parasitic MOS, Pinholes, and Cracks)

2-1-8-1. Alloy Spikes

The primary metallization material for semiconductor products is Al. Al has low electrical resistance compared to other materials, resulting in superior adherence to insulating materials such as silicon oxide film. Nevertheless, high-temperature treatment can cause the silicon in the silicon substrate to flow into the Al film and damage the junction in the area of the contact. This failure is referred to as an alloy spike. Alloy spikes cause breakdown voltage degradation and shorts, especially in shallow junctions.

Countermeasures include adding silicon to the Al, and forming a barrier metal between the Al and silicon.

2-1-8-2. Ion Contamination

Contamination from Na+ and other external ions introduced into passivation or into the interface during the manufacturing process greatly affects device reliability. [32)]

The Na+ ions introduced in the manufacturing process are deactivated by phosphide gettering. However, an applied electrical field can cause them to move into the passivation oxide film and collect in the field region, gate region or near the PN junction, resulting in failures due to parasitic MOS, Vth change, breakdown voltage degradation, etc.

Breakdown voltage degradation is characterized by the fact that recovery is achieved by baking without bias, similar to breakdown voltage from the above-described crystalline defects. Factors which accelerate degradation due to ion contamination include the strength of the electrical field applied, temperature as well as humidity.

For ion contamination, a protective film with ion-blocking capability such as phosphosilicate glass (PSG) is used. For external contamination, a film with an even superior ion-blocking effect such as a silicon nitride film is used for top passivation.

2-1-8-3. Polarization

PSG provides an ion gettering effect as previously mentioned. On the other hand, increased phosphorous content causes polarization, resulting in various types of instability and degradation [33)]

2-1-8-4. Parasitic MOS

As shown in Fig. 2-1-8-1, if the SiO2 surface becomes conductive, the electrode potential extends in a lateral direction to the adjacent PN junction, forming parasitic MOS due to the inversion of the field region.

Although measures against this type of failure mechanism are implemented from aspects of the design and manufacturing process, there is still a small chance that the problem will occur, depending on the humidity and ionic contamination in the external operating environment.

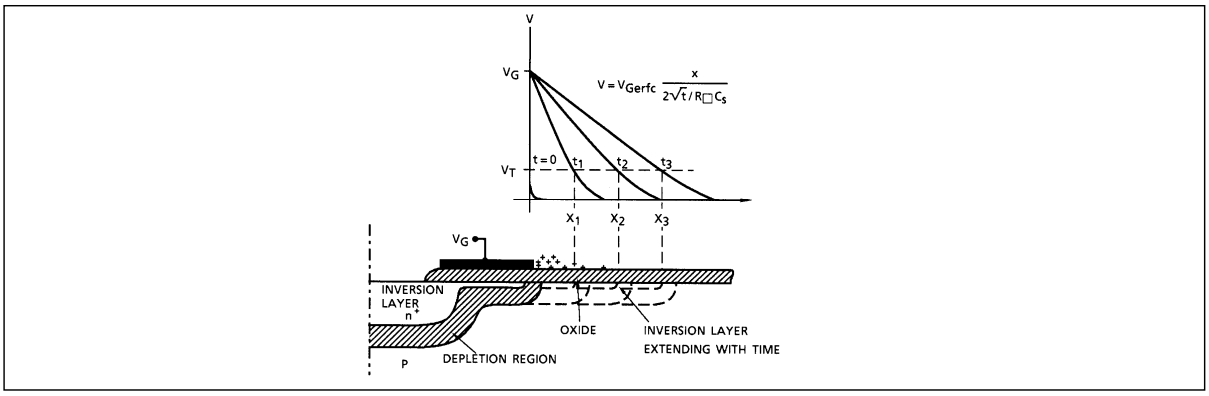


Figure 2-1-8-1 Extended Charge in Lateral Direction Model [34)]

2-1-8-5. Pinholes and Cracks

If passivations include defects such as pinholes or cracks, interlayer shorts can occur in multilayered metallization. Also, moisture, Na+ ions and/or other contaminants can enter in top passivation via the said defects, causing device operation instability, degradation or Al metal corrosion as previously described. Cracks can be formed by thermal stress in the manufacturing process or by mold distortion. The effects of mold distortion cannot be ignored, particularly with the increasing level of miniaturization and scaling in integrated circuits.

2-2. Assembly Process

Table 2-2 lists the main reliability failures of the assembly process.

Table 2-2 Main Reliability Failures of the Assembly Process

Process Elements	Reliability Failure Modes	Failure Mechanisms
Poor Wire Bonding	Bonding Strength Degradation, Resistance Increase	A crack-like nest is formed by the alloy of the wire electrode (purple plague), which causes strength degradation.
	Wire Breakage, Wire Contacts	In resin sealed products, there is wire fatigue breakage due to application of thermal cycle stress, and contact due to wire deformation during resin sealing.
Wiring Corrosion	Resistance Increase and Breakage due to Al Wiring Corrosion	Corrosion of wiring due to moisture invasion from outside and impurity ions in the resin.
Failure due to Sealing Resin	Characteristics Variation, Al Slides, Passivation Cracks	Characteristics Variation due to Resin Stress, Al Slides, Passivation Cracks
	Passivation Cracks	Cracks generated on the die surface due to mechanical stress such as temperature cycling of the resin filler
Poor Mounting Stress	Mounting Failure and Degradation of Moisture Resistance due to Package Cracks and Package Deformation	Due to heat at the time of mounting, the internal water vapor pressure of the moisture absorbed resin rises, the adhesion between resin and die/substrate/frame deteriorates, and package swelling and cracking occurs.
Ag Migration	Shorts Between Leads	Shorts Between Leads due to Migration of Ag within Plating
Whisker	Shorts Between Leads	Shorts Between Leads due to Whisker Growth of Sn within Plating

2-2-1. Wire Bonding Failures

There are two bonding methods used to connect the leads to the semiconductor chip electrode area: thermal compression and ultrasonic.

The following describes the bonding process and the failure mechanisms related to bonding wire.

(1) Au-Al Alloying

When bonding Au wire to Al or Al wire to Au film and subjecting the bonding area to high temperature, a formation of purple alloy ($AuAl_2$) is often observed.

This alloy is referred to as “purple plague.” In contrast, Au_2Al which readily occurs when the proportion of Au is high, has higher electrical resistance and is mechanically weaker than $AuAl_2$ and is referred to as the “white plague.”

Since Au and Al have different diffusion constants, voids accumulate depending on the change in volume of the generated compound, forming nests (cracks) where there is a high concentration of Al, resulting in bonding strength degradation and increased resistance. Bonding degradation will lead to ball peeling, temporary ball peeling during operation at high temperatures or opens due to the stress that occurs from vibration and the difference in molded resin and wire thermal expansion coefficients. However, such degradation can be considered virtually unproblematic if the heating process is properly controlled during the manufacturing process.

(2) Mechanical Stress

With resin-encapsulated products, thermal cyclic stress can cause additional mechanical stress on wires due to the difference between the thermal expansion coefficients of the resin and wire, resulting in an open wire due to wire fatigue. Also, wire deformation during molding can cause wires to come in contact with each other or with the edge of the chip under high temperatures, resulting in an electrical short. Countermeasures for this include process optimization and automation.

In hermetically sealed products, wires formed in a loop shape in the interior can open due to shock or vibration. This should be taken into account, especially when the semiconductor product is subjected to ultrasonic cleaning. Furthermore, mechanical damage during bonding can, in some cases, cause secondary product failure. However, this can be counteracted by optimization and/or automation of the manufacturing process.

2-2-2. Metal Corrosion

Al metal corrosion is a critical problem for reliability in resin-encapsulated devices. Some cases have also been reported for hermetically sealed devices as well. [35] The following provides a brief description of the Al corrosion mechanism in resin-encapsulated devices.

(1) General Model of Al Corrosion

Figure 2-2-2-1 shows a diagram of a resin-encapsulated device. In general, plastic materials have moisture permeability and absorption properties by their very nature. Here, “permeability” refers to the ease of water passage, and “absorption properties” refers to the ability to absorb moisture.

Resin has various kinds of ionic impurities that are introduced during the manufacturing processes. When the resin absorbs moisture, the ionic impurities are eluted and reach the internal chip surface. Depending on the size of the bias applied to fulfill the operational function of the device, positive or negative ions and moisture reach the Al metal surface by passing through micro-defects in the passivation film, thereby resulting in Al electrochemical reaction.

The result is a fatal failure such as an increase in Al metal resistance or an open. This is the general mechanism of Al metal corrosion failure.

(2) Moisture Penetration Route

The primary cause of Al metal corrosion is the intrusion of external moisture. Moisture is defined as water vapor in the atmosphere. There are two penetration routes as shown in Figure 2-2-2-1. One is through the gaps in the interface of the lead frame and resin, and the other is through the bulk and is dependent on the moisture permeability and absorption properties of the resin.

It is difficult to theorize which of these routes is more dominant since they depend on factors such as operating environment conditions and package type. Based on experimental data obtained through investigations using a moisture-sensitive chip encapsulated in a resin package, moisture penetration through the bulk can be approximated by a diffusion model. [36]

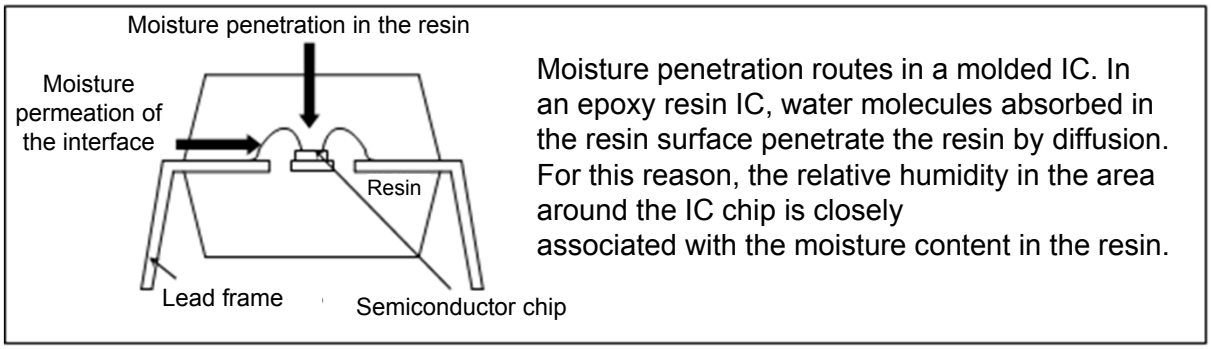


Figure 2-2-2-1 Schematic Diagram of Resin-Encapsulated Device

(3) Dependence on Applied Bias

As a result of temperature and humidity tests conducted under acceleration conditions of 80℃, 90% RH for a PSG passivation product with bias voltage varied at 5 V, 10 V, 15 V, 20 V and 25 V, dependence of Mean Time To Failure (MTTF) on applied voltage was obtained as shown in Figure 2-2-2-2. From the figure, it is apparent that the MTTF decreases with increased bias voltage.

Al corrosion that results from electrochemical reaction has different corrosion modes depending on bias polarity. This means that the failure mechanism varies with the polarity. The biased wiring with the relatively higher potential is called the anode, and that with the lower potential is called the cathode. Al corrosion occurring on the anode and cathode sides is referred to as anodic corrosion and cathodic corrosion, respectively.

Cathodic corrosion is predominant with the Al and Al-Si metals generally used, but cracks or pinholes in the passivation can cause anodic corrosion due to impurity ions (such as Cl^-).

Cathodic corrosion normally occurs in the crystal grain boundary of the Al film and appears dark when observed through an optical microscope. On the other hand, anodic corrosion is accompanied by a significant expansion of Al, sometimes causing cracks in the passivation which can propagate. In some instances, it appears as if Al is missing when the device is observed under an optical microscope. However, it sometimes remains as transparent Al_2O_3 based on analyses using electron probe micro analyzer (EPMA) or Auger electron spectroscopy (AES).

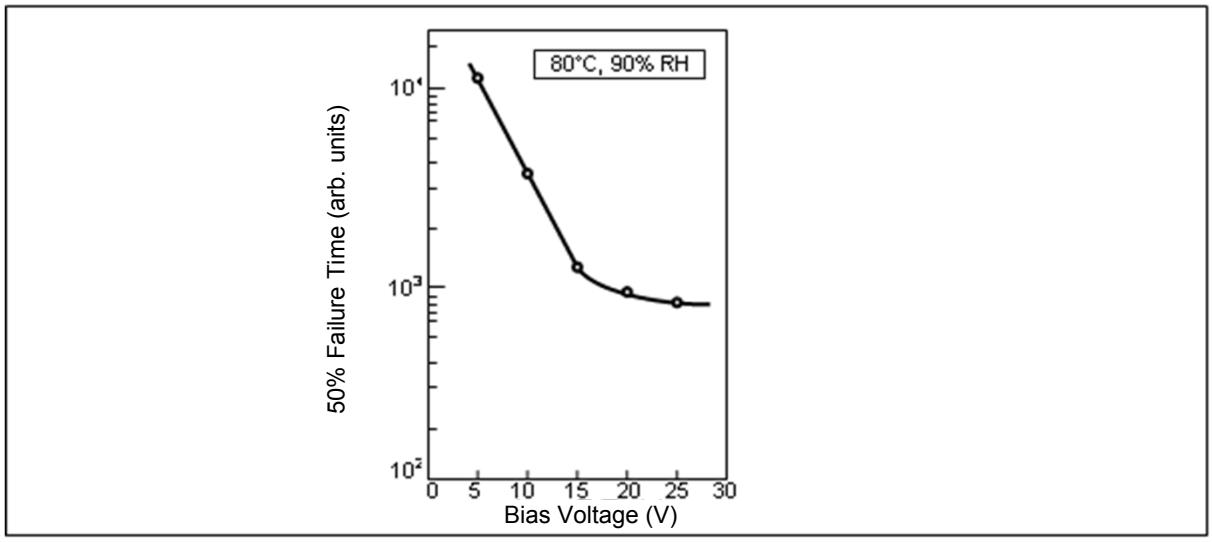


Figure 2-2-2-2 Dependency on Voltage in Humidity Resistance Acceleration Test

(4) Dependence of PSG Passivation on Phosphorous Concentration

It was previously described how the use of PSG film containing phosphorous is used in top passivation in order to subject the external ions to the gettering effect. However, an excessively high phosphorous concentration will significantly increase the potential for fatal Al metal corrosion. Phosphorous related corrosion is cathodic for Al or Al-Si metal and occurs as follows: [37)38)]

First, when PSG absorbs moisture, P_2O_5 in the PSG is eluted to form phosphoric acid, increasing the H+ ion concentration. As a result, H+ ions are attracted to the surface of the Al metal on the cathode side, allowing corrosion to progress according to the following reactions:

$$Al + 3H^{+} \rightarrow Al^{3+} + 3/2H_2\uparrow$$
$$Al^{3} + 3OH^{-} \rightarrow Al(OH)_3$$
$$Al(OH)_3 + OH^{-} \rightarrow AlO_2^{-} + 2H_2O$$

Figure 2-2-2-3 shows the relative life values versus phosphorous density in PSG which causes cathodic corrosion for Test Element Groups (TEGs) and LSIs. The figure shows that the life shift is sensitive to changes in phosphorous concentration.

Recently, however, the use of moisture resistant film (such as SiN) in top passivation to improve moisture resistance is eliminating this type of failure.

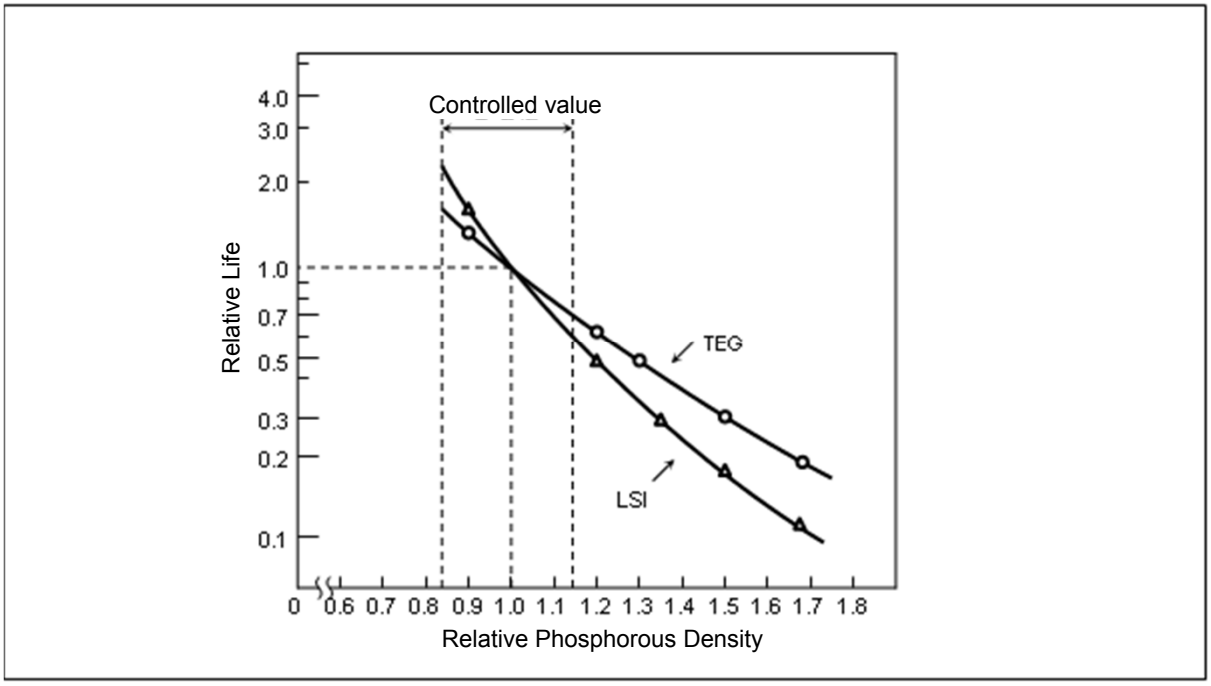


Figure 2-2-2-3 Dependence of Relative Life on Phosphorous Density Due to Al Metal Corrosion (Experimentally Controlled Example)

(5) Other Unexpected Events

In addition to the above items, factors contributing to Al corrosion include some that are attributable to the manufacturing process, such as seal leaks in hermetically sealed devices, contamination, and flaws in passivation due to improper handling; and those contributable to customers, such as contamination during handling, penetration of flux (including Cl) during soldering, and penetration of contaminants through the resin and lead interface, causing corrosion of internal metal when moisture condenses.

2-2-3. Failure due to Resin Encapsulation

(1) Ionic Impurities in Resin

As described previously, with resin-encapsulated devices, instability in and degradation of product operation or fatal Al corrosion can occur due to ionic impurities in the resin material. As a result, encapsulation must be performed using resin that contains a minimal level of ionic impurities so as to improve moisture resistance. Ionic impurities in the resin are evaluated using the hot water extraction method. Of the various ionic impurities, Cl- ion is thought to especially have a pronounced effect on moisture resistance.

The following are the results of an experiment conducted at Toshiba to determine the correlation between device instability and Al corrosion caused by ionic substances in the resin. [14] As already mentioned, formation of a parasitic MOS due to the accumulation of ions is one of the typical mechanisms of device degradation caused by ionic impurities in the resin. Utilizing this phenomenon, it is possible to evaluate the ionic substance in the resin by the ion accumulation rates on the gate oxide film, as shown in Figure 2-2-3-1. This is done by applying bias at high temperature to an ion-sensitive TEG device after it has been encapsulated by resin.

The ion accumulation model can be explained by the transient phenomenon model shown in Figure 2-2-3-1 (c). This model is based on the bulk resistivity ρv (or bulk resistance Rr), which is the reciprocal of the bulk conductivity, which in turn is proportional to the concentration of ionic impurities in the resin multiplied by the ionic charge multiplied by the ion mobility. The model also includes the resin-SiO2 interface resistance R_Γ and the oxide film's equivalent capacitance C_{ox}.

In this model, the potential of the oxide film surface (equivalent gate voltage V_G*) when $R_\Gamma >> Rr$ can be approximated by the expression:

$$V_G^* \approx V_A\left(1 - e^{-\frac{t}{\tau}}\right)$$

where V_A is the saturated value of V_G*, and τ equals $C_{ox}^* \cdot Rr$, a time constant dependent on the bulk resistance of the resin.

From the above, the corresponding relationship between Rr or ρv and τ is evident. The smaller the ρv or Rr, the larger the ion conductivity and, consequently, the greater the number of ions which reach the surface. This type of resin leads easily to unstable device operation and Al corrosion.

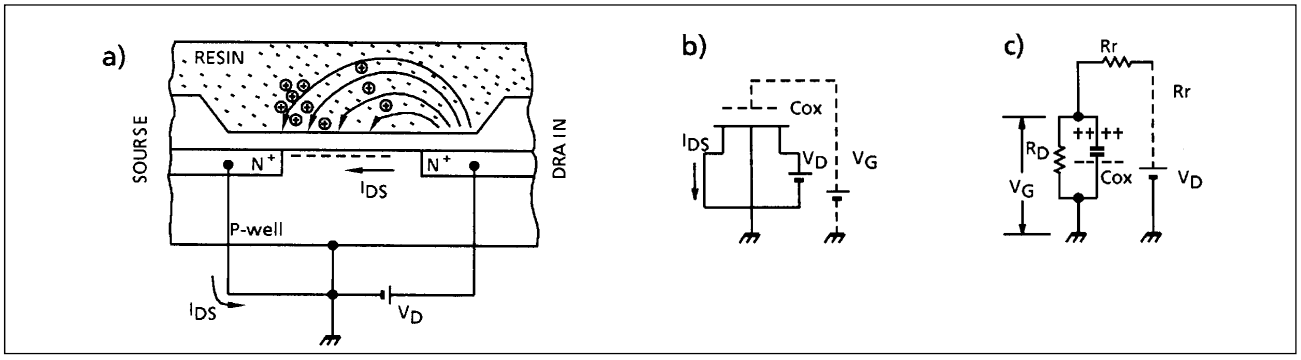


Figure 2-2-3-1 Charge Accumulation Model of Spacer Structure

Figure 2-2-3-2 shows the correlation of the above-described τ and the rate of Al metal corrosion. Al metal corrosion diminishes as τ becomes larger.

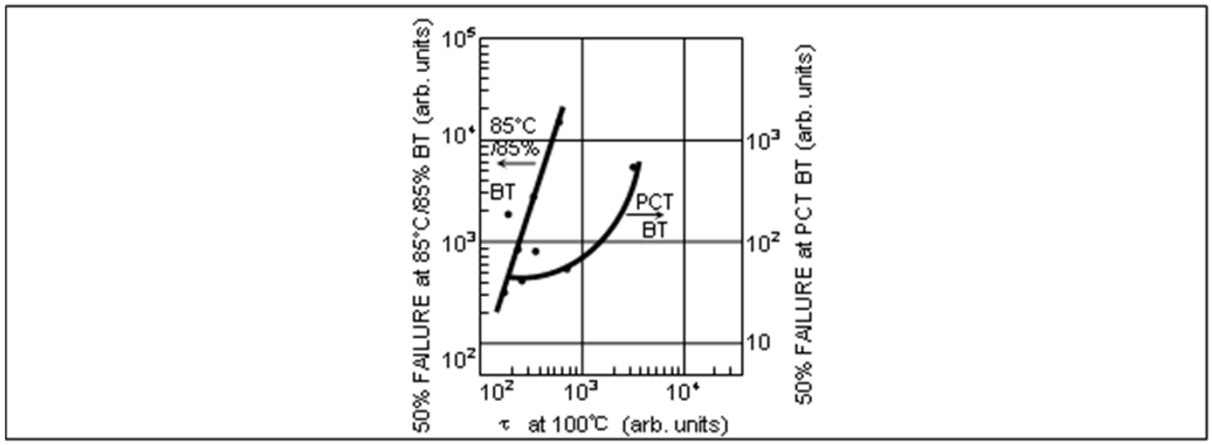


Figure 2-2-3-2 Correlation between Time Constant τ and Al Corrosion at High Temperature

Figure 2-2-3-3 shows the temperature dependency of τ. The activation energy is approximately 0.9 to 1 eV, which conforms to the temperature dependency of bulk resistance of resin shown in Figure 2-2-3-4.

Figure 2-2-3-5 shows the degradation of bulk resistance due to moisture absorption. The figure indicates that bulk resistance degrades as an exponential function of moisture absorption.

From the above, it can be said that high-temperature bulk resistance of resin and bulk resistance degradation by temperature and humidity are the important parameters in expressing resin reliability.

In addition, adhesion with the metal or chip surface, moisture permeability and moisture absorption are also factors that affect moisture resistance of resin-encapsulated products. The epoxy resin used in resin-encapsulated products is a controlled resin featuring low stress, high absorption, and minimal impurities.

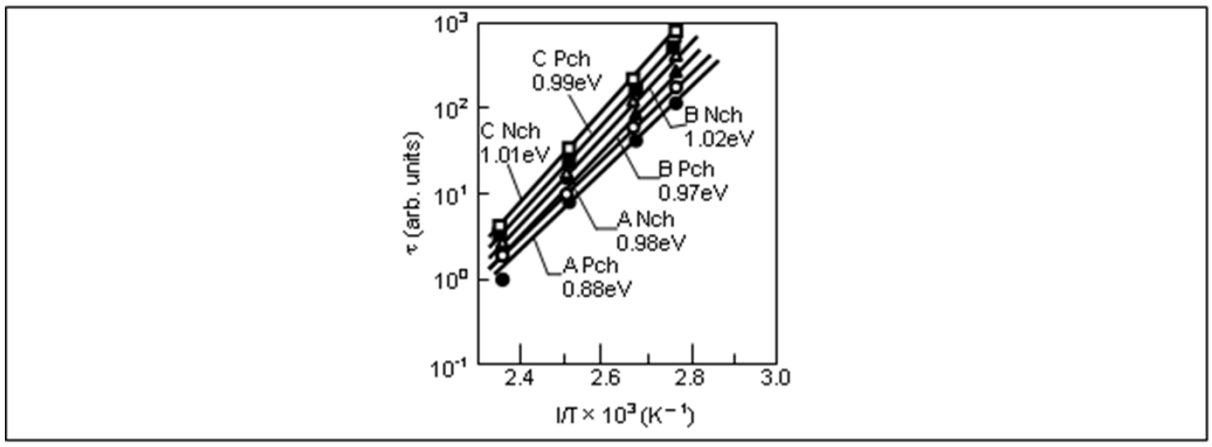


Figure 2-2-3-3 Temperature Dependency of Time Constant τ

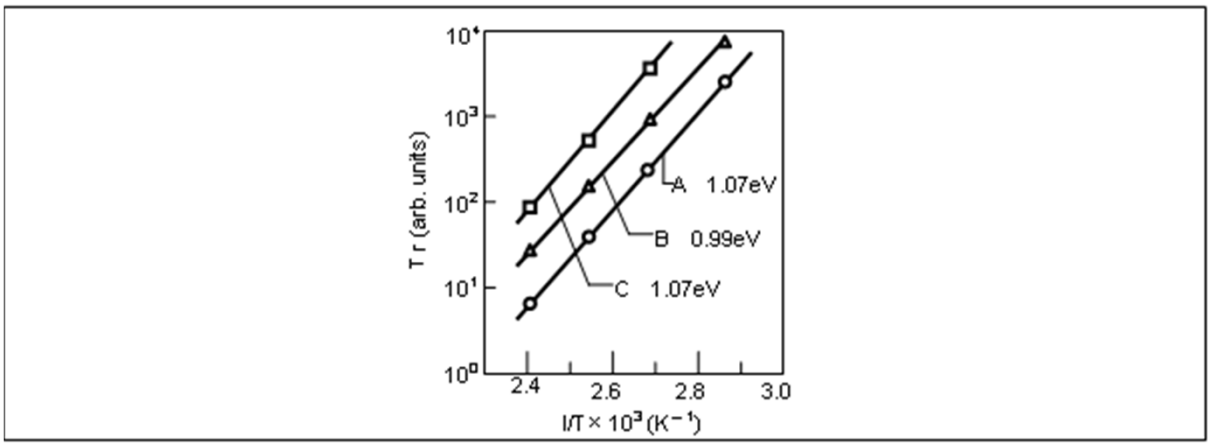


Figure 2-2-3-4 Temperature Dependency of Resin on Bulk Resistance

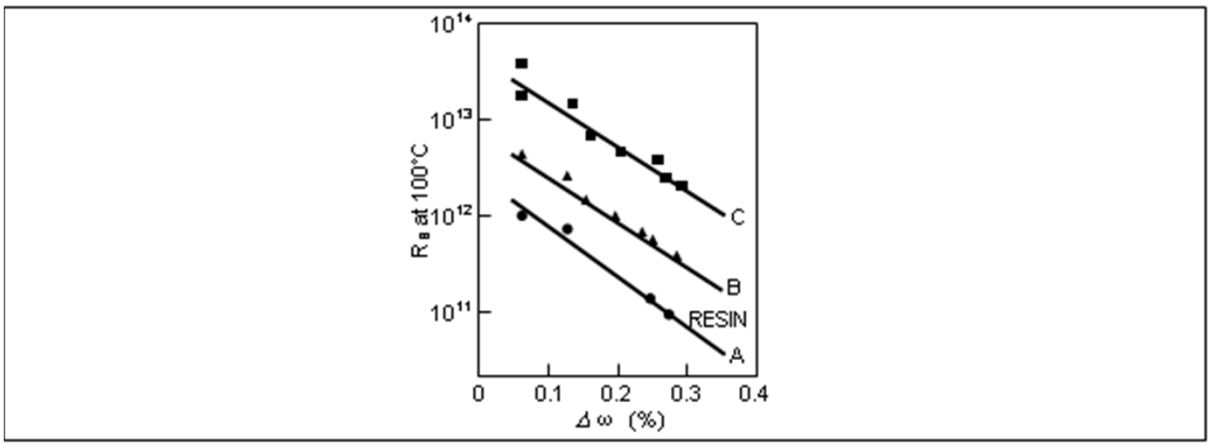


Figure 2-2-3-5 Dependency of Bulk Resistance on Humidity Absorption

(2) Various Problems Caused by Mold Distortion

Resin used for semiconductor encapsulation contracts as a result of resin polymerization, applying a significant amount of stress to the semiconductor chip in contact with the resin. Consequently, resistance values of the device resistor fluctuate due to a piezo-resistance effect, greatly affecting device characteristics. Stress also causes Al slide and passivation cracks.

A Toshiba experiment to determine the stress generated in a resin-encapsulated silicon chip is discussed below. [39)]

Stress is measured on TEG devices which have resistors constructed on the silicon chip. A general formula for the piezo-resistance effect is:

$$\delta\rho_i = \left(\frac{\Delta R}{R}\right)_i = \sum_{i=1}^{6} \pi'_{ij} \cdot \tau_j$$

where $\delta\rho_i$ is the resistance change rate, π'_{ij} is the piezo-resistance coefficient, and τ_j is the stress. For τ_j, the following formula is used:

$\tau_1 = \sigma_x$, $\tau_2 = \sigma_y$, $\tau_3 = \sigma_z$

$\tau_4 = \sigma_{yz}$, $\tau_5 = \sigma_{zx}$, $\tau_6 = \sigma_{xy}$

Since a silicon chip is extremely thin, it can be assumed that σ_x, $\sigma_y >> \sigma_z$. In addition, the piezo-resistance coefficient π'_{ij} is the tensor of the fourth order determined by the semiconductor conductivity type, crystal orientation, resistor direction and impurities present. The value of π'_{ij} can be found by applying a given stress for which these parameters are known to the TEG devices.

The stress is determined as follows:

$$\sigma_x = \frac{1}{2} + \left(\frac{1}{A} + \frac{1}{B}\right)\delta\rho_1 + \frac{1}{2}\left(\frac{1}{A} - \frac{1}{B}\right)\delta\rho_3$$

$$\sigma_y = \frac{1}{2} + \left(\frac{1}{A} - \frac{1}{B}\right)\delta\rho_1 + \frac{1}{2}\left(\frac{1}{A} + \frac{1}{B}\right)\delta\rho_3$$

$$\tau_{xy} = \frac{1}{C}(\delta\rho_2 - \delta\rho_4)$$

where coefficients A, B and C are as shown in Table 2-2-3-6.

Table 2-2-3-6 Coefficients Used in Stress Measurement [39)]

Coefficient / Orientation	A	B	C
100	$\pi_{11} + \pi_{12}$	$-\pi_{44}$	$-2\ (\pi_{11}-\pi_{12})$
111	$\pi'_{11} + \pi'_{12}$	$-\pi'_{11} + \pi'_{12}$	$-2\ (\pi'_{11}-\pi'_{12})$

Table 2-2-3-7 shows the stress measurement results when a TEG device with a chip size of 3 mm square is encapsulated in a 16-pin DIP package. Stress is found for the chip while it is in wafer form. Internal chip stress is found to be non-uniform, larger in a longitudinal direction at the center, and different at the center and periphery.

Table 2-2-3-7 Measured Mean Stress Using {100} P-Type Resistors [41)] Unit: N/cm^2

Location / Process		Mount	Mold	Cure 2h
a Center	σ_x	-4312	-11760	-16072
	σ_y	-5292	-16366	-22050
	t_{xy}	107.8	-58.8	39.2
b Periphery	σ_x	-4018	-6076	-11564
	σ_y	-5880	-7154	-13524
	t_{xy}	245	1479.8	1783.6

Figure 2-2-3-8 shows the TEG device used to find the distribution of internal chip stress. Resisters arranged in the three directions shown in (b) are treated as a unit, with 55 units to a chip.

Figure 2-2-3-9 shows the distribution of stresses σ_x, σ_y and τ_{xy} after encapsulation. These experimental results are fed back to the design section. [40)]

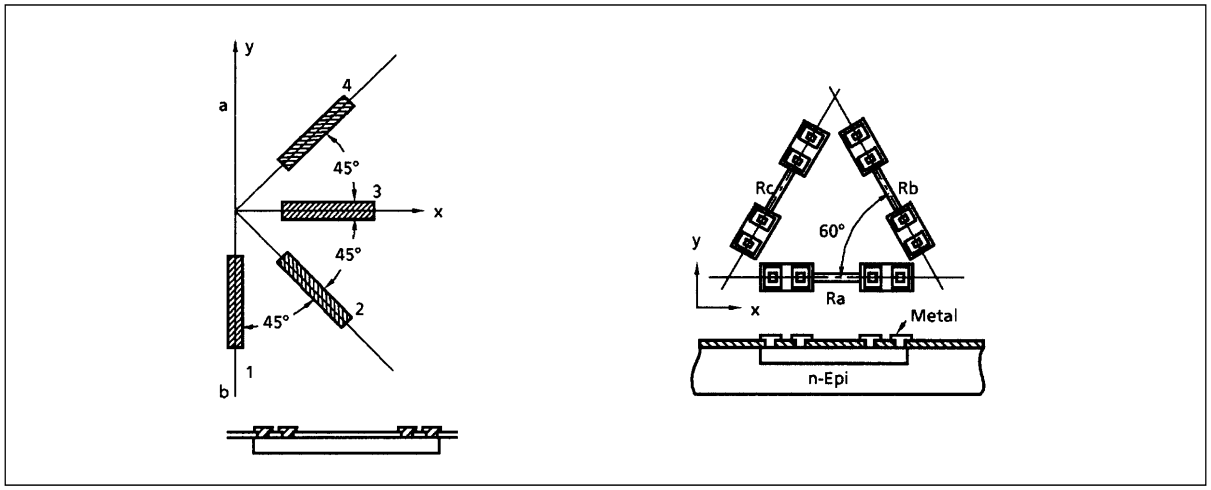


Figure 2-2-3-8 Structure of Resistor TEG [41)42)]

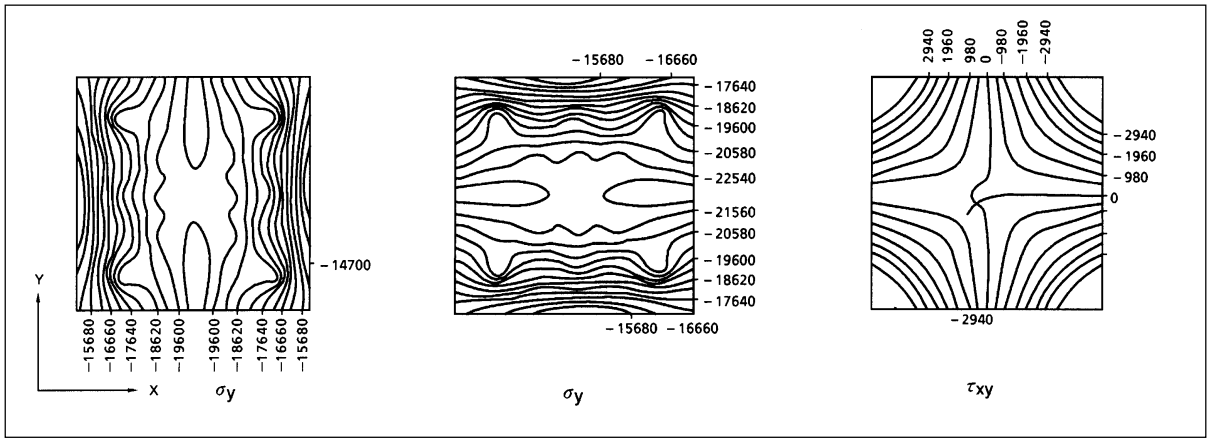


Figure 2-2-3-9 Stress Distribution after Encapsulation [41)]

(3) Top Passivation Crack Caused by Fillers in Mold Resin [42)]

Mold resins contain SiO_2 fillers. When these fillers exist in the interface between the chip and resin as inclusion, cracks can form in the passivation due to the mechanical stress indirectly produced by TCT and other factors, causing the Al beneath the crack to deform and the crack to extend to the interlayer film beneath the Al.

This can form a leakage path in the crack and cause a leak between the Al and the Poly-Si beneath the Al, resulting in device failure. A countermeasure is to apply a polyimide coating to the chip surface.

2-2-4. Mounting Failure

Resin-encapsulated packages are fabricated in various shapes since they are easily formed. Consequently, a wide variety of surface-mount products have been developed to increase the IC density on circuit boards. Compared to board-insertion type packages such as Dual Inline Packages (DIPs) and Single Inline Packages (SIPs), Surface Mounted Devices (SMDs) are prone to package cracks and degradation of moisture resistance since the resin may be exposed to direct heat during mounting. Recently, the trend towards using thin packages and increased chip size make surface-mounted devices even more susceptible to thermal stress during soldering.

In addition, with the development of lead-free products, the upper temperature limit for most packages has increased from 240 to 260℃. If this limit cannot be met by current resin, change to a resin with high adhesion properties must be considered.

The reliability of SMDs is sometimes determined by the soldering conditions. Thus, when products are mounted, moisture absorption control and soldering conditions must be carefully studied and considered. The following is a discussion of the soldering heat related package cracking mechanism.

2-2-4-1. Package Moisture Absorption and Moisture Removal Characteristics

Resin used for resin-encapsulated semiconductor products is basically porous and exhibits moisture permeability. For this reason, SMDs comprising especially thin resin can pose a significant reliability problem. This can occur during soldering when moisture, absorbed in the package, evaporates with a sudden rise in package temperature, causing the package itself to expand or the interface to peel away and gaps to form between the lead frame and resin.

In consequence, there is a close relationship between the amount of moisture absorbed by the SMD package and its reliability after soldering. The following discusses moisture absorption and moisture removal in an SMD.

(1) Moisture Absorption

Figure 2-2-4-1 shows the moisture absorption characteristics of a 256-pin LQFP (resin thickness: 1.4 mm) in each shelf environment (temperature, relative humidity). The horizontal axis indicates the time the semiconductor product remains on the shelf, and the vertical axis indicates the rate of change in the amount of moisture absorbed. The rate of change in moisture absorption is indicated as a percentage value found by dividing the amount of moisture absorbed by the weight of the package before the product was left on the shelf.

From this diagram, it is evident that when the temperature is low, more time is required for the saturation region to be reached; and when the relative humidity is low, the amount of moisture absorbed at saturation is smaller. Figure 2-2-4-2 shows comparative data for the moisture absorption characteristics of a 100-pin QFP (resin thickness: 2.7 mm) and a 20-pin SSOP (resin thickness: 1.2 mm) in a shelf environment at a temperature of 85℃ and a relative humidity of 85% RH, using identical encapsulating resin.

As understood by the diagram, the time to saturated moisture absorption varies with package size. When a soldering heat test is conducted with actual products, the produces undergo a moisture absorption process prior to testing and each package is evaluated with a different moisture absorption time.

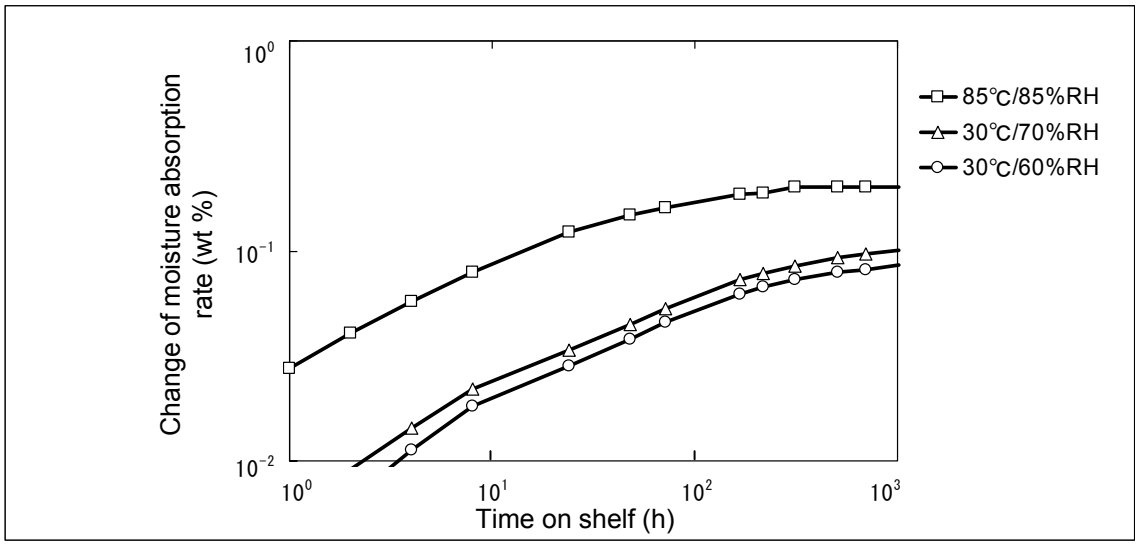


Figure 2-2-4-1. Moisture Absorption Characteristics of 256-Pin LQFPs (1.4 mm Thick) in Various Environments

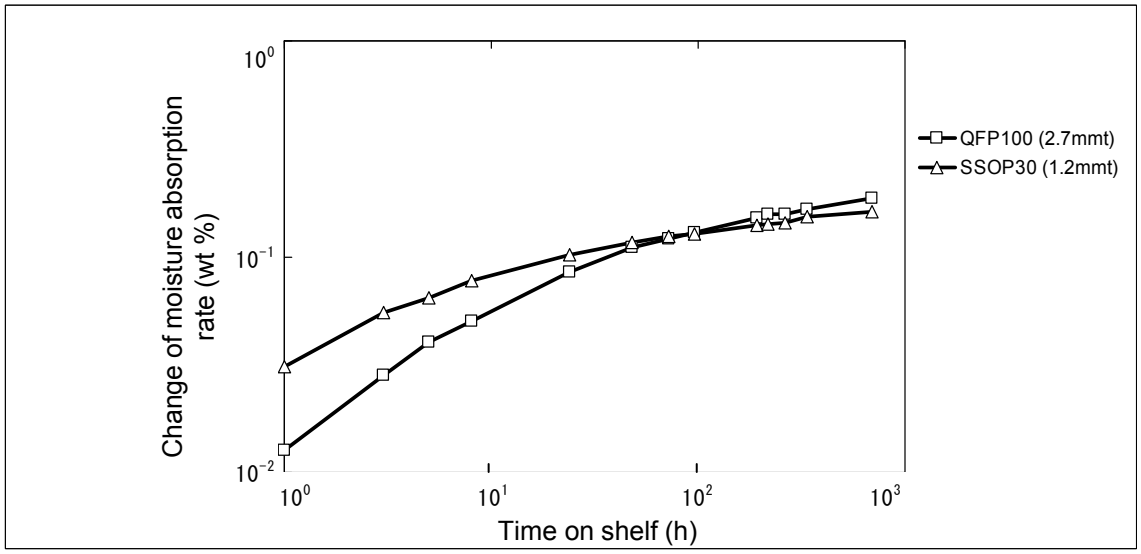


Figure 2-2-4-2. Package Moisture Absorption Characteristic Comparison at 85℃, 85% RH

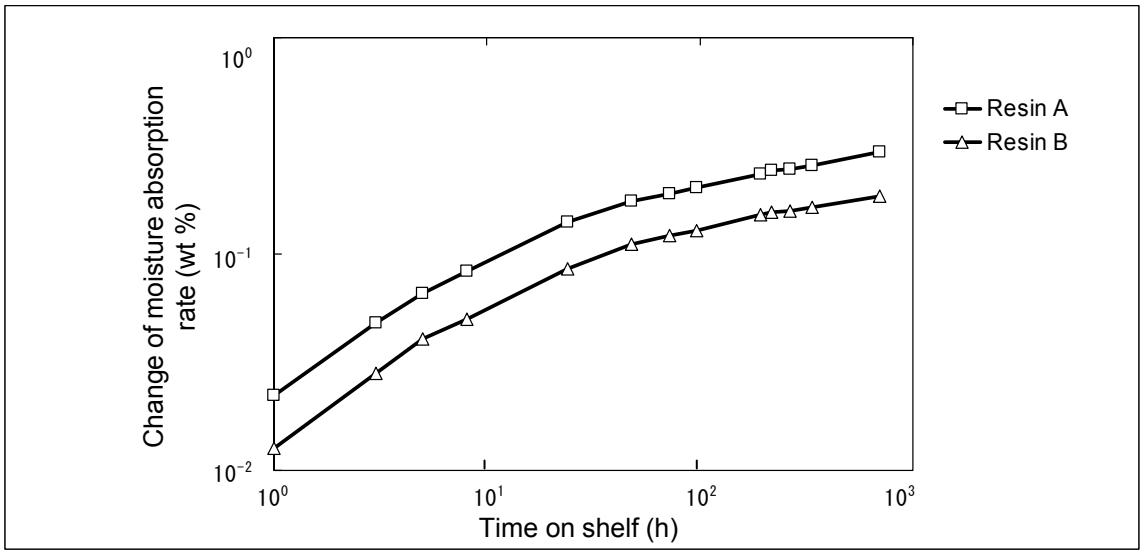


Figure 2-2-4-3. Package Moisture Absorption Characteristic Comparison at 85℃, 85% RH

Figure 2-2-4-3 shows comparative data for the moisture absorption characteristics of a 100-pin QFP (resin thickness: 2.7 mm) in a shelf environment at a temperature of 85℃ and a relative humidity of 85% RH, using different encapsulating resin. From the diagram it is evident that resin developed with minimal moisture absorption is used for some packages to improve heat resistance.

(2) Moisture Removal

Products with a large package or chip size, or those housed in a thin package, are subject to restrictions with respect to their soldering mount methods. As previously described, this is because the moisture in the package causes abnormalities in the package's outer appearance when soldering during mounting. To prevent this problem, the semiconductor product must be baked to remove the moisture from inside the package before it is soldered to the board.

Figure 2-2-4-4 shows the moisture removal characteristics for a 256-pin LQFP (resin thickness: 1.4 mm) in a shelf environment. The horizontal axis is the time the semiconductor product is left on the shelf, and the vertical axis is the rate of change of residual moisture content in the package, expressed as wt%.

The diagram shows that even a package that has become saturated with absorbed moisture can have virtually all moisture removed by backing at 125℃ for about 20 hours. Moisture removal characteristics are such that the higher the temperature, the less time required for moisture removal, with residual moisture after baking approaching 0. However, note that when removing moisture from products, the baking temperature is subject to restrictions depending on the thermal resistance of the tray and the product terminal soldering properties. Before moisture removal (baking), refer to the instructions on the product packaging material or contact the manufacturer.

Note that heat resistant trays are marked “HEAT PROOF,” meaning that they can normally resist temperatures of up to 125℃.

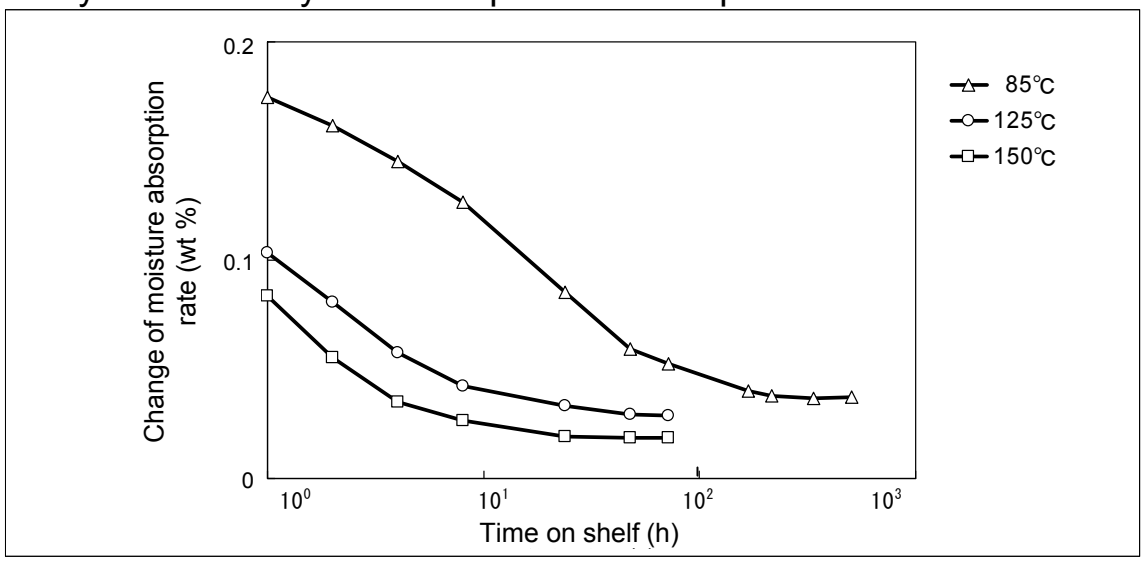


Figure 2-2-4-4. Moisture Absorption Characteristics of 256-Pin LQFP (1.4 mm Thick) at Each Shelf Environment

Since resin has a higher thermal resistance in comparison to metal, if thermal dissipation is inadequate, the chip temperature will increase, lowering operating margins and degrading materials, causing the semiconductor product to fail. Countermeasures include increasing the thermal conductivity of the resin material or attaching heat sinks. Although this is not problematic design-wise, various failures can still occur if the external temperature rises or power exceeding the rated value is applied.

Resin-encapsulated devices can ignite by accident if the above is not considered. Toshiba is therefore now making flame-resistant resins. The standards for the flame-resistance of resin are defined in the US Underwriters Laboratories Inc. (UL) Standard.

2-2-4-2. Package Cracking Mechanism

Figure 2-2-4-5 shows the process by which package cracking occurs. This mechanism is mainly caused by expansion when moisture collected beneath the die pads evaporates.

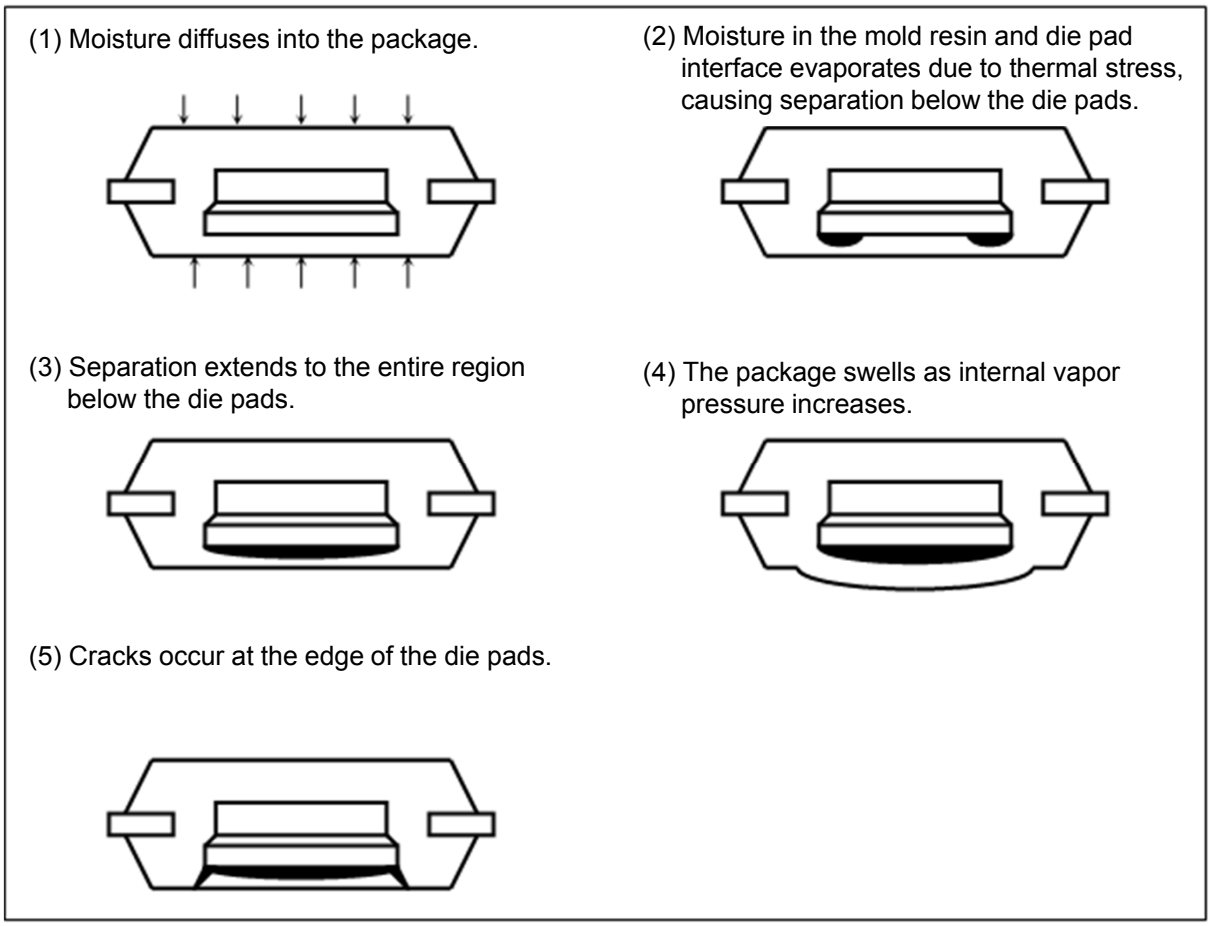


Figure 2-2-4-5 Package Cracking Mechanism

2-2-5. Ag Migration

Ion migration occurs with a variety of metals, but is especially known to occur with Ag. Migration is not viewed as largely problematic in Sn-Pb plating, but does require caution in lead-free plating that contains Ag. Migration refers to the movement of the metal component (plating) above the non-metal component (mounted substrate) in an electrical field. Because the metal that moves is conductive, migration causes an electrical short between leads, resulting in semiconductor-product failure.

2-2-6. Tin Whiskers

Although advances in the development of an Sn plating that suppresses whisker growth have been put to practical use in recent years, one of the reasons the external plating, which was originally Sn plating, has been switched to Sn-Pb plating is whisker growth.

Although the addition of lead suppressed whisker growth, with the increase in Sn content in external plating material due to the switch to lead-free plating, caution with regard to whisker growth is required. The Sn content in Sn-Pb plating is 63 to 90 wt% in comparison to 95% or higher in lead-free plating.

An Sn whisker is generally described as an Sn protrusion caused by oxidation, diffusion and compression stress that mechanically occurs. The Sn whisker can be found in the shape of a needle, nodule or spiral. The needle-shaped whisker in particular can grow quite long, resulting in electrical shorts between leads and, consequently, semiconductor-product failure.

2-3. Operating Environment

2-3-1. Electrostatic Discharge (ESD)

With advances in semiconductor-product fine-pattern processing and circuit integration technologies, performance has dramatically improved. However, along with fine-pattern processing, semiconductor-product degradation and damage from ESD has become a major problem. This section describes how static electricity occurs and how it damages products.

[1].ESD Model

(a) Human Body Model (HBM)

In this model, the human body serves as the source of static electricity, and the electrostatic discharge from the body damages semiconductor products. Although there are various discussions concerning how much static charge the body contains, evaluations are conducted using a capacitor discharge method with values set at 100 pF, 1500 Ω.

(b) Charged Device Model (CDM)

In this model, the semiconductor product itself becomes the source of static electricity due to sticking or the friction produced when the product approaches a charged object, resulting in a sudden discharge of electricity through the leads which damages products. Evaluations are conducted using dedicated CDM test equipment.

(c) Other

In addition to the above two models, there is the field-induced model (FIM) in which induced charge occurs when a product with an insulated structure, such as a MOS device, is exposed to a high electrical field, resulting in discharge that damages the device. There is also a small-size capacitor method (10 pF, 0 Ω) that reproduces CDM using the capacitor discharge method.

2-3-1-1. Equivalent Electrostatic Discharge Test Circuit

(1) Human Body Model (HBM)

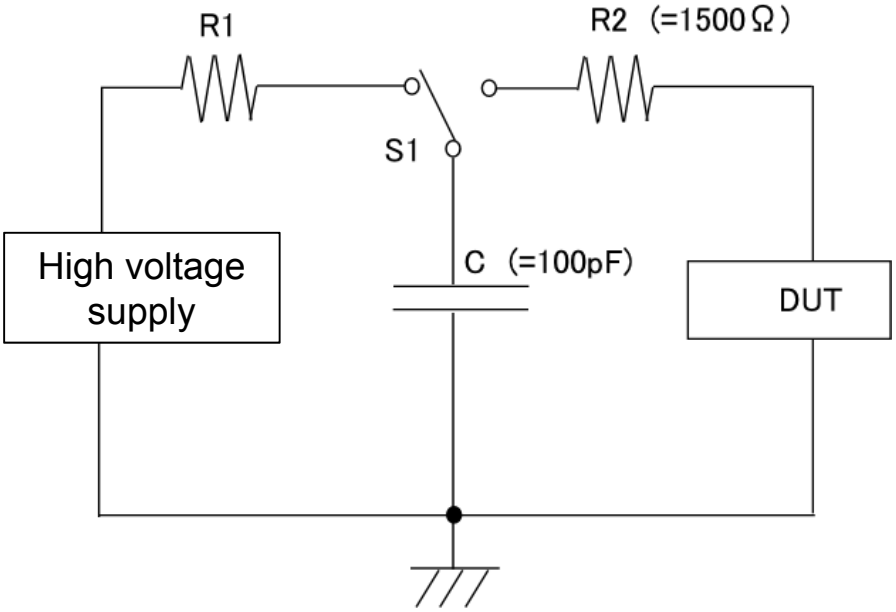


Figure 2-3-1-1 Equivalent circuit for Human Body Model (HBM) Test

(2) Charged Device Model (CDM)

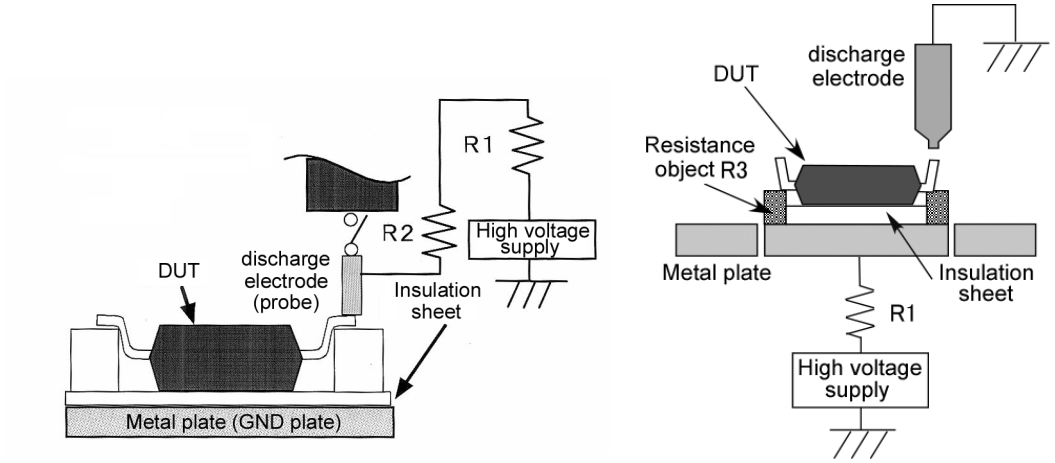


Figure 2-3-1-2 Equivalent circuit for Charged Device Model (CDM) Test
(Left figure: direct contact (DC) method, right figure: field induced (FI) method)

[2]. Failure mechanisms

The main static electricity failure mechanisms of semiconductor products are classified into two categories:

(1) Insulating film breakdown (gate oxide breakdowns, inter-layer film breakdowns)

(2) Thermal breakdown (junction breakdowns)

(1) Insulating film breakdown (gate oxide breakdowns, inter-layer film breakdowns)

A short circuit through the gate oxide or inter-layer insulating film causes an insulating film breakdown. It occurs mostly in semiconductor products having a gate oxide of MOS structure. Oxide film breakdown in a MOS structure occurs when voltage above the threshold is applied to oxide film with low thermal conductivity, or when the energy required to inflict damage is consumed by the MOS product.

The dielectric breakdown strength of oxide film is generally said to be 8 to 10 MV/cm. For this reason, products with a thin oxide film, e.g. 50 nm, exhibit dielectric breakdown at 40 to 50 V.

(2) Thermal breakdown (junction breakdowns)

Junction breakdown occurs when excessive current flow in the junction area raises the junction temperature locally, destroying it with heat. The Wunsch & Bell model that is based on a thermal diffusion formula is the model most commonly used to explain junction breakdown. [43)] In the model, the junction breakdown phenomenon is determined from the impressed pulse width and power density applied to the device.

Since junction energy consumption differs for a forward or reverse discharge, different breakdown voltages result. Since electrical discharge in the forward direction does not readily concentrate energy in a localized area in comparison to reverse discharge, the breakdown voltage for a forward discharge is higher.

2-3-2. Electrical Overstress (EOS)

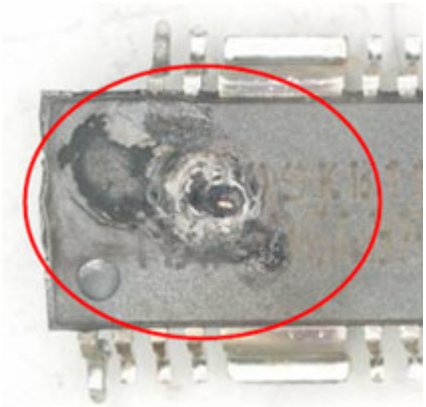
Destruction by EOS (Electrical Over Stress) is a mode in which semiconductor products are broken down by applying voltage or current exceeding the absolute maximum rating to them.

Even when the stress from the electrical energy is small, it may cause deterioration of the device, or minute wiring inside the product may melt or fuse. In this situation, there are many cases that cannot be judged visually, and it will appear to be a characteristic defect or a shorter product lifetime.

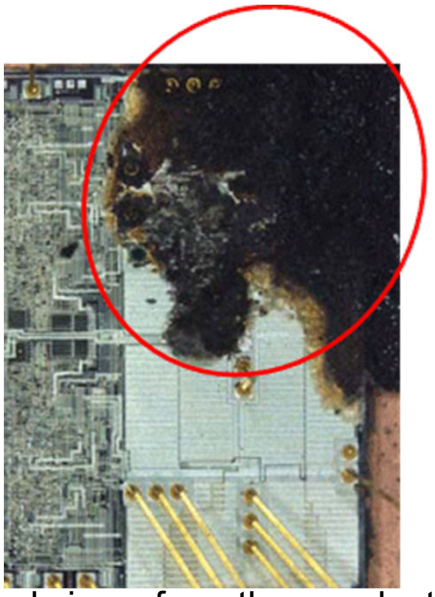
In addition, when electric energy such as the voltage or current is large, or abnormally strong voltage or abnormal current is applied for a long time, the package resin discolors or melts. There are also cases where it cracks.

< Destruction by EOS Example 1 >

[Photo 1] shows melted package resin due to breakdown by EOS, and [Photo 2] shows disassembled view of another product in the same state. Melted mold resin sticks to wires and chips, and it remains in this way during normal disassembly.



[Photo 1] Melted package resin due to breakdown by EOS

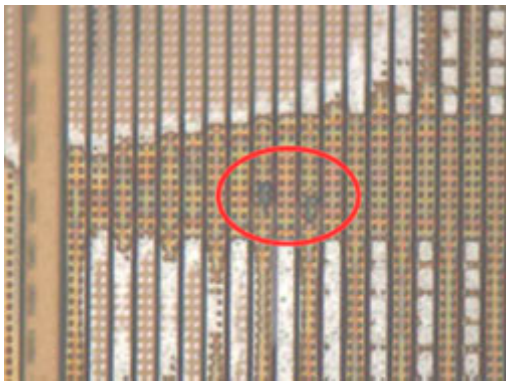


[Photo 2] Disassembled view of another product in the same state

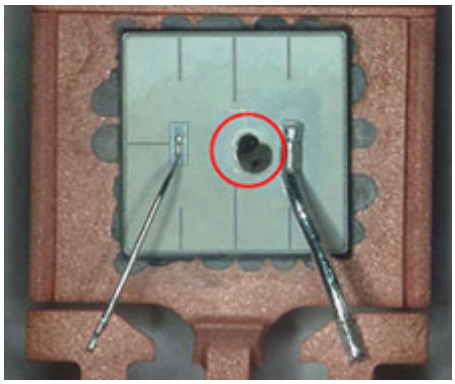
< Destruction by EOS Example 2 >

[Photo 3] is a trace of a breakdown that assumes that EOS is relatively little energy or applied for a short time.

It has stopped melting a minute part inside the circuit. In [Photo 4], the amount of energy that caused the breakdown was considerable. We can see that the circuit in the center of the chip is melting.



[Photo 3] Trace of breakdown when there is little energy or it is applied for a short time



[Photo 4] Trace of breakdown when there is a considerable amount of energy

2-3-3. Soft Errors [44)]

When cosmic rays (protons and charged particles of He, etc.) enter the atmosphere and collide with atmospheric elements, secondary particles are produced. The neutrons that are not charged reach the earth's surface, attenuating only at nuclear collision in the atmosphere.

The neutrons in cosmic rays are classified into high-energy neutrons of 10 to a few 100 MeVs, and low energy neutrons (thermal neutrons: approximately 0.025 MeV) that reach a thermal equilibrium at the earth's surface.

When high-energy neutrons collide with the Si nucleus of a device, the generated charged ions induce a large load, resulting in a soft error. The ^{7}Li and α-particles produced from a capture reaction with low energy neutrons (thermal neutrons) and ^{10}B are known to cause soft errors. These particles especially have a great effect on devices that employ boron phosphorous silicon glass (BPSG), which contain a lot of ^{10}B.

Neutron-induced soft errors depend on the operating environment of the device, such as the geographical environment (latitude, longitude, altitude, etc.) and radiation shielding environment (indoor/outdoor), and the radiation environment on the ground depends on factors such as solar activity.

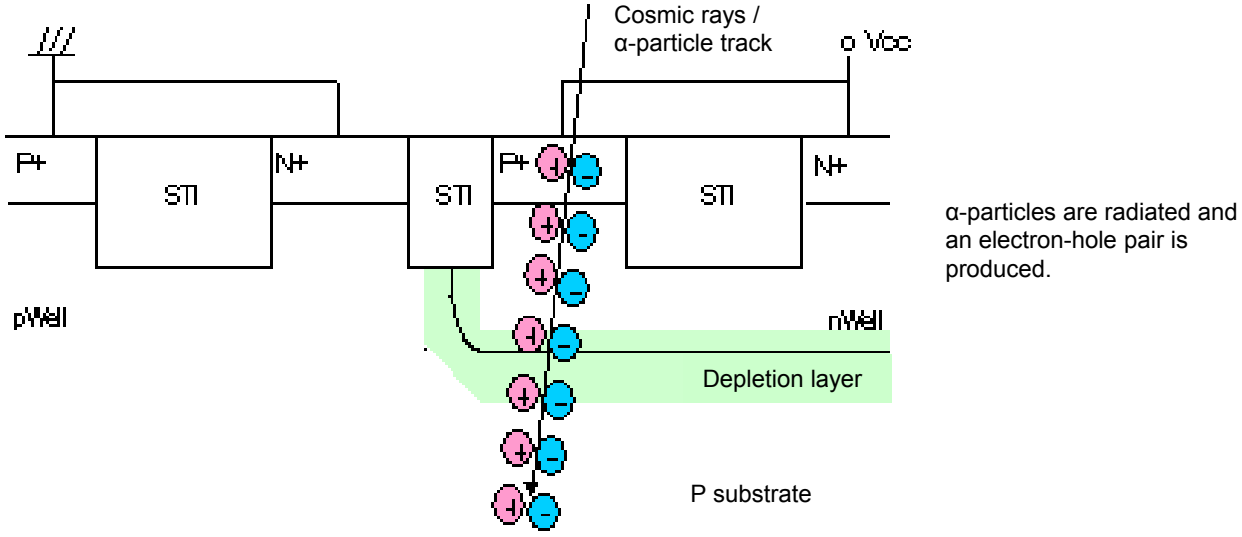


Figure 2-3-3-1 Soft Error Mechanisms

2-3-4. Latch-up

CMOS-ICs are sometimes destroyed when an excessive noise or voltage is applied to them through the input/output pins while it is active, causing a parasitic thyristor to conduct.

Figure 2-3-4-1 shows a CMOS sectional structure and equivalent circuit. As shown in Figure 2-3-4-1. CMOS Sectional Structure, CMOS has NPN and PNP parasitic transistors which form the PNPN thyristor structure shown in Equivalent Circuit.

For example, if a voltage greater than VDD max is applied to pin D, the emitter-to-base of Tr1 becomes forward-biased. The collector current of Tr1 drops to GND through RP causing a potential difference to develop across RP. This in turn forward-biases the emitter-to-base of Tr2 so that the collector current of Tr2 is supplied from VDD through RN, causing a potential difference to develop across RN. Consequently, increasingly greater amounts of positive feedback are applied, forward-biasing the base-to-emitter in Tr1 and forcing the thyristor structure to conduct. In the end, the CMOS IC breaks down.

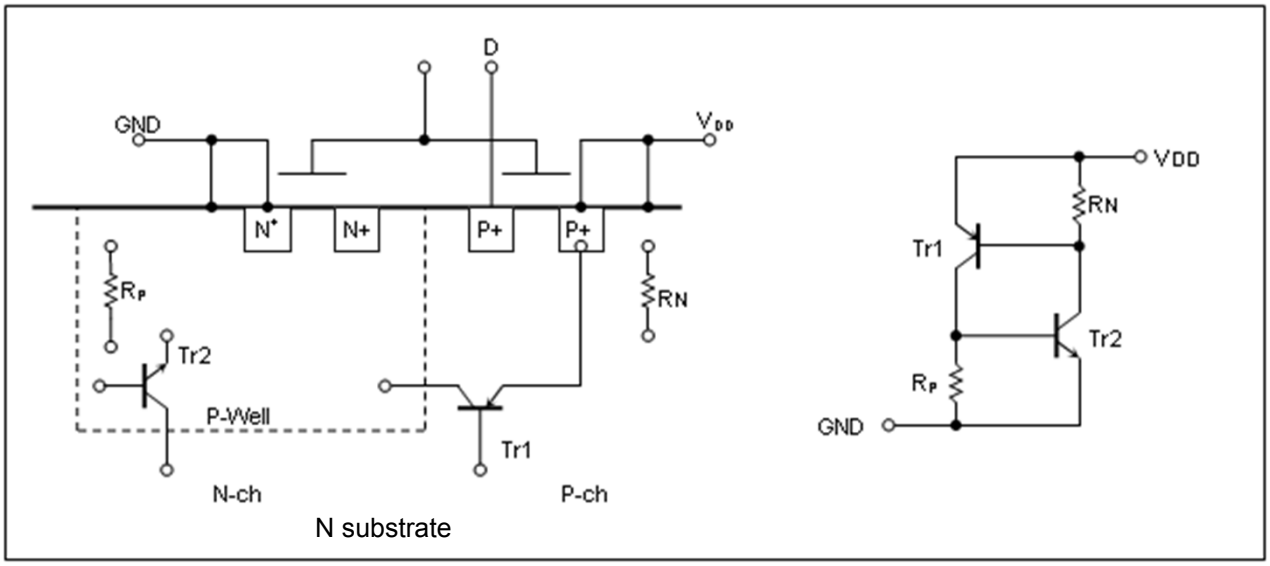


Figure 2-3-4-1 CMOS Sectional Structure and Equivalent Circuit

2-3-4-1. Latch-Up Test Circuit

The following shows two latch-up test circuits and the results of test implementation.

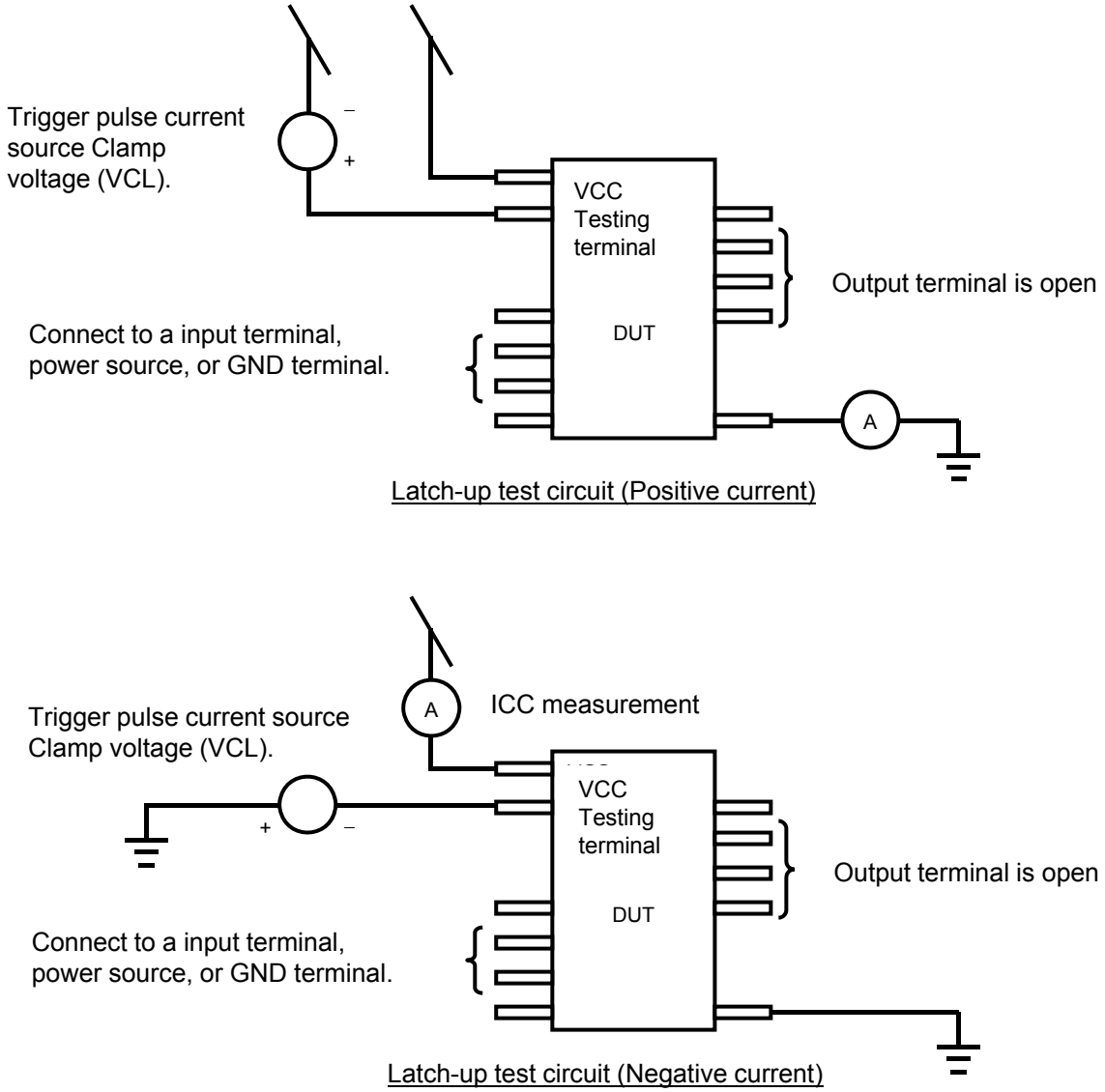


Figure 2-3-4-1 Latch-Up Test Circuit

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Chapter 3 Reliability Testing

Chapter 3 Reliability Testing

3-1. What is Reliability Testing

3-1-1. Significance and Purpose of Reliability Testing

The purpose of semiconductor-product reliability testing is primarily to ensure that shipped semiconductor products, after assembly and adjustment by the customer, exhibit the desired lifetime, functionality and performance in the hands of the end user.

Nevertheless, there are constraints of time and money. Because semiconductor products require a long lifetime and low failure rate, to test semiconductor products under actual usage conditions would require a great amount of test time and excessively large sample sizes.

The testing time is generally shortened therefore by accelerating voltage, temperature and humidity. In addition, statistical sampling is used, taking into account the similarities between process and design, so as to optimize the number of test samples.

Toshiba performs various reliability testing during new product development following the stages shown in Table 3-1-1-1. In recent years, customer demand for shorter development-to-shipment times, and the increasing advancement and complexity of semiconductor products, has made failure analysis extremely difficult. Consequently, evaluation of basic failure mechanisms must begin in the development phase, dividing products into different test element groups (TEG), such as process TEG and design TEG.

To verify product reliability, various lifetime and environment tests – a process referred to as design approval testing (DAT) – ensure that the required specifications and quality/reliability targets are met.

During mass production, semiconductor products are made under strict manufacturing control and screening to eliminate those with a potential for failure and ensure higher reliability. In addition, initial inspections of product characteristics and periodic reliability monitoring are used to assess whether or not the product quality level remains high.

Chapter 3 Reliability Testing

Tests are carried out with high efficiency and focus by classifying assessment levels according to product innovation and importance, and defining test items and assessment standards accordingly.

The various reliability testing described above, through problem identification and correction at each phase of semiconductor-product development, is used to provide customers with a level of reliability that ensures safe product use, and to maintain and improve reliability in the manufacturing phase as well.

3-1-2. Before Testing

The following points must be considered before implementing reliability tests in order to satisfy the objectives described above:

(1) For what applications will the semiconductor product be used?

(2) In what possible environments and operating conditions will the semiconductor product be used?

(3) What are the possible failure modes and mechanisms, and what kind of accelerated stress testing is appropriate?

(4) What level of reliability (failure rate, for example) does the market require for the semiconductor product?

(5) How long is the semiconductor product expected to be in service

(6) How does the semiconductor product rate in terms of innovation and importance?

These points must be considered when determining tests, stress conditions and sample sizes.

The following are accelerated stresses which can be applied to semiconductor products. They are described in detail in Chapter 3-3. Accelerated Lifetime Tests.

(1) Temperature

(2) Temperature and humidity

(3) Voltage

(4) Temperature difference

(5) Current

An important consideration in reliability testing is that the testing must contribute to the appropriate evaluation and improvement of semiconductor-product reliability.

It is therefore important to accumulate reliability testing results, to perform detailed failure analysis when failure occurs, and to feed back the results to the design department and manufacturing process.

Chapter 3 Reliability Testing

Table 3-1-2-1 Main Stages, Purposes and Contents of Reliability Testing

	Stage	Purpose	Content	Test Sample
Semiconductor Device Development	Material, process and basic design verification	To assess whether the material, process and design rules enable satisfaction of designed quality/reliability objectives and user specifications when applied to the product.	Metal (Al, Cu) electromigration and stress migration evaluation, gate oxide film breakdown voltage evaluation (TDDB test, breakdown voltage test), MOS transistor hot carrier injection (HCI) effect, negative bias temperature instability (NBTI) evaluation, failure rate for medium- and large-scale integrated circuits or products, new package mechanical strength and environment test, etc.	Process TEGs, function block TEGs, etc.
	Product reliability verification	To assess whether the product design satisfies the designed quality/reliability objectives and user specifications.	Development verification tests (lifetime test, environment test, etc.), structural analysis	Products
		To assess whether the product quality and reliability are maintained at prescribed levels.	Screening and reliability monitoring (by Si process generation and product family)	Products, TEGs

3-1-3. Reliability Test Methods

Reliability test methods include TEG evaluation, in which special sets of devices (referred to as a test element group or TEG) are created for each failure cause, and product evaluation, whereby the product is comprehensively evaluated.

3-1-3-1. TEG Evaluation

TEG evaluation targets basic failure mechanisms. In this method, a set of devices is manufactured especially for the evaluation and analysis of each failure mechanism. The method allows detailed evaluation and failure analysis of failure mechanisms, and is very effective for quantifying limits and acceleration capabilities. Table 3-1-3-1 shows an example of TEG evaluation method.

Depending on the objective, TEG evaluation can be performed either by on wafer or an encapsulated package. TEG evaluation has four major objectives:

(1) During DAT (design approval testing) of new technology and products, it is used to find the method of elimination for failure mechanisms that affect reliability. The various kinds of TEG shown in Table 3-1-3-1 are used to evaluate failure mechanisms attributable to the process or the design.

(2) Clarify failure mechanisms involved in defects found during the product evaluation phase.

(3) For monitoring manufacturing process parameters, monitor process quality control items such as film thickness, film shape and contamination, and failure rates for each process and design rule.

(4) Develop TEG for each function block and estimate product reliability lifetime and failure rate from each TEG combination.

In this manner, the TEG can be used for various purposes to precisely obtain accurate and appropriate data.

Table 3-1-3-1 TEG Evaluation Examples

TEG Structure	Evaluation Target	Design Process Parameter	Stress	Evaluation Method	Evaluation Parameters
MOS capacitor	Gate oxide film breakdown Ion drift Interface trap Process damage Variation in manufacturing conditions Radiation effect	Gate film thickness Gate film quality Oxidation method Gate film material Electrode material Contamination Surface area Shape Dimensions	Temperature Voltage Electric field Current	TDDB (constant current, constant voltage, step stress) Oxide film breakdown voltage test C-V (Pulse C-V) DLTS (deep level transient spectroscopy)	Failure rate vs. time Oxide film breakdown voltage QBD (oxide film breakdown charge) Electric field acceleration coefficient Activation energy COX (oxide film capacitance) Failure rate
MOS transistor	Hot carrier effect Negative bias stability Ion drift Interface trap Variation in manufacturing conditions Process damage Short channel effect Field leak	Gate size (W/L) Gate film thickness Gate film quality Electrode material Contamination Passivation material Shape and structure Ion implantation conditions	Temperature Electric field Mechanical stress Current	High temperature DC biased test. Low temperature DC biased test. Charge pumping test. DC pulse test.	DVth (threshold voltage degradation) DId (drain current degradation) Dgm (gm degradation) Voltage acceleration coefficient Activation energy Sub-threshold characteristics Field breakdown voltage
Multi-layer metallization (metal, diffusion layer, interlayer insulating film)	Stress Migration Electromigration Contact open Interlayer breakdown voltage Corrosion	Metallization material Metallization width Metallization space Through-hole diameter Contact diameter Step, hole shape Interlayer insulating film Passivation Molding resin	Temperature Current density Temperature gradient Voltage Mechanical stress Temperature and humidity	High temperature constant current test. High temperature storage test. Temperature cycle test Reflow treating (or processing) High temperature high humidity biased test. Pressure cooker test (or unbiased autoclave test)	Resistance change Failure rate vs. time Activation energy Current density dependence Open Short
Function block	Process monitoring Failure rate estimation Process approval Humidity resistance	Shape, dimensions, number of elements Gate film thickness Gate film quality Interlayer film quality	Temperature Voltage	High temperature biased (DC/pulse) test, Low temperature biased (DC/pulse) test, High temperature storage test, etc.	Failure rate vs. time Activation energy Voltage acceleration Standby current AC/DC parameters

3-1-3-2. Product Evaluation

Tests are carried out with high efficiency and focus by classifying assessment levels according to product innovation and importance, and defining test items and assessment standards accordingly.

TEG evaluation produces detailed and well-related data for each failure mechanism. However, defects due to inconsistencies and the synergy effect resulting from combinations of failure mechanisms are difficult to be detected. Therefore, as a complement to TEG evaluation, a comprehensive product evaluation must be performed.

Product reliability testing is preferably performed under actual field environment conditions to the extent possible and must always be repeatable. Therefore, standardized test method should be selected whenever possible. Tests complying with semiconductor-device test standards such as JIS, JEITA, MIL, IEC and JEDEC are required. Table 3-1-3-2 shows some of them.

Selecting the test methods, shown in Table 3-1-3-3, among common tests to semiconductor products as the methods compliant with JIS, JEITA, MIL, IEC and JEDEC, Toshiba standardizes them and conducts an appropriate test or tests selected according to product groups. In addition, tests for electrostatic discharge (ESD), latch-up strength, soft error and other conditions are performed under field environmental and climatic conditions.

Table 3-1-3-2 Reliability Test Standards

- JEITA (Japan Electronics and Information Technology Industries Association) Standards ED-4701/001A Environmental and endurance test methods for semiconductor devices (General) ED-4701/100A Environmental and endurance test methods for semiconductor devices (Life test I) ED-4701/200A Environmental and endurance test methods for semiconductor devices (Life test II) ED-4701/301A Environmental and endurance test methods for semiconductor devices (Stress test I-1) ED-4701/302 Environmental and endurance test methods for semiconductor devices (Stress test I-2) ED-4701/400A Environmental and endurance test methods for semiconductor devices (Stress test II) ED-4701/500A Environmental and endurance test methods for semiconductor devices (Miscellaneous)
- MIL (U.S. Military Standard) Standards MIL-STD-202 Test method standard for electronic and electrical component parts MIL-STD-883 Test method standard for microcircuits
- IEC (International Electrotechnical Commission) Standards IEC 60749 Semiconductor devices-mechanical and climatic test methods IEC 60068-1 Environmental testing Part1: General and guidance IEC 60068-2 Environmental testing Part2
- JEDEC Standards (Joint Electron Devices Engineering) JESD 22 Series Test Methods JESD 78 IC Latch-Up Test
- JIS (Japanese Industrial Standard) Standards [Basic] JIS C 025 (IEC 60068-2) Environment test methods (electric, electronic) and temperature change test methods
- Automotive Electronic Components Standard (AEC) AEC-Q100 Integrated Circuits (IC) AEC-Q101 Discrete Semiconductors (Transistors, Diodes, etc.)

Table 3-1-3-3 Product Reliability Test Method Examples (1/2)

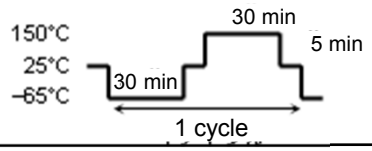
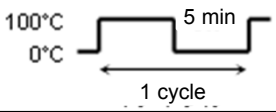
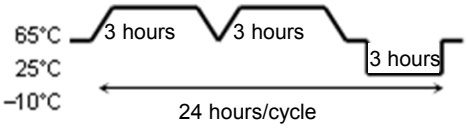
Type	Test	Description and Test Conditions	Compliant Standards			
			JEITA ED-4701	MIL-STD-883	IEC 60749	JESD22
Lifetime Test	High temperature operating life test	Apply electrical stress (voltage, current) and thermal stress to the device for an extended period of time and evaluate the resistance. Normal test conditions: Ta =125°C Power supply voltage = Max. operating voltage	101A	1005.8	Part 23	A108-C
	High temperature high humidity biased test	Apply electrical stress (voltage, current), thermal stress and moisture to the device for an extended period of time and evaluate the resistance. Normal test conditions: Ta = 85°C, RH = 85% Power supply voltage = Max. operating voltage	102A	-	Part 5	A101-C
	High temperature storage test	Apply high temperature to the device for an extended period of time. Normal test conditions: Ta =Tstg. max	201A	1008.2	Part 6	A103-C
	Low temperature storage test	Apply low temperature to the device for an extended period of time. Normal test conditions: Ta = Tstg. min	202A	-	-	-
	High temperature high humidity storage test	Apply high temperature, high humidity to the device for an extended period of time. Normal test conditions: Ta = 85°C, RH = 85%	103A	-	-	-
Thermal Environment Tests	Soldering heat resistance test	Evaluate heat resistance during soldering. Normal test conditions: Solder bath temperature: 260°C ± 5°C Dipping time: 10 ± 1 seconds Distance from immersed part from device body: 1.5 ± 0.8 mm	301D /302A	STD-750-2031	Part 20	B106-D/ A112-A
	Temperature cycle test	Evaluate the resistance to low and high temperatures and temperature change. Normal test conditions: 	105A	1010.7	Part 25	A104-D
	Thermal shock test	Evaluate the resistance to sudden temperature changes. Normal test conditions 	307B	1011.9	Part 11	A106-B
	Moisture resistance test (high temperature high humidity cycle test)	Evaluate resistance under high temperature, high humidity conditions. Normal test conditions: 	203A	1004.7	-	A100-C

Table 3-1-3-3 Product Reliability Test Method Examples (2/2)

		Contents and operating conditions	Compliant Standards			
			JEITA ED-4701	MIL-STD-883	IEC 60749	JESD22
Mechanical Tests	Vibration test	Evaluate resistance to the vibration applied during transport and usage. The test includes variable and constant frequency vibration; normally variable is used. Normal test conditions: Constant frequency vibration: 60 ± 20 Hz, 200 m/s^2 in three directions, 96 ± 8H in each direction Variable frequency vibration: 100 to 2000 Hz 200 m/s^2 in three directions, four cycles per direction, four minutes per cycle	403A	2007.2	Part 12	B103-B
	Mechanical Shock test	Evaluate resistance to the shock applied during transport and usage. Normal test conditions: Depends on device structure. With resin molded devices, shock acceleration of 15,000 m/s^2 is applied three times in each of four directions.	404A	2002.3	Part 10	B104-C
	Constant acceleration test	Evaluate resistance to constant acceleration. Normal test conditions: Depends on device structure. With resin molded devices, acceleration of 200,000 m/s^2 is applied in six direction, each for one minute	405A	2001.2	Part 36	-
	Terminal strength test	Evaluate whether or not the strength of the terminal area is sufficient for the force applied during installation and usage. Normal test conditions: Suspend a prescribed load onto the tip of the lead to bend it 90° and back. Apply tensile force in a direction parallel to the lead. The prescribed load varies according to device structure.	401A	2004.5	Part 14	B105-C
	Solder- ability test	Evaluate terminal solderability. Normal test conditions: Solder bath temperature: 245°C, Dipping time: 5 sec. (lead-free solder)	303A	2003	Part 21	B102-E
	Sealing test	Evaluate the airtightness of the seal. Use bubbles to detect large leaks. This test is suitable for metallic and ceramic packages.	503	1014	Part 8	A109-A
	Salt atmosphere test	Evaluate the resistance to corrosion in a salt atmosphere. Normal test conditions: 35°C, 5% salt solution, 24 hours	204A	1009	Part 13	A107-B
Other	Unbiased autoclave test (or Pressure cooker test)	Evaluate resistance when stored under pressure under high temperature, high humidity for a short period of time. Normal test conditions: 203 to 255kPa, RH = 100%	-	-	Part 33	A102-C
	Electrostatic discharge test	Evaluate the resistance to static electricity. Normal test conditions: Human body model: C = 100 pF, R = 1.5 kΩ, three discharges Device charge model	304A /305C	3015.7	Part 26 Part 27 *(Part 28)*	A114-E/ C101-C
	Latch-up strength test	Evaluate resistance to latch-up. Normal test conditions: Pulse current injection method, Vsupply overvoltage test	306B	-	Part 29	JESD78A

3-1-4. Failure Assessment Criteria

In general, failures are divided into fatal failures such as functional failure, opens and shorts, and other failures such as degradation of electrical characteristics and defective outer appearance which is detected as the failure in visual inspection. Toshiba in principle assesses failures based on the satisfaction of standards stipulated in specifications for the device.

3-2. Detailed Application Methods for Reliability Testing

3-2-1. Design Approval Test Procedures

Semiconductor reliability tests are performed in the research and development phase and in the mass production phase. During research and development, reliability tests are used to evaluate design quality, materials and processes. During mass production they are used as design approval tests and for periodic reliability monitoring.

As shown in Figure 3-2-1-1, the design approval test (DAT) procedure uses a test element group (TEG) primarily to evaluate the wafer process and package during research and development, and to obtain basic data for design optimization. The product is designed based on this data, and a prototype is used for the DAT. When evaluated, the product is classified into families according to the design rule and package, and reliability testing is performed on a representative product from each family.

The tests performed include electrical characteristics, early failure rate (EFR), long-term lifetime or random failure rate (IFR), threshold and environment tests. Reliability tests for products other than the representative products are mainly based on electrical characteristics and small samples. Table 3-2-2-1 shows an example of a DAT for a product.

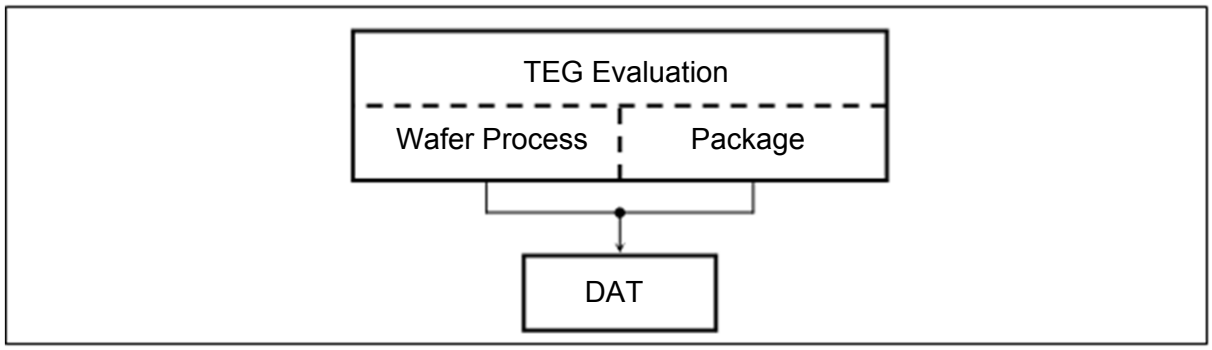


Figure 3-2-1-1 Design Approval Test Procedure

3-2-2. Reliability Monitoring during Mass Production

Products passing DAT undergo an initial quality assurance inspection before shipment. In addition, periodic reliability monitoring is performed to verify the reliability levels of shipped products. In the initial quality assurance inspection, product initial electrical characteristics and visual appearance are checked. The objectives are to verify the product quality of each product lot and to assure the quality of shipped products.

Periodic reliability verification, i.e., reliability monitoring, involves lifetime and environment tests performed on groups of products classified by process and package family. The reliability level is continuously monitored, failures are analyzed and results are fed back to the manufacturing process. In addition, data is accumulated allowing reliability to be further improved.

Table 3-2-2-1 Examples of Design Approval Test for a Product

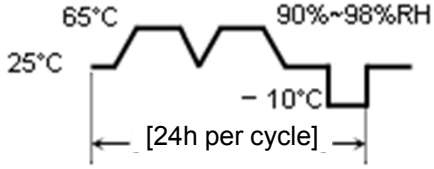
1. Si Reliability Tests (Example)

Test	Test Conditions	Remarks
High-Temperature Operation	Apply maximum guaranteed operating voltage or accelerated voltage at 125°C.	Test for 1,000 h
High-Temperature Bias	Apply maximum guaranteed operating voltage or accelerated voltage at 125°C.	Test for 1,000 h
High-Temperature Storage	150°C	Test for 1,000 h
Low-Temperature Operation	Apply maximum guaranteed operating voltage or accelerated voltage at -30°C.	Test for 1,000 h

2. Package Reliability Tests (Example)

Test	Test Conditions	Remarks
Temperature Humidity Bias	Apply maximum guaranteed operating voltage at 85°C/85%	Test for 1,000 h
High Accelerate Stress	Apply maximum guaranteed operating voltage at 130°C/85%	Test for 300 h
Temperature Cycling	One cycle consists of -65°C (20 min) followed by 150°C (20 min)	Test for 300 cycles
Pressure Cooker	127°C/100% (2.53×10^5Pa)	Test for 120 h

3. Thermal Environment Tests (Example)

Test	Test Conditions	Remarks
Soldering Iron Heat	Soldering temperature: 400°C, applied twice for 3 seconds	Only the leads are immersed
Temperature Cycling	One cycle consists of -65°C (20 min) followed by 150°C (20 min)	Test for 300 cycles
Thermal Shock	One cycle consists of 0°C (5 min) followed by +100°C (5 min), complete transition within 10 s	Test for 100 cycles
Moisture Resistance		Test for 10 cycles

4. Mechanical Tests (Example)

Test	Test Conditions	Remarks
Vibration Variable Frequency	100 to 2000 to 100 Hz |← (4 min) → | 200 m/s , applied in 2 or 3 directions, four times each	
Mechanical Shock	15000m/s^2, 0.5 ms, applied in four directions, 3 times each	
Constant Acceleration	200000 m/s^2, applied is 6 directions, each for one minute	

5. Other (Example)

Test	Test Conditions	Remarks
Solderability	Solder bath temperature: 245°C, applied once for five seconds (using flux)	Only the leads are soldered. Leads with solder deposition rates of 95% or higher are considered good.
Salt Atmosphere	Left in 5% salt spray atmosphere at 35°C for 24 h	

3-3. Accelerated Lifetime Tests

3-3-1. Purpose

With the ever-increasing requirements for part and device reliability, the need to evaluate product lifetime and failure rates quickly is now greater than ever. Reliability tests are conducted under test conditions that simulate potential stresses applied to semiconductor components. Depending on the situation, however, it may take an exceedingly long time until failure occurs or failure may not occur within the limited test time.

Therefore, stresses beyond those of actual operating conditions are applied to devices to physically and/or chronologically accelerate causes of degradation. In this way, device lifetime and failure rates can be determined, and failure mechanisms can be analyzed. This type of test is referred to as an accelerated lifetime test. Such tests are used to shorten the evaluation period and analyze mechanisms in detail.

The accelerated lifetime test is also sometimes used as a forced degradation test to forcibly accelerate a constant stress. It is also sometimes used as a limit test for accelerating stress to determine a limit value.

It is necessary to be noted that failure mechanisms in accelerated tests differ somewhat from those that occur under actual usage conditions. In general, if the degradation mechanism is simple, acceleration is also simple and lifetime and failure rates can be estimated relatively accurately. Complicated failure mechanisms, however, are difficult to simulate, even when best efforts are made to accelerate stresses simultaneously. This is because the different stress effects are interrelated. Therefore, analysis of acceleration data as well as estimation of lifetime and failure rates can be difficult. When performing accelerated lifetime tests, it is important to select test conditions that result in as few failure mechanism changes as possible and that minimize the number of failure mechanisms, making testing easy and simple.

3-3-2. Constant Stress and Step Stress

There are two types of accelerated lifetime testing: constant stress and step stress. In a constant stress test, the time-dependent failure distribution of a test sample subjected to constant stress at several stress levels is observed. In a step stress test, stress is applied to a test sample gradually in stepped increments, and the step at which failure occurs is observed.

A typical constant stress test is the application of the constant stress of power or ambient temperature exceeding the maximum rating. Weibull distribution is often used to verify that the failure mode has not been changed by the test. The validity of the accelerated test is confirmed if the shape parameter m of the Weibull distribution remains unchanged by the accelerated stress.

Figure 3-3-2-1 shows Weibull plots when the power consumption of a silicon transistor is changed. It is evident from the figure that parameter m is constant regardless of the power consumption level.

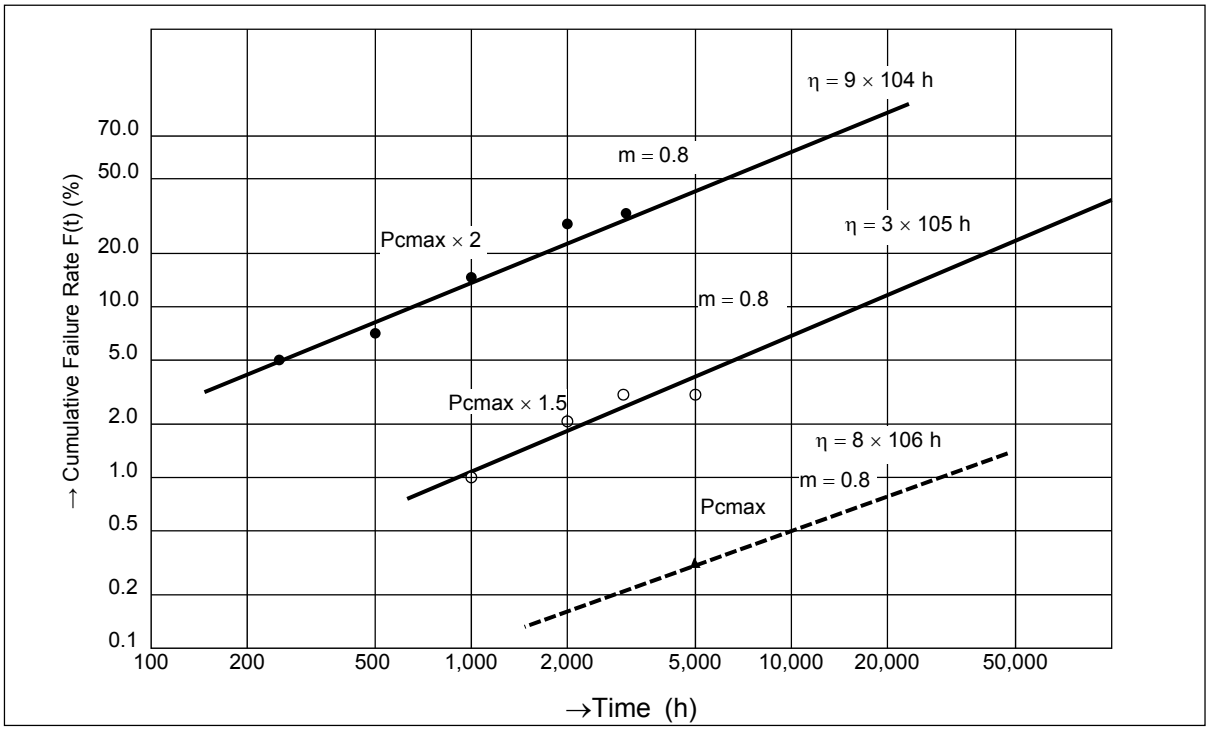


Figure 3-3-2-1 Weibull Distribution and Shape Parameter for Transistor Accelerated Lifetime Test

This same result should occur in both constant tests and step tests.

Thus, a step test produces the failure data corresponding to at least one constant stress. If the failure mode of the previous step is the same, a step test can be used to determine the critical temperature for the component and to estimate its lifetime. Figure 3-3-2-2 shows an example.

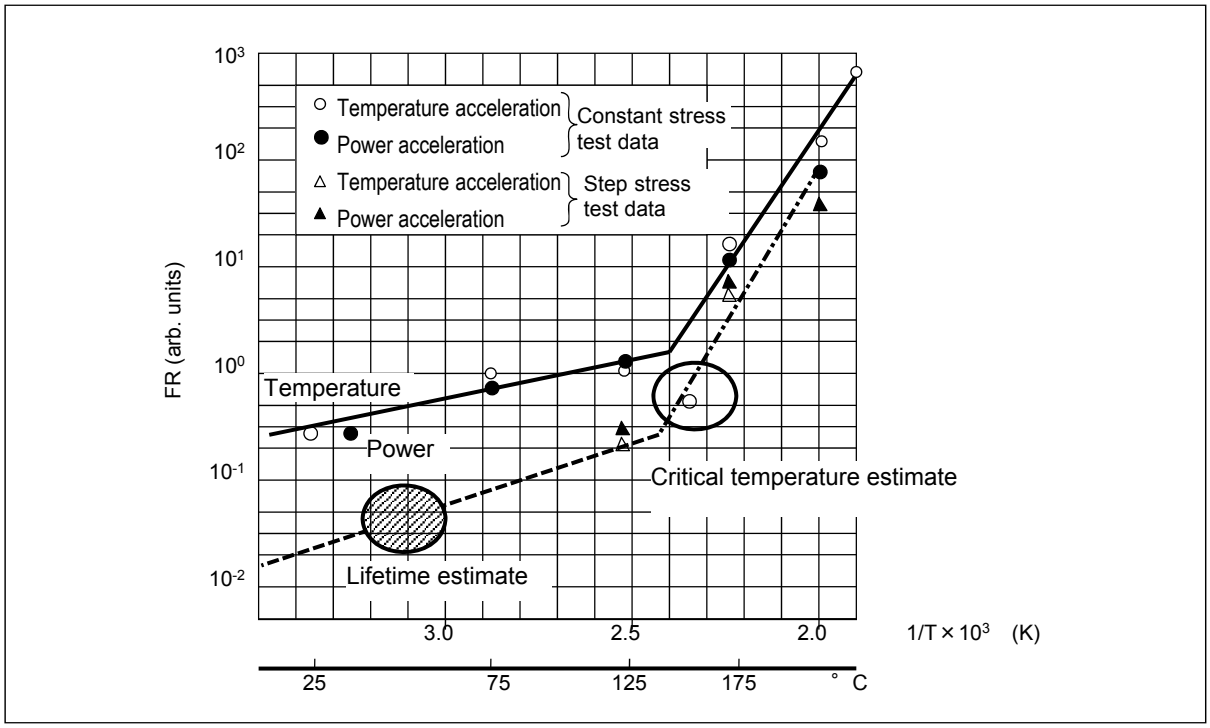


Figure 3-3-2-2 Failure Rate Estimation Step Stress

3-3-3. Temperature

Accelerated lifetime testing is closely associated with the physics of the failure. The physical and chemical reactions of semiconductor-product degradation are generally used as chemical kinetics. Chemical kinetics is a basic chemical reaction model that describes the temperature dependence of failures. The temperature dependence of failures are widely used with the Arrhenius model [1)] in accelerated lifetime testing of semiconductor products. Given a chemical reaction speed K, the Arrhenius equation can be expressed as:

$$K = A\exp\left(-\frac{E_a}{kT}\right)$$

E_a : Activation energy (eV)
k : Boltzmann's constant (where 8.6173×10^{-5}[eV/K] (1.3807×10^{-23}[J/K] in SI units))
T : Absolute temperature (K)
A : Constant

If the product's lifetime ends at a certain degradation B, then lifetime L can be expressed as L = B/K. Given B/A = A':

$$L = A'\exp\left(\frac{E_a}{k}\cdot\frac{1}{T}\right)$$

This equation expresses the relationship between temperature and lifetime. If the failure mechanism is uniform, lnL and 1/T can be plotted on a straight line as shown in Figure 3-3-3-1. That is, the acceleration from temperature T1 to T2 is lnL1/lnL2.

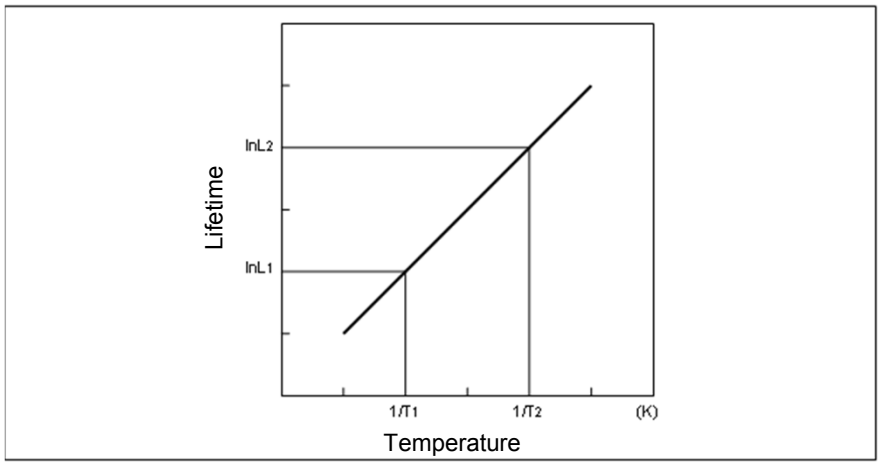


Figure 3-3-3-1 Relationship between Lifetime and Temperature

Given acceleration coefficient α and the lifetimes L_1 and L_2 at temperatures T_1 and T_2, respectively, the acceleration coefficient α can be found using the following formula:

$$\alpha = \frac{L_2}{L_1} = \exp\left\{\frac{E_a}{k} \cdot \left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right\}$$

Ea: Activation energy(eV)

k: Boltzmann's constant

T1, T2: Absolute temperature(K)

Figure 3-3-3-2 shows the relationship between the activation energy and the acceleration coefficient at each temperature. It can be seen from the Arrhenius equation that the acceleration due to temperature changes drastically with the activation energy Ea. Figure 3-3-3-3 shows the relationship between each activation energy level and the accelerated coefficient when the temperature difference as a parameter.

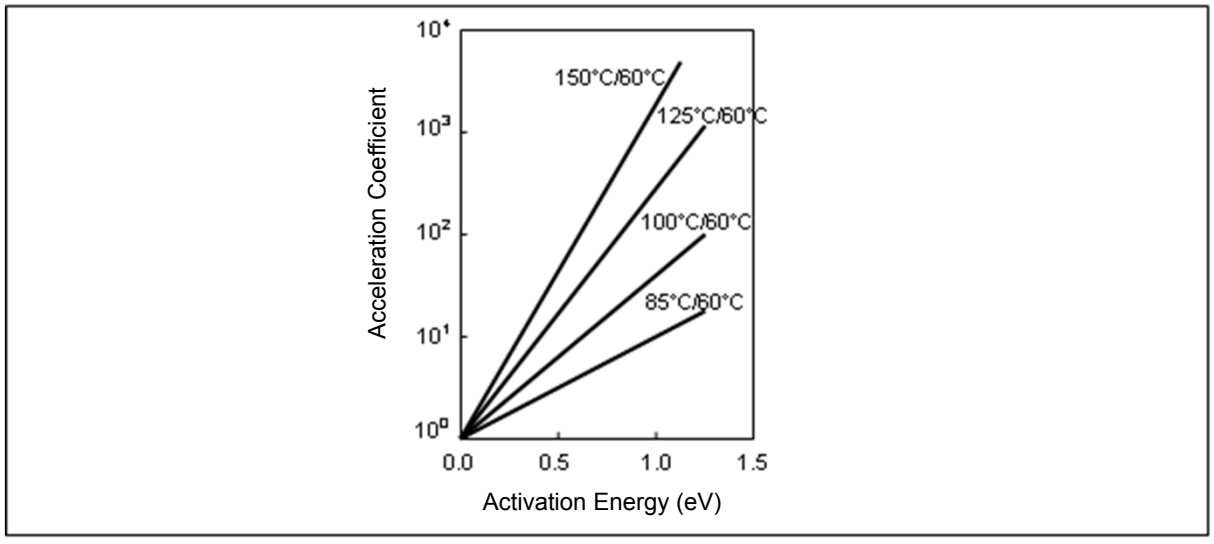


Figure 3-3-3-2 Relationship between Activation Energy and Acceleration Coefficient

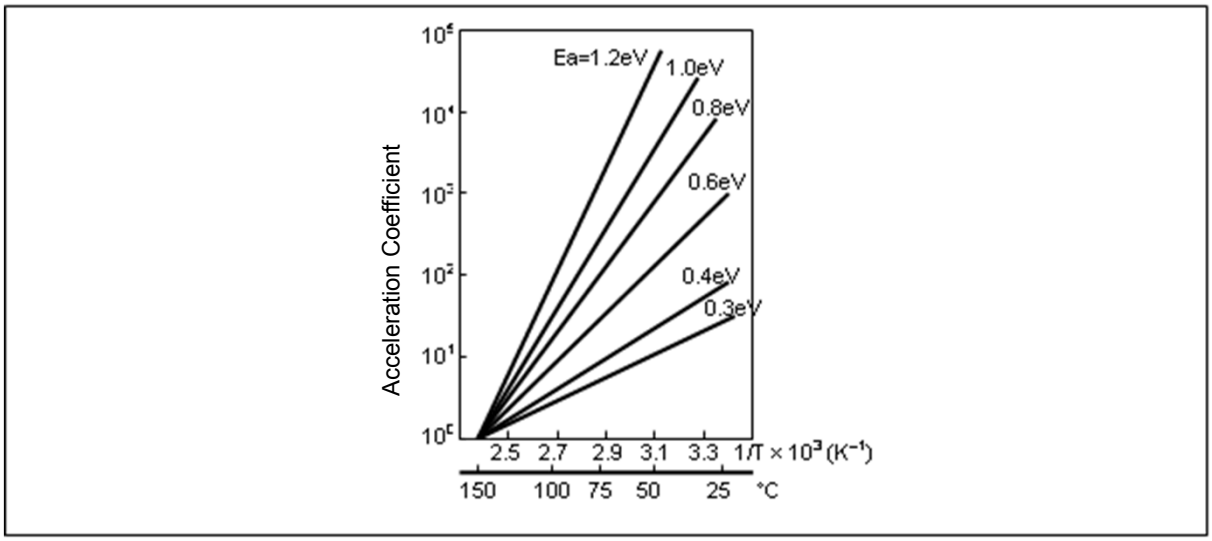


Figure 3-3-3-3 Relationship between Temperature and Acceleration Coefficient Using Activation Energy as a Parameter

Numerous sets of data have been disclosed regarding the relationship between temperature and lifetime or failure rate of semiconductor products. Some examples of data from experiments conducted by Toshiba are as follows:

(1) Temperature Acceleration of Intermetallic Formation of Bonding Wire

As temperature rises, intermetallic alloy begins to form at the junction of Au wire and the Al used on the pad, causing the contact resistance to increase and the contact to open. Figure 3-3-3-4 shows the relationship between the temperature and lifetime from the results of high-temperature storage testing.

From the lifetime values at different temperature conditions, it can be seen that the activation energy is approximately 1.0 eV.

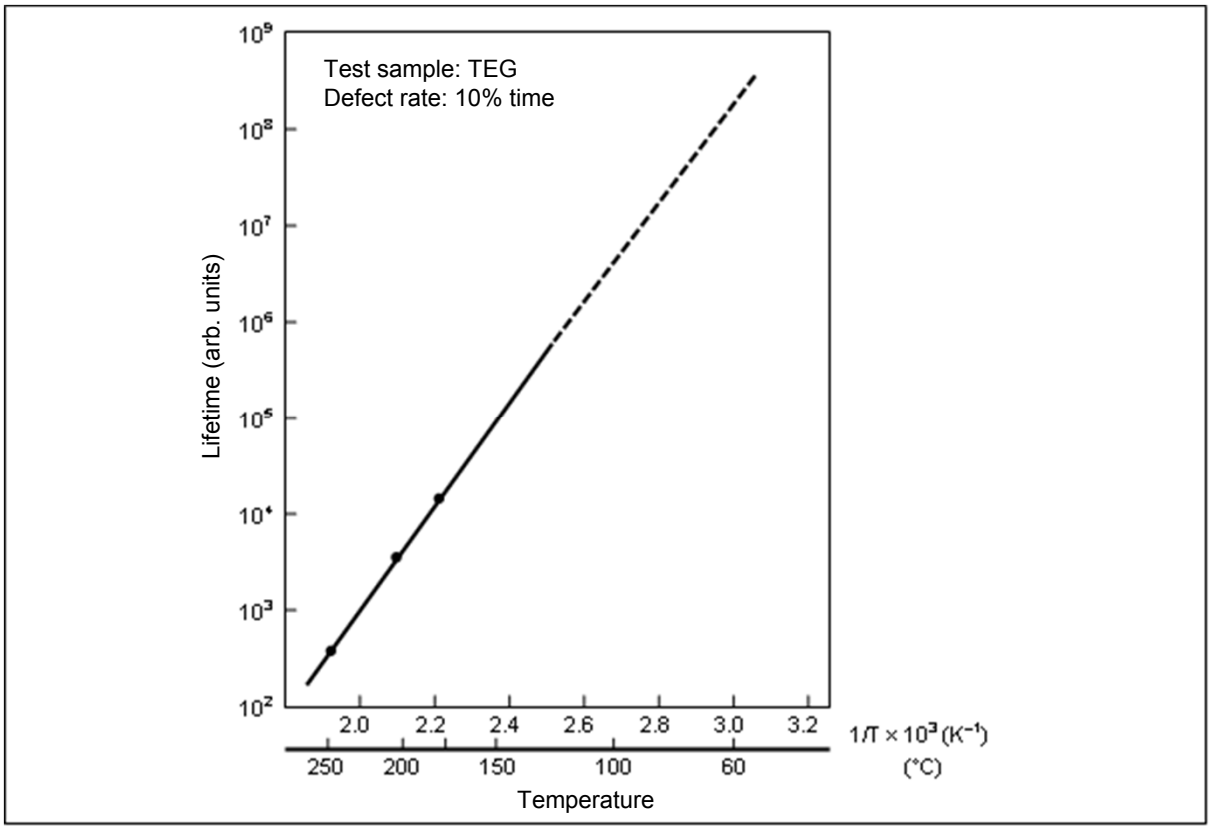


Figure 3-3-3-4 Temperature Dependence of Formation of Intermetallic Alloy in Bonding Wire

(2) Temperature Acceleration on Different Semiconductor Products

Various data have been reported for the relationship between the temperature and failure rate of semiconductor products. Figure 3-3-3-5 shows an example of data obtained from this type of experiment. The figure gives the acceleration rate for each device.

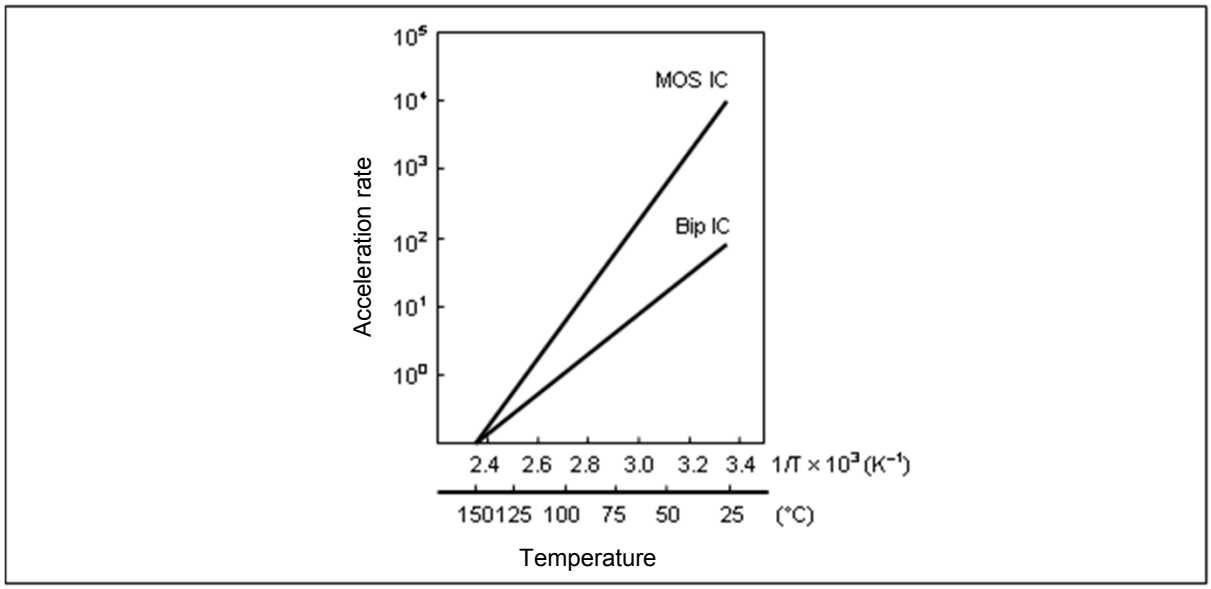


Figure 3-3-3-5 Example of Device Temperature Acceleration

The activation energy differs according to the failure mechanism. Table 3-3-3-6 shows typical failure mechanisms and activation energy values obtained from experiments performed by Toshiba and other organizations.

Table 3-3-3-6 Example of Device Temperature Acceleration

Failure Mode	Failure Mechanism	Activation Energy (ev)
Metal wiring failure (open, short, corrosion)	Al metal electromigration	0.4 to 1.2
	Al metal stress migration	0.5 to 1.4
	Au-Al alloy growth	0.85 to 1.1
	Cu metal electromigration	0.8 to 1.0
	Al corrosion (moisture penetration)	0.6 to 1.2
Oxide film voltage breakdown (insulation breakdown, leakage current increase)	Oxide film breakdown	0.3 to 0.9
h_{FE} degradation	Ion movement acceleration due to moisture	0.8
Characteristic value fluctuation	Degradation by NBTI	0.5 and up
	Na ion drive in SiO2	1.0 to 1.4
	Slow trapping of Si-SiO2 interface	1.0
Increased leakage current	Inversion layer formation	0.8 to 1.0

Note: The above-described obtained values differ according to the Si process generation and detailed structure. These values reflect results actually obtained as well as results from reported cases.

The model described so far was the Arrhenius model for temperature acceleration. Another failure model is the Eyring model. This model considers the effects of humidity, voltage and mechanical stress in addition to temperature. Given an average lifetime L, the relationship to temperature and stress can be expressed as:

$$\ln L = A + \frac{B}{T} - \alpha \ln S$$

L: Average lifetime
A, B, α: Constants
T: Temperature (K)
S: Stress other than temperature

3-3-4. Temperature and Humidity

3-3-4-1. Moisture Resistance Tests

Most semiconductor products of recent years are encapsulated in plastic resin. The reliability of these products largely depends on the moisture resistance of the package. Various types of moisture resistance evaluations tests have been developed in order to evaluate these devices quickly. Table 3-3-4-1 shows examples of these moisture resistance evaluation tests.

The tests are largely divided into two groups. The first group places the semiconductor product in a humid atmosphere, and the second group applies bias to the semiconductor product while subjecting it to humidity or after moisture has penetrated into the product. The classification is made according to the semiconductor-product type (such as the level of power consumption) and the type of failure mechanism to be detected.

If the acceleration rate is too fast, humidity resistance testing can produce failure modes that are different from those that appear during actual usage or problems related to test reproducibility may arise. Therefore, extra care must be taken when performing these tests. Particularly with saturated type PCTs (pressure cooker tests), unexpected failure modes that will never occur in the field (for example, pin-to-pin migration on outer leads) can occur because the semiconductor product may be exposed to conditions in which dew is formed. Consequently, care must be taken when performing assessments or when evaluating test results.

In addition, recently the mainstream semiconductor product has become the surface mounted device (SMD), accelerating compact and thin designs one step further. With these types of semiconductor products, the thermal stress during mounting and resin humidity absorption during storage cannot be ignored. To properly simulate actual usage conditions, the mounting stress is applied as part of a pretreatment process, and a humidity resistance test is conducted.

Table 3-3-4-1 Main Moisture Resistance Evaluation Test Methods

	Test		Example Conditions
Storage Test	High temperature high humidity storage test		85°C/85% RH 60°C/90% RH
	Pressure cooker test (or called Unbiased autoclave test)	Saturation type	121°C/100% RH 127°C/100% RH
		Non- saturation type	120°C/85% RH 130°C/85% RH
Biased Test	High temperature high humidity biased test		85°C/85% RH Biasing applied
	High acceleration stress test		130°C/85% RH Biasing applied

3-3-4-2. Moisture Resistance Acceleration Model

There have been a number of reports of accelerated models for estimating the reliability of plastic-encapsulated semiconductor devices based on humidity resistance test data. The model described in this section is the absolute water vapor pressure model. The relationship between lifetime and absolute water vapor pressure in the absolute water vapor pressure model[2)] is expressed by the equation below. The acceleration coefficient n is approximately 2.0 according to experimental data.

$$L = A \cdot V_p^{-n}$$

L: Moisture resistance lifetime (h)
Vp: Absolute water vapor pressure (Pa)
n: Accelerated coefficient
A: Experimental constant

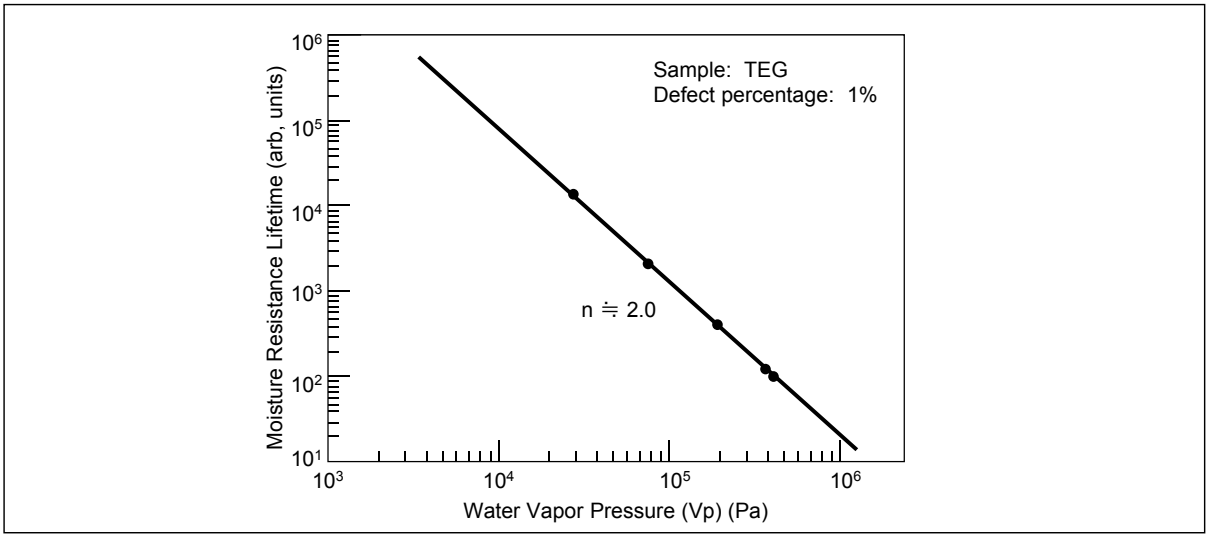


Figure 3-3-4-2 Example of Relationship Between Absolute Water Vapor Pressure and Moisture-Resistance Lifetime

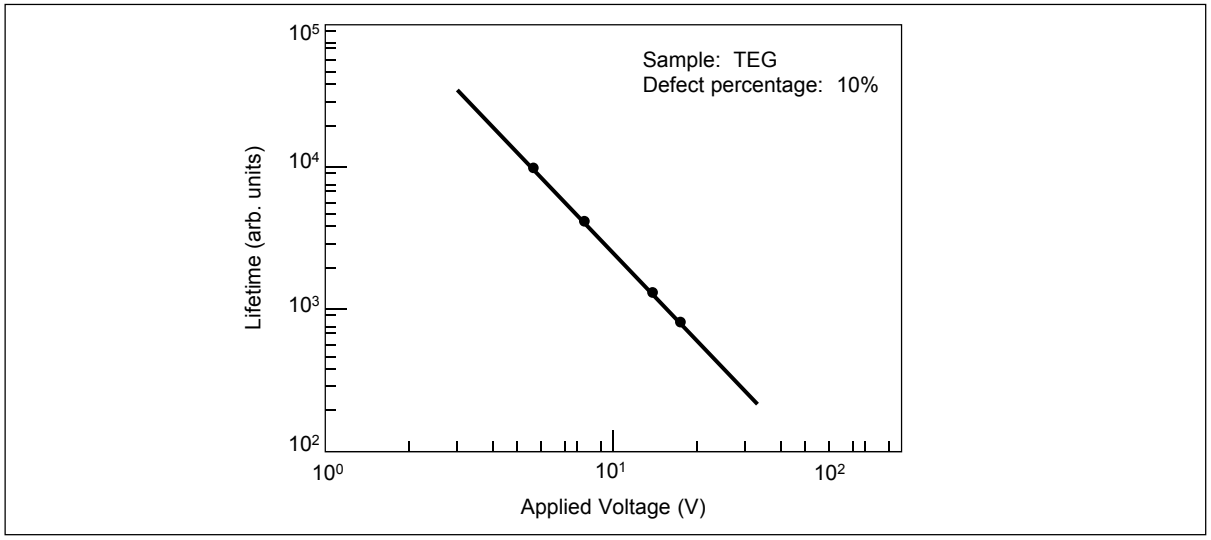


Figure 3-3-4-3 Example of Relationship Between Applied Voltage and Lifetime for Humidity and Resistance Test

Figure 3-3-4-3 shows an example of the relationship between applied voltage and lifetime in a humidity resistance test.

Moisture-resistance lifetime in the field can be estimated from acceleration test results by taking into consideration temperature, relative humidity and applied voltage conditions as well as the failure mechanism.

3-3-5. Voltage

Failure modes such as oxide film breakdown, hot carriers, Al corrosion and characteristic degradation due to mobile ions are accelerated by voltage. Of these, the failure mode that appears most dominantly as a result of voltage acceleration is oxide film breakdown. When a constant electric field is continuously applied to the oxide film, breakdown occurs over time, even if the electric field in the oxide film is below the breakdown limit.

The voltage acceleration model [3)] for time dependent dielectric breakdown (TDDB) can be expressed using the following equation, given time to failure TF and the voltage applied to oxide film V. Case examples have been obtained where the TDDB lifetime for a thick oxide film (film thickness: 5 nm or greater) is dependent on the electric field. In such a case, calculations can be performed by replacing voltage with the electric field.

$$T_F = A \exp(-\beta_V \cdot V)$$

or

$$T_F = A \exp(-\beta_E \cdot E)$$

TF: Time to failure
V: Voltage applied to oxide film
E: Electric field applied to oxide film
A: Constant
β_V: Voltage acceleration constant
β_E: Electric field acceleration constant

Therefore, using an example where the lifetime is dependent on the electric field and assuming the time to failure at E_1 and E_2 to be T_{F1} and T_{F2}, respectively, the acceleration rate A_F can be expressed as:

$$A_F = \frac{T_{F2}}{T_{F1}} = \exp\{-\beta_E(E_2 - E_1)\}$$

The time-dependent dielectric breakdown of oxide film can be tested by the following:

(1) Constant voltage test
(2) Step stress test
(3) Constant current test

These tests can be summarized as follows:

(1) Constant Voltage Test

A constant voltage stress test applies constant stress to the oxide film to evaluate the breakdown distribution over time.

In general, the TDDB lifetime distribution varies greatly and depends largely on voltage. Therefore, it can take an extremely long time to obtain results using this method and the failure distribution may not be clear. A step stress test can be performed to cope with this problem.

(2) Step Stress Test

The step stress test applies voltage to the oxide film in increased infixed steps at constant intervals to evaluate where breakdown will occur. The test produces results in a short period of time and the TDDB acceleration equation can be used to find out the overall failure distribution of the oxide film.

(3) Constant Current Test

The constant current test evaluates the failure distribution of the oxide film by applying a constant current as stress, based on the theory[4)] that the amount of electrical charge that passes through the oxide film until it breaks down will be constant. This test is not commonly used for oxide film lifetime estimations since usage conditions are expressed in terms of voltage or electric field intensity.

However, it is generally used for oxide film quality evaluation since standardized data is obtained.

Figure 3-3-5-1 shows the data for a constant electric field test performed by Toshiba. This data is an example for oxide film used in a Toshiba product. The applied electric field for the oxide film of the product is 3.125 MV/cm and the oxide film lifetime in normal use is 10 years or longer. The results of acceleration tests can be used in this manner to estimate the lifetime of oxide film in the field.

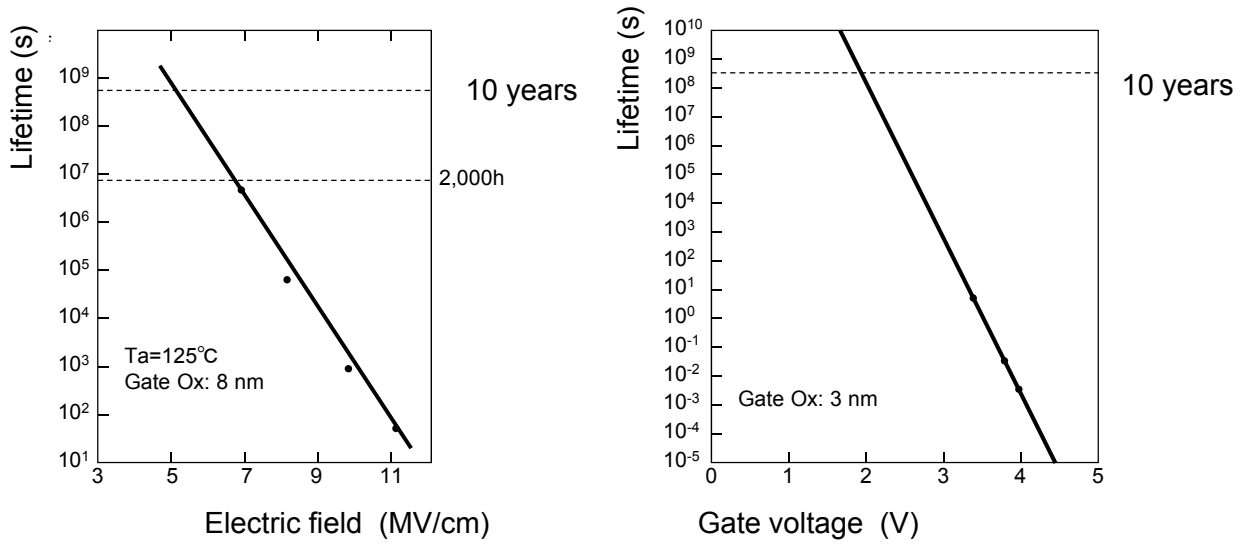


Figure 3-3-5-1 Examples of Constant Electric Field Test for Oxide Film

3-3-6. Temperature Difference

Tests for repeated thermal stress from the external environment or internal heat source include the temperature cycle test and thermal shock test. In these tests, the semiconductor product is subjected to repeated high/low temperature changes to determine temperature change resistance. The failure modes that occur during the tests include bonding opens, aluminum slide, passivation cracks, package cracks, chip cracks and characteristic fluctuation (due to piezo effects).

The temperature cycle test uses a gas as the heating medium, and the thermal shock test uses a liquid. In the temperature cycle test, the semiconductor product is generally subjected to its high and low storage temperature limits repeatedly. In some cases these limits are exceeded to achieve even greater acceleration. However, it should be noted that, because the test is conducted in product areas having different material physical characteristics, the behavior of the product during actual use may not match the test results.

Figure 3-3-6-1 shows the relationship between the number of cycles and the temperature difference found from the results of a temperature cycle test conducted by Toshiba. Temperature cycle test results can be obtained from the following equation:

$$N = A \cdot \Delta T^{-\alpha}$$

A: Constant
α : Acceleration coefficient
N: Number of cycles

From these test results, α = 7.5 is obtained for the aluminum slide failure mode and α = 5.0 is obtained for the package crack failure mode. The lifetime in the field can be estimated from these acceleration coefficients.

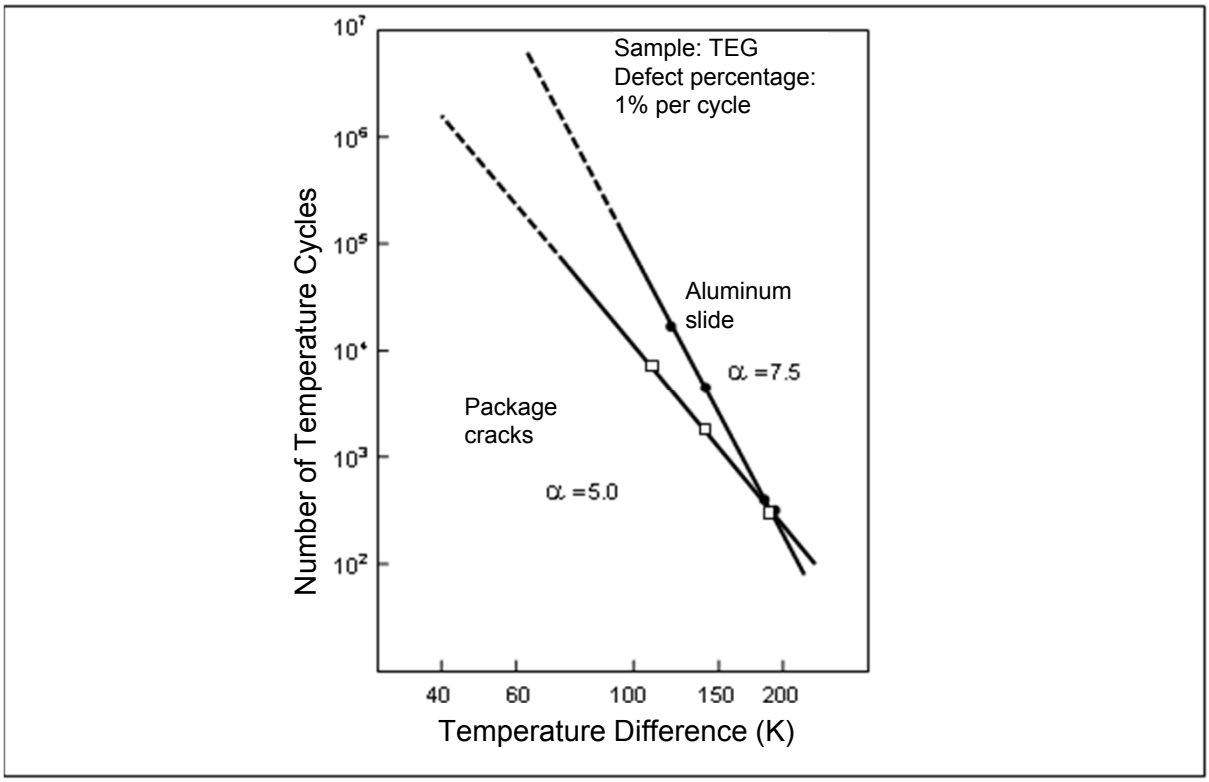


Figure 3-3-6-1 Relationship Between Number of Temperature Cycles and Temperature Difference

3-3-7. Current

Electromigration is the most well known current acceleration mode and is becoming more important as a failure mechanism as devices decrease in size and become highly integrated. [5)6)] The mechanism produced by electromigration is a phenomenon in which metal atoms in metallization move when current is applied. When the metal atoms move, metallization breakdown results. The electromigration lifetime is generally expressed as the median time to failure (MTF) using the following equation [7)].

$$MTF = AJ^{-n}\exp\left(\frac{E_a}{kT}\right)$$

J: Current density
n: Constant related to current
Ea: Activation energy
T: Absolute temperature
k: Boltzmann's constant
A: Constant related to metallization material, structure and dimensions

The DC constant current stress test is the most popular test method. Other tests available include the DC pulse current stress test, AC pulse current stress test and the DC constant voltage stress test.

The following describes the data of an electromigration experiment conducted by Toshiba. Figure 3-3-7-1 shows the relationship between current density and lifetime. From this figure, it is evident that as current density gets larger, lifetime gets shorter.

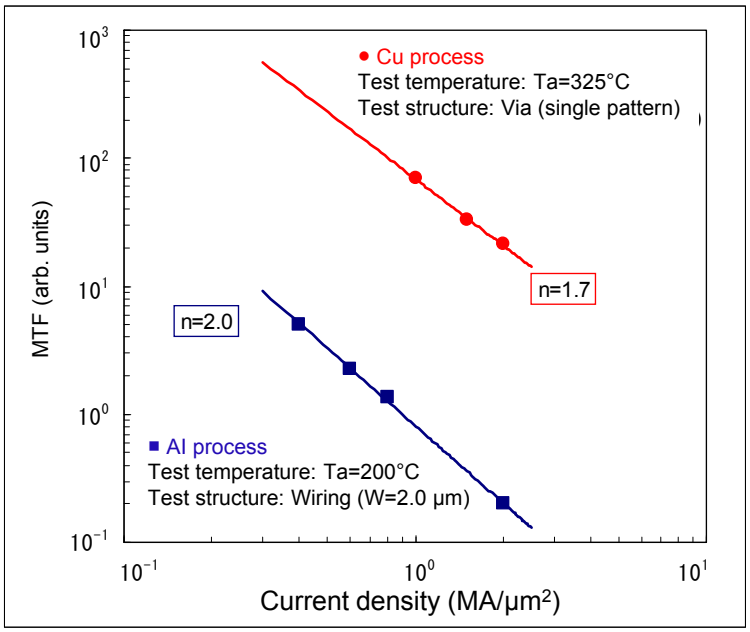


Figure 3-3-7-1 Relationship Between Electromigration Lifetime and Current Density (Example)

[Bibliography]

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Chapter 4 Failure Analysis

Chapter 4 Failure Analysis

4-1. Significance of Failure Analysis

As described in previous chapters, the causes and mechanisms of semiconductor-product failures are complex due to the involvement of various reliability factors. Toshiba makes every effort to enforce reliability control in its semiconductor manufacturing process based on the thorough investigation and comprehensive analysis of factors affecting reliability as well as problems that occur in the manufacturing process and in the field. Still, it is impossible to completely eliminate all failures. When a failure does occur, failure analysis is performed to identify the cause and action is promptly taken.

Some failures occur in the manufacturing process, others are identified during evaluation and inspection, and others arise in the field as a result of the passage of time or the environment. Failure analysis is performed in all of these cases.

In addition to identifying failure causes and mechanisms, failure analysis also involves various chemical and physical analyses for extracting and controlling parameters affecting reliability, beginning from the initial stages of the manufacturing process. The results are applied to the identification of manufacturing process conditions and the development of process control techniques. This failure analysis has become an important technical field within semiconductor production technology.

To correctly identify failure causes and mechanisms, failure analysis must be performed using various analytical instruments in accordance with detailed analytical procedures. This requires analytical techniques and experience based on breadth of knowledge of physics and chemistry as well as a physical understanding of the semiconductor itself.

When performing failure analysis, the following points must be considered:

(1) What are the symptoms of the failure, and when, where and under what circumstance did they appear? Is the failure repeatable? (Failure mode)

(2) Where is the failure located and what kind of stress was applied at the location? (Failure mechanism)

(3) Has the same failure occurred in the field? Is the probability of the failure predictable from the failure model? (Statistical analysis)

(4) Appropriate corrective action must be taken to prevent failure recurrence by developing techniques for controlling manufacturing process parameters sensitive to reliability and providing feedback to the manufacturing process.

(5) Ideally, failure analysis methods and strict reliability control must be utilized to estimate and identify the reliability of products without conducting evaluation tests.

Chapter 4 Failure Analysis

4-2. Instruments Used in Failure Analysis

Failure analysis of semiconductor products requires highly precise, highly sensitive analytical instruments capable of enabling observation at the nanometer and micrometer level. Such instruments can be used for measuring electrical characteristics, identifying failure locations and analyzing failure mechanisms. Table 4-2-1 lists instruments of high applicability that are used in failure analysis.

Table 4-2-1 Instruments Used in Failure Analysis

	Instrument	Analytical Application
Electrical Characteristics	Curve Tracer	Identification of breakdown voltage, leakage
	Oscilloscope	Identification of functions, AC characteristics
	Tester	Identification of DC and AC characteristics, functions
	Nanoprobe	Evaluation of single device characteristics
Identification of Failure Points	Photo emission microscope (PEM)	Luminescent spot detection
	Scanning laser microscope (OBIC/OBIRCH methods)	Operation analysis
	EB Tester Analysis (Voltage Contrast)	Operation analysis
Observation	Stereo microscope	Outer appearance
	Metallurgical microscope	Chip inspection
	Infrared microscope	Chip backside inspection
	Scanning probe microscope (SPM)	Surface shape and characteristics inspection
	Scanning capacitance microscope (SCM)	Surface carrier concentration inspection
	Scanning atomic force microscope (AFM)	Surface shape inspection
	Scanning electron microscope (SEM)	Shape inspection
	Transmission electron microscope (TEM)	Minute structure analysis
	X-ray fluoroscopy	Internal inspection
	Scanning acoustic tomography	Delamination and void inspection
	X-Ray CT	Materials and Structure Inspection
Analysis	Electron probe X-ray microanalyzer (EPMA)	Elemental analysis, composition analysis
	Auger electron spectroscope (AES)	Surface elemental analysis, status analysis
	Secondary ion mass analyzer (SIMS)	Elemental identification, surface elemental analysis
	Time-of-flight secondary ion mass analyzer (TOF-SIMS)	Elemental/molecular identification, top surface analysis
	X-ray photoelectron spectroscope (XPS)	Surface elemental analysis, status analysis
	Fluorescent X-ray analyzer	Impurity analysis, composition analysis
	Fluorescence microscope	Fluorescent material analysis
	Fourier transformation infrared spectrometer (FT-IR)	Status analysis
	Electron beam diffractometer	Crystallization analysis
	X-ray diffractometer	Crystallization analysis, stress measurement
	Thermal analyzer	Material analysis
	Gas mass analyzer	Material analysis
Sample Processing	Focused ion beam (FIB)	Sample processing
	Grinder, polisher	Sample processing
	Ion milling system	Sample processing

Chapter 4 Failure Analysis

4-2-1. Measuring Electrical Characteristics

In general, a curve tracer or similar device capable of measuring current-voltage characteristics is used to check for opens, shorts and breakdown voltage degradation. In addition, an oscilloscope is handy for conducting simple A/C characteristics checks.

Testers, such as large general-purpose testers for LSI, memory testers and linear IC testers, are used according to the device tested. Measurements obtained from the device are used to diagnose failures or analyze the circuit failure location based on comparisons with standard values.

4-2-2. Identifying the Failure Location

The first step in failure analysis is critical: identifying the failure location. There are several ways to do this.

A scanning infrared detector is used to find abnormal temperature distributions within the chip. An emission microscope, which detect weak luminescence, is used to detect minute leakages.

The methods used to analyze the operating state of a semiconductor product include the electron microscope based EBIC method and the scanning laser microscope based OBIC or OBIRCH method for PN junction electrical potential analysis, and the EB tester based voltage contrast method for wire electrical potential analysis.

4-2-3. Observing the Failure

In addition to metallurgical and stereo microscopes, the scanning electron microscope (SEM) and transmission electron microscope (TEM) are essential for identifying and inspecting failure locations. An infrared microscope and X-ray inspection system also provide critical information. In addition, the scanning tunnel microscope (STM) and atomic force microscope (AFM), which provide data up to the atomic level, are used.

4-2-4. Analyzing Elements[1)]

Solid surface analysis is particularly an effective means in semiconductor failure analysis. As shown in Figure 4-2-4-1, the principle generally involves projecting an excitation source, such as an electron beam, ion beam or electromagnetic wave (such as an X-ray) onto a solid surface, and then conducting elemental and chemical state analyses of the surface (or bulk) using the X-ray, secondary ion or Auger electron signals ejected by the excited material as the signal source.

Table 4-2-4-1 summarizes the characteristics of the solid surface analysis methods (systems). Of the equipment listed in the table, the electron probe X-ray microanalyzer (EPMA), Auger electron spectroscope (AES), secondary ion mass spectrometry (SIMS), X-ray photoemission spectroscope or electron spectroscope (XPS or ESCA) and the fluorescence X-ray spectroscope are frequently used. Use is determined by application, taking into consideration the area to be analyzed and sensitivity.

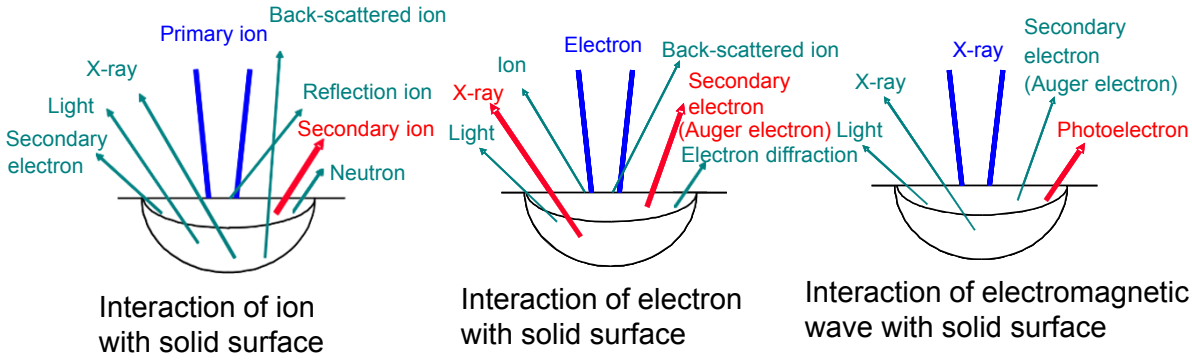


Figure 4-2-4-1 Interaction of Ion, Electron and Photoelectron (X-ray) with Solid Surface

Table 4-2-4-1 Comparison of Physical Surface Analysis Methods

Excitation Source	Signal Source	Analysis Technique	Data Obtained	Features/Other
Electron	Reflected primary electron	Low-speed electron energy loss spectroscopy (LEELS)	Adsorption state	Uses low-energy electrons of several eV. Shows vibration state of adsorbed molecule.
	Auger electron	Auger electron spectroscopy (AES)	Elemental analysis, bonding energy, state analysis based on chemical shift	A spectrum does below auger electron occurring by electron beam irradiation of the 3 - 20KeV degree that converged number of the diameters 10nm, and the measurement is possible at the top surface (2-3nm) in a micro area of the μm order.
	Ion	Electron impact drift method	Elemental analysis of adsorbed material.	Impact of minute current applied to surface removes adsorbed ions, performing mass separation.
	Characteristic X-ray	X-ray microanalyzer (EPMA)	Elemental analysis of minute area	Commonly used in microanalysis. Detectable depth is 2-3 μm
	Light	Cathode luminescence	Electron beam excited electron -electron hole re-coupling luminescence	Measures defects, precipitation, impurity precipitation and carrier diffused layers.
Ion	Reflected ion	Ion-scattering energy spectroscopy (ISS)	Outermost surface layer atomic structure, elements	Performs scattering primary ion energy separation using low-speed ions (100eV to several eV).
	Back-scattered ion	Rutherford backscattering spectroscopy (RBS)	Composition, elemental analysis, depth distribution	Measures energy of back-scattered ions using H+ or He+ of several hundred eV to several MeV.
	Secondary ion	Secondary ion mass analysis (SIMS)	Microanalysis, depth distribution	Thin film, surface analysis, microanalysis of bulk, concentration depth analysis
	Characteristic X-ray	Particle induced X-ray emission	Elemental analysis	Simultaneous multielement analysis at high sensitivity
X-ray, Ultra-violet ray	Photoelectron	Photoelectron spectroscopy (XPS) Vacuum ultraviolet electron spectroscopy (UPS)	Elemental analysis, electron coupling energy	Conducts electron coupling energy and elemental analysis by measuring photoelectron energy.
X-ray, Soft X-ray	Secondary X-ray	Fluorescence X-ray analysis	Elemental analysis	Enables quick analysis.
		Soft X-ray analysis	Electron state	Measures electron state of atom by irradiating with soft X-ray.
Pulse voltage	(Field Evaporation) ion	Three-dimensional atom probe analysis (3DAP/APT)	Three-dimensional atom distribution	・Three-dimensional element map is got in the resolving power of the atom level.

4-2-5. Sample Processing

Surface and cross-sectional observation and analysis of specific locations (failure locations) in the LSI are necessary in failure analysis. These types of observations and analyses require a precision processing method for samples. For this, a focused ion beam (FIB) system and precision polishing equipment capable of polishing in the chip state are utilized.

4-3. Failure Analysis and Reliability Improvement Measures

As described in Section 4-1, the purpose of failure analysis is to maintain the reliability required of a semiconductor product. Therefore, failure analysis includes the following objectives:

(1) Investigate the cause of failures that occur during trial production and evaluation and feed back the results to the design process so that reliability can be designed in at the process development stage.

(2) Investigate the cause of failures that occur in the manufacturing process and feed back the results to the manufacturing process to ensure mass production of the developed semiconductor product at stable quality and reliability levels. Strive to continuously improve quality and reliability in the manner.

(3) Investigate failures that occur in the field to determine whether the cause lies in the semiconductor product or in inappropriate use, such as overvoltage, noise or thermal stress, and give proper feedback. If a problem exists with the product, corrective action must be taken, tracing the product's history back to the design or manufacturing process. Figure 4-3-1 illustrates this procedure.

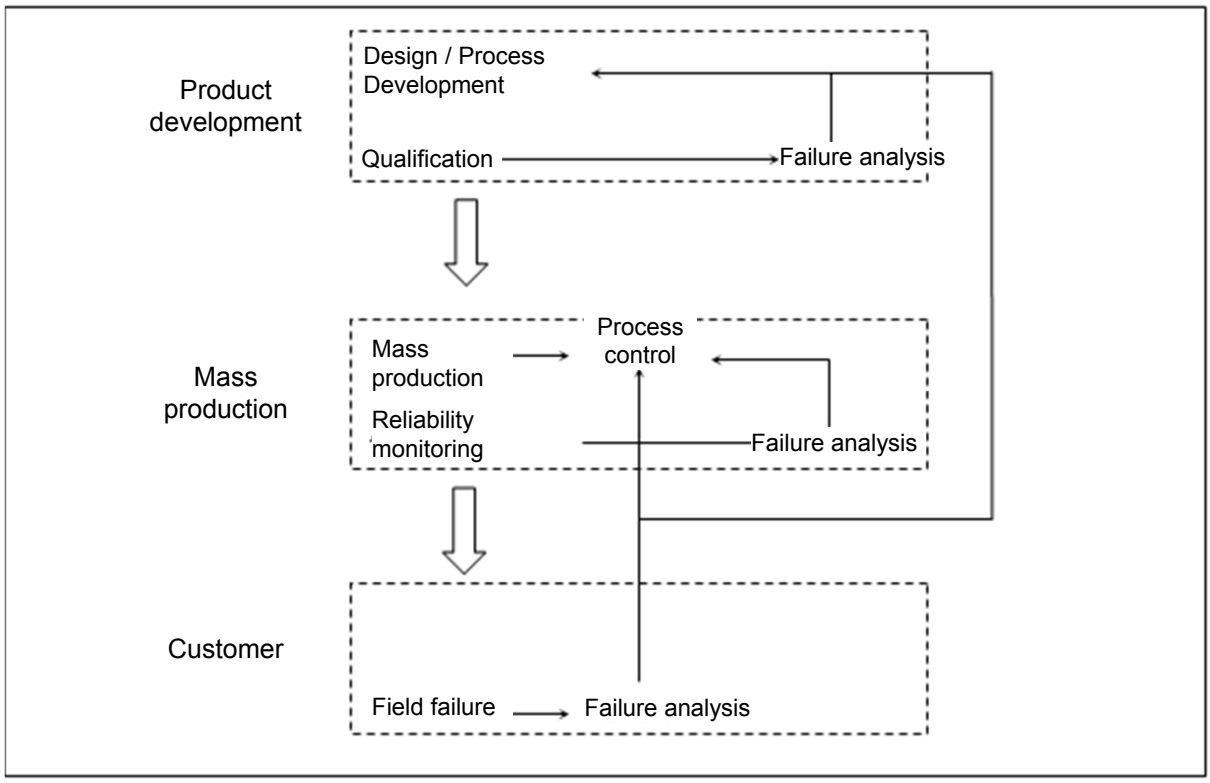


Figure 4-3-1. Procedure for Improving Reliability by Failure Analysis

Chapter 4 Failure Analysis

4-4. Failure Analysis Procedure

4-4-1. Failure Analysis Procedure for General Semiconductor Products

When performing failure analysis, it recommends to take a systematic approach. An example is shown in Figure 4-4-1-1.

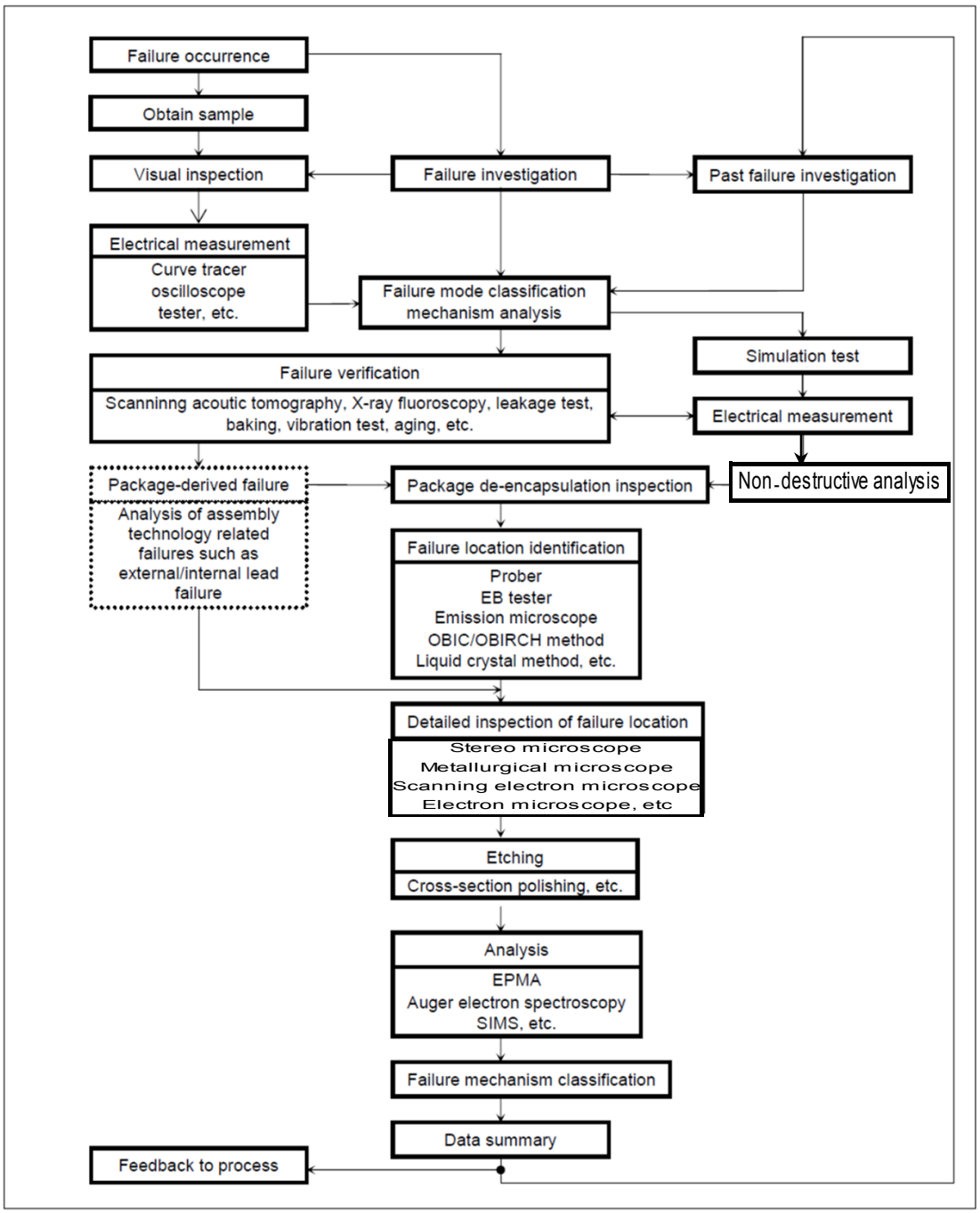


Figure 4-4-1-1. Example of Failure Analysis Procedure

Chapter 4 Failure Analysis

To obtain the data required for determining the failure mechanism, analysis should follow the flow shown.

Refer also to the failure analysis procedure defined in MIL-STD-883, Method 5003.

As soon as a failure sample is obtained, its history is investigated. Any related information, including manufacturing lot information (manufacturing date and storage period), failure information (whether the failure is total or intermittent, correlation to lot, failure rate), operating conditions (circuit conditions, thermal stress, mechanical stress) and environmental conditions (temperature, humidity, location, atmosphere), should be collected to aid in failure mechanism identification and simulation testing. Advance preparation of good samples for comparison with faulty samples is also an effective means of failure cause identification.

During the visual inspection, the exterior of the package is examined visually or with a stereo or metallurgical microscope in detail. Various failures can be identified in this way, allowing you to check abnormalities such as package cracks, migration between leads, rust or mechanical damage on leads. Surface elemental analysis is conducted as needed as part of the solid surface analysis described above in order to identify the failure cause.

Electrical characteristics are measured using a curve tracer, oscilloscope and testers, and the data is recorded. The quickest way to obtain failure mode data is by measuring the characteristics between terminals using a curve tracer. The failure mode is classified and the failure mechanism is analyzed based on a summary of failure investigation results, visual inspection results, electrical characteristics measurement results and past case examples and statistical data. Failure modes are broadly divided into three classifications: opens, shorts and degradation. Subsequent testing and analytical methods are determined based on this failure mode classification and failure mechanism estimation.

Chapter 4 Failure Analysis

Before the semiconductor product is de-encapsulated, baking, retesting, vibration testing, etc., are performed as needed to determine the failure mechanism. Also, an internal inspection by X-ray fluoroscopy is carried out prior to de-encapsulation to check wires and leads for opens and shorts.

The de-encapsulation method used to open the package is selected according to the presumed failure mechanism so as to enable semiconductor chip observation and analysis. If the de-encapsulation method is inappropriate, the necessary data may not be collectable, resulting in the failure cause to be left as unknown. Therefore, special precautions must be taken during package de-encapsulation.

De-encapsulation methods include: [1] dissolving using chemicals, [2] mechanical removal, and [3] incineration using a plasma reactor.

For ceramic and metal packages, mechanical de-encapsulation is easily achieved since no special equipment or tools are required.

The de-encapsulated sample is preferably analyzed immediately. However, if this is not possible, measures such as storing the sample in a desiccator need to be considered to prevent contamination and mechanical damage after de-encapsulation.

The most convenient and quick way of observing internal conditions in detail is with a metallurgical microscope. A stereo microscope can be used to examine bonding and mounting conditions, and a scanning electron microscope can be used to make observations and take photographs at high magnification.

If the cause of failure cannot be assessed by microscope observation, elemental analysis and state analysis of the failure location are performed. Optimal methods and the equipment, such as EPMA, AES or SIMS, are selected according to purpose.

If the failure location cannot be assessed by internal state observation, other techniques such as wire electrical potential measurement using an EB tester, emission microscope analysis, OBIC method or IR-OBIRCH method are considered effective means for failure location identification. Furthermore, etching, cross-sectional cuts or specific cross-sectional cuts of detailed areas by FIB processing are used to examine the failure location and determine the failure mechanism.

Results obtained from the above analyses are fed back to the manufacturing process and stored in a data bank as failure case examples for the purpose of improving the device and enhancing reliability.

4-4-2. Identifying Failure Locations in LSI

With recent trends in miniaturization, increasing multilayer wiring, increasing scales, faster speeds and increasing complexity, failure location identification has become increasingly difficult for LSIs. As a result, various LSI failure location identification techniques have been developed.

Figure 4-4-2-1 shows the general flow of failure location identification. The first step after failure occurrence is to reproduce the failure using some type of method. A study is then conducted to determine the optimum analytical method by the failure type. Once the method is selected, physical observations are made using analytical tools and instruments and the failure location is identified.

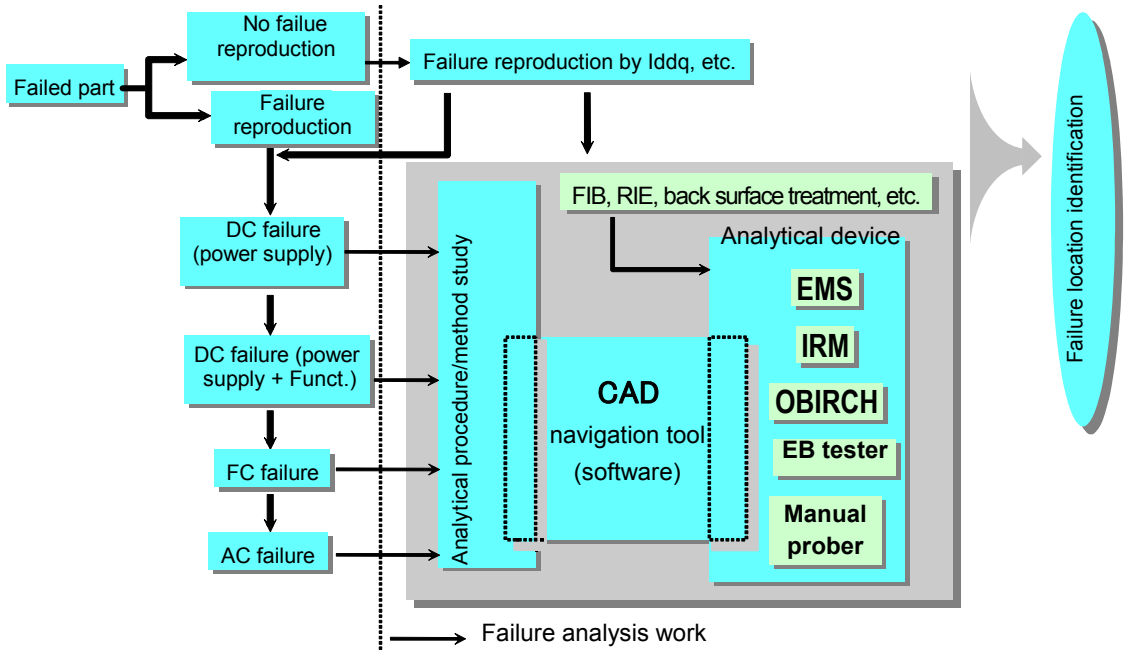


Figure 4-4-2-1 Flow of Failure Location Identification

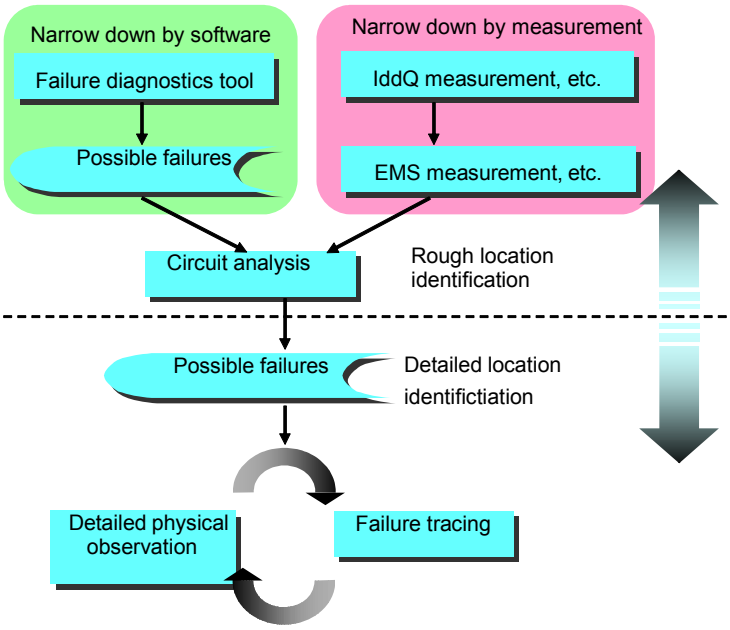


Figure 4-4-2-2 Failure Analysis Flow

Figure 4-4-2-2 shows a detailed view of the failure analysis flow after failure reproduction. Although the tools and analytical instruments used differ according to failure type, in general the failure location is identified by roughly narrowing down the failure location (the analysis target) using software and other tools and physical observations, and then analyzing and conducting detailed physical observations of the circuits of the resultant area.

Naturally, depending on the failure, the failure analysis flow will not necessarily proceed in this manner; the step of roughly identifying the failure location may be repeated or, conversely, may be used to identify the detailed failure location.

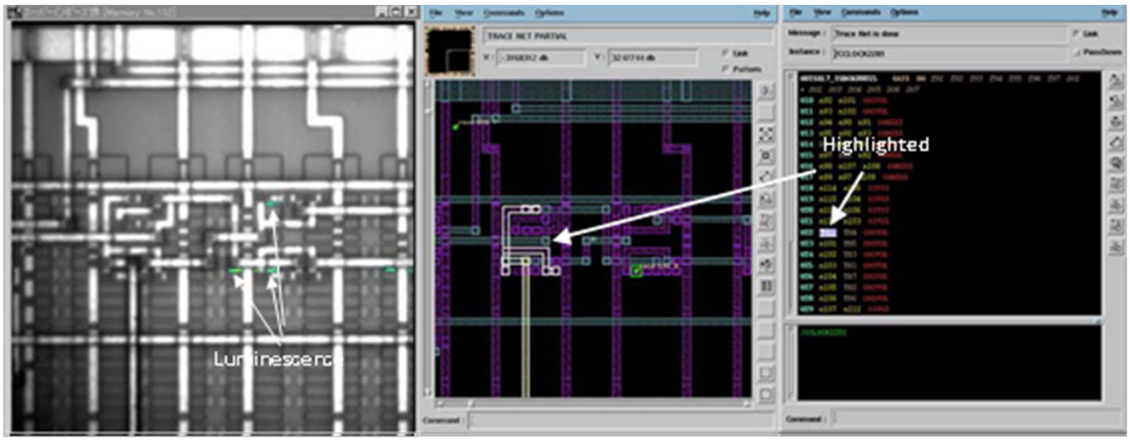
4-4-2-1. CAD Navigation System

When identifying a failure location, it is necessary to observe the circuit of the semiconductor product you want to examine using an analytical instrument or identify a circuit location observed. To efficiently proceed with analysis over a short period of time, therefore, the target transistor or wire location to be observed or, conversely, the circuit area of the location that was observed must be promptly identified at the time of analysis. Yet, specifying the desired physical circuit location within a semiconductor product is extremely difficult without use of design information (circuit and layout data) due to the increased scale and integration of semiconductor products in recent years.

In cases such as this, the CAD navigation system is applied. This system allows you to link the semiconductor product's physical coordinates on an analytical instrument with design information to simply trace the circuit without knowledge of layout design.

Figure 4-4-2-3 shows a display example of the CAD navigation system. In this figure, a) shows the observation screen for the emission microscope (EMS), b) the mask layout, and c) the circuit net list (equivalent to a circuit diagram that indicates the electrical connection relationship using text). The CAD navigation system enables observation screen and mask layout display interactive synchronization. Furthermore, the CAD navigation system also enables interactive synchronization of the mask layout and net list, indicating the corresponding wire and signal name by highlighting them in white, as shown in the figure.

By utilizing the CAD navigation system in this manner, the user can promptly identify the wiring location and chip location of the signal s/he wants to observe or, conversely, the layout location and circuit area of the location observed using an analytical instrument, thereby increasing analysis efficiency. In addition, while this example shows the EMS observation screen, other analytical instruments can be used in the same manner.



a) Observation Screen (EMS)　b) Mask Layout View　c) Net List View

Figure 4-4-2-3 CAD Navigation System Display Examples

4-4-2-2. Diagnostic Tool

To identify a failure location, a failure analysis instrument is required. This instrument allows you to conduct detailed investigations that will identify, for example, the location of a faulty transistor when a transistor fails. However, today's semiconductor products contain hundreds of millions of transistors. To identify the defective location by examining each transistor one by one is unrealistic. Since failure analysis instruments are more geared toward detailed analyses, it is important to first accurately narrow down the area to be observed so as to abbreviate the failure analysis TAT.

The diagnostic tool is used for this purpose. The diagnostic tool basically uses design information (circuit and mask layout information), test patterns and test results to logically narrow down possible locations of failure.

While many diagnostic methods have been proposed and developed into tools, the diagnostic method explained herein is the most basic method: one that employs a fault dictionary.

A simple explanation of a fault dictionary is provided below.

When testing a semiconductor product, a test pattern is used. This test pattern contains semiconductor-product input signals and expected output values. A diagnostic tool compares the expected value with the value actually output by the semiconductor product, assessing the semiconductor product as good or faulty based on whether or not the values are the same.

When the above-described test pattern is introduced into the semiconductor product, it is possible to examine by logic simulation whether or not the output value is faulty based on failure scenarios for the signals within the circuit. A fault dictionary is developed for products that involve a large number of signal failure scenarios that are known to result in faulty values. This dictionary summarizes when each faulty output value will occur for each presumed failure location. Figure 4-4-2-4 shows an example of a fault dictionary.

Figure 4-4-2-5 shows the method for extracting potential failures using the fault dictionary. For example, when a test pattern is introduced into a semiconductor product, fail time information is obtained as a part of the test result. The fault dictionary is then used to examine signal failure scenarios for failures detectable at a fail time matching the fail time in the test result. In this example, the fail times of signals IN2 and IN3 are the same as that of the test result. These two signals are therefore extracted as possible failure locations.

While the example shown here is an extremely simple example, various techniques are incorporated in the diagnostic tool to further improve the accuracy of identifying possible failure locations. At present, however, diagnostic tools do not necessarily provide the answers for all failures that occur within a semiconductor product, and cannot necessarily be used alone to identify failure locations. The diagnostic tool, however, can be used to narrow down the locations that should be examined using analytical instruments as described above, and is therefore extremely important in failure analysis.

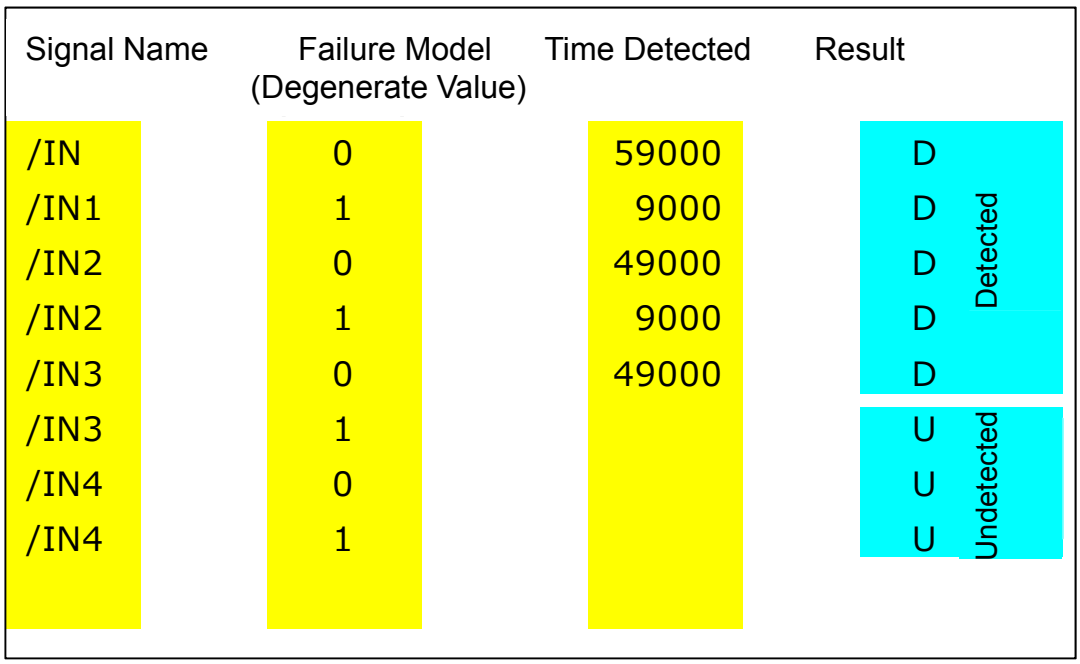


Figure 4-4-2-4 Fault Dictionary Example

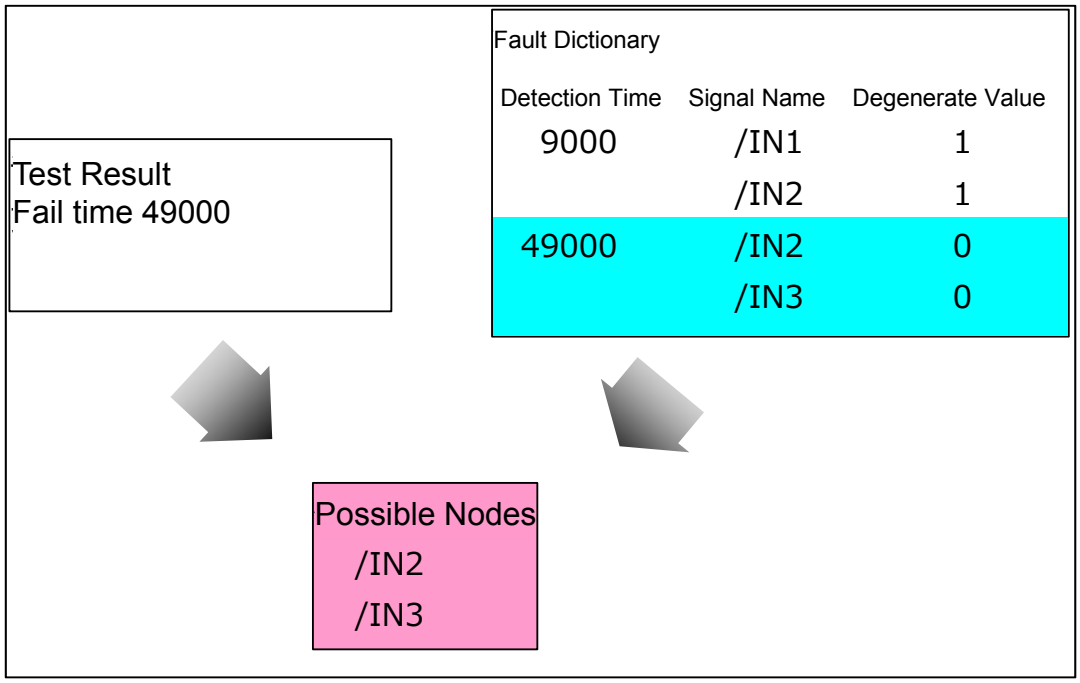


Figure 4-4-2-5 Example of Extraction of Possible Failure Locations Using Fault Dictionary

4-5. Layer Analysis

Since the IC is composed of multilayered wiring, we cannot confirm defects in the lower layer from the chip surface. Therefore, repeat the observation and removal of each layer, and confirm the presence or absence of defects. For removal of metal wiring and inter-layer insulating film, surface polishing, wet etching, or dry etching is used.

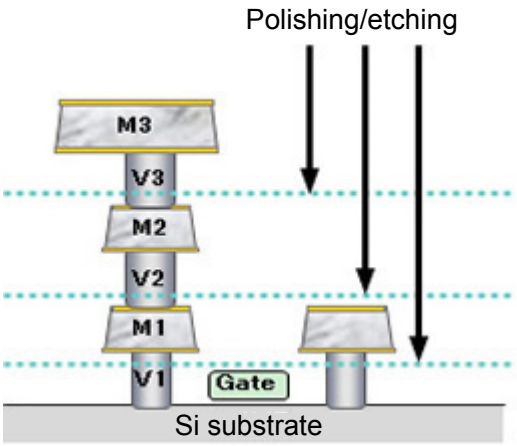


Figure 4-5-1. Image of Layer Analysis

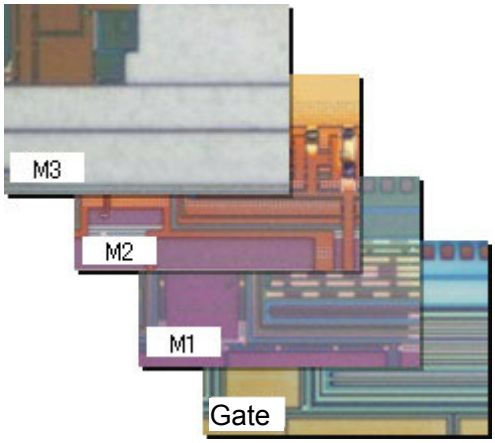


Figure 4-5-2. Observation Example of Each Layer

When layer analysis confirms defects such as foreign particles, wire breakage, or traces of breakdown, FIB processing or polishing is performed in the direction (cross section, plane) suitable for observing the defect, and SEM or TEM performs observation and analysis.

FIB : Focused Ion Beam

SEM : Scanning Electron Microscope

TEM : Transmission Electron Microscope

Chapter 4 Failure Analysis

4-6. Examples of Failure Analysis

This section describes the representative failure analysis methods and results using the following 20 examples:

(1) Failure location identification using an emission microscope

(2) Si chip backside analysis using an infrared emission microscope (IR EMS)

(3) Failure location identification using IR-OBIRCH

(4) Single element failure analysis using a nanoprobe system

(5) Failure location identification using an emission microscope and EB tester

(6) Gate oxide film breakdown analysis using SEM

(7) Interlayer particle analysis

(8) TEM cross-sectional analysis of failure location identified using OBIC

(9) Analysis of fine particles in LSI using Auger electron spectroscopy (1)

(10) Analysis of fine particles in LSI using Auger electron spectroscopy (2)

(11) Coupling status analysis of minute part using XPS

(12) Junction analysis using SCM

(13) Leak location identification using conductive AFM

(14) Analysis of bonding pad corrosion

(15) Analysis of package crack by reflow of surface mounted product

Chapter 4 Failure Analysis

4-6. Examples of Failure Analysis (Continued)

(16) Analysis of a surface-mount product soldering failure by board used

(17) Failure analysis of power MOS FET

(18) Failure analysis of SiC compound semiconductors

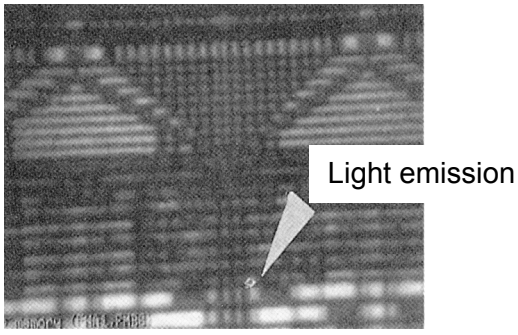
(19) Nondestructive observation of internal structure by scanning acoustic microscope (SAM)

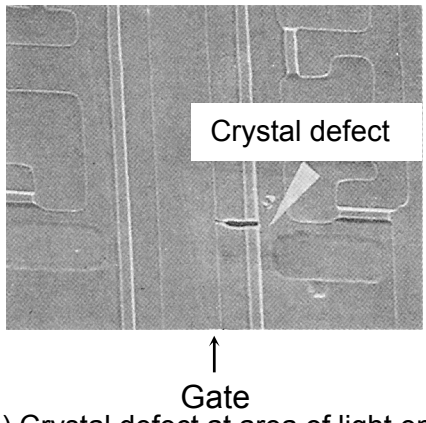
(20) Nondestructive observation of internal structure by 3-dimensional X-ray microscope (X-ray CT)

(21) Failure location identification using applied analysis(DLS analysis) of IR-OBIRCH (DLS:Dynamic Laser Stimulation)

(1) Failure Location Identification Using an Emission Microscope

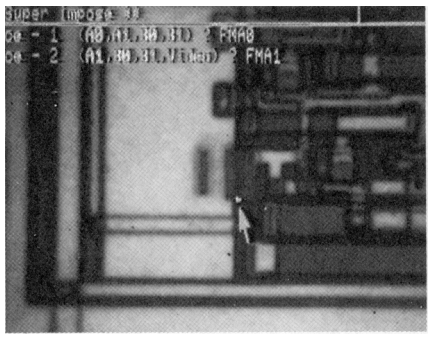
Purpose	To find out the cause of standby leakage failure during reliability test
Analysis and Result	Analysis was conducted using an emission microscope. Light emission was confirmed from the N-channel MOS in the address decoder circuit (Figure 4-6-1(a)). As a result of de-encapsulation, a crystal defect was found in the area of light emission. (Figure 4-6-1-(b)) With another sample, light emission was confirmed from the N-channel MOS in the AD converter front stage. (Figure 4-6-2-(a)) As a result of de-encapsulation, gate oxide film breakdown was confirmed in the area of light emission. (Figure 4-6-2-(b)) Failure mechanism is the n-channel MOS leakage due to crystal defect and gate oxide film breakdown (TDDB).

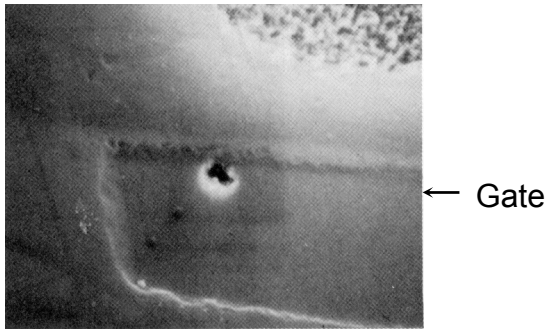




(a) Light emission from address decoder circuit (b) Crystal defect at area of light emission

Figure 4-6-1 Example of Standby Leakage Failure due to Crystal Defect





(a) Light emission from AD converter front stage circuit (b) Gate oxide film breakdown at area of light emission

Figure 4-6-2 Example of Standby Leakage Failure due to Gate Oxide Film Breakdown

(2) Si Chip Backside Analysis Using an Infrared Emission Microscope (IR EMS)[2)]

Purpose	To find out the cause of function failure during board mounting process
Analysis and Result	Light emission was detected from the Si chip backside when it was observed after mirror polishing using an IR EMS (Figure 4-6-3). Oxide film breakdown in the MOS capacitor was confirmed during observation after de-encapsulation using a scanning electron microscope (SEM) (Figure 4-6-4). Failure mechanism is oxide film breakdown due to ESD.

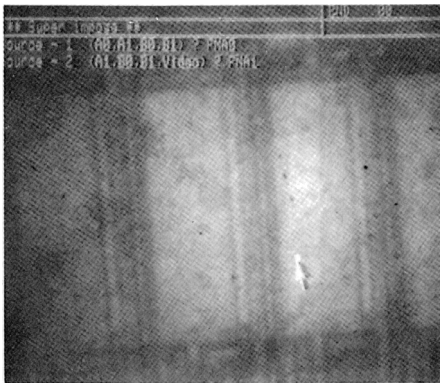


Figure 4-6-3 Overlapping of Light Emission and Pattern Images

(Emission Location Indicated by Arrow)

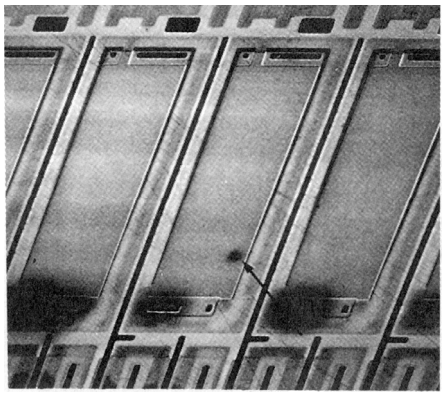


Figure 4-6-4 Oxide Film Surface after De-Encapsulation (SEM Image)

(3) Failure Location Identification Using IR-OBIRCH

Purpose	IR-OBIRCH identifies the failure location by scanning the sample surface using an infrared laser and then detecting any changes in resistance value caused by the laser. Compared with conventional methods such as the emission microscope, IR-OBIRCH offers higher detection sensitivity, enabling better identification of possible failure locations. IR-OBIRCH is not only effective in identifying the failure locations of shorts and electrical leakages, but also the failure locations of defects caused by high resistance.
Analysis and Result	The via-chain open failure location was identified using IR-OBIRCH. The failure location was detected based on the IR-OBIRCH data. As a result of TEM analysis of a cross-section of the location, the cause of failure was identified as a void in the via area.

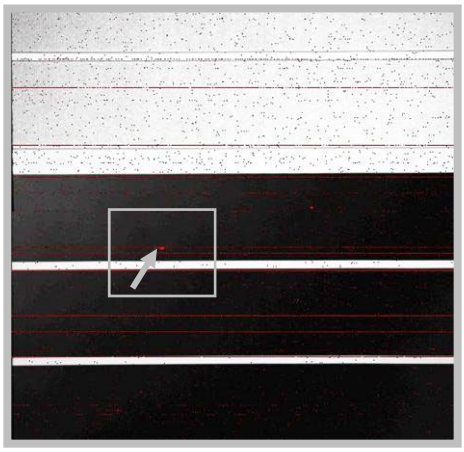


Figure 4-6-5 Example of Signal Detection By IR-OBIRCH

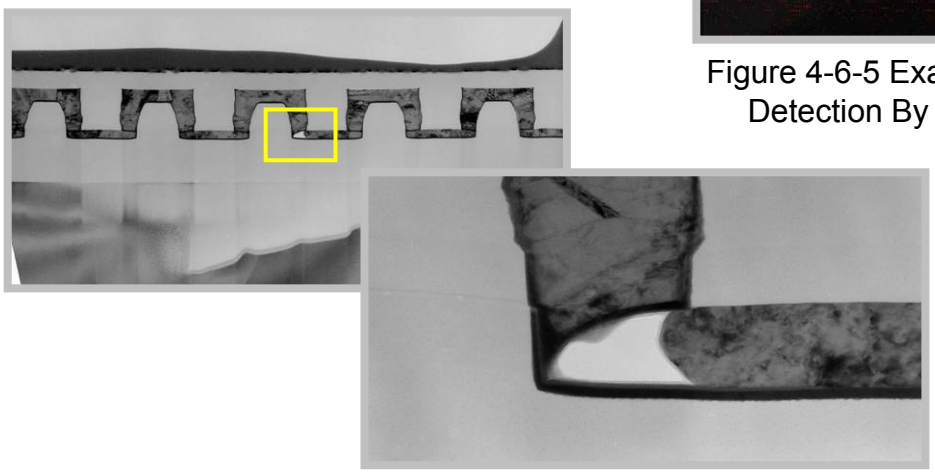


Figure 4-6-6 Result of Examining the Cross-Section of the Detected Location (TEM)

(4) Single Element Failure Analysis using a Nanoprobe System [3)4)]

Purpose

Direct contact was made with the electrode of the single transistor in the LSI and the electrical characteristics of the element were measured using a nanoprobe system. An investigation was conducted regarding the presence or absence of failure based on voltage – current characteristics and, by conducting comparisons with normal elements, the variance in characteristics caused by the failure. Although conventional technology requires preparation of a terminal for characteristics measurement by FIB processing, this system obtains element characteristics in a short period of time without resulting in damage.

Analysis and Result

The characteristics of the EEPROM write failure cell were measured using the nanoprobe system.

The faulty cell transistor's voltage – current characteristics between the substrate and the gate terminal used for data maintenance were compared with those of a normal cell transistor, resulting in the discovery that the leak current flowed from low voltage, thereby deteriorating write characteristics and causing poor data maintainability.

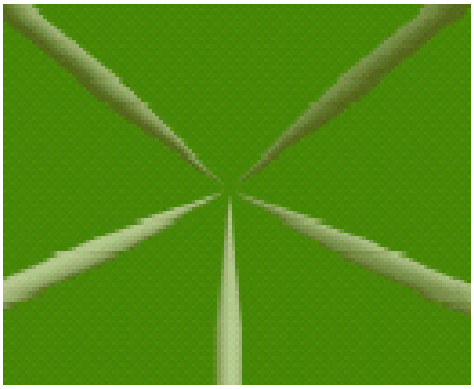


Figure 4-6-7 Photograph of Probe Terminal Tip of Nanoprobe System (Tip Diameter: 50 nm)

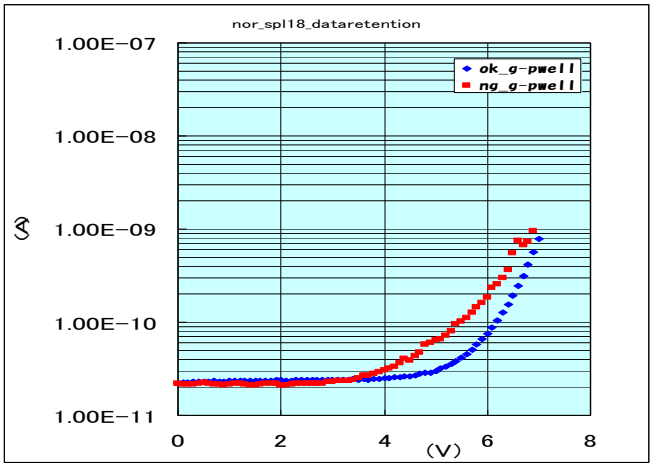


Figure 4-6-8 Voltage – Current Characteristics of Gate Terminal (Defective and Normal Cell Comparison)

(5) Failure Location Identification Using an Emission Microscope and EB Tester

Purpose	Function leakage failure during reliability test
Analysis and Result	With the IC set in a standby state, light emission from multiple locations was observed using an emission microscope. Furthermore, locations with open wiring were identified using an EB tester. Particles were subjected to cross-sectional processing using FIB, resulting in the identification of open Al metallization. Metallization that started to disconnect due to particles completely disconnected as a result of stress.

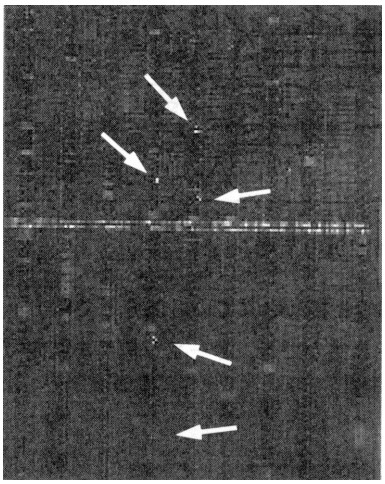


Figure 4-6-9 Light Emission Image by EMS

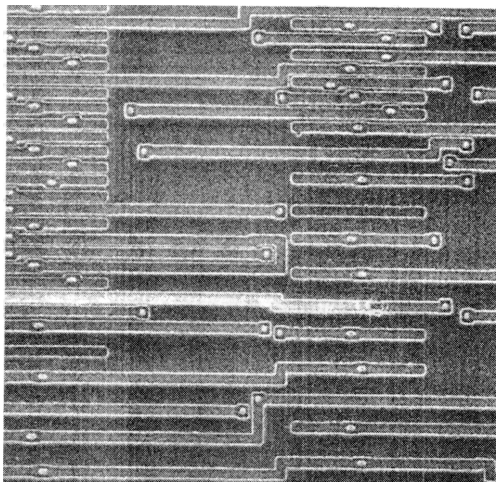


Figure 4-6-10 Observation by EB Tester

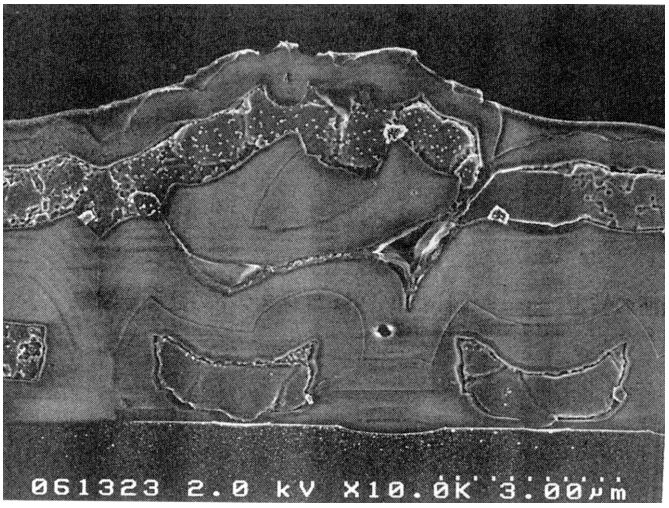
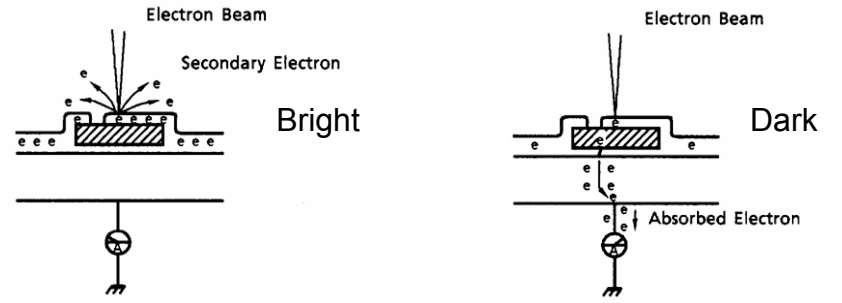


Figure 4-6-11 Cross-Section of Disconnected Location

(6) Gate Oxide Film Breakdown Analysis Using SEM [5)]

Purpose	Standby leakage failure during high-temperature operation product life test
Analysis and Result	Leakage (Figure 4-6-12) was confirmed between the gate electrode and substrate by removing the wiring connected to the gate electrode and employing a charge-up technique using SEM (Figure 4-6-13). Furthermore, gate oxide film breakdown was observed after gate electrode removal (Figure 4-6-14). Failure mechanism is the TDDB (Time Dependent Dielectric Breakdown) of oxide film.



(a) Normal Site (b) Abnormal Site

Figure 4-6-12 Identification of Gate Oxide Film Breakdown Location Using SEM [3)]

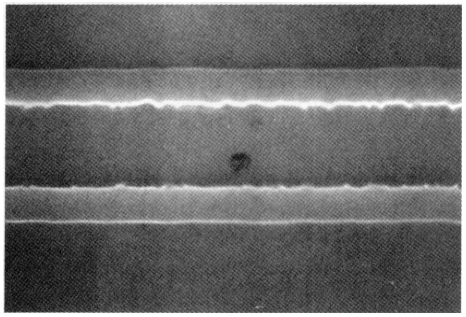


Figure 4-6-13 Example of Identification of Gate Electrode with Leak between Gate Electrode and Substrate

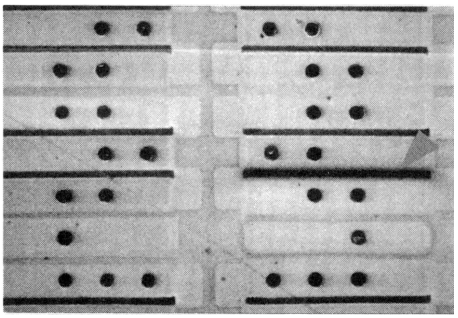


Figure 4-6-14 Gate Oxide Film Breakdown Location

(7) Interlayer Particle Analysis

Purpose	To find out the cause and location of Al metallization open due to particles.
Analysis and Result	Disconnected Al metallization opens were identified using the SEM charge-up technique, and a cross-section was prepared using an FIB and observed. The particle was identified using EPMA analysis. Al metallization was disconnected due to particle adhesion from the manufacturing equipment used in the interlayer formation process.

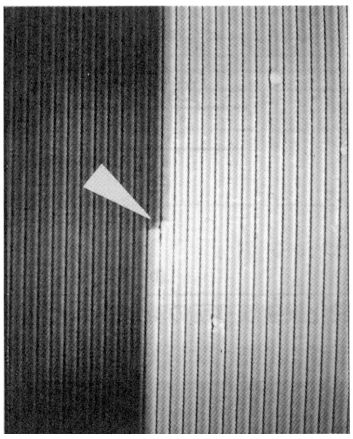


Figure 4-6-15 Identification of Open Location

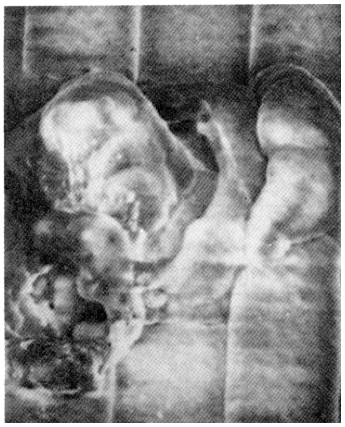


Figure 4-6-16 SEM Image of Particle

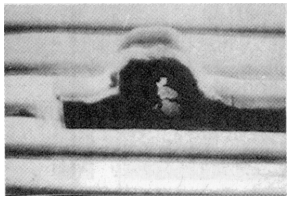


Figure 4-6-17 SEM Image

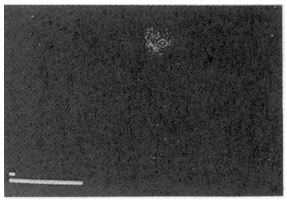


Figure 4-6-18 EPMA Fe X-Ray Image

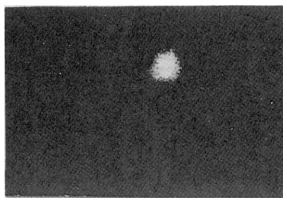


Figure 4-6-19 EPMA Cr X-Ray Image

(8) TEM Cross-Sectional Analysis of Failure Location Identified Using OBIC [6)]

Purpose

OBIC is a tool capable of measurement without bias, and is effective in the identification of failure locations such as leak locations of an initial product. In addition, with the advances in semiconductor-product miniaturization and film development, observation using a TEM is now required for accurately identifying the failure structure. Here, the minute structure of the failure location was identified using OBIC and observed using a TEM.

Analysis and Result

The gate leak location was identified using OBIC, a TEM sample was prepared by FIB processing, and the sample was observed using a TEM. At this time, the FIB processing location was accurately established by marking the position using the FIB and repeating OBIC measurement.

A defect in the gate oxide film was confirmed at the OBIC specified location. Poly-Si entered this area, resulting in a leak.

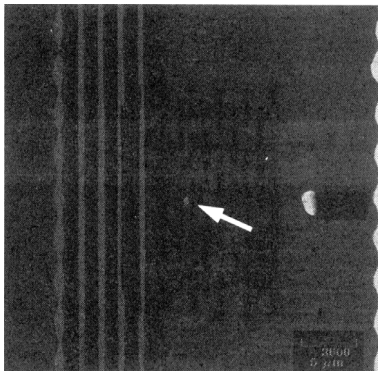


Figure 4-6-20 OBIC Observation Image
(FIB processing location established with high accuracy by FIB position marking)

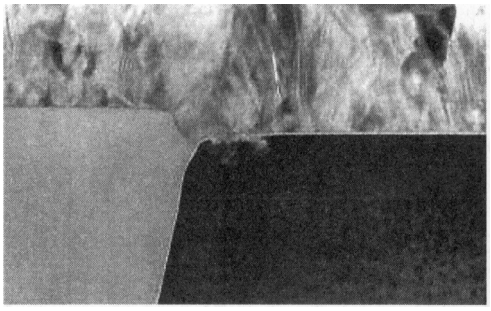


Figure 4-6-21 Cross-Sectional TEM Image of Location of Light Emission

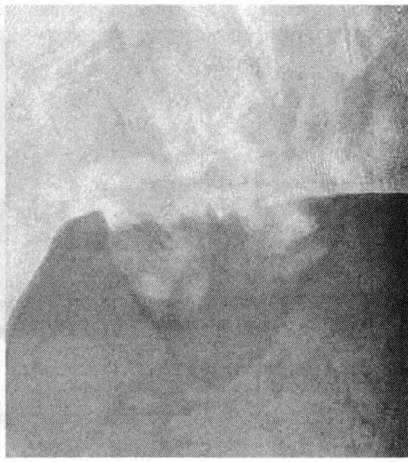


Figure 4-6-22 TEM Image (Enlarged):
Gate oxide film defect identified. Poly-Si entered this location.

(9) Analysis of Fine Particles in LSI Using Auger Electron Spectroscopy (1)

Purpose	To find out the cause of threadlike particles generation observed in the LSI. (Figure 4-6-23)
Analysis and Result	Figure 4-6-24 shows the cross-section of the particles observed using SEM. As a result of Auger electron surface analysis, Ti and Al were detected in the particles. The particles were found to be wiring residue that remained between metal wiring and adhered to the wiring in the early phase of passivation film formation. (Figure 4-6-25)

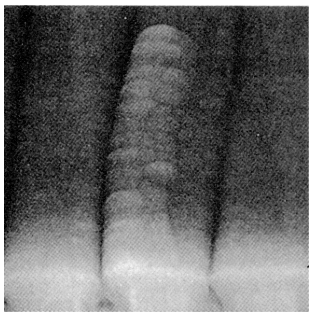


Figure 4-6-23 SEM Image

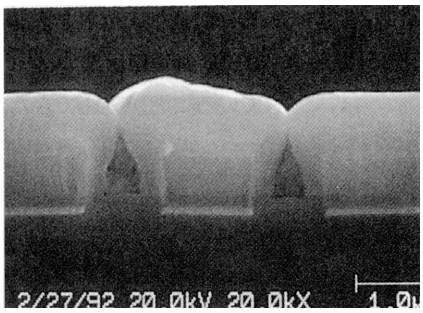
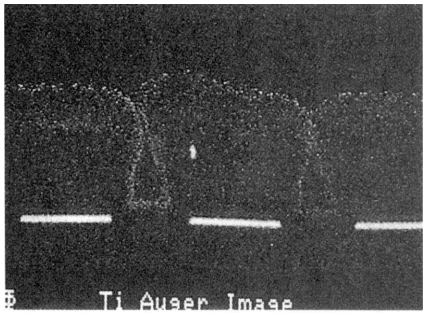
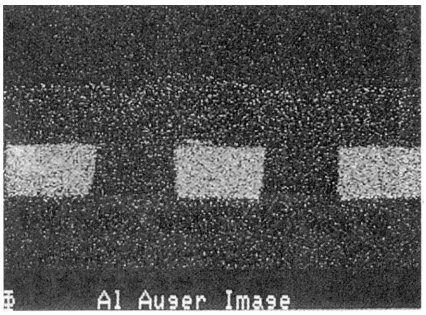


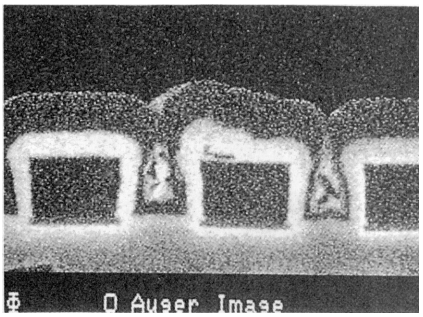
Figure 4-6-24 Cross-Sectional SEM Image



a) Auger Electron Image of Ti



b) Auger Electron Image of Al



c) Auger Electron Image of O

Figure 4-6-25 Auger Electron Cross-Sectional Analysis

(10) Analysis of Fine Particles in LSI Using Auger Electron Spectroscopy (2)

Purpose	To find out the cause of film-like particles generation observed on the contact area after surface polishing.
Analysis and Result	As a result of Auger electron qualitative analysis, Si was detected in the particles and, in the CMP process of BPSG, Poly-Si of the bit contact was found adhered between BPSG layers.

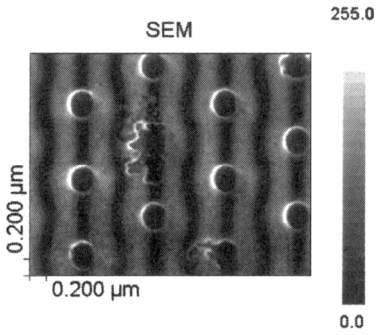


Figure 4-6-26 SEM Image

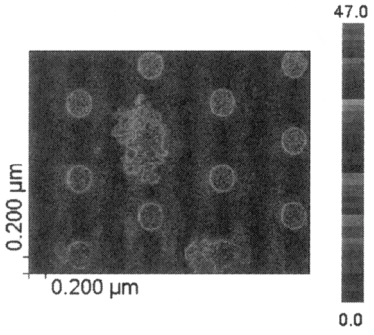


Figure 4-6-27 Auger Image of O + Si

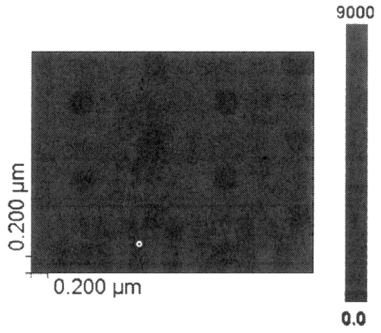


Figure 4-6-28 Auger Electron Image of O

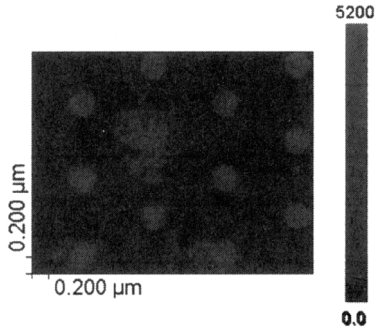


Figure 4-6-29 Auger Electron Image of Si

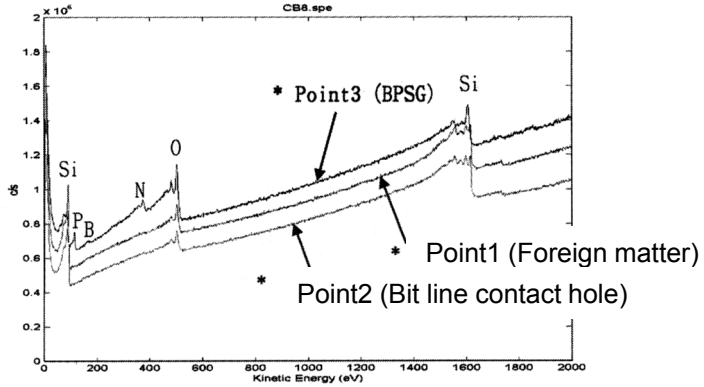


Figure 4-6-30 Auger Electron Energy Spectrum

(11) Coupling Status Analysis of Minute Part Using XPS

Purpose	A junction failure between the densely integrated Cu-Sn pad and chip bumps occurred. It has been found that the evaporated Au on junction failure was not diffused by heat treatment (Figure 4-6-31). The failure cause is examined by depth analysis based on Ar ion sputtering using XPS.
Analysis and Result	From Figure 4-6-32, it was found that the junction failure part has Sn oxide while the normal junction has Sn and Au being diffused. The Sn oxide prevents Sn and Au to diffuse on the junction failure part. It is found that the junction failure is caused by the generation of Sn oxide. It has been fed back to manufacturing process.

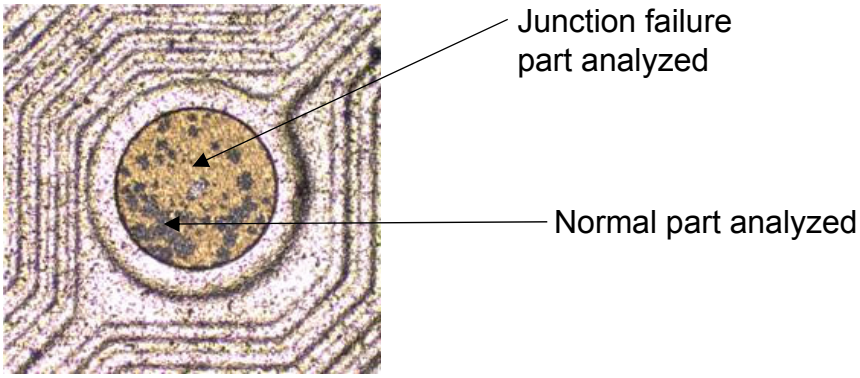
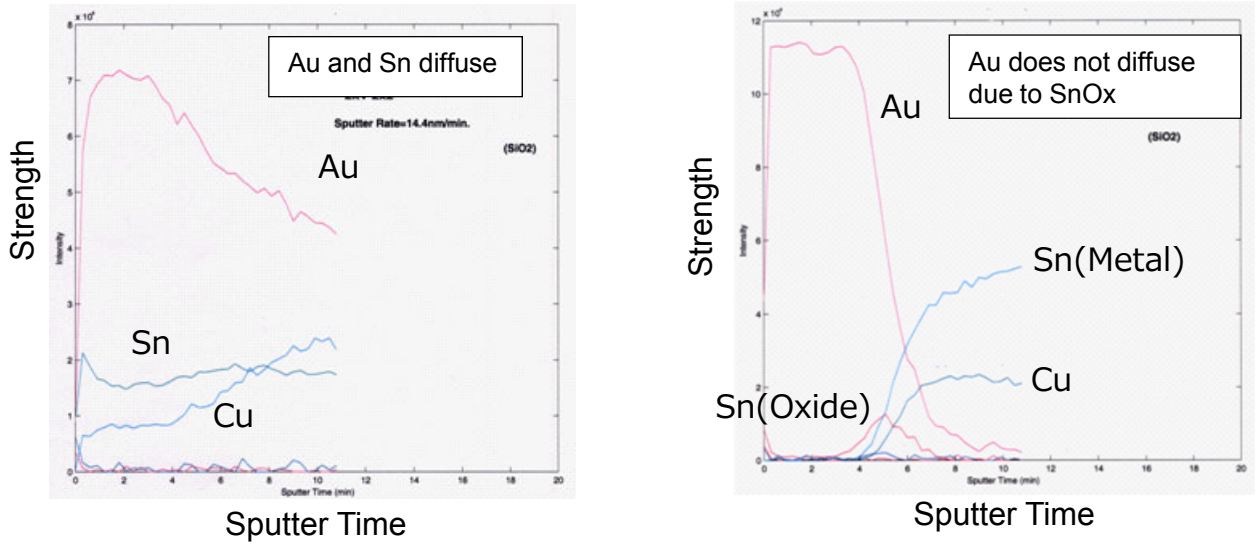


Figure 4-6-31 Status after Heat Treatment Applied to Evaporated Au on the Cu-Sn Pad



(a) Normal part (b) Junction failure part

Figure 4-6-32 Depth Profile Analysis on the Pad Using XPS

(12) Junction Analysis Using SCM

Purpose	The status of the P/N junctions scattered in the substrate was observed by creating an image of the variation of capacitance using an SCM. [7] This method is particularly effective in P/N assessment and local X_j and offset measurement.
Analysis and Result	The structure of the cross-sectional diffusion of the CCD area sensor was observed using an SCM. The diffusion layer distribution of the CCD area sensor was observed. This analysis makes it possible to provide information for process development and defect analysis, based on the P/N assessment and positional relationship with upper layer metallization etc.

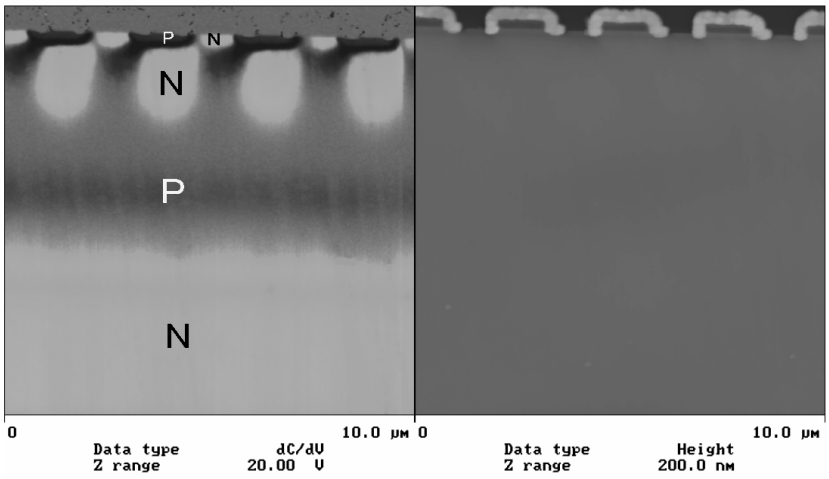


Figure 4-6-33 CCD Area Sensor (Left: SCM Image, Right: AFM Image)

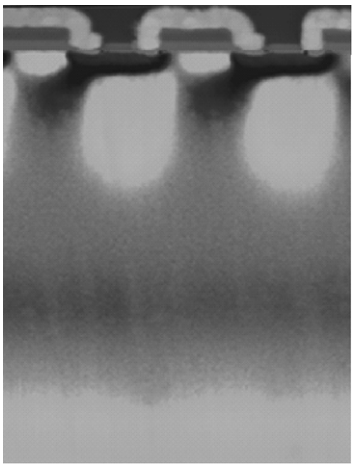


Figure 4-6-34 Diffusion Layer Positional Relationship (SCM Image and AFM Image Combined)

(13) Leak Location Identification Using Conductive AFM [8)]

Purpose

With the introduction of low dielectric constant film (hereafter "low-k film") into ULSI, leakage between metallization due to poor organic and inorganic film adhesion and Cu and barrier metal dispersion in the low-k film has become problematic. Prompt failure analysis and identification of leakage locations are now required.

To this end, leakage locations were identified using a conductive AFM.

Analysis and Result

A Cu/Low-K film sample was prepared in the form of a 30 mm^2 chip using FIB and fixed onto a conductive substrate. Bias voltage was applied to the sample stage, the current between the stage and probe was measured, and the leak location was identified from the current and shape images obtained.

Figure 4-6-35 shows the atmospheric conductive AFM measurement results of the Cu/Low-k film. The black areas are locations of high leakage current flow and low resistance. The organic film was found to readily produce current due its low resistance value in comparison to the SiO_2 and inorganic films. In addition, leakage was confirmed to occur from the entire organic film region.

From the above, it was speculated that because organic film has higher permeability and absorbability than other films, the water in the organic film reduces the film's resistance value.

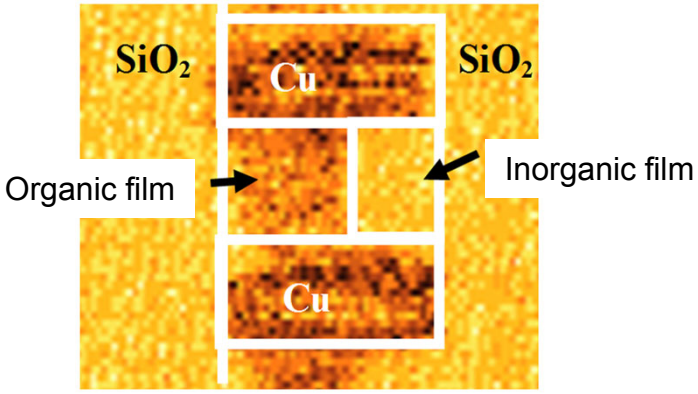
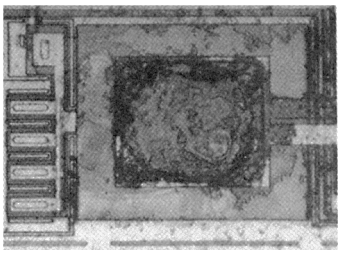


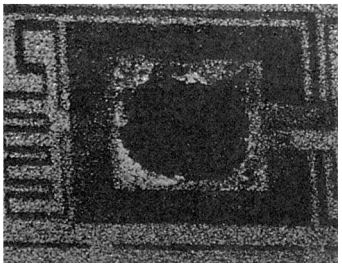
Figure 4-6-35 Cu/Low-k Film Conductive AFM Measurement Results

(14) Analysis of Bonding Pad Corrosion

Purpose	Open failure after humidity test
Analysis and Result	After sealing resin removal, an abnormality was found in a bonding pad area electrically opened. [Figure 4-6-36 a)] As a result of analysis using an EPMA, Al elution was confirmed and the impurity Cl was detected. [Figure 4-6-36 b) c)] Al corrosion of bonding pad area by Cl contamination



a) Microscope image of pad with open failure



b) Al X-ray image of a)

c) Cl X-ray image of a)

Figure 4-6-36 Example of Al Corrosion Analysis of Bonding Pad Area

(15) Analysis of Package Crack by Reflow of Surface Mounted Product

Purpose: To find out the cause of package cracks and bonding opens after moisture absorption and reflow.

Analysis and Result: A package crack from the edge of the chip was detected by scanning acoustic tomography observation, X-ray fluoroscopy observation and cross-sectional observation.

Internal moisture vaporized due to thermal stress at the time of reflow and, because the vapor pressure exceeded the rupture strength of the resin, the package cracked, causing the wire to break.

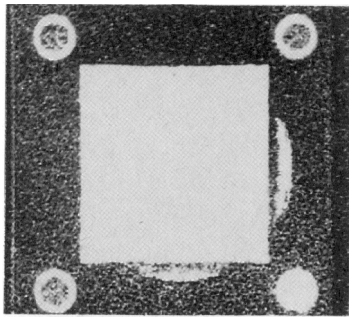


Figure 4-6-37 Observation by Scanning Acoustic Tomography

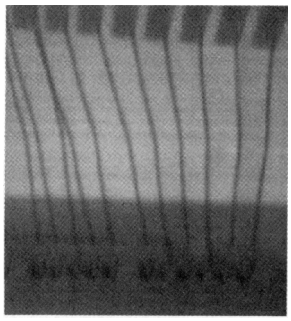


Figure 4-6-38 Observation by X-Ray Fluoroscopy (Wire Open)

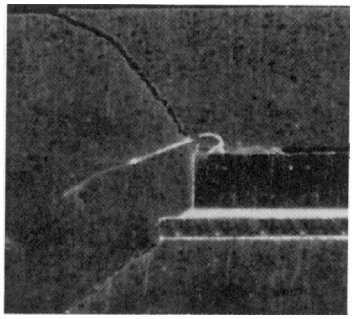
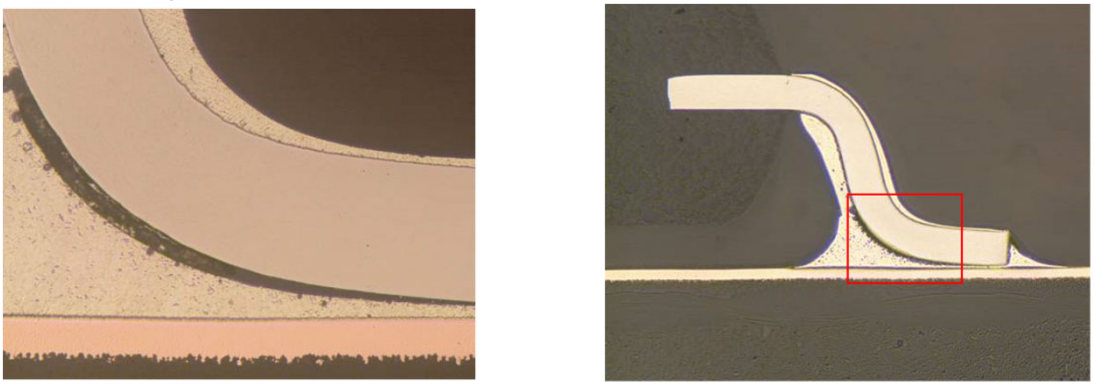


Figure 4-6-39 Cross-Sectional Observation

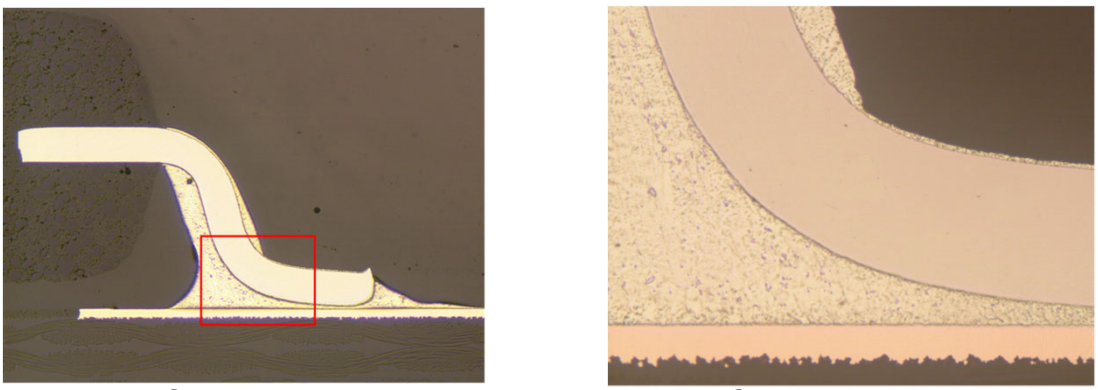
(16) Analysis of a Surface-Mount Product Soldering Failure by Board Used

Purpose	A reflow soldering failure has occurred to a TSOP type I (the package with 42 alloy leads on the shorter side) on the board A. The cause is determined.
Analysis and Result	Cross-sectionally cut and grinded contact of a lead and a board were observed with an optical microscope. A peel-off was found between the lead and the solder on the board A (Figure 4-6-40). On the board B (Figure 4-6-41), on the contrary, no separation was found between the lead and the solder. The soldering failure is caused by the large thermal expansion and reduction of the board A upon mounting. The board A has a larger coefficient of thermal expansion compared to the board B and has a much larger coefficient of thermal expansion compared to the leads. When heated and cooled through soldering, the difference between the expansion and reduction ratio of the board and the leads gaps the board and the leads.



(a) Scale-down observation (b) Scale-up observation

Figure 4-6-40 Cross-Section Observation Using Board A



(a) Scale-down observation (b) Scale-up observation

Figure 4-6-41 Cross-Section Observation Using Board B

(17) Failure Analysis of Power MOS FET

Purpose

A malfunction occurred in the customer's installation process. We want to isolate whether it is a problem in the installation process or in the semiconductor device itself. We have not confirmed the operation of the semiconductor device before installing it. Defects were revealed after implementation.

Analysis and Result

Failure mode: Short between the gate and source. Observed from the back side with OBIRCH, the signal was confirmed at an outer part of the gate wiring (Figure 4-6-42). From electric characteristics and the OBIRCH signal point, failures are assumed to be EOS breakdown. Gate oxide breakdowns, substrate cracks, and inter-layer film cracks were confirmed from observation of the OBIRCH signal point via cross section (Figure 4-6-43).

It is thought that electric current generated the Joule heat, the temperature rose locally to exceed the melting point, and it broke down.

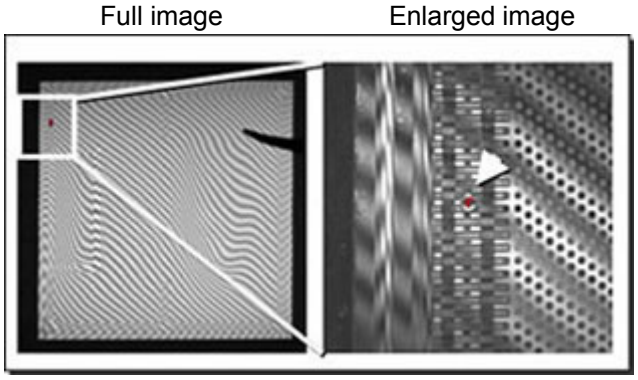


Figure 4-6-42 Example of Signal Detection by OBIRCH

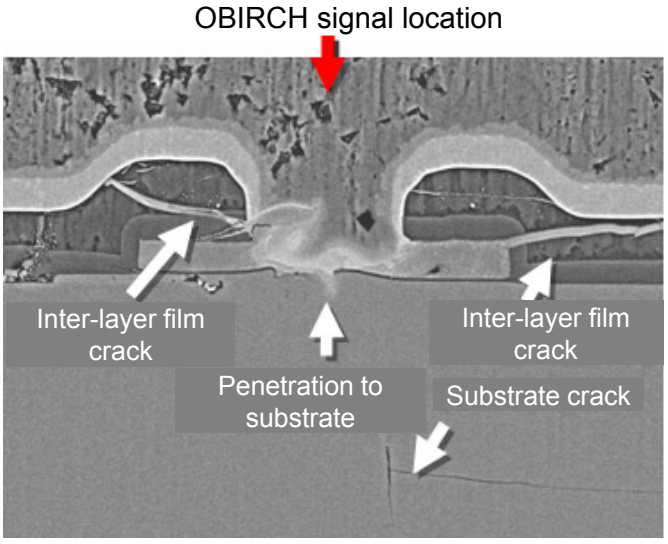


Figure 4-6-43 Cross-Section Observation Result of the Detection Point

(18) Failure Analysis of SiC Compound Semiconductors

Purpose	When we performed an ESD breakdown voltage test for SiC MOS FET, It was destroyed at 1 kV. We performed an analysis to clarify the breakdown point.
Analysis and Result	Failure mode: Short between the gate and source. The dotted OBIRCH signal was detected from the back side with OBIRCH (Figure 4-6-44). It is thought that there is a short at this spot. The deformation at the gate electrode and the melting on the SiC substrate were confirmed from the observation of the OBIRCH signal point through the cross section (Figure 4-6-45). In the ESD test, we found that the gate and source have been short-circuited due to the gate oxide breakdown.

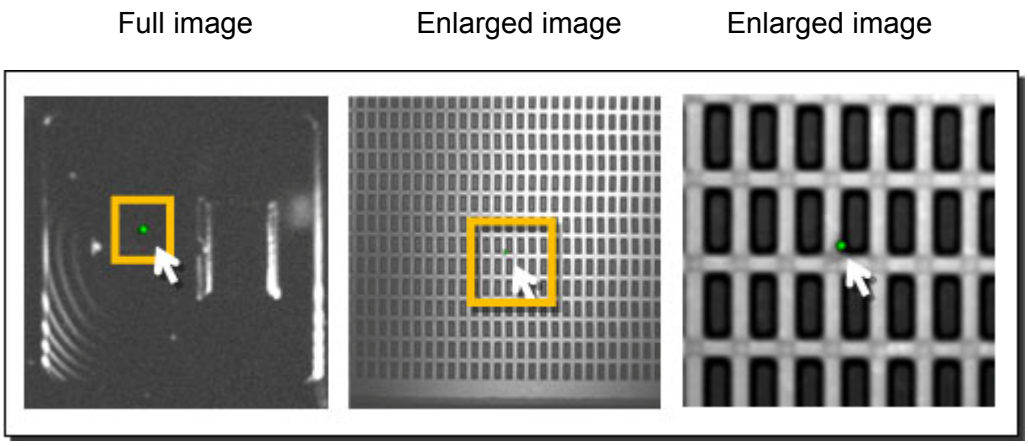


Figure 4-6-44 Example of Signal Detection by OBIRCH

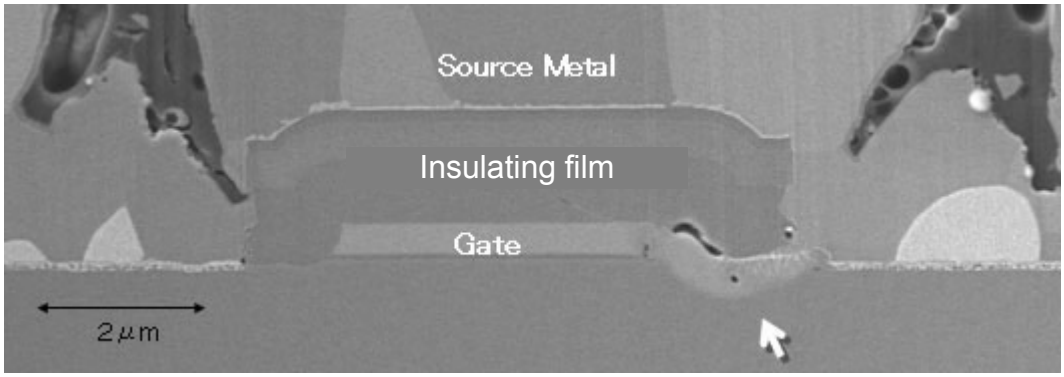
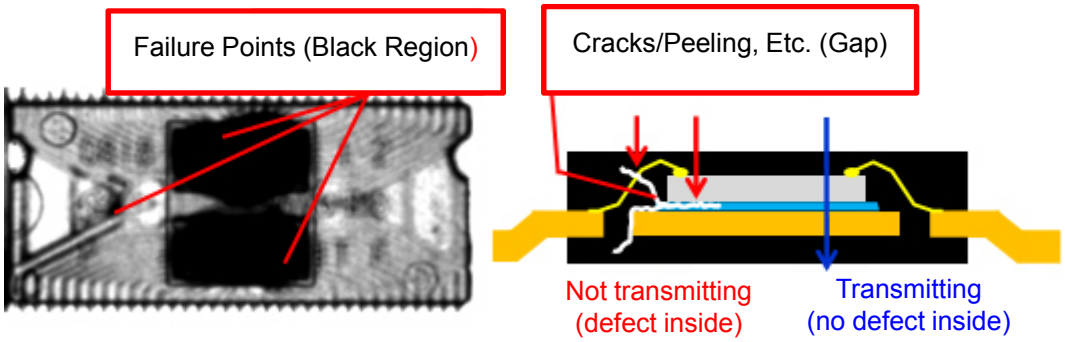


Figure 4-6-45 Cross-Section Observation Result of the Detection Point

(19) Nondestructive Observation of Internal Structure by Scanning Acoustic Microscope (SAM)

Purpose	We observed defects inside the package non-destructively using a scanning acoustic microscope (SAM).
Analysis and Result	For test pieces with multilayer structures, such as mount paste sandwiched between chip and bed, and multistage stacking devices, we first observed the entire interior by transmission observation and investigated the presence or absence of defects. Transmission observation of defective products confirmed abnormal spots (peeling and cracks) inside the package (Figure 4-6-46).



Transmission Image of a Defective Product

Observation Image of a Transmission Method

Figure 4-6-46 Nondestructive Observation of Defective Products

(20) Nondestructive Observation of Internal Structure by 3-Dimensional X-Ray Microscope (X-Ray CT)

Purpose	We observed defects inside the package non-destructively using a 3D X-ray microscope (X-ray CT).
Analysis and Result	In combination with a scanning acoustic microscope (SAM) for non-destructive inspection, we confirmed abnormal spots (chip cracks and substrate cracks) inside the package from detailed observation (Figure 4-6-47).

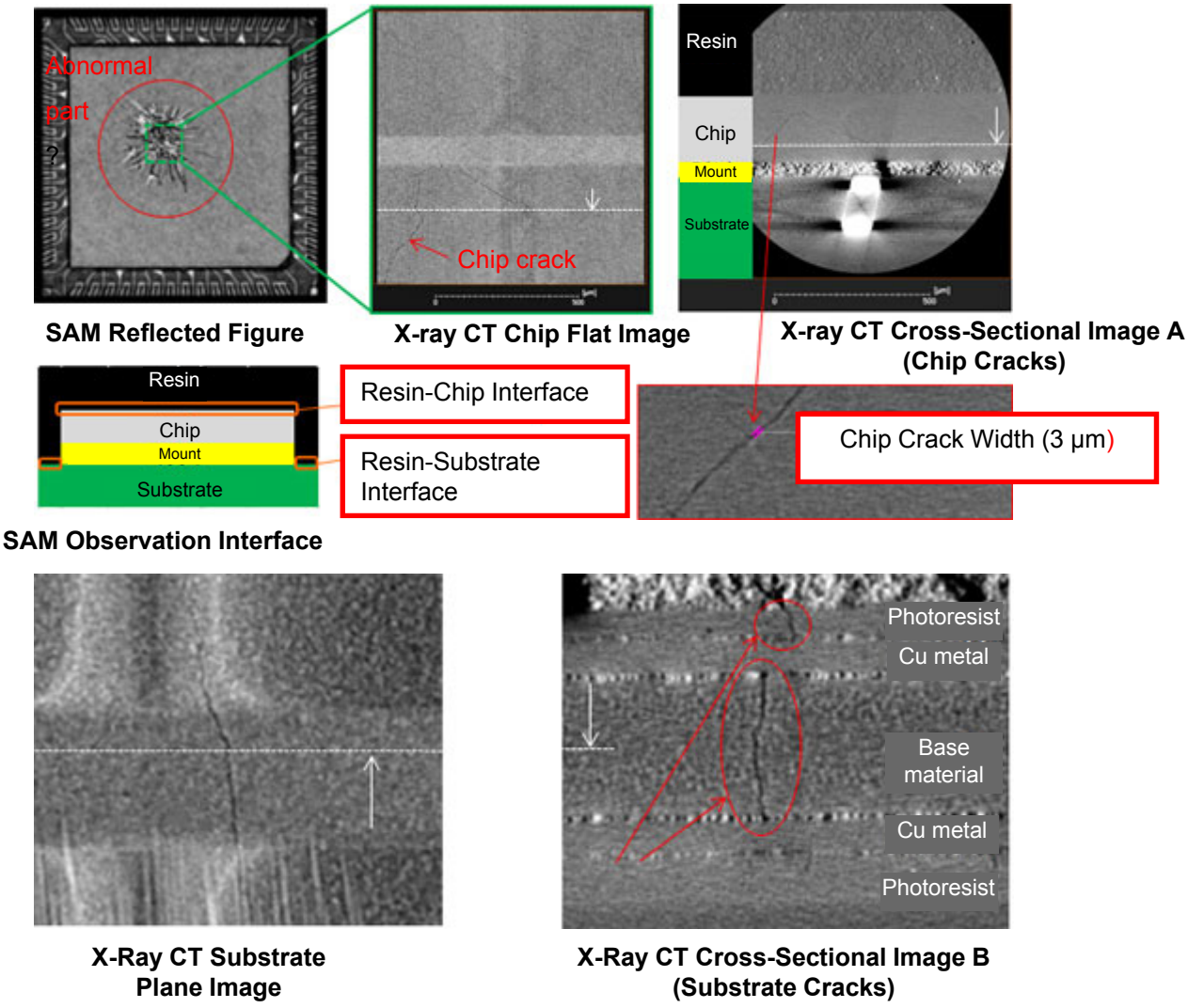


Figure 4-6-47 Nondestructive Observation of Defective Products

(21) Failure Location Identification Using applied analysis(DLS analysis) of IR-OBIRCH (DLS:Dynamic Laser Stimulation)

Purpose	When a tester connect to IR-OBIRCH equipment and let a laser scan on a device while repeating the test of the device, only when a laser is irradiated in the failure location,become able to change a state of the good/bad. It is clear at a glance and can distinguish a failure location by imaging this state and is effective for the identification of the failure location. (As for the difference between IR-OBIRCH and DLS analysis, IR-OBIRC is used for the identification of the failure location of DC failure. DLS is used for the identification of the failure location of various failure mode(function failure or AC failure analysis)).
Analysis and Result	A failure location of function failure was identified by the DLS analytical method of the IR-OBIRCH equipment. DLS observation result, the failure location was identified. As a result of TEM analysis,the cause of failure was identified as a void by poor implantation in the via area

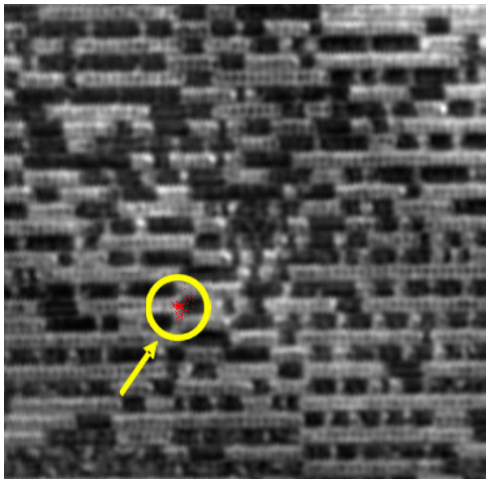


図4-6-48 DLS observation image

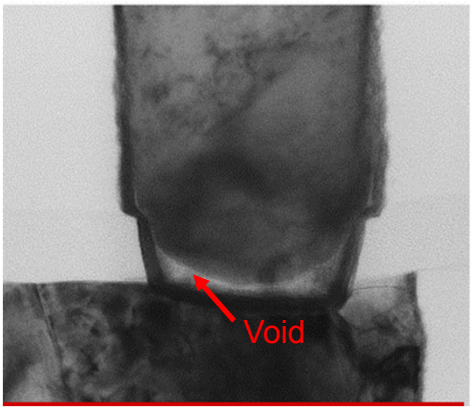


図4-6-49 Result of Examining the Cross-Section of the Detected Location (TEM)

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Chapter 5 Mathematics of Reliability

Chapter 5 Mathematics of Reliability

5-1. Estimating Reliability

5-1-1. Non-Parametric Estimation of Reliability Scales

As previously described, various indices such as the reliability R(t), failure distribution function F(t), failure rate λ(t) and mean life μ are used to quantify reliability, according to the situation.

Normally, each index is found after the life distribution has been identified. However, sometimes it is necessary to determine the reliability without any knowledge of the life distribution. The estimation method used in this case is referred to as the non-parametric method.

In non-parametric estimation, the indices R(t) and F(t) is expressed using the F distribution as follows:

$$\hat{R}(t) = \frac{1}{1 + \frac{r+1}{n-r} F_{\alpha}(\nu_1, \nu_2)}$$

$$\hat{\mathrm{F}}(\mathrm{t}) = 1 - \hat{R}(t)$$

where,

$\hat{\mathrm{R}}(\mathrm{t})$ = Estimated reliability after time t has elapsed

$\hat{\mathrm{F}}(\mathrm{t})$ = Estimated cumulative failure rate up until time t

r = Number of failures that occurred during the test
n = Number of failures that occurred during the test
F=Upper α percentage point of F distribution corresponding to the variances ν_1 and ν_2

$$\nu_1 = 2n - 2r$$

$$\nu_2 = 2r + 2$$

(1- α) = Probability that the estimated reliability $\hat{\mathrm{R}}(\mathrm{t})$ is equal to or greater than the true reliability. This is called the reliability level.

5-1-2. Estimating and Testing the Life Distribution Shape

(1) Estimating the Distribution Shape

The distribution shape of the life is determined by making a histogram from the data, assuming a distribution from the shape of the histogram, and then testing whether the assumption is correct. If the assumption is found to be incorrect, a different distribution is assumed and test is attempted. These steps are repeated until the correct distribution is obtained. A probability paper can be used to estimate the distribution from a histogram. Normal, log-normal and Weibull probability papers are available. The paper that gives a straight line when the data is plotted with time on the horizontal axis and cumulative failure rate on the vertical axis indicates the applicable type of distribution. (That is, normal distribution can be applied if the plot is straight on normal distribution probability paper.)

For example, let us plot a graph on Weibull probability paper using total six failures, with two failures at 1000 h, one at 2000 h, two at 3000 h and one at 5000 h for the tested 1000 products (see Figure 5-1-1).

The data falls approximately on a straight line and the shape parameter m is 0.7. Therefore, this distribution can be considered a Weibull distribution.

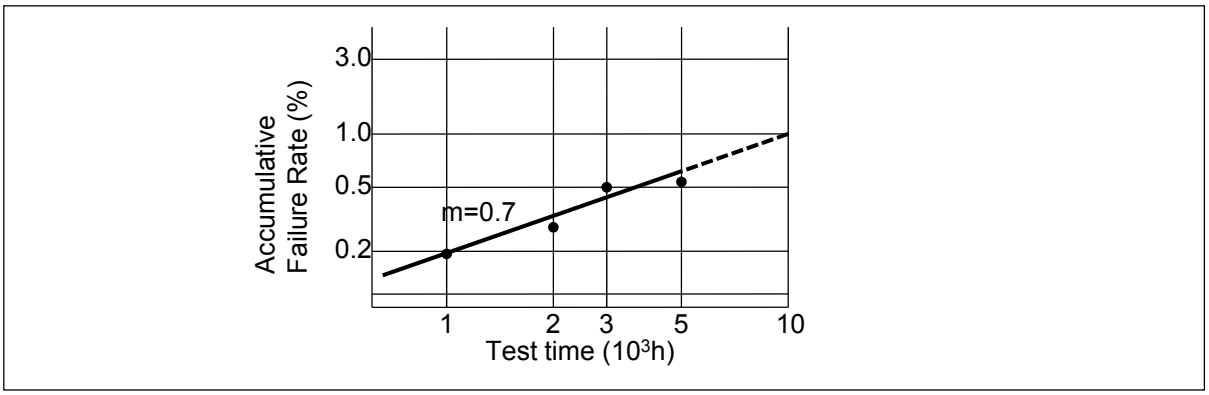


Figure 5-1-1 Example of Continuous Operation Test

(2) Test of Distribution Shape

A method called χ^2 test is used to confirm whether the distribution of a population is equal to the estimated distribution which is based on measured values.

Assume that the failure rate is fi in each interval ti – 1 to ti when n items of the product are tested with the test time divided into k intervals (t1, t2, t3, t4 . . . tk). Next, the failure frequency pi is obtained from the distribution to be tested.

When

$$x = \sum_{\mathrm{i=m}}^{\mathrm{k}} \frac{\left(F_i - p_i\right)^2}{p_i}$$

is substituted, if n is sufficiently large and $np_i > 10$, the distribution of x is approximated by a χ^2 distribution in which the degree of freedom $\phi = k - 1$. In order to test the assumption that the actual failure frequency occurring at each t_i is equal to the value obtained from the distribution to be verified, the value $\chi^2\,\alpha;\,\phi$ which satisfies

$$\Pr\left(\chi^2 \geqq \chi^2(\alpha,\phi)\right) = \alpha$$

is determined from the χ^2 table and compared with the χ^2 obtained. If

$$x \leqq \chi^2(\alpha,\phi)$$

then the estimated distribution is correct.

In the above equation, α is referred to as the level of significance of the statistics. In other words, the risk that the result of test is incorrect is no more than α %. Usually a value of 5% or 10% is used.

If the distribution to be tested has m parameters, and if the parameters are estimated from data and the distribution is then tested, the degree of freedom ϕ of the χ^2 distribution is expressed as:

$$\phi = \text{k-m-1}$$

5-1-3. Parametric Estimation of Reliability Scales

When the distribution shape of the life has been identified, various indices required for reliability evaluation can be obtained by estimating the distribution parameters. The estimated parameters are themselves a function of the sampled values and form a certain distribution. The parameter values are different each time when they are sampled even from the same population. The two evaluation methods are used. One is point estimation, in which the parameters are estimated at a single point, and another is interval estimation, in which the parameters are estimated within a certain interval. An “interval estimate of confidence level γ” means that the probability that the parameter for the population exists between θ_L (lower estimate) and θ_U (upper estimate) is γ %. The confidence level is sometimes abbreviated CL.

(1) Exponential Distribution

(a) Fixed Number Testing Method

In the fixed number testing method, testing is terminated when a predetermined number of failures occurs. The parameter for the exponential distribution λ (failure rate) is expressed as follows:

$$\overline{\lambda} = \frac{r}{\sum_{i=1}^{r} t_i + (n-r)t_r}$$

$$\lambda_L = \frac{\chi^2\left(1-\frac{\alpha}{2}, 2r\right)}{2r} \cdot \overline{\lambda}$$

$$\lambda_U = \frac{\chi^2\left(\frac{\alpha}{2}, 2r\right)}{2r} \cdot \overline{\lambda}$$

where,

$\bar{\lambda}$ = Point estimate of λ

λ_L= Lower limit of λ interval estimate

λ_U= Upper limit of λ interval estimate

n = Number of tested samples

r = Total number of failures

t_i = Time when the i-th failure occurred

$\chi^2(\alpha,\phi)$ = Point where $P(\chi^2 \geqq \chi^2(\alpha, \phi)) = \alpha$ in a χ^2 distribution with degree of freedom ϕ

The estimated values of the mean life μ are expressed as follows:

$$\bar{\mu} = 1/\bar{\lambda}$$

$$\mu_L = 1/\lambda_U$$

$$\mu_U = 1/\lambda_L$$

Where

$\bar{\mu}$ = Point estimate of mean life

μ_L = Lower limit of mean life interval estimate

μ_U = Upper limit of mean life interval estimate

Furthermore, the point estimate of R(t) and upper and lower limits of interval estimate are expressed as:

$$\bar{R}(t) = e^{-\bar{\lambda}\cdot t}$$

$$\bar{R}_u(t) = e^{-\bar{\lambda}_L\cdot t}$$

$$\bar{R}_L(t) = e^{-\bar{\lambda}_U\cdot t}$$

(b) Fixed Time Testing Method

In the fixed time testing method, the test is terminated at a predetermined time t_c regardless of the number of failures. The point estimate and interval estimate of λ are expressed as follows:

$$\overline{\lambda} = \frac{r}{\sum_{i=1}^{r} t_i + (n-r)\cdot t_c}$$

$$\lambda_L = \frac{\chi^2\left(1-\frac{\alpha}{2}, 2r+2\right)}{2r}\cdot\overline{\lambda}$$

$$\lambda_U = \frac{\chi^2\left(\frac{\alpha}{2}, 2r+2\right)}{2r}\cdot\overline{\lambda}$$

(2) Normal Distribution

There are two normal distribution parameters: μ and σ^2. Parameter μ is the mean life and σ^2 is the variance of the distribution. The point estimates of these values are expressed as follows:

$$\overline{\mu} = \frac{\sum_{i=1}^{n} t_i}{n}$$

$$\overline{\sigma}^2 = \frac{\sum_{i=1}^{n} (t_i - \overline{\mu})^2}{n-1}$$

The upper limit μ_U and lower limit μ_L of the mean life within the reliability interval are:

$$\mu_U = \overline{\mu} + t(\alpha, n-1) \cdot \sqrt{\frac{\overline{\sigma}^2}{n}}$$

$$\mu_L = \overline{\mu} - t(\alpha, n-1) \cdot \sqrt{\frac{\overline{\sigma}^2}{n}}$$

And the upper limit σ_L^2 and lower limit σ_U^2 of the variance σ^2 within the reliability interval are:

$$\sigma_L{}^2 = \frac{(n-1)\overline{\sigma}^2}{\chi^2\left(1-\frac{\alpha}{2}, n-1\right)}$$

$$\sigma_U{}^2 = \frac{(n-1)\overline{\sigma}^2}{\chi^2\left(\frac{\alpha}{2}, n-1\right)}$$

where

$t(\alpha,n-1)$ = The value of t for which $P(t > t(\alpha,n-1)) = \alpha$ in the t distribution table

$\chi^2\left(\frac{\alpha}{2}, n-1\right) =$ The value of χ^2 for which $P\left(\chi^2 \geq \chi^2\left(\frac{\alpha}{2}, n-1\right)\right) = \frac{\alpha}{2}$

in the χ^2 distribution table

(3) Weibull Distribution

The Weibull distribution has three parameters: m, t_o and γ, and it is very difficult to analyze data by calculation. Hence, the Weibull probability paper is often used for estimation. If m is known and $\gamma = 0$, t_o is expressed as follows:

$$\bar{t}_0 = \frac{\sum_{i=1}^{r} t_i^{\,m} + (n-r)t_r^{\,m}}{r}$$

(4) Log-Normal Distribution

Similar to normal distribution, there are two parameters μ and σ^2. The point estimates are expressed as

$$\overline{\mu} = \frac{\sum_{i=1}^{n} \ln t_i}{n}$$

$$\overline{\sigma}^2 = \frac{\sum_{i=1}^{n} \left(\ln t_i - \overline{\mu} \right)^2}{n-1}$$

And the estimate $\overline{M}$ of the mean life is:

$$\overline{M} = \exp\left(\overline{\mu} + \frac{\sigma^2}{2} \right)$$

5-1-4. Using Probability Papers

Distribution studies using a probability paper are very simple and require no complicated calculations. The method is widely used to verify distribution parameter theories and to find distribution parameters.

Various types of probability paper are available and their use is widely known. Described below are a few tips on how to plot data on probability paper and determine whether the result is a straight line.

Many plotting methods have been devised for processing data on probability paper and making estimates as accurate as possible. The plot for a product for which n samples have been tested and for which the i-th product was defective is (ti, Fi), where ti is the time after which product number i failed and Fi is the cumulative failure rate.

The following values are generally used to plot Fi:

(1) i / n

(2) $(i - 0.5) / n$

(3) $(i - 1) / (n - 1)$

(4) $i / (n + 1)$

(5) $(i - \alpha_i) / (n - \alpha_i - \beta_i + 1)$

(1) to (4) are very simple, but the last datum (that is the nth datum) is not utilized in (1) and the first datum is not utilized in (3). Therefore, (2) or (4) is recommended.

Method (5) has been devised as an improvement over (4): $\alpha_i = \beta_i = 3/8$ for the normal distribution; $\alpha_i = 0.52\ (1\text{-}1/m)$ and $\beta_i = 0.5\text{-}0.2\ (1\text{-}1/m)$ for the Weibull distribution with shape parameter m.

When determining the straightness of the curve, the conventional least square method can be used. However, the data will not be distributed evenly and the variance will be smallest around the central part of the curve. Thus, when drawing the curve, make sure that it adheres closely to these central points.

5-2. Failure Distribution Model

5-2-1. Rope Model

The previous section described the mathematical methods for estimating the life distribution. The life distribution can be further narrowed down if the relationship between the life distribution and failure is known. When viewed from this perspective, the exponential distribution can be considered as a distribution of products which fail when randomly subjected to m harmful shocks per unit time. Similarly, the gamma distribution can be thought of as the case where a product receives k shocks before it fails.

Now assume that a product consists of many components, just as a rope consists of many strands. A rope fails when all of its strands are cut. Therefore, the following relationship exists between the reliability of a product and the reliability of its components:

$$R_D = 1 - \prod_{i=1}^{k} \left(1 - R_i\right)$$

where R_D is the reliability of the product, and R_i is the reliability of the ith component, and k is the number of components. Given that the distribution shape of the life for each component forms an independent exponential distribution with the same shape, the distribution for the product as a whole is a gamma distribution with a shape parameter k and a scale parameter m that is the same m value as the exponential distributions for the components.

A product that will fail only when all of its components fail is referred to as a “rope model” or “parallel model.” This model is used to study the problem of product fatigue and redundancy in design. When k in a gamma distribution becomes large, the distribution becomes similar to a normal distribution and the mean value becomes equal to k/m. Therefore, a normal distribution can be considered an extreme case of the rope model.

5-2-2. Weakest Link Model

In contrast to the rope mode, a model similar to a chain of k links, where the failure of the weakest link results in the failure of the entire chain, is referred to as the “weakest link model.” This also applies to an article of equipment consisting of k components where the failure of any single component results in the failure of the equipment as a whole. For this reason, the weakest link model is also referred to as the “serial model.” In this case, the following relationship exists between the reliability RD of the product and the reliability Ri of the components.

$$R_D = \prod_{i=1}^{k} R_i$$

k: Number of components

The Weibull distribution is one of the distributions that represent the weakest link model. In addition, the following double-exponential distribution, an extreme case of the Weibull distribution, is also used to represent the weakest link model.

$$F(t) = 1 - \exp\left\{ - \exp\left(\frac{t}{n} \right) \right\}$$

5-2-3. Proportional Effect Model

Given that X1 < X2 < X3 < . . . . < Xn are the fatigue cracks at each phase, the size of the fatigue crack at each phase is proportional to that of the previous phase. That is, if the relationship below exists, then the distribution of Xn is a log-normal distribution.

$X_i = \alpha_i X_{i-1}$

α_i= Constant

i=1, 2, ……

5-2-4. Stress and Strength Model

In this type of model, a product fails when stress accumulates beyond its strength. In this model, failure can be calculated as the overlap of the stress distribution and the strength distribution.

If stress and strength are both normal distributions, the life distribution will also be a normal distribution. If the average stress at a given time is μ_s and the standard deviation is σ_s, and similarly for the strength distribution, if μ_k is the average and σ_k is the standard deviation, then the level of unreliability represented by the area of normal strength distribution in which the strength is below zero, the average is equal to ($\mu_k - \mu_s$) and the standard deviation is equal to $\sqrt{\sigma^2 k + \sigma^2 s}$.

5-2-5. Reaction Theory Model

This model attempts to estimate life using a failure physics method. It assumes that a failure is caused at a microscopic level, where changes at the atomic and molecular levels cause harmful reactions and result in failure when the changes reach a certain threshold. The following stress and life relations based on the Arrhenius model of chemical reactions are widely used.

$$\ln L = A + \frac{B}{T} - \alpha \ln S$$

L= Mean life

A, B, α = Constants

T= Temperature (°K)

S= Stress other than temperature

5-2-6. Reliability Model for Equipment

(1) Serial Model

For an article of equipment consisting of n components, if the equipment fails when one of its components fails, the reliability Rs(t) of the equipment can be expressed as a function of the reliability of each component Ri(t) as follows:

$$R_s(t) = 1 - \prod_{i=1}^{n} R_i(t)$$

(2) Parallel Model

For an article of equipment consisting of n' components running in parallel, with the equipment continuing to function as long as any of the parallel components is still running, the following is true:

$$R'_s(t) = 1 - \prod_{i=1}^{n'} (1 - R_i(t))$$

In this case, the reliability is better than that of equipment consisting of only one component.

Chapter 5 Mathematics of Reliability

5-3. Failure Rate Estimation

5-3-1. Overview

It is important from the point of view of equipment reliability and safety to estimate failure rates for semiconductor products used in electronic equipment released to the market.

Failure rates are estimated by calculating an acceleration coefficient based on an accelerated lifetime test or by gathering failure conditions from products used in the field.

5-3-2. Estimating Failure Rates Using Accelerated Lifetime Tests

When estimating field failure rates from test data, the actual number of failures is often very small or sometimes zero. In such cases, the failure rate must be estimated based on a certain confidence level. With semiconductor components, the upper reliability limit is often used, assuming that the failure distribution is an exponential distribution. This method is specified in JIS C5003 (General rules for determining the failure rate of electronic components during tests) and uses the following equation:

Total test time: T (Number of test samples n × Test time t)

α : the value equivalent to the number of generating failures according to the confidence level to which setup was done

Failure rate: $\lambda = \dfrac{a}{T}$

Here, calculate α using Table 5-3-2-1.

Table 5-3-2-1 The Average Value of the Confidence Level Corresponding to the Number of Failures [1)]

Number of Failures	α	
	Confidence Level 60%	Confidence Level 90%
0	0.917	2.30
1	2.02	3.89
2	3.11	5.32
3	4.18	6.68
4	5.24	7.99
5	6.29	9.27
6	7.34	10.5
7	8.39	11.8
8	9.43	13.0
9	10.5	14.2
10	11.5	15.4

The following describes how to calculate the failure rate based on a specific example.

Assume that 100 semiconductor devices are subjected to high-temperature testing (Ta = 125 ℃, at rated operating voltage) for 2,000h with zero faults.

To find the failure rate, first calculate the acceleration AF (voltage acceleration coefficient AV × temperature acceleration coefficient AT) to obtain the total component hours.

The voltage acceleration coefficient AV can be obtained from the failure rates for actual applied voltage and test voltage conditions. It is assumed that the actual usage voltage is within the rated specification.

Given that the actual usage temperature is 50℃ and the typical activation energy of the expected failure mode is 0.8 eV, the temperature acceleration coefficient AT is obtained using the Arrhenius equation as follows:

$$A_T = \frac{L_1}{L_2} = \exp\left\{\frac{E_a}{K} \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right\}$$

$$= \exp\left\{\frac{0.8}{8.617 \times 10^{-5}} \times \left(\frac{1}{50 + 273} - \frac{1}{125 + 273}\right)\right\}$$

$$\fallingdotseq 225$$

Acceleration coefficient A_F = Voltage acceleration coefficient A_V × Temperature acceleration coefficient A_T

= 1 × 225

= 225

Given the number of samples 100 and test time t_n for sample number n, the total test time (component hours) is:

$$= \sum_{n=1}^{100} (t_n \times A_F)$$

= 100 × 2000 × 225

= 4.5×10^7 C. H. (Component hours)

Because the number of failures r = 0, given a reliability level of 60%,

$$\lambda = \frac{0.92}{4.5 \times 10^{7}}$$

$$\fallingdotseq 2.0 \times 10^{-8}$$

$$= 20\text{FIT } (10^{-9}\text{h})$$

Therefore, in this case the estimated failure rate in the field is 20 FIT.

In a similar manner, the failure rate of a device under actual usage conditions can be estimated from the accelerated test data provided that the major failure modes and failure mechanisms for the device are understood.

Chapter 5 Mathematics of Reliability

[Bibliography]

Reliability Handbook, edited by W. G. Ireson (McGraw Hill) Introduction to Reliability Engineering, by H. Shiomi (Maruzen)

1) JIS C5003

Appendix

Appendix

1. Sampling Inspection

1-1. Sampling Inspection

A sampling inspection is the inspection of a small percentage of products taken from a lot (i.e., a collection of similar products, parts or materials) based on a predefined method. During the inspection, the samples are tested and the entire lot is either accepted or rejected by comparing the test results with assessment criteria. If there is no variance in lot quality characteristics, the quality of all products in the lot can be identified by picking a single sample from the lot and conducting a quality check on that sample. If there is quite a bit of variance, however, an inspection lot is constructed from production lots that were made under identical conditions so as to minimize variance.

1-2. Sampling Inspection Methods

(1) Sampling Inspection by Standards

In the sampling inspection by standards method, standards for protecting the seller and standards for protecting the buyer are developed to ensure satisfaction of both seller and buyer requirements. Seller protection is given by defining probability α, a fixed small number that indicates the probability that a good-quality lot will be rejected during inspection (producer's risk); and buyer protection is given by defining probability β, a fixed small number that indicates the probability that a poor-quality lot will be accepted during inspection (consumer's risk).

For example:

When producer's risk α = 0.05, five out of 100 good-quality lots will be rejected during inspection. When consumer's risk β = 0.1, ten out of 100 poor-quality lots will be accepted during inspection.

(2) Sampling Inspection by Screening

In the sampling inspection by screening method, if the sampled products pass the sampling inspection, all products are accepted as is, but if the sampled products fail the inspection, all products are inspected or "screened." This type of method does not apply to destructive inspection, which does not permit inspection of all products.

(3) Sampling Inspection with Adjustment

This method enables rational inspections based on the use of inspection result information to date. For those lots with a good quality history, the reduced inspection is used. For those lots with a poor quality history, the tightened inspection is performed. The inspection standard is then adjusted as changes occur in the status of inspection lot acceptance. This method is defined in JIS Z9015-1.

1-3 Sampling Inspection and OC Curve

In the inspection method referred to as “sampling inspection by attributes (JIS Z 9002),” it is desirable that a good lot in which the defect rate is p0% is rendered acceptable [acceptable quality level (AQL = p0%)], and a bad lot in which the defect rate is p1% or less is rendered unacceptable.

Thus, a policy is established such that if a sample size n is taken from a lot and the number of defects found is c or less, the lot passes inspection, and if the number exceeds c, the lot fails inspection. This is referred to as the sampling inspection by attributes, and is abbreviated (n, c).

Using binomial distribution, the probability that X products will be defective in sample size n can be found using the following equation:

$$P(x) = \frac{n!}{x!(n-x)!} p^{x} (1-p)^{n-x} \qquad (x=0, 1, 2, 3, \cdots n)$$

The graph with the horizontal axis representing the defect rate and the vertical axis representing the probability of lot acceptance, is referred to as the operating characteristic (OC) curve.

Appendix

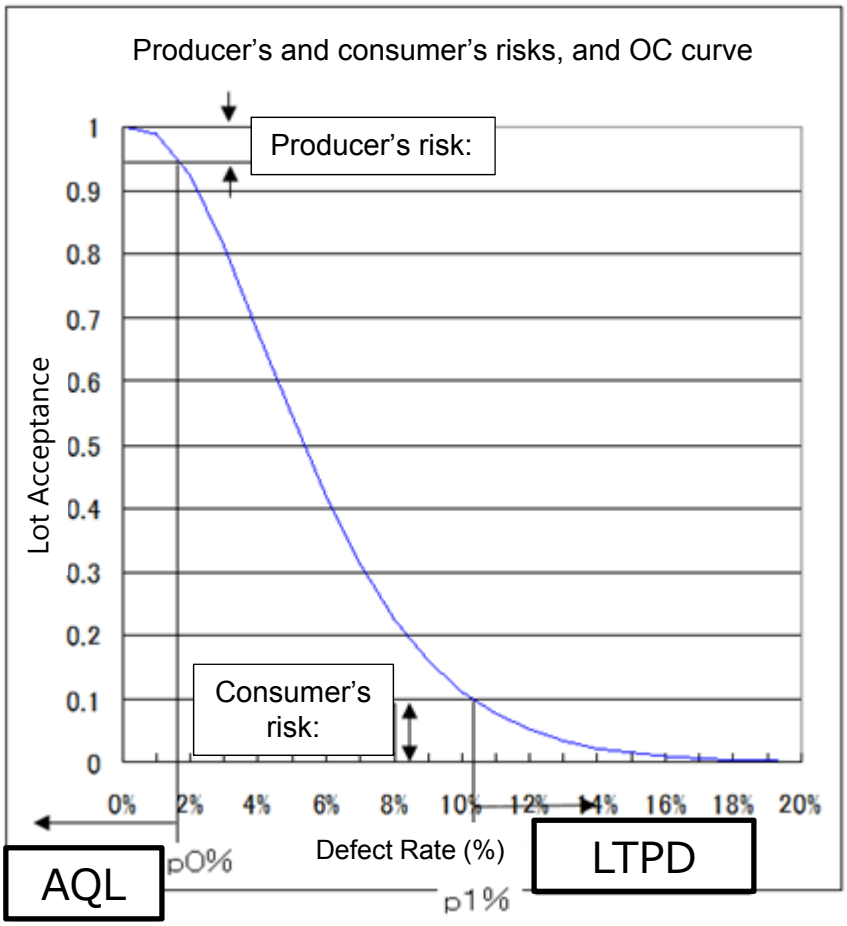


Figure 1-3-1 OC Curve

The sampling inspection by attributes, or the OC curve, is defined by the following four elements:

(1) Acceptable Quality Level (AQL): the maximum percentage of defectives (p0) in a lot considered definitely acceptable.

(2) Producer's risk (α): the probability of lots that meet the AQL will not be accepted.

(3) Lot Tolerance Percent Defective (LTPD): the minimum percentage of defectives (p1) in a lot considered definitely unacceptable.

(4) Consumer's risk (β): the probability of lots that exceed the LTPD will be accepted

1-4 Mathematics of Sampling Inspection by Attributes

Given a sampling plan (n, c), the probability that a lot with a defect rate of p% will be accepted based on the sampling plan can be found as follows.

Suppose the probability that x defective products will appear in a sample size n is P(x). The probability of lot acceptance L(p) is the sum of the probabilities P(0), P(1), . . ., P(c-1), P(c) of 0, 1, . . . , (c-1), c defective products occurring in the sample, and can be found using the following formula:

$$L(p) = P(0) + P(1) + \cdots P(c) = \sum_{x=0}^{c} P(x)$$

Next, with sampling inspection by attributes, P(x) is calculated based on hypergeometric distribution as follows:

$$P(x) = P(x, n, p, N) = \frac{\binom{Np}{x}\binom{N - Np}{n - x}}{\binom{N}{n}}$$

where, N is the lot size.

However, as N increases, hypergeometric distribution and binomial distribution become approximate in value. Therefore, in practice, when N/n > 10, performing the calculation based on a simpler binomial distribution can be used.

Appendix

1-5 Sampling Table

Table 1-5-1 shows the various inspection levels that indicate tested quantities (MIL-STD-105). If there is no particular level specified, inspection level II is normally used.

Table 1-5-1 Lot Size and Sample Code Letter

Lot size	Special Inspection Levels				General Inspection Levels		
	S-1	S-2	S-3	S-4	I	II	III
2 – 8	A	A	A	A	A	A	B
9 – 15	A	A	A	A	A	B	C
16 – 25	A	A	B	B	B	C	D
26 – 50	A	B	B	C	C	D	E
51 – 90	B	B	C	C	C	E	F
91 – 150	B	B	C	D	D	F	G
151 – 280	B	C	D	E	E	G	H
281 – 500	B	C	D	E	F	H	J
501 – 1200	C	C	E	F	G	J	K
1201 – 3200	C	D	E	G	H	K	L
3201 – 10000	C	D	F	G	J	L	M
10001 – 35000	C	D	F	H	K	M	N
35001 – 150000	D	E	G	J	L	N	P
150001 – 500000	D	E	G	J	M	P	Q
500001 or higher	D	E	H	K	N	Q	R

MIL-STD-105

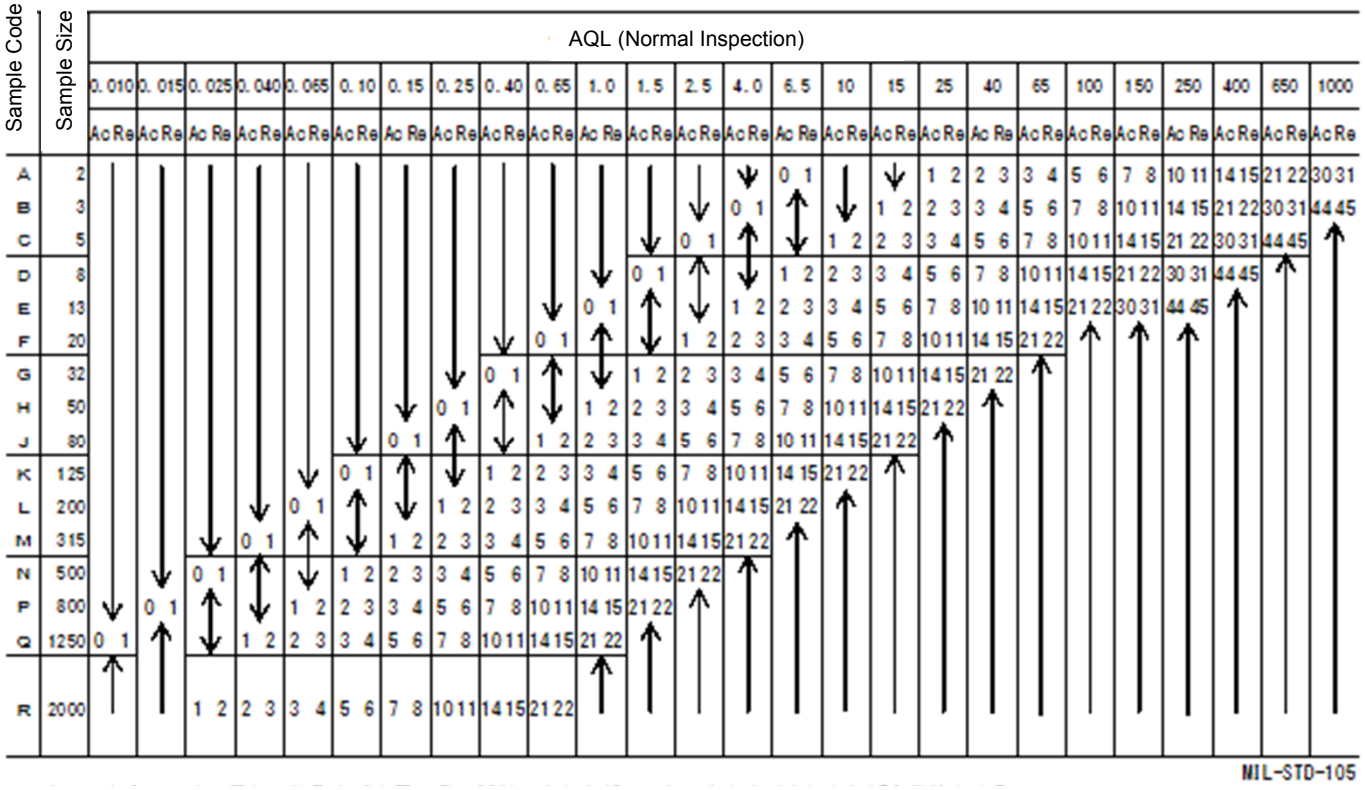
Note: MIL-STD-105 was replaced by ANSI Z1.4.

The sample size is determined by the sample size code letter. The applicable sample size code letter is determined by the specified lot size and inspection level in Table 1-5-2.

With a lot size of “501 – 1200” and a general inspection level of II, the sample code is “J” and the lot acceptance quality level applied is based on the “Single Sampling Plan for Normal Inspection” (Table 1-5-2). Thus, from Table 1-5-2, based on an AQL of 0.15%, the sample size is “80,” Ac is “0,” and Re is “1.” That is, the lot acceptance quality level requires zero defects in a sample size of 80.

Appendix

Table 1-5-2 Single Sampling Plan for Normal Inspection



Sample Code	Sample Size	AQL (Normal Inspection)																														
		0.010		0.015		0.025		0.040		0.065		0.10		0.15		0.25		0.40		0.65		1.0		1.5		2.5		4.0		6.5		10		15		25		40		65		100		150		250		400		650		1000	
		Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re
A	2																											0	1					1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	30	31
B	3																											0	1					1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	30	31	44	45
C	5																											0	1					1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	30	31	44	45		
D	8																							0	1					1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	30	31	44	45				
E	13																					0	1					1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22	30	31	44	45						
F	20																											1	2	2	3	3	4	5	6	7	8	10	11	14	15	21	22										
G	32																																																			
H	50																																																			
J	80																																																			
K	125																																																			
L	200																																																			
M	315																																																			
N	500																																																			
P	800																																																			
Q	1250																																																			
R	2000																																																		

MIL-STD-105

↓= Use first sampling plan below arrow. If sampling size equals, or exceeds, lot or batch size, do full-lot inspection.
↑= Use first sampling plan above arrow.
Ac = Acceptance number
Re = Rejection number

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