Basic Knowledge of Discrete Semiconductor Devices

Chapter III  Transistors

• Bipolar Transistors (BJTs)
• Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)
• Insulated-Gate Bipolar Transistors (IGBTs)

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Types of Transistors

Transistors are 3-terminal semiconductor devices that are classified into three types: bipolar, field effect and insulated-gate bipolar. Bipolar transistors are current-driving devices, and field-effect transistors (FETs) and insulated-gate bipolar transistors (IGBTs) are voltage-driving devices.

- Bipolar transistors (BJTs)
  - Small signal transistors
    - (2SAxx, 2SCxx, TTAxx, TTCxx)
    - Power transistors
      - (2SAxx, 2SBxx, 2SCxx, 2SDxx, TTAxx, TTBxx, TTCxx, TTDxx)
      - Built-in resistor transistors
        - (RNxx)
    - MOSFETs
      - Metal-oxide-semiconductor field-effect transistors
        - (2SKxx, 2SJxx, SSMxx, TPCxx, TKxx, TTKxx, TJxx etc.)
  - Field-effect transistors (FETs)
  - Insulated-gate bipolar transistors (IGBTs)
    - Junction FETs (JFETs)
      - Junction field-effect transistors
        - (2SKxx, 2SJxx, TTKxx)
    - IGBTs
      - (GTxx)
There are two types of bipolar transistors: **NPN type** and **PNP type**. NPN-type lineup ranges from high- to low-voltage products, and PNP type lineup includes products 400 V or lower (products 200 V or lower voltage are widely available).

They change small signals to large signals. This is called **amplification**. The ratio of collector current $I_C$ and base current $I_B$ ($I_C/I_B$) is called DC current gain, denoted as $h_{FE}$.

When small current ($I_B$) flows from base to emitter, current of $I_B \times h_{FE}$ flows from collector to emitter.

**BJTs are current-driven devices** driven by base current.

**Operation of NPN transistor**
- Base current: Positive current from base to emitter
- Collector current: Positive current from collector to emitter

**Operation of PNP transistor**
- Base current: Negative current from emitter to base
- Collector current: Negative current from emitter to collector
Built-in Resistor Transistors (BRTs)

BRTs are BJTs with built-in resistors. BJTs are often used together with resistors in electronic equipment. By using BRTs, which are transistors integrated with resistors, it is possible to eliminate the need for separate resistors.

(Ex. LED driving circuit)

**Fig. 3-2(a) Application example of BJT**

**Fig. 3-2(b) Equivalent circuit of BRT**

**Fig. 3-2(c) Why BJT needs resistance in its base circuit**

Unstable operation
It is difficult to control without current limitation

Stable operation
It is easier to control input current by inserting input resistance.

Tend to malfunction affected by noise of base.
Current directly flows to base of transistor, and it turns on.

Rare malfunction
Malfunction is rare, because noise goes through R2, which works as a bypass.
<Operation of JFETs>

JFET: Junction Field-Effect Transistor
(1) In N-channel-type junction field-effect transistor (Fig. 3-3(a)), electrons flow from source to drain when voltage is applied between source and drain.
(2) Electron flow of (1) is suppressed by applying reverse voltage between gate and source. (Narrowing path of electron flow)
(3) Electron flow of (1) can be controlled by changing width of depletion layer by reverse voltage between gate and source.

As shown above, voltage applied between gate and source controls the condition between drain and source. So FETs are voltage-driven devices.

(Note: Direction of current flow is opposite to that of electron flow. The mechanism of widening depletion layer is the same as for diode. In the case of JFET, current flows even if voltage between gate and source is zero, as shown above.)
Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)

Production and sales of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) currently exceed those of any other type of transistors.

There are two types of MOSFETs: N channel (See Fig.3-4(a) Nch below) and P channel (See Fig.3-4(b) Pch below). Nch is used in AC/DC power sources, DC/DC converters, AC-driven equipment, etc. Pch is widely used in load switches, high side switches, etc.

MOSFETs are voltage-driven devices that control drain current by application of voltage between gate and source. Differences between bipolar transistors and MOSFETs are listed in Table 3-1.

Table 3-1 Comparison of BJT and MOSFET

<table>
<thead>
<tr>
<th>BJT (Current-driven device)</th>
<th>MOSFET (Voltage-driven device)</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Small input impedance</td>
<td>• <strong>Large input impedance</strong></td>
</tr>
<tr>
<td>• Large reverse transfer capacitance</td>
<td>• Small reverse transfer capacitance</td>
</tr>
<tr>
<td>• Narrow safe operating region</td>
<td>• <strong>Wide safe operating region</strong></td>
</tr>
<tr>
<td>• Enables low-voltage operation (On voltage is 0.6-0.7V)</td>
<td>• Low gate power consumption</td>
</tr>
<tr>
<td></td>
<td>• Easy driving</td>
</tr>
</tbody>
</table>

Fig. 3-4(a) Symbol and operation of N-channel-type MOSFET

Fig. 3-4(b) Symbol and operation of P-channel-type MOSFET
Explained below are the differences of ON/OFF operation of BJT and MOSFET at output (collector-emitter or drain-source) depending on base or gate input voltage.

1. Base current of BJT starts flowing when base voltage increases, and collector current flows proportional to base current. When base voltage exceeds threshold voltage between base and emitter $V_{BE}$ (about 0.7 V), collector current can flow. On the other hand, to keep collector current flowing, base current must keep flowing. So, large driving power is needed. (Driving at low base voltage is possible, but large driving power is needed.)

2. MOSFET forms channel by applying voltage between gate and source. So, it needs a certain amount of gate voltage. But, once channel is formed, it stays in ON state and drain current continues flowing. Thus, this mechanism enables driving at low power. To change from ON state to OFF state, channel is removed by discharging accumulated gate charge. (Compared with BJT, larger gate voltage is needed but smaller driving power.)

Fig. 3-5(a) Switching operation of BJT

Fig. 3-5(b) Switching operation of MOSFET
This page explains the structure and operation of MOSFET by referring to planar gate MOSFET shown in Fig. 3-6(a).

1. Apply voltage between drain and source in positive polarity. (Drain-source voltage: \( V_{DS} \))
2. Apply voltage between gate and source in positive polarity. (Gate-source voltage: \( V_{GS} \))
3. As a result, electrons are attracted to P layer under a gate insulator film and P layer turns to N layer. (Such P layer that turned to N layer is called an “inversion layer.”)
4. All regions of MOSFET become N layer (from drain side: “N+”–“N–”–“inversion layer(N)”– “N+”) due to inversion mentioned in (3).
5. As a result, MOSFET works as resistance, and drain current determined by applied \( V_{DS} \) and load flows.

Planar gate MOSFET (π-MOS in Toshiba)

Trench gate MOSFET (U-MOS in Toshiba)

Note: “+”, “-” following N/P indicates density of dopant. “+” means high density and low resistance; “-” means low density and high resistance.

Fig. 3-6(a) Structure and operation of planar gate MOSFET

Fig. 3-6(b) Structure and operation of trench gate MOSFET
MOSFET Performance Improvement: Decision Factors of $R_{DS(ON)}$

(1) Decision factors of MOSFET’s $R_{DS(ON)}$ are as shown in Fig. 3-7 and Formula 3-(1). In low- and high-voltage MOSFET, device structure depends on the ratios of these decision factors.

(2) For example, in the case of $V_{DSS}=600$ V, $R_{drift}$ is the majority, and in the case of 30 V, the ratio of $R_{ch} + R_{J-FET}$ is high. Against this background, D-MOS (π-MOS) structure products are the mainstream medium- and high-voltage MOSFETs (250 V or higher), and trench MOS products are the mainstream MOSFETs for voltage under 200 V.

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**Planar MOS (π-MOS in Toshiba)**

- **Source**
- **Gate**
- **Drain**

Fig. 3-7(a)

ON resistance decision factors of D-MOS

$$R_{DS(ON)} = R_{sub} + R_{drift} + R_{J-FET} + R_{ch} + R_{N+}$$

In the case of $V_{DSS}=600$ V, the order is $R_{drift} >> R_{ch} > R_{J-FET}$, $R_{N+}$, $R_{sub}$, and $R_{DS(ON)}$ depends on $R_{drift}$.

In the case of $V_{DSS}=30$ V, the order is $R_{ch} >> R_{drift} > R_{N+}$, $R_{sub}$. $R_{DS(ON)}$ depends on $R_{ch}$ that can be minimized by fine patterning of trench MOS structure.

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**Trench MOS (U-MOS in Toshiba)**

- **Source**
- **Gate**
- **Drain**

Fig. 3-7(b)

ON resistance decision factors of Trench MOS

$$R_{DS(ON)} = R_{sub} + R_{drift} + R_{ch} + R_{N+}$$

Formula 3-(1)
The major issue of MOSFETs is “how to decrease ON resistance while utilizing pellet efficiently.” To resolve this issue, it is necessary to:

1. High voltage: Reduce resistance of \( R_{\text{drift}} \) by advanced super junction process.
2. Low voltage: Minimize resistance of \( R_{\text{ch}} \) by fine patterning of trench structure and reduce resistance of \( R_{\text{sub}} \) by thinning wafer.

In this regard, Toshiba is promoting DTMOS IV for high-voltage MOSFETs, and U-MOS VIII and U-MOS IX for low-voltage MOSFETs.

**Summary of approach to low ON resistance**

\[
R_{\text{ON}} = R_{\text{sub}} + R_{\text{drift}} + R_{\text{J-FET}} + R_{\text{ch}} + R_{\text{N+}}
\]

**Methods**
- Fine pattern
- Fine pattern
- Trench
- Super junction
- Thin wafer (High density of N++)

**Disadvantages**
- Increment of \( C_{\text{iss}} \)
- Same as above
- Long production TAT
- Difficult to produce

**Improvements**
- Shorter channel
- Trench & shorter channel
- Single epitaxial
- Thin-wafer technology

---

**Fig. 3-8 Factors for ON resistance of MOSFET**

**Methods**
- Fine pattern
- Fine pattern
- Trench
- Super junction
- Thin wafer (High density of N++)

**Disadvantages**
- Increment of \( C_{\text{iss}} \)
- Same as above
- Long production TAT
- Difficult to produce

**Improvements**
- Shorter channel
- Trench & shorter channel
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**Summary of approach to low ON resistance**

\[
R_{\text{ON}} = R_{\text{sub}} + R_{\text{drift}} + R_{\text{J-FET}} + R_{\text{ch}} + R_{\text{N+}}
\]

**Methods**
- Fine pattern
- Fine pattern
- Trench
- Super junction
- Thin wafer (High density of N++)

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- Increment of \( C_{\text{iss}} \)
- Same as above
- Long production TAT
- Difficult to produce

**Improvements**
- Shorter channel
- Trench & shorter channel
- Single epitaxial
- Thin-wafer technology
MOSFET Performance Improvement:
Super Junction MOSFETs (SJ-MOS)

1. SJ-MOS has pillar-shaped P layer (P pillar layer) in N layer. P and N layers are aligned alternately. (See Fig. 3-9(b).)

2. Depletion layer spreads in N- layer by applying $V_{DS}$, but the way it spreads differs for SJ-MOS compared with the case of general D-MOS. (See Fig. 3-9(a)/(b) for electric field intensity. Electric field intensity indicates the status of depletion layer.)

3. In the case of D-MOS the electric field intensity is the strongest at P/N- layer interface. When the electric field intensity exceeds the limit of silicon, break-over phenomenon (breakdown phenomenon) occurs, and this is the voltage limit. On the other hand, in the case of SJ-MOS, the electric field intensity is uniform in N- layer.

4. As a result, SJ-MOS can be designed with N- layer that has lower resistance, realizing low-ON resistance products. SJ-MOS can realize the same ON resistance as that of D-MOS but with smaller chip size than D-MOS.

Ex) Device with 600V voltage
$R_{ON}A = 90\Omega \cdot \text{cm}^2$ (π-MOS VII)

Ex) Device with 600V voltage
$R_{ON}A = 25\Omega \cdot \text{cm}^2$ (DT-MOSII) $R_{ON}A = 15\Omega \cdot \text{cm}^2$ (DT-MOSIV)

Fig. 3-9(a) Structure and electric field of D-MOS (π-MOS in Toshiba)

Fig. 3-9(b) Structure and electric field of SJ-MOS (DTMOS in Toshiba)
Summary of Features of MOSFETs by Structure

Features of MOSFETs and main applications based on their structures are shown in Table 3-2.

- High voltage: It is difficult to exploit advantages of U-MOS (Trench MOS) at high voltage.
- Low ON resistance: U-MOS is advantageous 250 V or less; DTMOS is advantageous above 250 V.

Few applications need high current at voltage from 250V to 500V. Thus, DTMOS lineup comprises products for 600V or higher.

- High current: The same tendency as for low ON resistance.
- High speed: U-MOS is disadvantageous for high-speed switching owing to increment of gate capacitance ($C_{iss}$). But, high-speed switching products with low $R_{ON} \times C_{iss}$ are commercialized (For U-MOS, design for low $R_{ON}$ and design for high-speed applications are separate.)

Expected applications are as follows: π-MOS for small- to medium-capacity converters, U-MOS for batteries, and DTMOS for medium- to large-capacity converters.

Table 3-2. Advantages and applications of MOSFETs by structure

<table>
<thead>
<tr>
<th>Names at Toshiba</th>
<th>(\pi)-MOS</th>
<th>U-MOS</th>
<th>DTMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>General name</td>
<td>D-MOS Planer gate MOS</td>
<td>Trench gate MOS</td>
<td>SJ-MOS</td>
</tr>
<tr>
<td>High voltage</td>
<td>Excellent up to 900 V</td>
<td><strong>Better up to 250 V</strong></td>
<td>Excellent 600 V or higher</td>
</tr>
<tr>
<td>Low ON voltage</td>
<td>Fair</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td>High current</td>
<td>Fair</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td>High speed</td>
<td>Good</td>
<td><strong>Good/Excellent</strong></td>
<td>Excellent</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Application</th>
<th>Field</th>
<th>Equipment</th>
<th>Field</th>
<th>Equipment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Small- to medium-capacity converters</td>
<td>Chargers, adaptors small- to medium-size TVs, LED lighting</td>
<td>Battery applications</td>
<td>PCM, NBPC, DC/DC converters, motor equipment for automobile</td>
</tr>
<tr>
<td></td>
<td>Medium- to large-capacity converters</td>
<td>Base station &amp; server power supplies, medium- to large-size TVs, power conditioners</td>
<td><strong>Medium- to large-capacity converters</strong></td>
<td><strong>Base station &amp; server power supplies, medium- to large-size TVs, power conditioners</strong></td>
</tr>
</tbody>
</table>
Performance of MOSFETs: Drain Current and Power Dissipation

Power dissipation and drain current that are typical absolute maximum ratings are calculated below. (Some different expressions have appeared recently to ensure consistency with competitors’ announcements.)

Power dissipation is calculated by thermal resistance and channel temperature. Drain current is calculated by the calculated power dissipation and ON resistance, using Ohm’s law.

**P\text{D}:** Power dissipation

⇒ Power loss allowed in designated temperature condition of the device

Q) How much is \( P\text{D} \) of MOSFET with \( T_{ch(max)}=150\,^\circ C, \, T_c=25\, ^\circ C, \, R_{th(ch-c)}=3.13\, ^\circ C/W \)?

A) \( P\text{D} = \frac{T_{ch(max)} - T_c}{R_{th(ch-c)}} = \frac{150\, ^\circ C - 25\, ^\circ C}{3.13\, ^\circ C/W} = 39.9\, W \div 40\, W \)

**I\text{D}:** Drain current

⇒ DC rating: DC current that flows in forward direction. (defined at room temperature)

Q) How much is \( I\text{D} \) rating of MOSFET with \( P\text{D}=40\, W, \, R_{DS(ON)}=0.16\, \Omega \) Max?

A) \( I\text{D} = (P\text{D}/R_{DS(ON)})^{1/2} = (40\, W/0.16\, \Omega)^{1/2} = 15.8\, A \)

**I\text{DP}:** Pulse drain current

⇒ Maximum drain current at designated pulse width. Generally, about 4 times DC current

Q) How much is \( I\text{DP} \) of MOSFET with \( I\text{D}=15.8\, A \)?

A) \( I\text{D} \times 4 = 15.8\, A \times 4 = 63.2\, A \)

The \( R_{DS(ON)} \times A \) of SJ-MOS (DT-MOS) is reduced by performance improvement. (DTMOS vs π-MOS VII=1:6) \( R_{DS(ON)} \) is reduced to 1/6 for the same cell area. ⇒ Current density is increased.
Performance of MOSFETs: Avalanche Capability

MOSFETs do not break even at voltage exceeding $V_{DSS}$ (rated voltage) when energy and drain current are within certain levels and temperature is under the rated channel temperature $T_{ch}$. This is called avalanche capability. The allowable energy is called avalanche energy and the current is called avalanche current.

**Avalanche energy**
\[ \Rightarrow \text{Allowable maximum energy even when applied voltage exceeds } V_{DSS} \text{ under designated conditions} \]

**Avalanche current**
\[ \Rightarrow \text{Allowable maximum current under avalanche condition} \]

\[ E_{AS} = \int_0^{t_a} i_a(t) V_{BR} dt, \quad i_a(t) = I_{AR} \left(1 - \frac{t}{t_a}\right) \]

\[ E_{AS} = \int_0^{t_a} I_{AR} V_{BR} \left(1 - \frac{t}{t_a}\right) dt \]

\[ = I_{AR} V_{BR} \left[t - \frac{t^2}{2t_a}\right]_0^{t_a} \]

\[ = \frac{t_a}{2} (I_{AR} V_{BR}) \]

Fig. 3-10 Avalanche capability (energy, current) test circuit, waveform and calculation formula

SJ-MOS has larger current density than D-MOS ($\pi$-MOS), and smaller avalanche capability at the same current rating.

DTMOS IV vs $\pi$-MOS VII: about 1/2.5
Performance of MOSFETs: Characteristic of Capacitance

\(C_{\text{iss}}\), \(C_{\text{rss}}\), and \(C_{\text{ooss}}\) are all important factors that influence switching characteristic of MOSFET.

**\(C_{\text{iss}}\): input capacitance** \(C_{\text{iss}} = C_{\text{gd}} + C_{\text{gs}}\)

⇒ Sum of gate-drain and gate-source capacitance: It influences delay time; bigger \(C_{\text{iss}}\) makes longer delay time.

**\(C_{\text{rss}}\): Reverse transfer capacitance** \(C_{\text{rss}} = C_{\text{gd}}\)

⇒ Gate-drain capacitance: Bigger \(C_{\text{rss}}\) makes characteristic of drain current rising deteriorate, which is disadvantageous for MOSFETs’ loss. Low capacitance is needed to drive at high speed.

**\(C_{\text{ooss}}\): Output capacitance** \(C_{\text{ooss}} = C_{\text{gd}} + C_{\text{ds}}\)

⇒ Sum of gate-drain and drain-source capacitance: It influences turn-off characteristic and loss with light load. In the case of large \(C_{\text{ooss}}\), turn-off \(dv/dt\) decreases, which is advantageous for noise. But loss with light load increases.

When \(V_{\text{DS}}\) is low (under 7 V in Fig. 3-11(b)), depletion layer is generated around P-layer, and so total area of depletion layer becomes large. But depletion layer aligns in-line by increasing \(V_{\text{DS}}\) and \(C_{\text{ds}}\) greatly decreases. Therefore, \(C_{\text{rss}}/C_{\text{ooss}}\) becomes small.
Performance of MOSFETs: Safe Operating Area
(Or Area of Safe Operating)

There are two modes of safe operating area (SOA).

1. **Forward Bias SOA (F.B. SOA):** Usable area of current and voltage at ON status.
2. **Reverse Bias SOA (R.B. SOA):** Usable area of current and voltage at turn-off operation.

Applied pulse width is very narrow because of use under switching operation.

Each mode can be defined as shown in Fig. 3-12(a).

- **Rated voltage and current operation at turn-off of MOSFET**
  is generally guaranteed in the same way as avalanche guarantee. Thus, R.B.SOA is not announced.
- **F.B.SOA** consists of three restriction areas, rated current, rated voltage and thermal resistance areas, and secondary breakdown area.
- **Three restriction areas** are limited by ratings of device or calculated from thermal resistance. But secondary breakdown area is obtained by measurement of actual device.

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**Fig. 3-12(a)** Defining SOA in actual operation

- **R.B.SOA is applied**
- **F.B.SOA is applied**

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**Fig. 3-12(b)** Example of MOSFET’s F.B.SOA

- **SINGLE NON-REPETITIVE PULSE** $T_c=25^\circ C$
- **CURVES MUST BE DERATED LINEARLY WITH INCREASE IN TEMPERATURE.**
Insulated-Gate Bipolar Transistors (IGBTs)

An IGBT (Insulated-Gate Bipolar Transistor) is a combination of a voltage-driven MOSFET and a bipolar transistor that can send high current. IGBTs are suitable for high-current applications.

**[Equivalent circuit and operation details]**
- Equivalent circuit of an IGBT is shown in Fig. 3-13(b). An NPN transistor is designed not to be driven by $R_{BE}$.
- Applying ON signal to gate of an Nch MOSFET turns conduction state.
- As a result, base current flows from emitter to base. This base current decreases ON resistance of the Nch MOSFET. (conductivity modulation effect)

**[Comparison with MOSFET]**
- Gate driving operation is the same as for Nch MOSFETs.
- In ON status, decrement of ON resistance of Nch MOS enables high current flow.
- PNP transistor’s emitter-base voltage drop occurs in the entire current area. (About 1.0V is accumulated as ON voltage.)
Operation of Insulated-Gate Bipolar Transistors (IGBTs)

Operation of the IGBT connected as in Fig. 3-14(a) is shown below.

1. Inversion layer is made in P layer under gate by applying positive voltage to gate. The Nch MOSFET in Fig. 3-14(b) turns on like a normal Nch MOSFET.

2. When the Nch MOSFET is ON status, collector’s potential is positive. So, holes are injected from P+ through N+ to N-, and this injection accelerates injection of electrons from emitter.

3. As a result, increment of carriers (electrons and holes) decreases resistance of N- layer that normally has high resistance (conductivity modulation effect). This operates as the Nch MOSFET that varies its ON resistance as shown in Fig. 3-14(b).

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Fig. 3-14(a) Operation of IGBT

Fig. 3-14(b) Equivalent circuit of IGBT and image of actual operation
**Performance Improvement of IGBTs: Evolution of Vertical Design**

Vertical design of IGBTs has gone through a change as shown in Fig. 3-15(a). It started with PT structure. Recently, thin PT structure (generally called “Field Stop”) has become the mainstream design in line with the use of thinner wafers. (Gate structure is the same as that of MOSFET.)

**PT (Punch Through) structure**
- Lifetime control in N-layer (drift layer)
- Emitter (E) Gate (G)
- Collector (C)

**NPT (Non-Punch Through) structure**
- Control of dopant in P+ layer.
- Injection control of carrier (hole)
- Emitter (E) Gate (G)

**Thin PT (Field Stop) structure**
- Control of dopant in P+ layer.
- Injection control of carrier (hole)
- Emitter (E) Gate (G)

![Fig. 3-15(a) Transition of IGBT’s vertical design](image)

**Performance Improvement of IGBTs:**

**Evolution of Vertical Design**

- Achieving high-speed switching and low $V_{CE(sat)}$
- Having positive relation between temperature and $V_{CE(sat)}$
- High breakdown capability

**Fig. 3-15(b) Difference of forward characteristic between PT type and NPT type**

$V_{CE(sat)}$ characteristic of PT type has “Q point,” which is the cross point of high temperature and room temperature. In the case of NPT type, (same as MOSFET) $V_{CE(sat)}$ at high temperature is larger than that at room temperature. Thus, collector current is balanced in parallel driving.

**Note:** $V_{CE(sat)}$ characteristic – voltage drop when collector current flows in forward direction.
What are RC-IGBTs and IEGTs?

**Reverse conductive IGBT: RC-IGBT**
- Structure of an RC-IGBT is shown in Fig. 3-16(a). A diode is made by forming N layer partially in P layer that works as collector of the IGBT. This diode works as an FWD(*1) that is generally inserted in circuit with the IGBT.
- Thin wafer technology enabled commercialization of RC-IGBTs. A diode and an IGBT are combined in one chip. Thus, assembly is easy and reasonable, but because it is difficult to control diode and IGBT separately, RC-IGBTs are not suitable for certain applications.

(*1: FWD—Free Wheeling Diode. Generally, it is used to send reflux current generated by reactor.)

**Injection-enhanced gate transistor: IEGT**
- Decrement of carrier density of a high-voltage IGBT in its emitter side of drift layer (N-layer) makes it difficult to obtain low $V_{CE(sat)}$.
- IEGTs have been developed to obtain low $V_{CE(sat)}$ at high voltage (generally, more than 1,200 V).
- Fig. 3-16(b) shows IEGT’s structure and principle.
- It has trench gate structure and dummy trench gate structure. As a result, carriers are accumulated under dummy gate structure. And this mechanism increases carrier density.
- High carrier density decreases resistance of drift layer, and makes $V_{CE(sat)}$ low.
IGBTs are suitable for applications that have easy driving circuit and need high current. They are currently used in IH (Induction Heating) equipment adopting soft-switching under 50kHz, home appliances, vehicles, and a wide variety of AC drives. In future, their application fields are expected to expand to include various AC drives.

Table 3-3. Typical application of IGBTs

<table>
<thead>
<tr>
<th>Application of IGBTs</th>
<th>Features</th>
<th>Voltage</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Home appliance and induction heating equipment</strong></td>
<td>(1) Only for soft switching (voltage/current resonance) (2) Low switching loss (3) Includes an FWD</td>
<td>600V to 1800V</td>
<td>Cooking equipment, IH rice cooker, Inverter microwave oven, Remaining IH heating of copier</td>
</tr>
<tr>
<td><strong>General inverter</strong></td>
<td>(1) For hard switching (2) High breakdown capacity (3) Includes an FRD</td>
<td>600V</td>
<td>Inverter washer, UPS, Inverter controller, Inverter air conditioner, Air conditioner for automobile</td>
</tr>
</tbody>
</table>

Note: IGBTs are not so suitable for high-speed switching as MOSFETs because of bipolar operation.
This page compares forward characteristic of the MOSFET(D-MOS) and the IGBT at voltage from 500V to 600V. In low-current area, the MOSFET has small voltage drop, and has an advantage. On the other hand, forward voltage characteristic of the IGBT is better than that of the MOSFET in high-current area, as shown in Fig. 3-17. As forward characteristic of the MOSFET has strong positive dependence on temperature, the difference in performance of IGBT and MOSFET widens as temperature increases.

**Fig. 3-17 Comparison of forward characteristic between MOSFET and IGBT**

This figure compares medium- and high-voltage products. Low-voltage MOSFETs, such as trench MOSFETs, have much lower ON resistance than IGBTs in working current area.

In view of these characteristics and switching performances:

• MOSFETs are adopted for applications such as switching power supply operating at about 100 kHz and at low current density.

• IGBTs are adopted for applications such as AC drive operating under 20 kHz and at high current density.
## Comparison of Transistors by Structure

<table>
<thead>
<tr>
<th>Structure of transistors</th>
<th>Bipolar Transistor (BJT)</th>
<th>MOSFET</th>
<th>IGBT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate (base) driving method</td>
<td><strong>Current driving</strong> (Low input impedance)</td>
<td><strong>Voltage driving</strong> (High input impedance)</td>
<td><strong>Voltage driving</strong> (High input impedance)</td>
</tr>
<tr>
<td>Gate (base) driving circuit</td>
<td>Complicated (Many part counts)</td>
<td>Simple</td>
<td>Simple</td>
</tr>
<tr>
<td>Forward characteristic</td>
<td><strong>Low ( V_{CE(sat)} )</strong> (High current region) No threshold voltage</td>
<td><strong>High ON voltage</strong> (Unipolar operation)</td>
<td><strong>Low ( V_{CE(sat)} )</strong> With threshold voltage</td>
</tr>
<tr>
<td>Switching speed</td>
<td><strong>Low speed</strong> (with carrier accumulation effect)</td>
<td><strong>Ultra high speed</strong> (Unipolar operation)</td>
<td><strong>High speed</strong> (Middle of MOSFET and BJT)</td>
</tr>
<tr>
<td>FWD (Include body diode)</td>
<td>No</td>
<td>Yes (Body diode)</td>
<td>No (Yes in RC structure)</td>
</tr>
<tr>
<td>Safe operating area</td>
<td>Narrow</td>
<td>Wide</td>
<td>Middle</td>
</tr>
</tbody>
</table>
## Datasheets of MOSFET: Maximum Ratings

### <Absolute maximum ratings>

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source voltage</td>
<td>$V_{DSS}$</td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source voltage</td>
<td>$V_{GSS}$</td>
<td>±30</td>
<td>V</td>
</tr>
<tr>
<td>Drain current DC</td>
<td>$I_D$</td>
<td>12</td>
<td>A</td>
</tr>
<tr>
<td>Drain power dissipation (Tc = 25°C)</td>
<td>$P_D$</td>
<td>45</td>
<td>W</td>
</tr>
<tr>
<td>Single pulse avalanche energy (Note 2)</td>
<td>$E_{AD}$</td>
<td>350</td>
<td>mJ</td>
</tr>
<tr>
<td>Avalanche current</td>
<td>$I_{AR}$</td>
<td>12</td>
<td>A</td>
</tr>
<tr>
<td>Repetitive avalanche energy (Note 3)</td>
<td>$E_{AR}$</td>
<td>4.5</td>
<td>mJ</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>$T_{ch}$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>$T_{stg}$</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

- **Drain-source voltage ($V_{DSS}$)**: Maximum voltage of drain to source that can be applied.
- **Gate-source voltage ($V_{GSS}$)**: Maximum voltage of drain to source that can be applied.

Circuit must be designed not to exceed this voltage including surge voltage.

- **Drain current ($I_D$)**: Maximum drain current.
- **Drain current (pulsed) ($I_{DP}$)**: Maximum pulsed drain current.

Normally, pulse width is described in safe operating area.

- **Power dissipation ($P_D$)**: Power loss allowed to generate in the device. It is allowable thermal capability at $T_c=25°C$.
- **Avalanche energy, single-pulse and continuous ($E_{AS}$)**: Maximum allowed energy under designated condition.
- **Avalanche current ($I_{AR}$)**: Maximum current at avalanche operation.
- **Channel temperature ($T_{ch}$)**: Maximum channel temperature where the device can operate.
- **Storage temperature ($T_{stg}$)**: Temperature range for storage without operating the MOSFET.

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: $V_{DD}=90$ V, $T_{ch}=25°C$ (initial), $L=4.36$ mH, $R_G=25$ Ω, $I_{AR}=3.0$ A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature.

This transistor is an electrostatic-sensitive device. Please handle with caution.
 datasheets of MOSFET: electrical characteristics

<THERMAL CHARACTERISTICS>
Used to calculate channel temperature

<ELECTRICAL CHARACTERISTICS>

• Gate leakage current ($I_{GSS}$)
  Cut-off current from gate to source
• Drain cut-off current ($I_{DSS}$)
  Cut-off current from drain to source
• Drain-source breakdown voltage ($V_{(BR)DSS}$)
  Breakdown voltage between drain and source
  Gate and source are shorted not to make channel.
• Gate threshold voltage ($V_{th}$)
  Gate-source voltage that can send designated drain current

• Drain source ON resistance ($R_{DS(ON)}$)
  It corresponds to collector-emitter saturation voltage ($V_{CE(sat)}$) of bipolar transistor. Voltage drop is expressed as resistance under designated condition. It has positive thermal coefficient.
• Forward transfer admittance ($|Y_{fs}|$)
  A ratio with change of output current and change of gate input voltage. Its unit is “S: siemens”, same as [A]/[V].
Datasheets of MOSFET: Capacitance and Switching Characteristics

<table>
<thead>
<tr>
<th>Electrical characteristics</th>
</tr>
</thead>
</table>

- Input capacitance \( C_{iss} \) equivalent to \( C_{gd} + C_{gs} \)
- Gate-drain and gate-source capacitance
- Reverse transfer capacitance \( C_{rss} \) equivalent to \( C_{gd} \)
- Gate-drain capacitance
- Output capacitance \( C_{oss} \) equivalent to \( C_{gd} + C_{ds} \)
- Gate-drain and drain-source and gate-drain capacitance

### Switching time

<table>
<thead>
<tr>
<th></th>
<th>( t_r )</th>
<th>( t_{on} )</th>
<th>( t_f )</th>
<th>( t_{off} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise time</td>
<td>40</td>
<td>80</td>
<td>15</td>
<td>110</td>
</tr>
<tr>
<td>Turn-on time</td>
<td>100</td>
<td>150</td>
<td>15</td>
<td>150</td>
</tr>
<tr>
<td>Fall time</td>
<td>40</td>
<td>80</td>
<td>15</td>
<td>110</td>
</tr>
<tr>
<td>Turn-off time</td>
<td>100</td>
<td>150</td>
<td>15</td>
<td>150</td>
</tr>
</tbody>
</table>

- **Rise time** \( (t_r) \)
  - It is the time when drain-source voltage varies from 90% to 10%.
- **Turn-on time** \( (t_{on}) \)
  - It is the time between the instant when gate-source voltage rises to 10% and the instant when drain-source voltage falls to 10%.

- **Fall time** \( (t_f) \)
  - It is the time when drain-source voltage varies from 10% to 90%.
- **Turn-off time** \( (t_{off}) \)
  - It is the time between the instant when gate-source voltage falls to 90% and the instance when drain-source voltage rises to 90%.
## Datasheets of MOSFET: Body Diode

### <Electrical characteristics>

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous drain reverse current (Note 1)</td>
<td>IDR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>12</td>
<td>A</td>
</tr>
<tr>
<td>Pulse drain reverse current (Note 1)</td>
<td>IDRP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>48</td>
<td>A</td>
</tr>
<tr>
<td>Forward voltage (diode)</td>
<td>VDSF</td>
<td>IDR = 12 A, VGS = 0 V</td>
<td>—</td>
<td>—</td>
<td>—1.7</td>
<td>V</td>
</tr>
<tr>
<td>Reverse recovery time</td>
<td>trr</td>
<td>IDR = 12 A, VGS = 0 V, dlDR/dt = 100 A/μs</td>
<td>1000</td>
<td>1200</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Reverse recovery charge</td>
<td>Qrr</td>
<td>dlDR/dt = 100 A/μs</td>
<td>—</td>
<td>13</td>
<td>—</td>
<td>μC</td>
</tr>
</tbody>
</table>

- Continuous drain reverse current (I<sub>DR</sub>)
  Forward current of drain-source diode with DC.
- Pulse drain reverse current (I<sub>IDRP</sub>)
  Forward current of drain-source diode with pulse.
- Forward voltage (diode) (V<sub>DSF</sub>)
  Voltage dropdown of drain-source diode with forward current.
- Reverse recovery time (t<sub>rr</sub>)
  Reverse recovery time of drain-source diode under designated condition.
- Reverse recovery charge (Q<sub>rr</sub>)
  Reverse recovery charge of drain-source diode under designated condition.
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