

Toshiba Custom SoC/ASIC Design: Leverage Our System and Silicon Expertise

Collaborating in the Design and Development of Custom SoCs/ASICs.

Experience in System Level and Chip Design

Toshiba, a premier semiconductor manufacturer, has provided leading companies with Custom SoCs/ASICs for over three decades. Toshiba customers benefit from access to an extensive portfolio of industry-standard and customizable IP, robust design methodologies and leadership in producing high-complexity and low-power SoCs/ASICs with the industry's most advanced packaging technologies.

Flexible Engagement Model

We excel in providing a flexible engagement model starting at architectural design, RTL, netlist or GDS handoff with step-by-step collaboration throughout the design cycle to meet your schedule and your budget.

Advanced Process Technologies and IP Libraries

Key offerings include 130/90/65/40/28 nm CMOS process technologies, standard cell libraries and PDKs. Our broad and proven IP portfolio and extensive design expertise results in a high level of design confidence and first-time success.

U.S. Design Centers

Toshiba operates two U.S.-based, world-class Design Centers located in San Diego, Calif. and Marlborough, Mass. Our seasoned design implementation teams will work closely with you to ensure a successful design experience.

Toshiba offers design implementation with deep experience in DFM, mixed signal design, high-speed and low-power design, along with mask making and wafer fabrication, yield management and wafer test, bumping and assembly.

Flexible Design Services and Innovative Technologies

- ▶ Continuous collaboration from architectural design through production
- ▶ Flexible hand-off model starting at:
 - Architectural design
 - RTL
 - Netlist
 - GDS
- ▶ Broad IP library and IP design services
- ▶ Low risk manufacturing and foundry relationships
- ▶ System level technologies and application expertise in networking, mobile, consumer, multimedia, storage and other applications
- ▶ Proven methodologies for:
 - Analog, logic, memory and low-power
- ▶ Fully-staffed U.S.-based expert design centers with capability to collaborate seamlessly
 - San Diego, Calif.
 - Marlborough, Mass.
- ▶ Novel 3D packaging solutions such as chip-on-chip, package-on-package and SCS (ASIC + DRAM) including TSV
- ▶ Robust implementation methodology delivers predictive design closure on timing, power, signal integrity and manufacturability
- ▶ Chip and package co-design methodology enables optimization of SoC/ASIC for cost and performance
- ▶ Advanced low-power methodology and special libraries for low-power SoC/ASIC designs
- ▶ World-class development turnaround time using Toshiba's highly optimized and predictable design flow

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CONTACT INFORMATION

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Technology

- ▶ Industry leader in designing high-performance system-level ICs in 130/90/65/40/28 nm
- ▶ Eight-layer copper for 90/65/40 nm CMOS technology
- ▶ Logic densities up to 800,000 gates/mm² (65 nm); 2,100,000 gates/mm² (40 nm); 4,300,000 gates (28 nm)
- ▶ Cost-effective embedded DRAM cores of less than 10 mm sq for 32 Mb in 65 nm
- ▶ High-performance I/O: PCI Express, USB 2.0/3.0, XAUI, Fiber Channel, SONET/SDH, SATA, HDMI, MIPI®, DisplayPort™, DDR2/3
- ▶ High-performance and high pin-count packages
- ▶ Cost-effective 1 Gb DRAM integration with an ASIC in a Stacked Chip SoC (SCS)

Electronic Design Automation

Toshiba EDA solutions use commercial tools from leading EDA companies including Synopsys, Cadence, Magma, Mentor Graphics and Apache for synthesis, implementation, power and signal integrity, and logic, timing and physical verification. Our centralized EDA group in San Jose, Calif. develops customized implementation and low-power methodologies for both high-performance and low-power SoC/ASIC designs.

Choosing Toshiba

As a worldwide leader in chip design and manufacturing, Toshiba possesses the requisite design experience, tools, design methodologies, IP libraries and manufacturing expertise to give its customers a complete, end-to-end Custom SoC/ASIC development process with quality results and minimized NRE.

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