

Product Brief

Highlights

- 4K Ultra High Definition (HD) video HDMI® output into MIPI® Display Serial Interface (DSI).
- Enables MIPI DSI dual link interface displays to accept up to Ultra HD (4K) resolution video from HDMI source.
- Ideal for mobile and CE solutions with LCD displays requiring Ultra HD over MIPI DSI dual link.
- Support for common 3D formats and compatible protocols with the HDMI 1.4b standard.
- Support for up to:
 - 4096 x 2160 @24bpp video resolution at refresh rate of 24 fps
 - 3840 x 2160 @24bpp video resolution at refresh rates of 30 fps
- Enables YCbCr to RGB and YCbCr to RGB color format conversion.
- I2S and SLIMbus® audio support.
- Applications include head mounted displays (HMDs), 3D video viewers, LCD monitors and displays, smart projectors and digital cameras.

TC358870 Ultra HD Display Serial Interface Converter Chipset (4K HDMI® to MIPI® DSI)

Description

The Toshiba TC358870 High Definition Multimedia Interface (HDMI®) to MIPI® Display Serial Interface (DSI) converter chipset supports 4K video resolution for next-generation Ultra High Definition display applications. The TC358870 enables a source device with 4K HDMI video output to drive an Ultra HD (4K) or Quad HD (2560 x 1440) LCD display with a MIPI DSI dual-link interface.

The demand for mobile computing has increased the use of small form factor high-resolution displays. These applications may require 4K or Quad HD resolution LCD displays to support video input over HDMI. MIPI DSI is a commonly used high-speed input interface for Ultra HD resolution LCD displays. The Toshiba TC358870 bridge chips enable a 4K HDMI output capable source to drive an LCD display with a MIPI DSI dual link interface.

The maximum resolution supported is 4096 x 2160 @ 24 fps, limited by 297 MHz maximum HDMI bandwidth. The bridge

supports common 3D video formats and protocols compatible with the HDMI 1.4 standard. The TC358870 interfaces to the display with a configurable MIPI DSI dual-link interface (for a total of 8 data lanes at speeds of up to 1.0 Gbps per lane).

The Toshiba TC358870 is a follow on part to the Toshiba TC358779 adding a 297 MHz HDMI receiver (Rx) and a MIPI DSI dual link interface to support next-generation 4K Ultra HD video format.

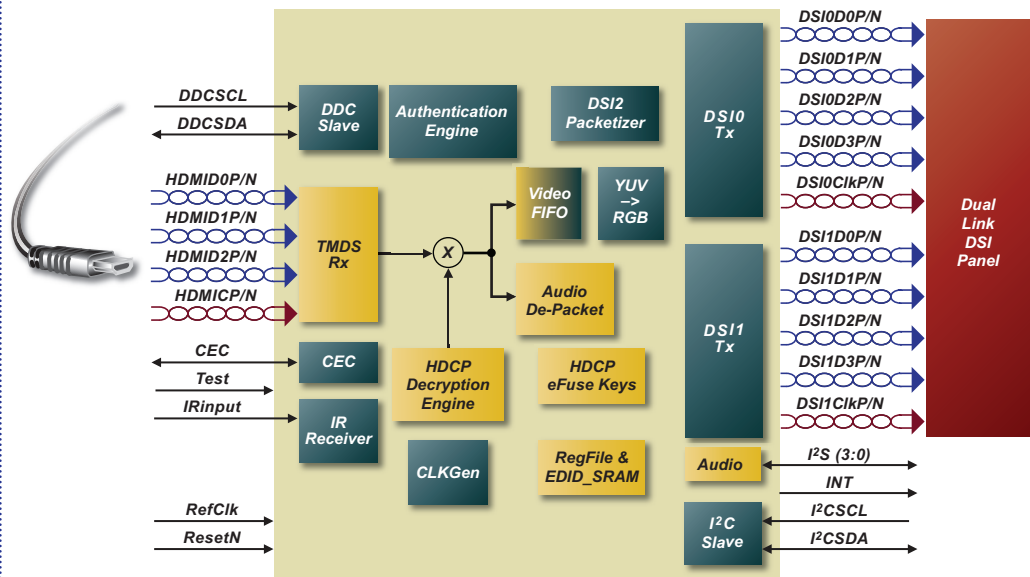
The Toshiba TC358870XBG comes in a small 80-pin package (7 mm x 7 mm), 0.65 mm ball pitch and 1.0 mm maximum height designed for a non-HDI Board. It is designed with clock and power management circuitry to support low power states.

Features

HDMI-RX Interface

- HDMI 1.4b
 - Video format support
 - Up to 4096 x 2160 (4Kx2K) @ 24 fps RGB or YCbCr444: 24-bpp (bit-per pixel)
 - Up to 3840 x 2160, @ 30 fps, RGB or YCbCr444: 24-bpp

TC358870 Display Serial Interface Converter Chipset Block Diagram



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- Color format conversion support
 - 4:2:2 to 4:4:4
 - 4:4:4: to 4:2:2
 - RGB888 to YCbCr (4:4:4/4:2:2)
 - YCbCr (4:4:4/4:2:2) to RGB888/666
- Maximum HDMI clock speed of 297 MHz
- Audio support
 - Internal Audio PLL to track N/CTS value transmitted by the ACR packet
- 3D support
- Support for HDCP1.4 decryption
- EDID support, release A, revision 1 (Feb 9, 2000)
 - First 128 byte (EDID 1.3 structure)
 - First E-EDID extension: 128 bytes of CEA extension version 3 (specified in CEA 861-D)
 - Embedded 1K-byte SRAM (EDID_SRAM)
- S/P-DIF Audio Interface
 - Supports 2-channels
- MIPI SLIMbus Audio Interface
 - Up to 8-channel data (2, 4, 6 or 8)
 - Supports Active Framer (Host) mode as well as active framer outside the chip
 - Active Manager is not supported.
 - Supports isochronous, pushed and pulled protocols
 - Supports up to 28.8MHz root clock frequency (in Active Framer mode)
- I²C Slave Interface
 - Support for normal (100KHz), fast mode (400 KHz) and ultrafast mode (2MHz)
 - Used by an external Master to configure all TX358870 internal registers
 - Support for two I²C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)

DSI TX Interface

- MIPI DSI compliant (Version 1.1 22 November 2011)
- DSI dual link support
 - DSI0 and DSI1: Each link supports 4 data lanes @1.0 Gbps (8-data lanes total)
 - DSI0 carries the left half data of HDMI Rx video stream and DSI1 carries the right half data of HDMI Rx video stream
 - DSI0 can be assigned/programmed to either DSI Tx
- Video data format support
 - RGB888, YCbCr444, YCbCr 422 16-bit and YCbCr 422 24-bit
 - YCbCr inputs can be converted into RGB888 before outputting

Audio Output Interface

Any of the four audio interfaces are available: I²S, TDM, S/P-DIF or SLIMbus (pins are multiplexed)

- I²S Audio Interface
 - Up to 4 data lanes for 8-channel data

Power Supply Inputs

- Core: 1.1V and MIPI D-PHY: 1.2V
- I/O: 1.8V–3.3V
- HDMI, audio and analog PLL: 3.3V

Package

- TC358870XBG package for non-HDI board:
 - 80-pin, 7.0 x 7.0 mm, 0.65 mm ball pitch, 1.0 mm maximum height

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