

TX4939XBG-400 64-bit RISC Processor

Highlights

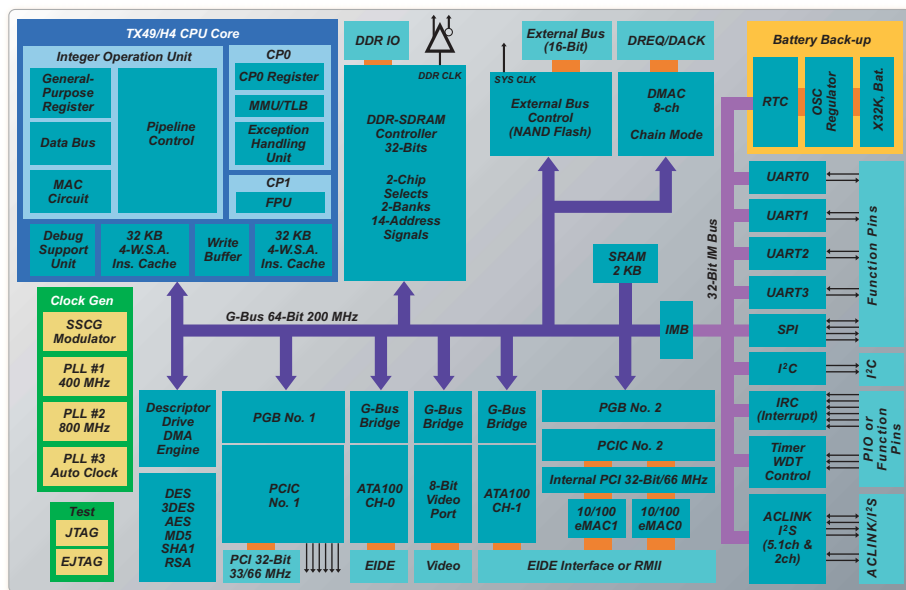
- First 90 nm embedded PCI MIPS RISC processor product with 400 MHz TX49/H4 core
- High-performance security engine that off-loads CPU core for implementing IPsec, SSL and FEC algorithms
- 32-bit DDR400 DRAM controller
- High-power PCI controller
- 8/16-bit local bus for NAND/NOR flash and other I/O devices
- Two, 100 MB ATA/ATPI channels
- Three serial or one serial and one 8-bit parallel video ports compliant to ITU Bt.656 standard
- On-chip Ethernet MAC and NAND flash memory controller
- Real time clock (RTC) with battery backup support
- Built-in SSCG provides the maximum EMI reduction

Description

The TX4939 is the newest member of TX49 MIPS RISC microprocessor family. It is ideally suited for low-power, high-performance applications like IP set-top-boxes, home gateways and multimedia appliances. The TX4939 microprocessor is a highly integrated standard product based on the Toshiba TX49/H4 400 MHz processor core, a 64-bit MIPS I, II, III instruction set architecture (ISA) compatible with additional instructions.

The TX4939 has multiple on-chip peripheral functions including 8/16-bit local bus controller, a highly optimized security engine, serial/parallel video ports, ATA controllers, a DDR SDRAM controller, a NAND flash controller, Ethernet MAC controllers (RMII), a PCI controller, a DMA controller, an interrupt controller, an AC-link controller, serial and parallel ports, timers/counters and real-time clock with battery back-up support (RTC).

TX4939 Block Diagram



Features

- TX49/H4 core (on-chip IEEE754 compliant single/double precision FPU)
- DDR SDRAM controller (2 channels: 32-bit/100-200MHz)
- 8/16-bit local bus for NAND/NOR flash and other I/O devices
- 32-bit PCI controller (33 MHz/66 MHz) with 4 clock outputs, arbiter and interrupts for 6 devices
- PCI boot and satellite mode (PCI slave mode) support
- Direct memory access controller (8 Channels [4 Channels are dedicated to ACLC])
- SIO (4 channels, ch2 and ch3 are multiplexed with synchronous parallel interface (SPI))
- SPI (multiplexed with SIO ch2, ch3)
- 8-bit video port (SPI)
- Serial TS video port (Max 3-ports)
- Timer/counter (3 channels)
- AC-link controller / I2S (5.1ch) / I2S (2ch)

www.Toshiba.com/taec

Product Brief

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- Ether MAC with RMI (2 channels)
- 2-channel 100 MB ATA/ATPI IDE I/F
- Security engine—DES/3DES/AES/MD5/SHA1/RSA/EXOR for FEC
- Battery backup RTC (48-bit linear counter, 250 bytes CMOS RAM)
- Extensive power management feature
- Any internal controller can stop clock and keep RESET status
- On-chip SRAM (2 KB)
- Interrupt controller (NMI, 4 external inputs for PCI and 3 external interrupt inputs for external bus)
- Low-power consumption (Typ. <2 watts)
- The TX4939 operates at 1.2V (internal), 2.5V (DDR) and 3.3V (I/O block), and supports the low-power consumption mode (Halt Mode).
- Maximum operating frequency (for the CPU): 400 MHz
- IEEE1149.1 (JTAG) support: debugging support unit
- Built-in clock generator
- 20 MHz single Xtal operation. Single source for all necessary clocks including audio sampling clock
- Audio sampling at 96, 48, 44.1, 32, 24, 22.05, 16, 8 KHz (x512)
- Built-in spread spectrum clock generator (SSCG)
- Baud rate clock source 14.7456 MHz
- Package: PBGA 456 pins: 1.00 mm ball pitch. Thirty-six pins are thermal ball for heat dissipation
- 27 mm x 27 mm package size

TX System RISC Development Tools

- Reference Board: Main Reference Board—RBTX4939

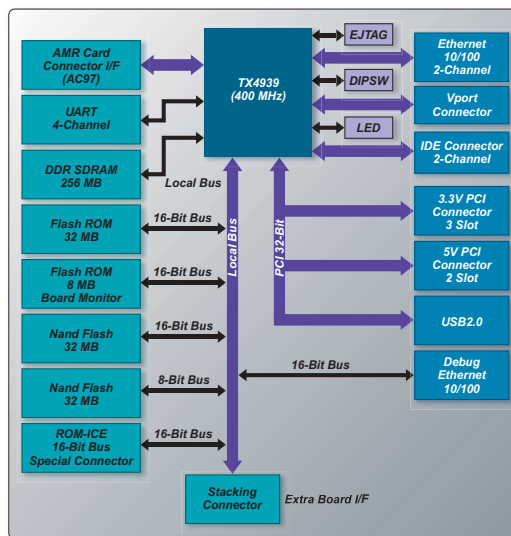
Operating Systems

- Wind River Systems, Inc.: VxWorks
- Monta Vista Software, Inc.: Monta Vista Linux
- Microsoft Corporation: Windows CE.NET

Development Tools

- Green Hills Software, Inc.: MULTI 2000 Compiler & Debugger, Green Hills Probe (JTAG Emulator)
- Wind River Systems, Inc.: Wind River Probe with Debugger
- YDC (Yokogawa) : AdvicePlus Emulator with Debugger
- Macraigor : TX49 Emulator

TX4939 Reference Board Block Diagram



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