100-V Class Two-step-oxide Field-Plate Trench MOSFET to Achieve Optimum RESURF Effect and Ultralow On-resistance

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Abstract—We propose a 100-V class two-step-oxide Field-Plate MOSFET (2-step FP-MOSFET), which is formed by two steps of thick-oxide to simplify the structure and fabrication process. By optimizing design parameters, we reveal the 2-step FP-MOSFET can achieve sufficient RESURF (Reduced Surface Field) effect and an ultralow specific on-resistance (Ron·A). Measurement results showed breakdown voltage of 109.9 V and the Ron·A of 27.7 mohm·mm² with good process controllability. Moreover, as figure-of-merit of the 2-step FP-MOSFET, Ron·Qg and Ron·Qsw were reduced by 27.1% and 4.7%, respectively, compared with conventional one. Power loss estimation is also discussed by simple calculation.

Keywords—field plate, RESURF, shielded gate, oxide slope, figure-of-merit, power loss.

I. INTRODUCTION

Field-plate trench MOSFETs (FP-MOSFETs) have been continuously developed for high efficiency and low energy consumption power electronics [1]–[9]. In particular, 100-V class MOSFETs are expected to be applied to 48-V input power converters and 48-V battery automobile systems. In the FP-MOSFET, vertical field plates inside trench have RESURF (Reduced Surface Field) effect in mesa region with high impurity concentration, so that tradeoff between breakdown voltage (VBD) and specific on-resistance (Ron·A) is drastically improved. We have reported that multiple stepped oxide (MSO) FP-MOSFET can achieve an ultralow Ron·A [10]. It was close to an ideal gradient field-plate structure in previous work [10]. The most part of the VBD is determined by poly-silicon field-plate length LFP, and the remaining part is shared by p-base/n-drift junction and trench bottom region. Field-plate oxide thickness tOX,b and tOX,t correspond to a position of top and bottom of the LFP, respectively. Oxide-slope K is defined by

\[ K = \frac{L_{FP}}{t_{OX,t} + \alpha - t_{OX,b}}, \]  

(1)

where \( \alpha \) is trench angle. In particular, the tOX,b and drift layer concentration (ND) are important to obtain an appropriate charge balance. An optimum charge density (Qopt) in the mesa region against both sides' field-plates, is given by

\[ Q_{opt} = \frac{2E_r \varepsilon_i}{q}, \]  

(2)

where \( E_r \) is average of the vertical electric field at the VBD, \( \varepsilon_i \) is permittivity of silicon and \( q \) is elementary charge. To obtain the VBD over 100 V, the \( E_r \) is estimated to 2.5E5 ~ 3.5E5 V/cm by TCAD simulation. The relationship between the mesa width (W mesa) and the ND is expressed by

\[ N_D = \frac{Q_{opt}}{W_{Mesa}}, \]  

(3)

When the \( W_{Mesa} \) is 1.0 \( \mu m \), the ND is calculated to 3.2E16 ~ 4.5E16 /cm².

Fig. 2(a)–(d) shows simulated 2-D potential contours and 1-D vertical electric field distributions along trench sidewall for conventional, MSO and 2-step FP-MOSFETs, at ND = 3.0E16 /cm². Both of FP-MOSFETs indicate mostly uniform electric field distribution and obtain a sufficient VBD (112 ~ 117 V), on the contrary, the conventional one degrades VBD.

II. DEVICE STRUCTURE AND DESIGN PARAMETERS

The device structures and significant design parameters for conventional, MSO and 2-step FP-MOSFETs are shown in Fig. 1(a)–(c). Those FP-MOSFETs apply the source field-plate structure, so-called the shielded-gate structure [7], to promise very low gate-drain charge (Qgd), instead of the gate field-plate structure in previous work [10]. The most part of the VBD is determined by poly-silicon field-plate length LFP, and the remaining part is shared by p-base/n-drift junction and trench bottom region. Field-plate oxide thickness tOX,b and tOX,t correspond to a position of top and bottom of the LFP, respectively. Oxide-slope K is defined by

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In this study, we propose an advanced device structure, named 2-step FP-MOSFET, which is formed by two steps of thick-oxide and two steps of poly-silicon field-plate to simplify the structure and fabrication process. By optimizing plural design parameters, we reveal the 2-step FP-MOSFET can achieve sufficient RESURF effect and an ultralow Ron·A. Moreover, we describe figure-of-merit (FOM) and power loss in comparison with conventional FP-MOSFET.

![Fig. 1. Cross-sectional structures and significant design parameters of three kinds of FP-MOSFETs in this study. (a) Conventional FP-MOSFET, (b) MSO FP-MOSFET [10], and (c) 2-step FP-MOSFET.](image)
III. OPTIMUM DESIGN BY TCAD SIMULATION

As investigation of optimum design, we simulated N_D dependence of the V_B of both MSO (K = 6.9 ~ 15.5) and 2-step (K = 6 ~ 26) FP-MOSFETs, as shown in Fig. 3. The conventional FP-MOSFETs (K = 40) are shown in each graph. The t_OX,b is fixed to 600 nm, which can obtain approximately 110 V. It is found that peak V_B (V_B,peak) is changed by the N_D and the K. The tendency is different in three kinds of FP-MOSFETs.

By redrawing the results in Fig. 3 into Fig. 4, it is found that the V_B,peak over 110 V can obtain at K = 10.2 in the MSO FP-MOSFETs and at wide range of K = 6.9 ~ 26 in the 2-step FP-MOSFETs (Fig. 4(a)). This is because there is existence of the point of inflection in the electric field distribution of the 2-step FP-MOSFET (Fig. 2(d)), therefore the V_B increases compared with the MSO FP-MOSFET even if the N_D is high. In addition, when “N_D at V_B,peak” is around 3.5E16 ~ 3.75E16/cm^3, minimum R_ONA can achieve at K = 8 ~ 9.7 in the 2-step FP-MOSFET (Fig. 4(b), “R_ONA at V_B,peak”). This N_D is 1.5 times higher and the R_ONA is 21% lower than those of the conventional FP-MOSFET.

![Fig. 2. Simulated 2-D potential contours for (a) conventional, (b) MSO and (c) 2-step FP-MOSFETs. (d) 1-D vertical electric field distributions along trench sidewall. (N_O = 3.0E16/cm^3).](image)

![Fig. 3. Simulated N_D dependences of V_B for (a) MSO FP-MOSFETs (K = 6.9 ~ 15.5) and (b) 2-step FP-MOSFETs (K = 6 ~ 26). Conventional FP-MOSFETs (K = 40) are shown in each graph.](image)

![Fig. 4. Simulated oxide-slope K dependences of (a) peak breakdown voltage V_B,peak and (b) “N_D at V_B,peak” and “R_ONA at V_B,peak” for conventional, MSO and 2-step FP MOSFETs (t_OX,b = 600 nm).](image)

![Fig. 5. Simulated W_Mesa dependences of V_B,peak and “N_D at V_B,peak” for 2-step FP-MOSFETs. (t_OX,b = 600 nm, K = 9.2) (image)

![Fig. 6. Simulated N_D and W_Cell dependences of R_ONA for 2-step (K=9.2) FP-MOSFETs. “N_D at V_B,peak” for conventional and 2-step FP-MOSFETs are shown in x-axis.](image)

![Fig. 7. Simulated 3-D potential contours (black lines) and impact-ionization generation rate (color). (a) Without and (b) with termination trench.](image)
IV. FABRICATION PROCESS

Representative process steps for the 2-step FP-MOSFET are shown in Fig. 8. (a) The trench of around 5.5-μm depth is formed by reactive ion etching (RIE), and followed by first thick oxidation. (b) By using sacrificial layer inside the trench, the thick oxide is etched down to approximately half-depth of the trench, and followed by second thick oxidation. (c) Poly-silicon field-plate is formed by chemical vapor deposition (CVD) and RIE. (d) First interlayer oxide is filled in the trench by CVD and etched back to appropriate depth. (e) Gate oxidation and gate poly-silicon CVD are performed continuously. (f) The gate poly-silicon is etched. After that, following process steps such as p-base, n'-source, p'-body, second interlayer oxide, contact, surface metallization, wafer thinning and back-side metallization are performed.

TEM (Transmission Electron Microscope) photograph of a unit cell structure of fabricated 2-step FP-MOSFET is shown in Fig. 9. To relax a strong stress inside the trench during the gate poly-silicon forming, U-shaped gate structure is applied.

V. CHARACTERIZATION OF DEVELOPED FP-MOSFET

A. Breakdown Voltage and On-resistance

Deviation of the $V_B$ in three case of the trench depth that are deep (5.9 μm), medium (5.5 μm) and shallow (5.1 μm), is shown in Fig. 10. In both $N_D$ variation of +/-10% (Fig. 10(a)) and $t_{OX,b}$ variation of +/-10% (Fig. 10(b)), it was confirmed that the process controllability was very good. Average of $V_B$ at drain current $I_D = 10$ mA was 109.9 V and the standard deviation was 0.50 V, under the center design and the process condition.

Subsequently, $R_{ON}$ packaged in SOP-8 was measured, under the condition of gate voltage $V_{GS} = 10$ V and $I_D = 30$ A. The $R_{ON,A}$ obtained by deduction of the package resistance indicated average value of 27.7 mΩ mm² and good deviation of 0.46 mΩ mm², as shown in Fig. 11. This $R_{ON,A}$ of the 2-step FP-MOSFET is ultralow in ever reported 100-V class device and improved by 16.6% compared with that of the conventional FP-MOSFET. Moreover, as shown in Fig. 12, temperature coefficient of $R_{ON,A}$ (from 25 to 150 degrees C) was 1.83 and it was superior to 2.15 of the conventional FP-MOSFET. This is because the 2-step FP-MOSFET has lower drift resistance compared with the conventional FP-MOSFET.

B. Figure-of-Merit

When the 2-step FP-MOSFET is applied in high efficiency switching circuit, gate charge properties, i.e., gate-source charge ($Q_{gs}$), gate-drain charge ($Q_{gd}$), total gate charge ($Q_{t}$) and output charge ($Q_{out}$), are very important. Moreover, as an indicator of the switching property, $Q_{sw}$ is defined by sum of the gate charge measurements. Fig. 13 compares figure-of-merit ($FOM$) of the conventional and the 2-step FP-MOSFET, under the conditions of $V_{DS} = 50$ V and $I_D = 35$ A as the gate charge measurement.
It was confirmed that $R_{ON}Q_{g}$ and $R_{ON}Q_{oss}$ were reduced by 27.1% and 4.7%, respectively, compared with those of the conventional device. The effect of the $Q_{g}$ reduction includes modification of the gate-source insulating film structure in the fabricated device. On the other hand, $R_{ON}Q_{oss}$ was increased.

Thus, improvement of the tradeoff between $R_{ON}Q_{g}$ and $Q_{oss}$ is further challenge to realize ultimate power MOSFET.

VI. CONCLUSIONS

We proposed the advanced trench MOSFET, which has two steps of field-plate. By designing plural parameters, the 2-step FP-MOSFET achieved optimum RESURF effect and 1.5 times higher $N_{D}$ compared with the conventional one. In the fabricated device, we confirmed superior tradeoff, $V_{th}$ of 109.9 V and $R_{ON}A$ of 27.7 mΩ·mm². The measurement results also showed small deviation and good process controllability. Moreover, $R_{ON}Q_{g}$ and $R_{ON}Q_{oss}$ were reduced by 27.1% and 4.7%. The power loss was estimated to improve by 12.7% in the assumed half-bridge as low-side operation. The developed 2-step FP-MOSFET has advantage, especially in using as high current switching, due to the ultralow $R_{ON}A$.

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