TLP5214A Smart Gate Driver Coupler
Inverter applications

Design Guide

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION
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1. Introduction

Operational stability and reliability are key characteristics of FA devices such as AC servos and general-purpose inverters, as well as inverters used in power conditioners for solar and wind power systems.

Overcurrent and noise in inverter circuits may cause a system malfunction with the potential for equipment damage. The typical ways to protect the IGBT and power MOSFET are: (a) current monitoring with a current transformer (CT); (b) current monitoring with a current sensing resistor; and (c) IGBT saturation voltage monitoring. While each of these has its advantages and disadvantages, approach (c) is the lowest cost solution and has the fastest operating speed and lowest power loss.

The TLP5214A has a built-in IGBT non-saturation ($V_{CE(SAT)}$) detector suitable for IGBT saturation monitoring as per approach (c), active mirror clamping and fault signal feedback. These functions provide superior performance and stability (compared to existing products) particularly with respect to instantaneous pulse noise during switching and non-saturation. The TLP5214A also helps to minimize design effort in peripheral circuit design, reduction outside components, and reduce PCB area. Thus the device suits for a driver coupler for middle power IGBT and power MOSFET direct drive devices. In addition the device guarantees minimum isolation voltage of 5,000Vrms, so it is equally suitable for many types of industrial machinery and equipment.

This Design Guide is based on a typical application involving an inverter circuit featuring the TLP5214A. TLP5214A product information including performance characteristics is provided on the datasheet and in the application note.

For detail of the TLP5214A → Click Here

1.1. Target applications

- IGBT/power MOSFET gate drive for FA devices, general-purpose inverters and controllers for AC motors and brushless DC motors

Typical inverter application
Note: Optically coupled isolation amplifier TLP7820 is used for motor phase current detection

For detail of the TLP7820 → [Click Here]

2. Application circuit examples and bill of materials

2.1. Inverter circuits

Figures 2.1 and 2.2 show examples of inverter circuits for the TLP5214A. The Design Guide (this document) gives two circuit designs, one is with mirror clamping and no negative supply, and the other is with negative supply but no mirror clamping. Table 2.1 shows the two designs.

<table>
<thead>
<tr>
<th>Diagram</th>
<th>Negative power supply</th>
<th>Mirror clamping</th>
<th>$V_{CH}$</th>
<th>$-V_{EH}$</th>
<th>$V_{DH}$</th>
<th>$V_{CL}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>RD021-SCHEMATIC1-01</td>
<td>No</td>
<td>Yes</td>
<td>17V</td>
<td>-</td>
<td>5V</td>
<td>5V</td>
</tr>
<tr>
<td>RD021-SCHEMATIC2-01</td>
<td>Yes</td>
<td>No</td>
<td>17V</td>
<td>10V</td>
<td>5V</td>
<td>5V</td>
</tr>
</tbody>
</table>

Table 2.2 shows the relevant output specifications.

<table>
<thead>
<tr>
<th></th>
<th>Supplty voltage ($V_P$)</th>
<th>Output drive frequency</th>
<th>Output current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300</td>
<td>10</td>
<td>±10 A</td>
</tr>
</tbody>
</table>

Due to affection between output drive frequency and the length of the cable, adjust and check the frequency with final product.
(a) Block diagram for inverter circuit 1

(b) U-Phase diagram for inverter circuit 1
(c) V-phase diagram for inverter circuit 1

(d) W-phase diagram for inverter circuit 1
Figure 2.1 Inverter circuit 1 using TLP5214A (RD021-SCEMATIC1-01)

(a) Block diagram for inverter circuit 2

(e) MCU elements in inverter circuit 1
(b) U-phase diagram for inverter circuit 2

(c) V-phase diagram for inverter circuit 2
(d) W-phase diagram for inverter circuit 2

(e) MCU elements in inverter circuit 2

Figure 2.2 Inverter circuit 2 using TLP5214A (RD021-SCHEMATIC2-01)
2.2. Bill of materials

Tables 2.3 and 2.4 are the bill of materials of the TLP5214A inverter circuits shown in Figures 2.1 and 2.2.

**Table 2.3  Bill of material for TLP5214A inverter circuit 1 (RD021-SCHEMATIC1-01)**

<table>
<thead>
<tr>
<th>No.</th>
<th>Label</th>
<th>Qty</th>
<th>Value</th>
<th>Product code</th>
<th>Manufacturer</th>
<th>Description</th>
<th>Package name</th>
<th>Standard dimensions in mm (inches)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IC1,IC2,IC7,IC8, IC13,IC14</td>
<td>6</td>
<td>-</td>
<td>TC7SZ14F</td>
<td>TOSHIBA</td>
<td>Buffer</td>
<td>SMV</td>
<td>2.9×2.8</td>
</tr>
<tr>
<td>2</td>
<td>IC3,IC9,IC15</td>
<td>3</td>
<td>-</td>
<td>OPA237</td>
<td>Texas Instruments</td>
<td>Op Amp</td>
<td>8SOIC</td>
<td>6x4.9</td>
</tr>
<tr>
<td>3</td>
<td>IC4,IC5,IC10, IC11,IC16,IC17</td>
<td>6</td>
<td>-</td>
<td>TLP5214A</td>
<td>TOSHIBA</td>
<td>Photocoupler</td>
<td>SO16L</td>
<td>10.3×10.0</td>
</tr>
<tr>
<td>4</td>
<td>IC6,IC12,IC18</td>
<td>3</td>
<td>-</td>
<td>TLP7820</td>
<td>TOSHIBA</td>
<td>Isolation Amplifier</td>
<td>SO8L</td>
<td>11x5.8</td>
</tr>
<tr>
<td>5</td>
<td>IC19</td>
<td>1</td>
<td>-</td>
<td>MCU</td>
<td>-</td>
<td>MCU</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>Q1,Q2,Q3,Q4, Q5,Q6</td>
<td>6</td>
<td>-</td>
<td>GT30J341</td>
<td>TOSHIBA</td>
<td>IGBT</td>
<td>TO-3P(N)</td>
<td>20×15.5</td>
</tr>
<tr>
<td>7</td>
<td>D1,D6,D7,D8, D13,D14,D15, D20,D21</td>
<td>9</td>
<td>-</td>
<td>CMF05</td>
<td>TOSHIBA</td>
<td>Diode</td>
<td>M-FLAT</td>
<td>2.4×4.7</td>
</tr>
<tr>
<td>8</td>
<td>D2,D3,D9,D10, D16,D17</td>
<td>6</td>
<td>-</td>
<td>CRZ10</td>
<td>TOSHIBA</td>
<td>Zener Diode</td>
<td>S-FLAT</td>
<td>1.6×3.5</td>
</tr>
<tr>
<td>9</td>
<td>D4,D5,D11,D12, D18,D19</td>
<td>6</td>
<td>-</td>
<td>CUS05F30</td>
<td>TOSHIBA</td>
<td>Diode</td>
<td>USC</td>
<td>2.5×1.25</td>
</tr>
<tr>
<td>10</td>
<td>R1,R2,R20,R23, R24,R42,R45, R46,R64</td>
<td>9</td>
<td>10kΩ</td>
<td>100 mW ±5%</td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>R3,R8,R9,R10, R25,R30,R31, R32,R47,R52, R53,R54</td>
<td>12</td>
<td>10kΩ</td>
<td>100 mW ±0.5%</td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>R4,R5,R6,R7, R26,R27,R28, R29,R48,R49, R50,R51</td>
<td>12</td>
<td>160Ω</td>
<td>100 mW ±5%</td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>R11,R12,R33, R34,R55,R56</td>
<td>6</td>
<td>1kΩ</td>
<td>100 mW ±5%</td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>R13,R16,R17, R35,R38,R39, R57,R60,R61</td>
<td>9</td>
<td>100Ω</td>
<td>250 mW ±5%</td>
<td>2012</td>
<td>2.0 x 1.2 (0805)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>R14,R15,R36, R37,R58,R59</td>
<td>6</td>
<td>10Ω</td>
<td>100 mW ±5%</td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>R18,R19,R40, R41,R62,R63</td>
<td>6</td>
<td>1kΩ</td>
<td>100 mW ±1%</td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>R21,R43,R65</td>
<td>3</td>
<td>10kΩ</td>
<td>100 mW ±1%</td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Table 2.4  Bill of material for TLP5214A inverter circuit 2 (RD021-SCHEMATIC2-01)

<table>
<thead>
<tr>
<th>No.</th>
<th>Label</th>
<th>Qty</th>
<th>Value</th>
<th>Product code</th>
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<td>-</td>
<td>TLP5214A</td>
<td>TOSHIBA</td>
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<td>10.3×10.0</td>
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<td>4</td>
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<td>5</td>
<td>IC19</td>
<td>1</td>
<td>-</td>
<td>MCU</td>
<td>-</td>
<td>MCU</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>Q1,Q2,Q3,Q4, Q5,Q6</td>
<td>6</td>
<td>-</td>
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<td>-</td>
<td>CRZ10</td>
<td>TOSHIBA</td>
<td>Zener Diode</td>
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<tr>
<td>-----</td>
<td>-------</td>
<td>-----</td>
<td>-------</td>
<td>--------------</td>
<td>--------------</td>
<td>-------------</td>
<td>-------------</td>
<td>-----------------------------------</td>
</tr>
<tr>
<td>9</td>
<td>D4,D5,D11, D12,D18,D19</td>
<td>6</td>
<td>-</td>
<td>CUS05F30</td>
<td>TOSHIBA</td>
<td>Diode</td>
<td>USC</td>
<td>2.5 x 1.25</td>
</tr>
<tr>
<td>10</td>
<td>R1,R2,R20,R23, R24,R42,R45, R46,R64</td>
<td>9</td>
<td>10kΩ</td>
<td></td>
<td></td>
<td></td>
<td>100 mW ±5%</td>
<td>1608</td>
</tr>
<tr>
<td></td>
<td>R3,R8,R9,R10, R25,R30,R31, R32,R47,R52, R53,R54</td>
<td>12</td>
<td>10kΩ</td>
<td></td>
<td></td>
<td></td>
<td>100 mW ±0.5%</td>
<td>1608</td>
</tr>
<tr>
<td></td>
<td>R4,R5,R6,R7, R26,R27,R28, R29,R48,R49, R50,R51</td>
<td>12</td>
<td>160Ω</td>
<td></td>
<td></td>
<td></td>
<td>100 mW ±5%</td>
<td>1608</td>
</tr>
<tr>
<td>11</td>
<td>R11,R12,R33, R34,R55,R56</td>
<td>6</td>
<td>1kΩ</td>
<td></td>
<td></td>
<td></td>
<td>100 mW ±0.5%</td>
<td>1608</td>
</tr>
<tr>
<td>12</td>
<td>R13,R16,R17, R35,R38,R39, R57,R60,R61</td>
<td>9</td>
<td>100Ω</td>
<td></td>
<td></td>
<td></td>
<td>250 mW ±5%</td>
<td>2012</td>
</tr>
<tr>
<td>13</td>
<td>R14,R15,R36, R37,R58,R59</td>
<td>6</td>
<td>10Ω</td>
<td></td>
<td></td>
<td></td>
<td>100 mW ±5%</td>
<td>1608</td>
</tr>
<tr>
<td>14</td>
<td>R18,R19,R40, R41,R62,R63</td>
<td>6</td>
<td>1kΩ</td>
<td></td>
<td></td>
<td></td>
<td>100 mW ±1%</td>
<td>1608</td>
</tr>
<tr>
<td>15</td>
<td>R21,R43,R65</td>
<td>3</td>
<td>10kΩ</td>
<td></td>
<td></td>
<td></td>
<td>100 mW ±1%</td>
<td>1608</td>
</tr>
<tr>
<td>16</td>
<td>R22,R44,R66</td>
<td>3</td>
<td>20mΩ</td>
<td>WSHP2818R0200FEB</td>
<td>Vishay</td>
<td>10 W ± 1%</td>
<td>-</td>
<td>7.1 x 4.6</td>
</tr>
<tr>
<td>17</td>
<td>C1,C2,C3,C6, C7,C10,C18, C22,C23,C24, C27,C28,C31, C39,C43,C44, C45,C48,C49, C52,C60</td>
<td>21</td>
<td>100nF</td>
<td>Ceramic, 50 V, ±10%</td>
<td></td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>C4,C21,C25, C42,C46,C63</td>
<td>6</td>
<td>1nF</td>
<td>Ceramic, 50 V, ±10%</td>
<td></td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>C5,C8,C26,C29, C47,C50</td>
<td>6</td>
<td>68pF</td>
<td>Ceramic, 50 V, ±10%</td>
<td></td>
<td>1005</td>
<td>1.0 x 0.5 (0402)</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>C9,C30,C51</td>
<td>3</td>
<td>10μF</td>
<td>Ceramic, 25 V, ±10%</td>
<td></td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>C11,C12,C14, C15,C32,C33, C35,C36,C53, C54,C56,C57</td>
<td>12</td>
<td>1μF</td>
<td>Ceramic, 50 V, ±10%</td>
<td></td>
<td>2012</td>
<td>2.0 x 1.2 (0805)</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>C13,C34,C55</td>
<td>3</td>
<td>10μF</td>
<td>Ceramic, 6.3 V, ±10%</td>
<td></td>
<td>2012</td>
<td>2.0 x 1.2 (0805)</td>
<td></td>
</tr>
<tr>
<td>No.</td>
<td>Label</td>
<td>Qty</td>
<td>Value</td>
<td>Product code</td>
<td>Manufacturer</td>
<td>Description</td>
<td>Package name</td>
<td>Standard dimensions in mm (inches)</td>
</tr>
<tr>
<td>-----</td>
<td>------------------------</td>
<td>-----</td>
<td>---------</td>
<td>--------------</td>
<td>--------------</td>
<td>----------------------------------</td>
<td>--------------</td>
<td>-----------------------------------</td>
</tr>
<tr>
<td>25</td>
<td>C19,C20,C40, C41,C61,C62</td>
<td>6</td>
<td>120pF</td>
<td>Ceramic, 50 V, ±10%</td>
<td>1608</td>
<td>1.6 x 0.8 (0603)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For the detail of the TLP5214A → [Click Here]
For the detail of the TLP7820 → [Click Here]
For the detail of the GT30J341 → [Click Here]
For the detail of the CMF05 → [Click Here]
For the detail of the CRZ10 → [Click Here]
For the detail of the CUS05F30 → [Click Here]
For the detail of the TC7SZ14F → [Click Here]
3. Inverter circuit design guide

This section explains the key design consideration for an inverter circuit using the TLP5214A.

3.1. Blanking time

Blanking time ($t_{\text{BLANK}}$) is the time until overcurrent protection is enabled. The TLP5214A outputs a gate drive current from $V_{\text{OUT}}$ in response to input signal, and DESAT is initiated at the same time. For products where the power device takes a long time to turn on, DESAT detects the voltage level and enters shutdown mode while the collector-emitter voltage ($V_{\text{CE}}$) is still decreasing. The $t_{\text{BLANK}}$ value can be adjusted the time taken for voltage detection to occur, however it is important not to exceed the IGBT short-circuit withstand capability (IGBT time until failure in the presence of overcurrent).

$t_{\text{BLANK}}$ is related to blanking capacitor ($C_{\text{BLANK}}$), DESAT threshold voltage ($V_{\text{DESAT}}$), blanking capacitor charging current ($I_{\text{CHG}}$) and DESAT leading edge blanking time ($t_{\text{DESAT(LEB)}}$) by the following equation:

$$t_{\text{BLANK}} = \frac{C_{\text{BLANK}} \times V_{\text{DESAT}}}{I_{\text{CHG}}} + t_{\text{DESAT(LEB)}}$$

Where $V_{\text{DESAT}}$ and $I_{\text{CHG}}$ are constants (standard values are 6.5 V and 240 µA respectively), and $t_{\text{DESAT(LEB)}}$ is 1.1µs (Typ.). Regarding Figure 3.1, it has GT30J341 (Discrete IGBT) which has 5µs ($t_{\text{SC}}$) value, $t_{\text{BLANK}}$ must be set not exceeding this value. If we use $C_{\text{BLANK}} = 120$ pF, then:

$$t_{\text{BLANK}} = \frac{120 \times 10^{-12} (F) \times 6.5 (V)}{240 \times 10^{-6} (A)} + 1.1 \times 10^{-6} (s) = 4.35 \mu s < 5\mu s$$

A higher $C_{\text{BLANK}}$ value would change the slope of the DESAT terminal voltage, meaning a longer time for overcurrent protection to be enabled shown in Figure 3.2. The $C_{\text{BLANK}}$ value should be set to a $t_{\text{BLANK}}$ time that is within the short-circuit withstand capability period for the power device without causing overcurrent detection errors. Figure 3.2 shows the relation between $t_{\text{BLANK}}$ and $C_{\text{BLANK}}$. Note that in actual circuits, $t_{\text{BLANK}}$ is also affected by not only $C_{\text{BLANK}}$ but also factors such as the parasitic capacitance of diodes on the DESAT line.
Figure 3.1  Blanking time $t_{\text{BLANK}}$

Figure 3.2  Blanking capacity $C_{\text{BLANK}}$ vs. blanking time $t_{\text{BLANK}}$
3.2. IGBT short-circuit threshold voltage

The DESAT terminals monitor the collector-emitter voltage $V_{CE}$ of the external IGBT during $I_F$ input. The DESAT protection circuit activates when the terminal voltage $V_{DESAT}$ exceeds 6.5 V (Typ.). The monitored $V_{CE}$ value is different from the actual IGBT $V_{CE}$ one due to monitoring through diode and resister. Figure 3.3 shows how to adjust the short-circuit threshold voltage when diodes are used.

If $V_{th(IGBT)}$ is defined the short-circuit threshold voltage based on the IGBT voltage, we can use multiple diodes connection to the DESAT terminals as shown in Figure 3.3, considering the IGBT safe operating range, the voltage drop for $V_F$ during multiple elements will force $V_{th(IGBT)}$ down to a new value (New $V_{th(IGBT)}$) as per the equation below. It is important to choose diodes with high tolerant and fast reverse recovery time.

$$NEW\ V_{th(IGBT)} = V_{DESAT} - (n \times V_F + R_{DESAT} \times I_{CHG})$$

where $n$ is the number of diodes

For circuits shown in Figure 2.1 and Figure 2.2, GT30J341 IGBT ($V_{GE(OFF)} = 5.5$ V), a single CMF05 diode ($V_F = 2.7$ V @ 50 µA) and 100 Ω $R_{DESAT}$ are used. Therefore we have:

$$New\ V_{th(IGBT)} = 6.5 - (1 \times 2.7\ (V)) + 100\ (\Omega) \times 50\ (\mu A) \approx 3.8\ V$$

![Figure 3.3](image_url)
3.3. Control signal waveform shaping

In case of the control board and motor control board are separated, the longer distance to the TLP5214A may cause generating inductance and other impacts during wiring and the input signal slope is potentially changed.

In Figure 3.4, it has an additional hysteresis buffer circuit before the TLP5214A input terminal to shape the input signal waveform.

![Control signal waveform shaping](image)

Figure 3.4   Control signal waveform shaping

3.4. Current control shunt resistor

In Figure 2.1 and Figure 2.2, they use the TLP7820 for motor control in a three shunt current detection configuration that measures three-phase current on the controller side. Details of the current detection circuit design are given in the TLP7820 document (RD013-RGUIDE-02).

For detail of reference guide for TLP7820 current detection circuit → [Click Here](#)

3.5. Thermal design

In order to supply electric charge to (or withdraw it from) the power device gate over a short period, the gate driver photocoupler has to generate (or absorb) large amounts of output current quickly during switching. With this reason, photocoupler switching loss and heat must also be considered. Switching loss is determined by many factors including the photocoupler drive frequency, drive voltage, gate capacity and gate resistance of power device. The loss of photo detection side accounts for the bulk of the photocoupler losses. Those losses generate heat, so most of the heat is at the photo detection side. Peripheral circuit design must take care of the maximum rated junction temperature for the light receiving chip and LED chip in the photocoupler.
The following definitions are used in this document.

- **P**\text{all}: total power loss in photocoupler
- **P**\text{O,all}: power loss in light receiving chip
- **P**\text{D}: power loss on LED side
- **I**\text{F}: LED forward current
- **V**\text{F}: LED forward voltage
- **P**\text{O,DC}: current consumption during DC operation
- **P**\text{O(bias: on)}: DC current consumption with LED on
- **P**\text{O(bias: off)}: DC current consumption with LED off
- **P**\text{O,SW}: power consumption during switching
- **duty**: photocoupler duty ratio
- **E**\text{SW}: electrostatic energy during switching
- **I**\text{CH}: H level supply current
- **I**\text{CL}: L level supply current
- **V**\text{CC}: positive supply voltage on output side
- **V**\text{EE}: negative supply voltage on output side (\(V_{EE} < 0\))
- **f**\text{SW}: switching frequency
- **R**\text{G}: gate resistance
- **R**\text{ON,H}: photocoupler output resistance (high)
- **R**\text{ON,L}: photocoupler output resistance (low)
- **C**\text{G}: gate capacity (\(Q_{G} = C_{G} \times V_{CC}\) equivalent)
- **I**\text{OP, WORST}: maximum value of peak output current
- **T**\text{J,LED}: LED chip junction temperature*
- **T**\text{J,Photo}: light receiving chip junction temperature*
- **R**\text{TH(j-a),LED}: thermal resistance of LED chip**
- **R**\text{TH(j-a),Photo}: thermal resistance of light receiving chip**

* TLP5214A maximum rated value = 125 °C
** Thermal resistance of TLP5214A on standard JEDEC substrate:
\[
R_{th(j-a),LED} : 0.165 \degree C/mW \quad R_{th(j-a),Photo} : 0.07 \degree C/mW
\]
Figure 3.5 shows the calculation model (which applies equally to TLP5214A).

![Figure 3.5](image)

**Figure 3.5  Calculating power loss in the light receiving chip**

The procedure for determining power loss in the photocoupler light receiving chip is given below. The power loss in the light receiving chip during switching operation is the sum of power consumption during DC operation and switching loss.

1. **Power loss in light receiving chip**
   
   \[ P_{o,all} = P_{o,DC} + P_{o,sw} \]

2. **Power consumption during DC operation**
   
   \[ P_{o,DC} = P_{o(bias:on)} + P_{o(bias:off)} \]
   
   \[ = \text{duty} \times I_{CC} \times (V_{cc} + |V_{EE}|) + (1 - \text{duty}) \times I_{CL} \times (V_{cc} + |V_{EE}|) \]

3. **Power consumption during switching**

   The amount of electrostatic energy \( E_{sw} \) stored and/or released in a switching operation \( C_g \) is defined by:

   \[ E_{sw} = \frac{C_g \times (V_{cc} + |V_{EE}|)^2}{2} \]

   Given that \( f_{sw} \) of the \( C_g \) electrostatic energy \( E_{sw} \) is consumed by \( R_g, R_{on,H} \) and \( R_{on,L} \) per second, the power consumption during switching \( P_{o,sw} \) is calculated as:

   \[ P_{o,sw} = E_{sw} \times \left[ \frac{R_{on,H}}{R_g + R_{on,H}} + \frac{R_{on,L}}{R_g + R_{on,L}} \right] \times f_{sw} \]
(4) The following equations can be used to calculate the peak output current and the maximum value of the estimated peak output current of the photocoupler output stage MOSFET on-resistance $I_{op,\text{worst}}$ (note that peak output current will generally be lower in practice, since a photocoupler output stage MOSFET on-resistance is also present).

$$I_{op,\text{worst}} = \frac{(V_{cc} + |V_{EE}|)}{R_g}$$

This value is used to determine the characteristics curve for the photocoupler output stage on-resistance.

$$R_{on,H} = \frac{[V_{OH} - V_{CC}] (@ I_{op,\text{worst}})}{I_{op,\text{worst}}}$$

Note: $[V_{OH} - V_{CC}] (@ I_{op,\text{worst}})$ is taken from the characteristics curve

$$R_{on,L} = \frac{V_{OL} (@ I_{op,\text{worst}})}{I_{op,\text{worst}}}$$

Note: $V_{OL} (@ I_{op,\text{worst}})$ is taken from the characteristics curve

We substitute the resistance value into the $P_{o,sw}$ equation to find the switching power consumption.

(5) LED power loss

LED power loss is given by the following equation:

$$P_D = \text{duty} \times I_F \times V_F$$

Calculation example

The following circuit conditions are used for calculation example.

$V_{CC} = 15 \, \text{V}, \, V_{EE} = 0 \, \text{V}, \, I_{CH} = 3.8 \, \text{mA}, \, I_{CL} = 3.8 \, \text{mA}$ (rated maximum for TLP5214A)

$C_g = 25 \, \text{nF}, \, R_g = 10 \, \Omega, \, \text{duty} = 0.5, \, f_{sw} = 10 \, \text{kHz}, \, T_a = 110^\circ \text{C}$

$I_F = 10 \, \text{mA}, \, V_F = 1.45 \, \text{V}$ (TLP5214A $I_F - V_F$ curve with $T_a = 110^\circ \text{C}, \, I_F = 10 \, \text{mA}$)

Light-receiving DC loss

$$P_{o,DC} = P_{o(bias:on)} + P_{o(bias:off)}$$

$$= \text{duty} \times I_{CH} \times (V_{cc} + |V_{EE}|) + (1 - \text{duty}) \times I_{CL} \times (V_{cc} + |V_{EE}|)$$

$$= 0.5 \times 3.8(\text{mA}) \times 15(\text{V}) + 0.5 \times 3.8(\text{mA}) \times 15(\text{V}) = 57 \, \text{mW}$$
Peak output current

\[ I_{\text{op,worst}} = \frac{(V_{cc} + |V_{EE}|)}{R_g} = \frac{15(V)}{10(\Omega)} = 1.5 \, A \]

Photocoupler output stage on-resistance

If we substitute 1.5 A into the \( V_{OH}-I_{op} \) characteristics curve for TLP5214A (Figure 3.6) we get \( [V_{OH}-V_{CC}](@ I_{op,worst}) = -1.2 \, V \) and \( V_{OL}(@ I_{op,worst}) = 1.0 \, V \), which gives us on-resistances values as follows:

\[ R_{on,H} = \frac{[V_{OH} - V_{CC}](@ I_{op,worst})}{I_{op,worst}} = \frac{-1.2(V)}{-1.5(A)} = 0.8 \, \Omega \]

\[ R_{on,L} = \frac{V_{OL}(@ I_{op,worst})}{I_{op,worst}} = \frac{1.0(V)}{1.5(A)} = 0.7 \, \Omega \]

**Figure 3.6** Estimating the photocoupler output stage MOSFET on-resistance from the \( V_{OH}-I_{op} \) curve

Switching loss

\[ P_{o,sw} = E_{sw} \times \left[ \frac{R_{on,H}}{(R_g + R_{on,H})} + \frac{R_{on,L}}{(R_g + R_{on,L})} \right] \times f_{sw} \]

\[ = \frac{C_g \times (V_{cc} + |V_{EE}|)^2}{2} \times \left[ \frac{R_{on,H}}{(R_g + R_{on,H})} + \frac{R_{on,L}}{(R_g + R_{on,L})} \right] \times f_{sw} \]

\[ = 25(nF) \times (15(V))^2 \times \left[ \frac{0.8(\Omega)}{(10(\Omega) + 0.8(\Omega))} + \frac{0.7(\Omega)}{(10(\Omega) + 0.7(\Omega))} \right] \times 10(kHz) \]

\[ = 3.9 \, mW \]
Loss in the light receiving chip is given by the following equation:

\[ P_{o,all} = P_{o,DC} + P_{o,sw} = 57\text{mW} + 3.9\text{mW} = 60.9\text{mW} \]

**LED power loss**

LED power loss is given by the following equation:

\[ P_D = \text{duty} \times I_F \times V_F = 0.5 \times 10\text{(mA)} \times 1.45\text{(V)} = 7.3\text{mW} \]

**Total photocoupler power consumption**

\[ P_{all} = P_D + P_{o,all} = 7.3\text{mW} + 60.9\text{mW} = 68.2\text{mW} \]

A simplified estimate of the junction temperatures in this example (\( T_{j,LED} \) and \( T_{j,Photo} \)), ignoring thermal interference between the LED and light-receiving chip, is shown below.

This gives us an idea of the usable range in terms of thermal considerations.

\[ T_{j,LED} = T_a + \Delta T_{j,LED} = 110\text{(°C)} + 0.165\text{(°C/mW)} \times 7.3\text{(mW)} = 111.2\text{°C} < 125\text{°C} \]

\[ T_{j,Photo} = T_a + \Delta T_{j,Photo} = 110\text{(°C)} + 0.07\text{(°C/mW)} \times 60.9\text{(mW)} = 114.3\text{°C} < 125\text{°C} \]

Thermal resistance is different from the material of the substrate, the land pattern and the layer structure. Also, the photocoupler output terminal capacitance includes the parasitic capacitance of the substrate. So the above calculation should be considered no more than a general guide.

**Note**

When the TLP5214A enters protection mode the FAULT output LED on the feedback side lights and the FAULT terminal output switches from high to low to indicate an IGBT error. If protection mode is continued, the FAULT output LED on the secondary side also lights and a current of approximately 10 mA starts flowing between the \( V_{CC2} \) and \( V_E \) terminals, increasing the power loss on the secondary side. When protection mode activate, the system must be shut down and reboot immediately (see Figures 3.7 and 3.8).

Ex) \( V_{CC2} = 30\text{V} \), FAULT mode engaged

If feedback LED current = 10 mA and the voltage at the light-receiving chip on the secondary side is 28 V (not including LED voltage drop), then power loss in the light-receiving chip is 28 V x 10 mA = 280 mW. If we take into account thermal resistance on the light-receiving chip side of the TLP5214A, the temperature increase is 0.07 x 280 = 19.6°C. This could be an issue in a hot operating environment.
Figure 3.7   Internal circuit diagram (operation path during fault)

Figure 3.8   TLP5214A timing chart (protection engaged)
4. Product overview

4.1. General

The TLP5214A is an advanced, highly integrated 4.0A output current IGBT gate drive photocoupler housed in a long creepage and clearance SO16L package.

- Peak output current: ±4.0 A (max.)
- Operating temperature range: -40 to +110°C
- Supply current: 3.8 mA (max.)
- Power supply voltage: 15 to 30 V
- Threshold input current: 6 mA (max.)
- Propagation delay (t_{PLH} / t_{PHL}): 150 ns (max.)
- DESAT leading edge blanking time: 1.1 µs (typ.)
- Common mode transient immunity: ±35 kV/µs (min.)
- Isolation voltage: 5,000 Vrms (min.)
- Safety standards
  - UL approved: UL1577, File No. E67349
  - c-UL approved: CSA (Component Acceptance Service) No. 5A, File No. E67349
  - Option (D4) VDE: DIN EN60747-5-5, EN60065 or EN60950-1, EN62368-1 *
  - CQC: GB4943.1 and GB8898 Japan Factory (Pending)
  - * When a EN60747-5-5 approved type is needed, please designate “Option(D4)”

4.2. Appearance and terminal configuration

General appearance and markings

![TLP5214A Appearance and Markings](image)

Figure 4.1   TLP5214A appearance and markings
### TLP5214A terminals

<table>
<thead>
<tr>
<th>Terminal No.</th>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
<th>Internal circuit configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VS</td>
<td>GND</td>
<td>GND on input side</td>
<td>Tr.(Open collector)</td>
</tr>
<tr>
<td>2</td>
<td>VCC1</td>
<td>IN</td>
<td>Positive supply on input side</td>
<td>Tr./Photo Di</td>
</tr>
<tr>
<td>3</td>
<td>FAULT</td>
<td>OUT</td>
<td>IGBT short (non-saturation) fault feedback; outputs L when IGBT non-saturation detected</td>
<td>Tr.(Open collector)</td>
</tr>
<tr>
<td>4</td>
<td>VS</td>
<td>GND</td>
<td>GND on input side</td>
<td>Tr.(Open collector)</td>
</tr>
<tr>
<td>5</td>
<td>CATHODE</td>
<td>GND</td>
<td>LED cathode on input side</td>
<td>LED</td>
</tr>
<tr>
<td>6</td>
<td>ANODE</td>
<td>IN</td>
<td>LED anode on input side</td>
<td>LED</td>
</tr>
<tr>
<td>7</td>
<td>ANODE</td>
<td>IN</td>
<td>LED anode on input side</td>
<td>LED</td>
</tr>
<tr>
<td>8</td>
<td>CATHODE</td>
<td>GND</td>
<td>LED cathode on input side</td>
<td>LED</td>
</tr>
<tr>
<td>9</td>
<td>VEE</td>
<td>IN</td>
<td>Negative supply on output side; connect to VS if using positive supply (VCC2) only</td>
<td>DMOS/CMOS</td>
</tr>
<tr>
<td>10</td>
<td>VCLAMP</td>
<td>IN</td>
<td>Active mirror clamp terminal; connect to IGBT gate (or to VEE if unused)</td>
<td>DMOS</td>
</tr>
<tr>
<td>11</td>
<td>VOUT</td>
<td>OUT</td>
<td>Output for IGBT turn-on turn-off</td>
<td>DMOS</td>
</tr>
<tr>
<td>12</td>
<td>VEE</td>
<td>IN</td>
<td>Negative supply on output side; connect to VS if using positive supply (VCC2) only</td>
<td>DMOS/CMOS</td>
</tr>
<tr>
<td>13</td>
<td>VCC2</td>
<td>IN</td>
<td>Positive supply on output side</td>
<td>DMOS/CMOS</td>
</tr>
<tr>
<td>14</td>
<td>DESAT</td>
<td>IN</td>
<td>IGBT short (non-saturation) detection terminal; monitors VCC3 through high-voltage FRD</td>
<td>CMOS</td>
</tr>
<tr>
<td>15</td>
<td>LED</td>
<td>IN</td>
<td>Feedback LED test terminal; leave OPEN for user use</td>
<td>LED/CMOS</td>
</tr>
<tr>
<td>16</td>
<td>VS</td>
<td>GND</td>
<td>Supply common on output side</td>
<td>-</td>
</tr>
</tbody>
</table>

**Figure 4.2** TLP5214A terminals
4.3. Internal circuit block diagram

![Internal circuit block diagram](image)

Note: 1 µF bypass capacitor required between pins 9 (VEE) and 13 (VCC2) and between pins 13 and 16 (VE).

**Figure 4.3** TLP5214A internal circuit block diagram

4.4. Truth table

<table>
<thead>
<tr>
<th>IF</th>
<th>UVLO (VCC2-VE)</th>
<th>DESAT (14 pin DESAT terminal input)</th>
<th>FAULT (3 pin FAULT terminal output)</th>
<th>VO</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>Not Active (&gt;VUVLO^+)</td>
<td>Not Active</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>ON</td>
<td>Not Active (&gt;VUVLO^+)</td>
<td>Low (&lt;VDESATH)</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>ON</td>
<td>Not Active (&gt;VUVLO^+)</td>
<td>High (&gt;VDESATH)</td>
<td>Low (FAULT)</td>
<td>Low</td>
</tr>
<tr>
<td>ON</td>
<td>Active (&lt;VUVLO^-)</td>
<td>Not Active</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>OFF</td>
<td>Active (&lt;VUVLO^-)</td>
<td>Not Active</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>
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