

ESD Protection Diodes Silicon Epitaxial Planar

DF2B6M4BSL

1. General

The DF2B6M4BSL is a TVS diode (ESD protection diode) that protects semiconductor components from static electricity and noise in electronic device antennas and high-speed interface ports.

This product has ultra-low capacitance characteristics, it is possible to suppress the deterioration of signal quality that is a concern in antennas and high-speed signal lines. And the DF2B6M4BSL provides low V_{peak} voltage when ESD is applied and superior protective performance.

DF2B6M4BSL is housed in an ultra-compact package (0.62 mm \times 0.32 mm) to meet applications that require a small footprint.

2. Applications

Mobile Equipment

IoT Equipment

Wearable Equipment

- · Wi-Fi
- · Anntena
- · DisplayPort Interface
- · USB/HDMI
- · PCI Express

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

3. Features

- (1) Suitable for use with a 5.0 V signal line. $(V_{RWM} \le 5.5 \text{ V})$
- (2) Low harmonic distortion

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f = 2.4 \text{ GHz}, 20 \text{ dBm input}
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2nd Harmonics: -65.5 dBm (Reference)

3rd Harmonics: -54.4 dBm (Reference)

f = 5.0 GHz, 20 dBm input

2nd Harmonics: -64.7 dBm (Reference)

3rd Harmonics: -55.5 dBm (Reference)

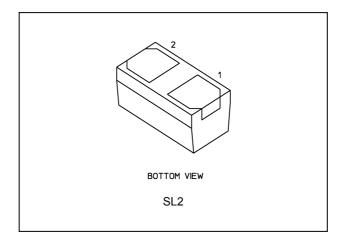
- (3) Low V_{peak} : $V_{\text{CL-max-peak}} = 215 \text{ V}$ (Reference) (@IEC61000-4-2(Contact), +8 kV)
- (4) Compact package is suitable for use in high density board layouts such as in mobile devices.

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(0.62 mm × 0.32 mm size (Nickname: SL2))



4. Packaging



5. Example of Circuit Diagram

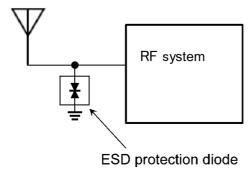


Fig. 5.1 High frequency antenna circuit

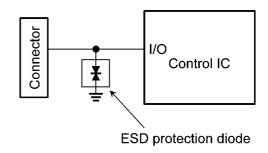


Fig. 5.2 High-speed signal circuit

6. Quick Reference Data

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V_{RWM}	(Note 1)	_	_	_	5.5	V
Total capacitance	Ct		V _R = 0 V, f = 1 MHz	_	0.12	0.15	pF
Dynamic resistance	R _{DYN}	(Note 2)	_		1.05	_	Ω
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	V _{ESD}	(Note 3)	_	8		ı	kV

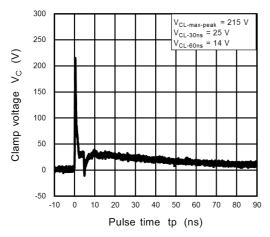
Note 1: Recommended operating condition.

Note 2: TLP parameters: $Z0 = 50 \Omega$, tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 8 \text{ A}$ and $I_{PP2} = 16 \text{ A}$.

Note 3: Criterion: No damage to devices.



6.1. ESD Clamp Waveform (Note)



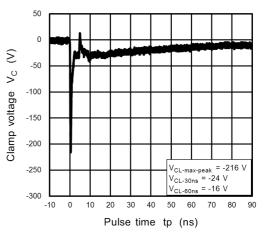


Fig. 6.1.1 +8 kV

Fig. 6.1.2 -8 kV

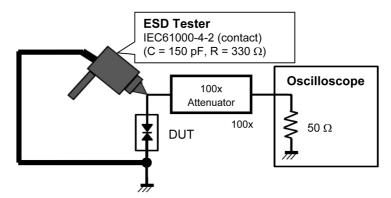
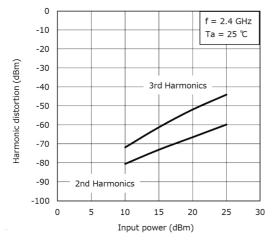


Fig. 6.1.3 IEC61000-4-2 (Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



6.2. Harmonic distortion characteristics (Note)



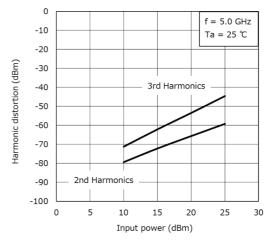


Fig. 6.2.1 f = 2.4 GHz

Fig. 6.2.2 f = 5.0 GHz

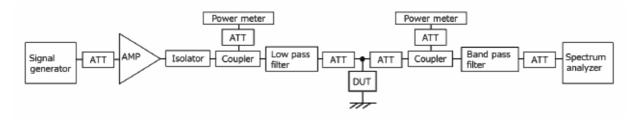
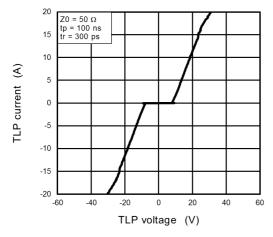


Fig. 6.2.3 Schematic diagram of harmonic distortion evaluation system

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



6.3. TLP Characteristics (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

6.4. Clamp Voltage - Peak Pulse Current (V_C - I_{PP}) (Note)

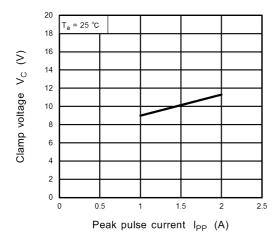


Fig. 6.4.1 V_C - I_{PP}

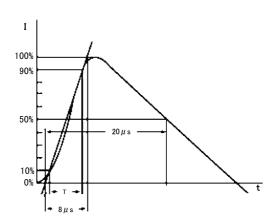


Fig. 6.4.2 Based on IEC61000-4-5 8/20 μ s pulse.

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Rev.1.0



7. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2) (Contact)	V _{ESD}	(Note 1)	±8	kV
Electrostatic discharge voltage (IEC61000-4-2) (Air)			±8	
Peak pulse power (tp = 8/20 μs)	P _{PK}		30	W
Peak pulse current (tp = 8/20 μs)	I _{PP}	(Note 2)	2.0	Α
Junction temperature	Tj		150	°C
Storage temperature	T _{stg}		-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2. Note 2: According to IEC61000-4-5.

8. Electrical Characteristics (Unless otherwise specified, Ta = 25 °C)

 V_{RWM} : Working peak reverse voltage

V_T: Trigger voltage

V_H: Holding voltage

(Reverse breakdown voltage)

It1: Test current (Reverse breakdown current)

I_R: Reverse current V_C: Clamp voltage

I_{PP}: Peak pulse current

R_{DYN}: Dynamic resistance

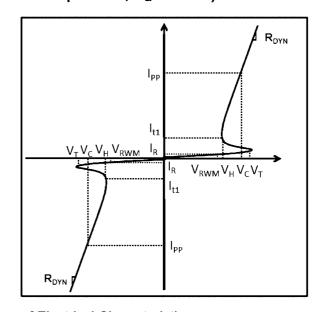


Fig. 8.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V_{RWM}	(Note 1)	_	_	_	5.5	V
Total capacitance	Ct		V _R = 0 V, f = 1 MHz	_	0.12	0.15	pF
Dynamic resistance	R_{DYN}	(Note 2)	_	_	1.05	_	Ω
Trigger voltage	V_{T}		_	5.6	_	_	V
Holding voltage	V _H		I _{t1} = 1mA	5.6	6.2	8.0	V
Reverse current	I _R		V _{RWM} = 5.5 V	_	_	0.1	μА
Clamp voltage	V _C	(Note 3)	I _{PP} = 1 A	_	9	_	V
			I _{PP} = 2 A	_	11.3	15	
		(Note 2)	I _{TLP} = 8 A	_	16.5	_	V
			I _{TLP} = 16 A	_	25	_	

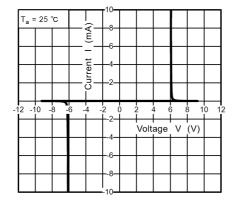
Note 1: Recommended operating condition.

Note 2: TLP parameters: $Z0 = 50 \Omega$, tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 8 A$ and $I_{PP2} = 16 A$.

Note 3: Based on IEC61000-4-5 8/20 μ s pulse.



9. Characteristics Curves (Note)





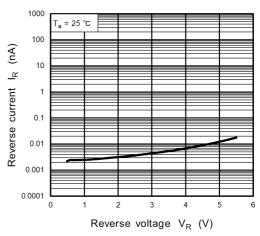


Fig. 9.2 I_R - V_R

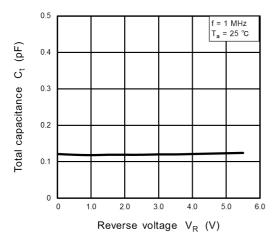


Fig. 9.3 $C_t - V_R$

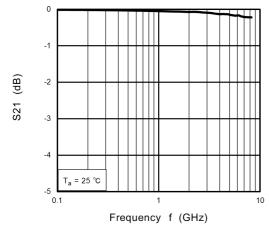
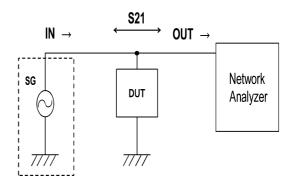


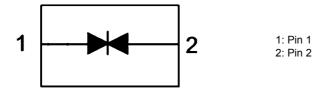
Fig. 9.4 S21 - f



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

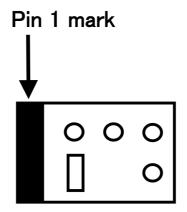


10. Internal Circuit (Note)

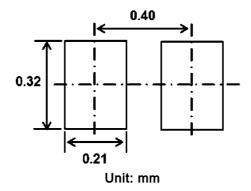


Note: Connect Pin 2 to GND when using Pin 1 for I/O. Connect Pin 1 to GND when using Pin 2 for I/O.

11. Marking (Top view)



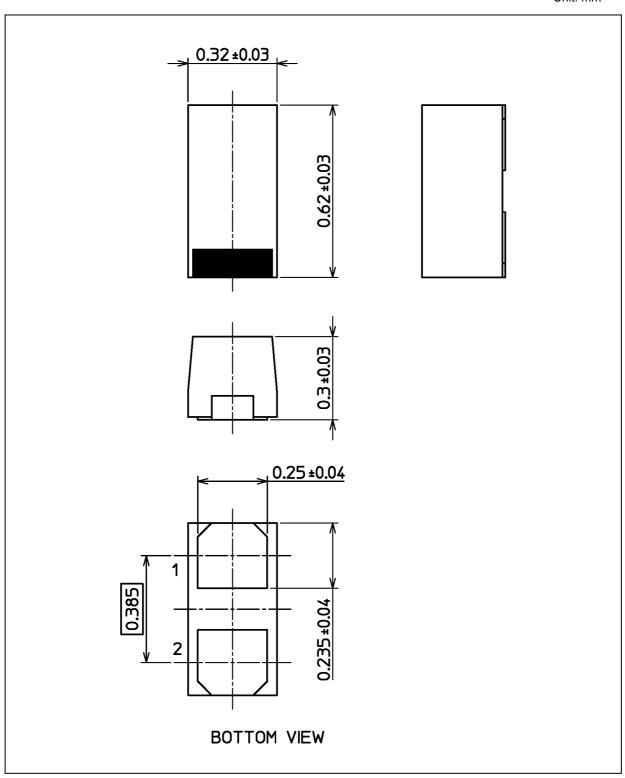
12. Land Pattern Dimensions (for reference only)





Package Dimensions

Unit: mm



Weight: 0.2 mg (typ.)

	Package Name(s)	
Nickname: SL2		



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