

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K106TU

High-Speed Switching Applications

- 4 V drive
- Low ON-resistance: $R_{on} = 530 \text{ m}\Omega$ (max) (@ $V_{GS} = 4 \text{ V}$)
 $R_{on} = 310 \text{ m}\Omega$ (max) (@ $V_{GS} = 10 \text{ V}$)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current	DC	I_D	1.2
	Pulse	I_{DP}	2.4
Drain power dissipation	P_D (Note 1)	800	mW
	P_D (Note 2)	500	
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

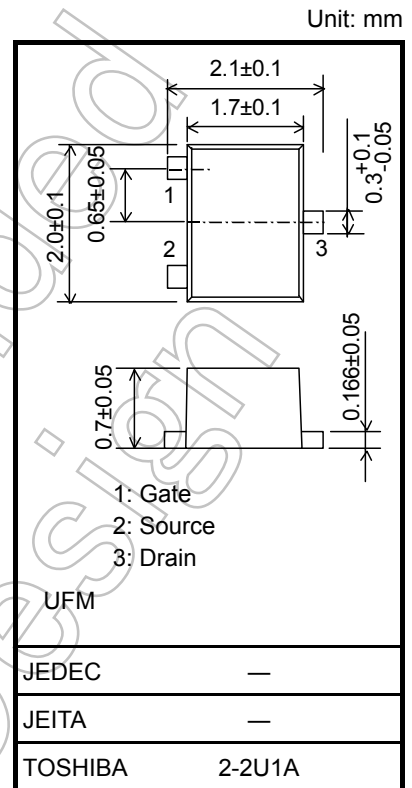
Note 1: Mounted on a ceramic board.
(25.4 mm × 25.4 mm × 0.8 mm, Cu Pad: 645 mm²)

Note 2: Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)

Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1 \text{ mA}, V_{GS} = 0$	20	—	—	V
Drain cutoff current	I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	—	—	1	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$	—	—	±1	μA
Gate threshold voltage	V_{th}	$V_{DS} = 5 \text{ V}, I_D = 0.1 \text{ mA}$	1.1	—	2.3	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 5 \text{ V}, I_D = 0.6 \text{ A}$ (Note 3)	0.58	1.16	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = 0.6 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 3)	—	230	310	mΩ
		$I_D = 0.6 \text{ A}, V_{GS} = 4 \text{ V}$ (Note 3)	—	390	530	
Input capacitance	C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	36	—	pF
Output capacitance	C_{oss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	30	—	pF
Reverse transfer capacitance	C_{rss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	10	—	pF
Switching time	Turn-on time	$V_{DD} = 10 \text{ V}, I_D = 0.6 \text{ A},$ $V_{GS} = 0 \text{ to } 4 \text{ V}, R_G = 10 \Omega$	—	21	—	ns
	Turn-off time		—	8	—	
Drain-source forward voltage	V_{DSF}	$I_D = -1.2 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 3)	—	-1.0	-1.4	V

Note 3: Pulse test

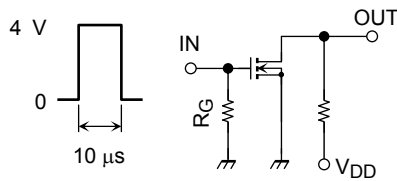


Weight: 6.6 mg (typ.)

Start of commercial production
2005-02

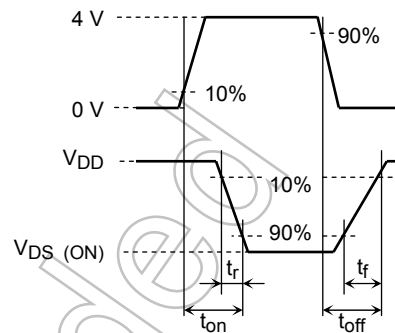
Switching Time Test Circuit

(a) Test Circuit



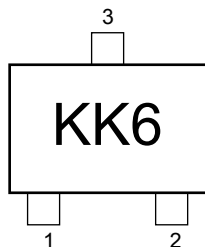
$V_{DD} = 10\text{ V}$
 $R_G = 10\ \Omega$
 Duty $\leq 5\%$
 V_{IN} : $t_r, t_f < 5\text{ ns}$
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}

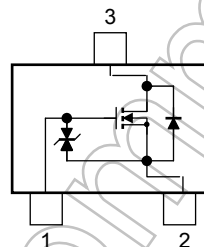


(c) V_{OUT}

Marking



Equivalent Circuit (top view)



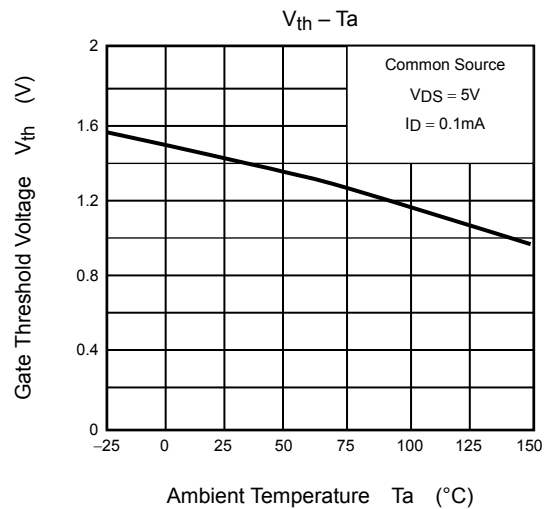
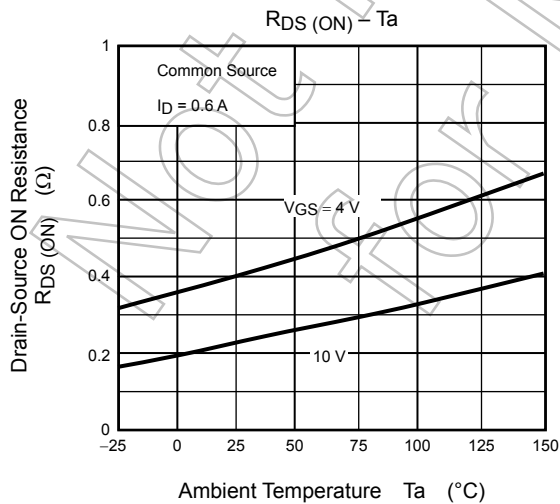
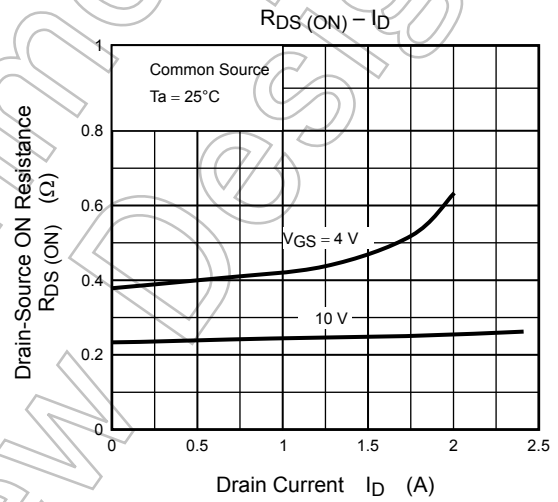
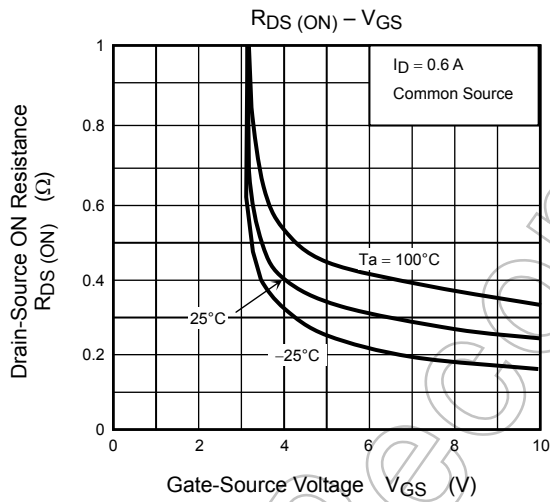
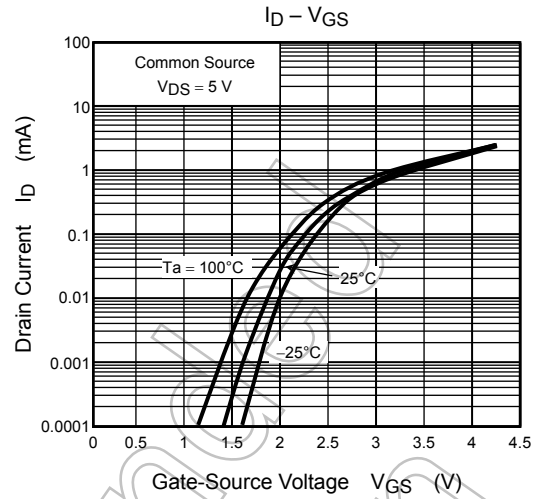
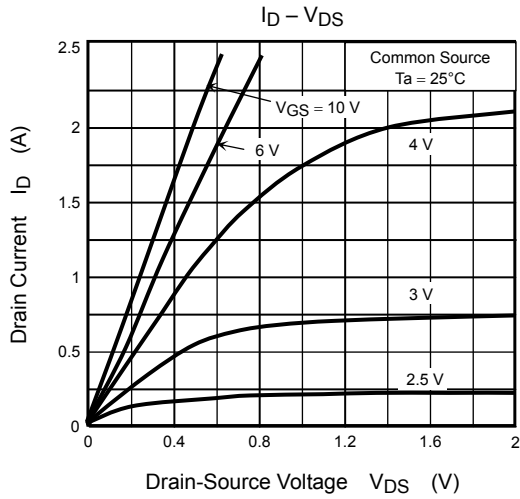
Note

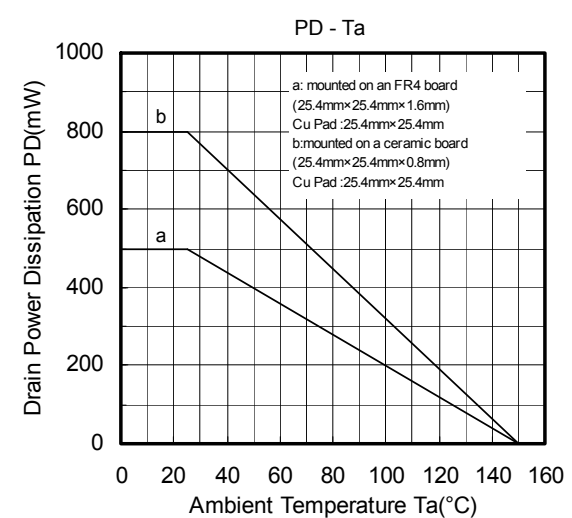
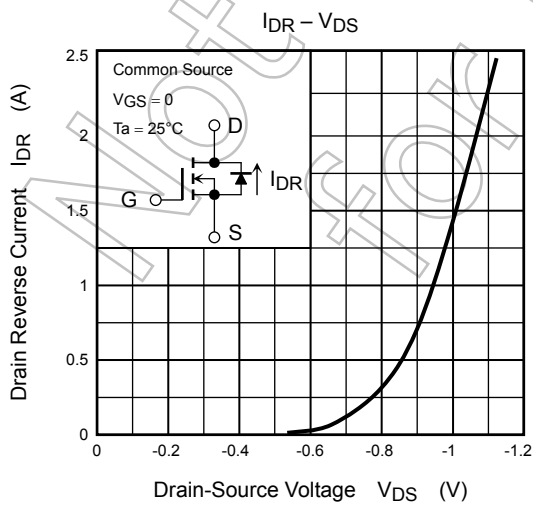
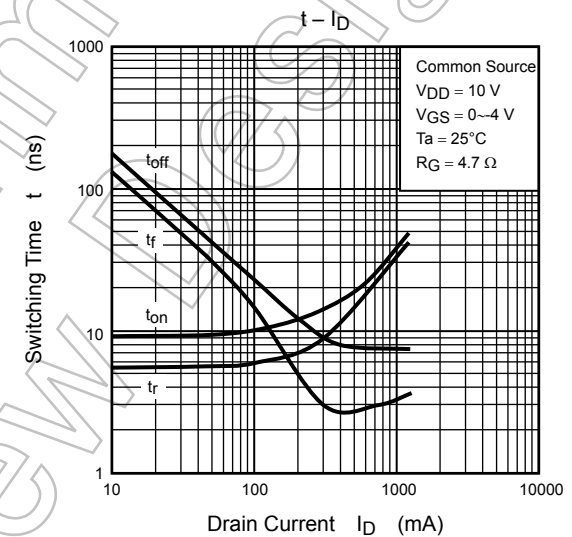
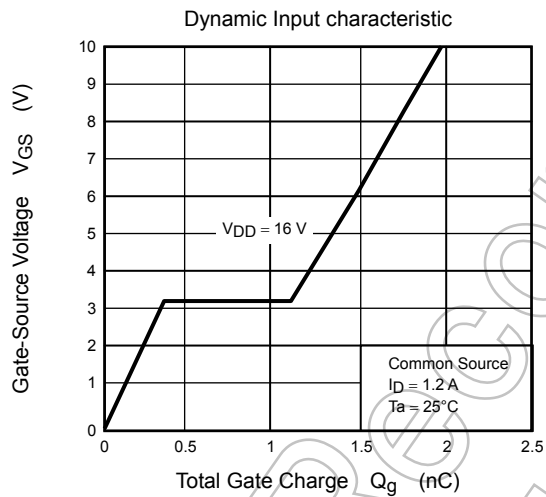
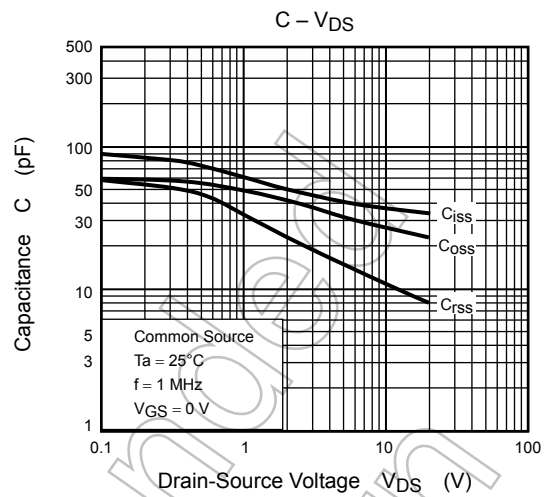
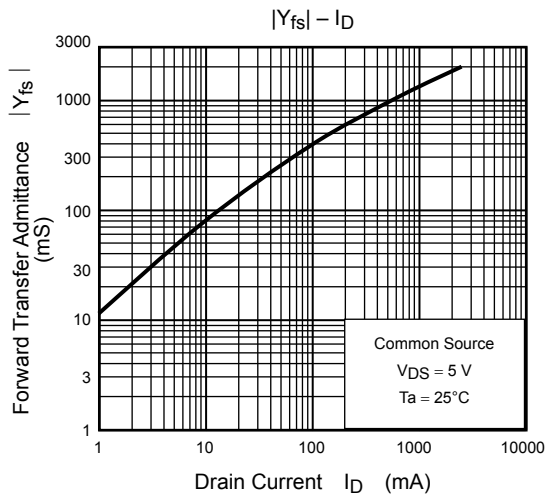
V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = 0.1\text{ mA}$ for this product. For normal switching operation, $V_{GS(on)}$ requires a higher voltage than V_{th} , and $V_{GS(off)}$ requires a lower voltage than V_{th} . (The relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(on)}$.)

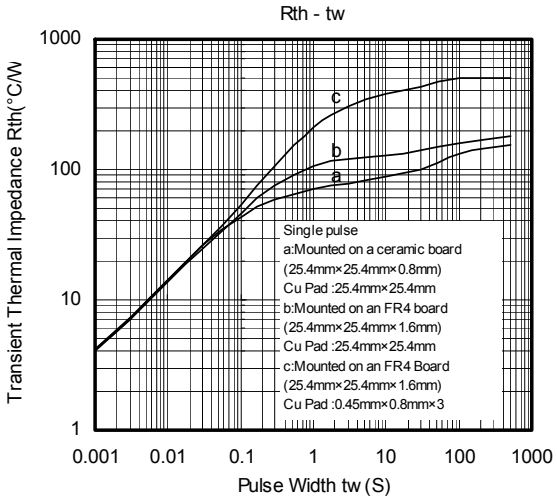
Take this into consideration when using the device.

Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, be sure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.







Not Recommended for New Design

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