

CMOS Linear Integrated Circuit Silicon Monolithic

TC75W71FU, TC75W72FU, TC75W73FU

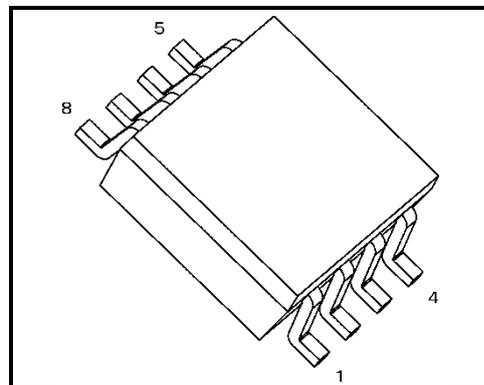
High speed Dual comparator

1. Description

The TC75W71FU, TC75W72FU, TC75W73FU are a CMOS type general-purpose dual comparator capable of single power supply operation and using lower supply currents than the conventional bipolar comparators.

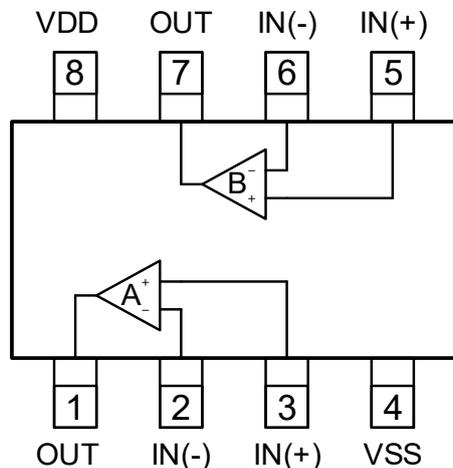
2. Features

- Propagation Delay at 3.3 V_{DD} @ 25 °C
 - 45 ns (Max) high-to-low
 - 30 ns (Max) low-to-high
- Rail to Rail Input
- Wide supply voltage range: 1.8 V to 5.5 V
- Package: SM8
- Output type
 - TC75W71FU: Push-pull
 - TC75W72FU: Push-pull
 - TC75W73FU: Open-drain



Weight:
SM8 (SOT-505) : 0.020 g (Typ.)

3. Pin Connection (Top View)



4. Product list

Part name	Input Hysteresis voltage	Output type	Top marking
TC75W71FU	None	Push-pull	5W71
TC75W72FU	Yes	Push-pull	5W72
TC75W73FU	Yes	Open-drain	5W73

Start of commercial production
2025-09

5. Absolute Maximum Ratings (Note) (Ta = 25 °C)

Characteristics	Symbol	Rating	Unit	
Supply voltage	$V_{DD} - V_{SS}$	6.0	V	
Analog input voltage	V_{IN}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$ or 6.0 which is smaller	V	
Output voltage	V_{OUT}	TC75W71FU	$V_{SS} - 0.3$ to $V_{DD} + 0.3$ or 6.0 which is smaller	V
		TC75W72FU		
		TC75W73FU	$V_{SS} - 0.3$ to 6.0	
Power dissipation	P_D	250	mW	
Junction temperature	T_j	150	°C	
Storage temperature	T_{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g., the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e., operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e., reliability test report and estimated failure rate, etc.).

Note: Since this product sometimes brings about latch-up, which is peculiar to CMOS devices, note the following points:

- Don't raise the voltage level of I/O pins beyond V_{DD} , nor lower it below V_{SS} .
Consider the timing for power supply, too.
- Don't let any abnormal noise enter the device.

6. Operating Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	1.8 to 5.5	V
Input voltage range	V_{IN}	$V_{SS} - 0.2$ V to $V_{DD} + 0.2$ V	V
Operation temperature	T_{opr}	-40 to 125	°C

7. Electrical Characteristics

7.1. DC Characteristics (V_{DD} = 3.3 V, V_{SS} = GND, Ta = -40 °C to 125 °C)

Characteristics	Symbol	Test condition	Ta = 25 °C			Ta = -40 °C to 125 °C (Note 1)		Unit
			Min	Typ.	Max	Min	Max	
Supply current	I _{DD}	V _{OUT} = High, V _{IN} = V _{SS}	–	294	370	–	508	μA
		V _{OUT} = Low, V _{IN} = V _{SS}	–	450	563	–	761	μA
Power supply rejection ratio	PSRR	V _{DD} = 1.8 V to 5.0 V, V _{IN} = V _{SS}	39	70	–	–	–	dB
Input offset voltage	V _{IO}	V _{SS} < V _{IN} < V _{DD}	-17	±3	17	–	–	mV
Input offset voltage drift	V _{IO} drift	V _{IN} = V _{SS}	–	±2	–	–	–	μV/°C
Input Hysteresis voltage (Note1)	V _{HYST}	TC75W72FU, TC75W73FU (Note2) V _{IN} = V _{SS}	1.0	3.5	5.5	–	–	mV
Input offset current	I _{IO}	V _{IN} = V _{SS}	–	0	–	–	192	nA
Input bias current	I _I	V _{IN} = V _{DD} /2	–	0	–	–	196	nA
Common mode input voltage	CMV _{IN}	–	V _{SS}	–	V _{DD}	–	–	V
Common mode input signal rejection ratio	CMRR	V _{SS} < V _{IN} < V _{DD}	39	66	–	–	–	dB
High-Level Output Voltage	VOH	TC75W71FU, TC75W72FU I _{OUT} = -1 mA	V _{DD} - 0.15	–	–	–	–	V
Low-Level Output Voltage	VOL	I _{OUT} = 1 mA	–	–	0.15	–	–	V
Short-Circuit Current	ISC	–	–	±25	–	–	–	mA

Note 1: This parameter is warranted by design.

Note 2: TC75W71FU does not incorporate input hysteresis voltage.

7.2. DC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = -40 °C to 125 °C)

Characteristics	Symbol	Test condition	Ta = 25 °C			Ta = -40 °C to 125 °C (Note 1)		Unit
			Min	Typ.	Max	Min	Max	
Supply current	I _{DD}	V _{OUT} = High, V _{IN} = V _{SS}	–	276	349	–	476	μA
		V _{OUT} = Low, V _{IN} = V _{SS}	–	422	533	–	719	μA
Power supply rejection ratio	PSRR	V _{DD} = 1.8 V to 5.0 V, V _{IN} = V _{SS}	39	70	–	–	–	dB
Input offset voltage	V _{IO}	V _{SS} < V _{IN} < V _{DD}	-17	±3	17	–	–	mV
Input offset voltage drift	V _{IO} drift	V _{IN} = V _{SS}	–	±2	–	–	–	μV/°C
Input Hysteresis voltage (Note1)	V _{HYST}	TC75W72FU, TC75W73FU (Note2) V _{IN} = V _{SS}	1.0	3.5	5.5	–	–	mV
Input offset current	I _{IO}	V _{IN} = V _{SS}	–	0	–	–	192	nA
Input bias current	I _I	V _{IN} = V _{DD} /2	–	0	–	–	196	nA
Common mode input voltage	CMV _{IN}	–	V _{SS}	–	V _{DD}	–	–	V
Common mode input signal rejection ratio	CMRR	V _{SS} < V _{IN} < V _{DD}	34	66	–	–	–	dB
High-Level Output Voltage	VOH	TC75W71FU, TC75W72FU I _{OUT} = -1 mA	V _{DD} - 0.2	–	–	–	–	V
Low-Level Output Voltage	VOL	I _{OUT} = 1 mA	–	–	0.2	–	–	V
Short-Circuit Current	ISC	–	–	±6	–	–	–	mA

Note 1: This parameter is warranted by design.

Note 2: TC75W71FU does not incorporate input hysteresis voltage.

7.3. DC Characteristics (VDD = 5.0 V, VSS = GND, Ta = -40 °C to 125 °C)

Characteristics	Symbol	Test condition	Ta = 25 °C			Ta = -40 °C to 125 °C (Note 1)		Unit
			Min	Typ.	Max	Min	Max	
Supply current	IDD	VOUT = High, VIN = VSS	-	323	407	-	547	μA
		VOUT = Low, VIN = VSS	-	497	622	-	827	μA
Power supply rejection ratio	PSRR	VDD = 1.8 V to 5.0 V, VIN = VSS	39	70	-	-	-	dB
Input offset voltage	VIO	VSS < VIN < VDD	-17	±3	17	-	-	mV
Input offset voltage drift	VIOdrift	VIN = VSS	-	±2	-	-	-	μV/°C
Input Hysteresis voltage (Note1)	VHYST	TC75W72FU, TC75W73FU (Note2) VIN = VSS	1.0	3.5	5.5	-	-	mV
Input offset current	IIO	VIN = VSS	-	0	-	-	192	nA
Input bias current	II	VIN = VDD/2	-	0	-	-	196	nA
Common mode input voltage	CMVIN	-	VSS	-	VDD	-	-	V
Common mode input signal rejection ratio	CMRR	VSS < VIN < VDD	43	66	-	-	-	dB
High-Level Output Voltage	VOH	TC75W71FU, TC75W72FU IOUT = -4 mA	VDD - 0.3	-	-	-	-	V
Low-Level Output Voltage	VOL	IOUT = 4 mA	-	-	0.3	-	-	V
Short-Circuit Current	ISC	-	-	±54	-	-	-	mA

Note 1: This parameter is warranted by design.

Note 2: TC75W71FU does not incorporate input hysteresis voltage.

7.4. AC Characteristics (Note 1)

(VDD = 1.8 V to 5.0 V, VSS = GND, Ta = 25 °C, TC75W71FU, TC75W72FU)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Low to High, 100 mV Overdrive	tPLH	VIN(+) = -100mV to +100 mV, VIN(-) = VSS, VDD = 1.8 V, CL = 50 pF, RL = 10 kΩ	-	28	-	ns
		VIN(+) = -100mV to +100 mV, VIN(-) = VSS, VDD = 3.3 V, CL = 50 pF, RL = 10 kΩ	-	23	45	ns
		VIN(+) = -100mV to +100 mV, VIN(-) = VSS, VDD = 5.0 V, CL = 50 pF, RL = 10 kΩ	-	23	-	ns
High to Low, 100 mV Overdrive	tPHL	VIN(+) = +100mV to -100 mV, VIN(-) = VSS, VDD = 1.8 V, CL = 50 pF, RL = 10 kΩ	-	19	-	ns
		VIN(+) = +100mV to -100 mV, VIN(-) = VSS, VDD = 3.3 V, CL = 50 pF, RL = 10 kΩ	-	14	30	ns
		VIN(+) = +100mV to -100 mV, VIN(-) = VSS, VDD = 5.0 V, CL = 50 pF, RL = 10 kΩ	-	12	-	ns
Rise Time	tR	VIN(+) = -100mV to 100 mV, VIN(-) = VSS, VDD = 1.8 V, CL = 50 pF, RL = 10 kΩ	-	16	-	ns
		VIN(+) = -100mV to 100 mV, VIN(-) = VSS, VDD = 3.3 V, CL = 50 pF, RL = 10 kΩ	-	6	-	ns
		VIN(+) = -100mV to 100 mV, VIN(-) = VSS, VDD = 5.0 V, CL = 50 pF, RL = 10 kΩ	-	4	-	ns
Fall Time	tF	VIN(+) = +100mV to -100 mV, VIN(-) = VSS, VDD = 1.8 V, CL = 50 pF, RL = 10 kΩ	-	13	-	ns
		VIN(+) = +100mV to -100 mV, VIN(-) = VSS, VDD = 3.3 V, CL = 50 pF, RL = 10 kΩ	-	5	-	ns
		VIN(+) = +100mV to -100 mV, VIN(-) = VSS, VDD = 5.0 V, CL = 50 pF, RL = 10 kΩ	-	3	-	ns

Note 1: This parameter is warranted by design.

7.5. AC Characteristics (Note 1)

($V_{DD} = 1.8\text{ V to }5.0\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25\text{ }^\circ\text{C}$, TC75W73FU)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
High to Low, 100 mV Overdrive	tPHL	$V_{IN(+)} = +100\text{ mV to }-100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 1.8\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$	-	16	-	ns
		$V_{IN(+)} = +100\text{ mV to }-100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$	-	11	30	ns
		$V_{IN(+)} = +100\text{ mV to }-100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$	-	10	-	ns
Fall Time	tF	$V_{IN(+)} = +100\text{ mV to }-100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 1.8\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$	-	13	-	ns
		$V_{IN(+)} = +100\text{ mV to }-100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$	-	4.6	-	ns
		$V_{IN(+)} = +100\text{ mV to }-100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 5.0\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$	-	3.4	-	ns

Note 1: This parameter is warranted by design.

7.6. AC Waveform

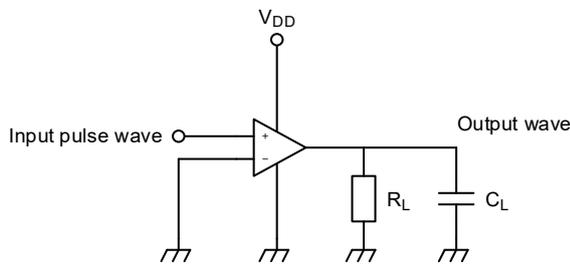


Fig. 7.6.1 Propagation delay time tPLH, tPHL, Rise time tR, Fall time tF (TC75W71FU, TC75W72FU)

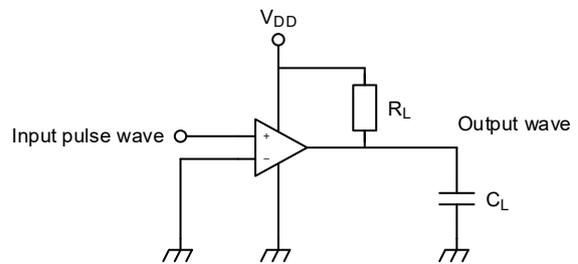


Fig. 7.6.2 Propagation delay time tPHL, Fall time tF (TC75W73FU)

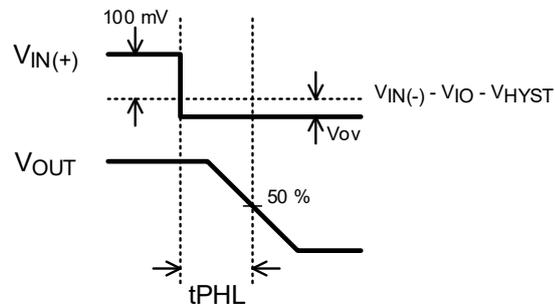
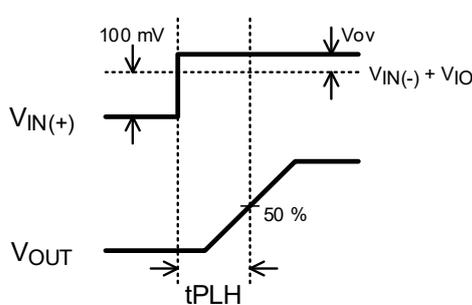


Fig. 7.6.3 Propagation delay time tPLH, tPHL (Note 2)

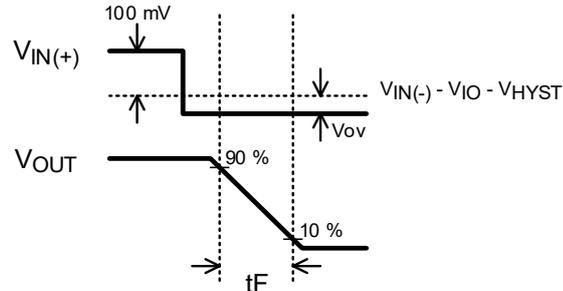
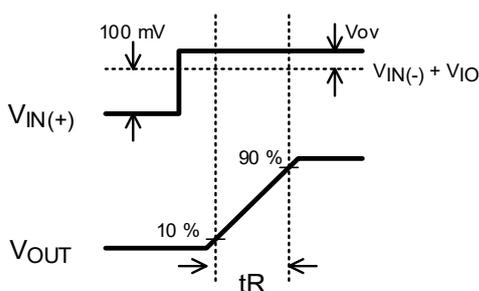


Fig. 7.6.4 Rise time tR, Fall time tF (Note 2)

Note 2: TC75W71FU does not incorporate input hysteresis voltage.

8. Representative characteristics (Note)

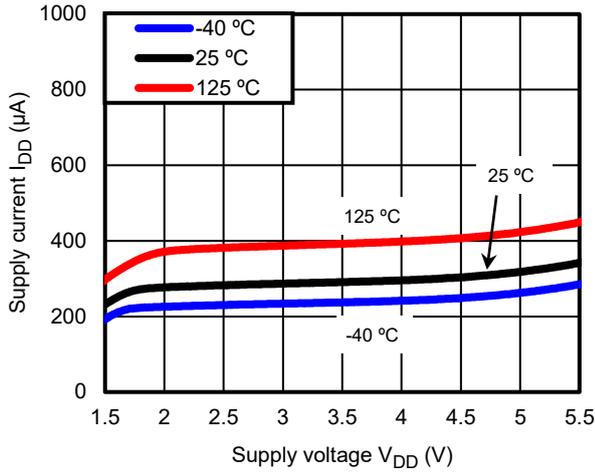


Fig. 8.1 Supply current I_{DD}
 $V_{OUT} = \text{High}, V_{IN} = V_{SS}$

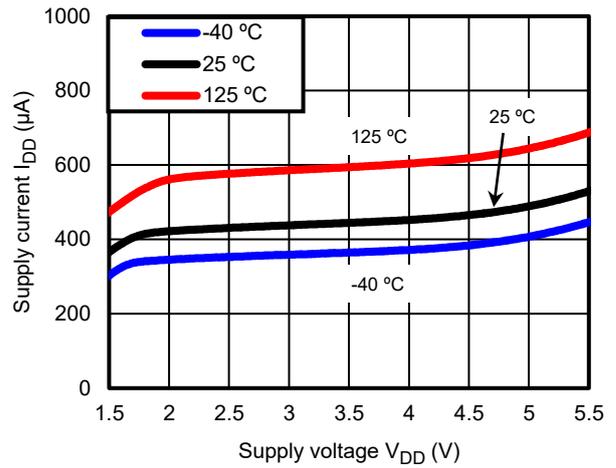


Fig. 8.2 Supply current I_{DD}
 $V_{OUT} = \text{Low}, V_{IN} = V_{SS}$

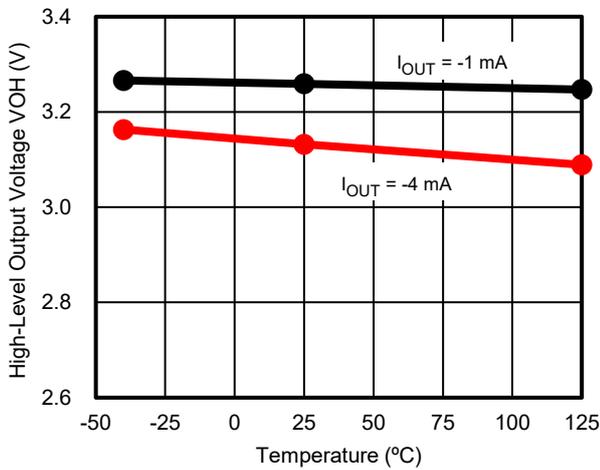


Fig. 8.3 High-Level Output Voltage V_{OH}
 $V_{DD} = 3.3 \text{ V}$

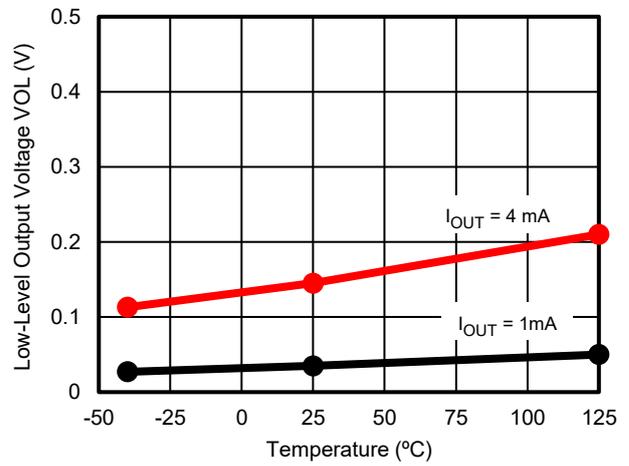


Fig. 8.4 Low-Level Output Voltage V_{OL}
 $V_{DD} = 3.3 \text{ V}$

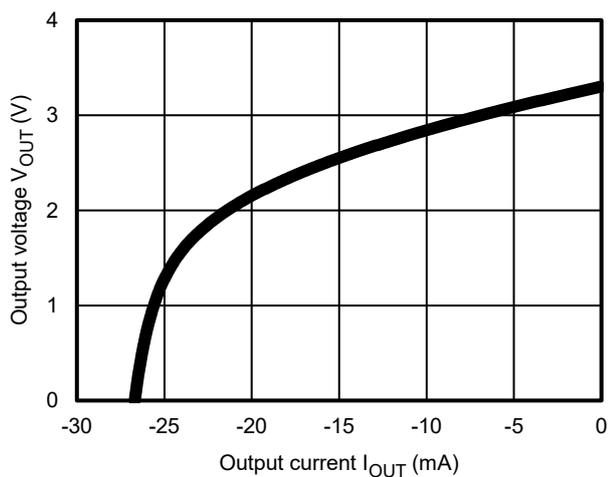


Fig. 8.5 High-Level Output Voltage V_{OH}
 $V_{DD} = 3.3 \text{ V}, T_a = 25 \text{ °C}$

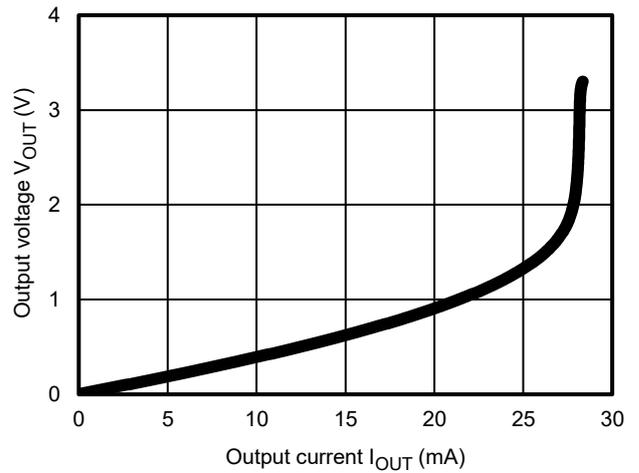


Fig. 8.6 Low-Level Output Voltage V_{OL}
 $V_{DD} = 3.3 \text{ V}, T_a = 25 \text{ °C}$

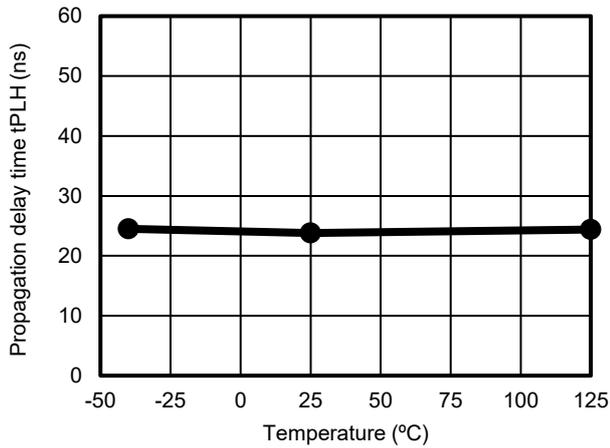


Fig. 8.7 Propagation delay time tPLH
 $V_{IN(+)} = -100\text{mV to } +100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 3.3\text{ V}$,
 $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$

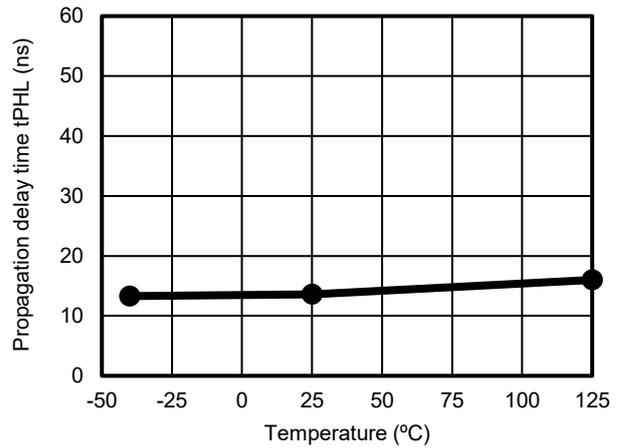


Fig. 8.8 Propagation delay time tPHL
 $V_{IN(+)} = +100\text{mV to } -100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 3.3\text{ V}$,
 $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$

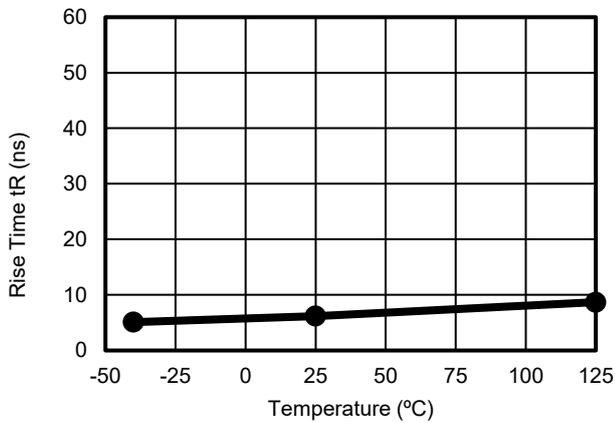


Fig. 8.9 Rise time tR
 $V_{IN(+)} = -100\text{mV to } +100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 3.3\text{ V}$,
 $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$

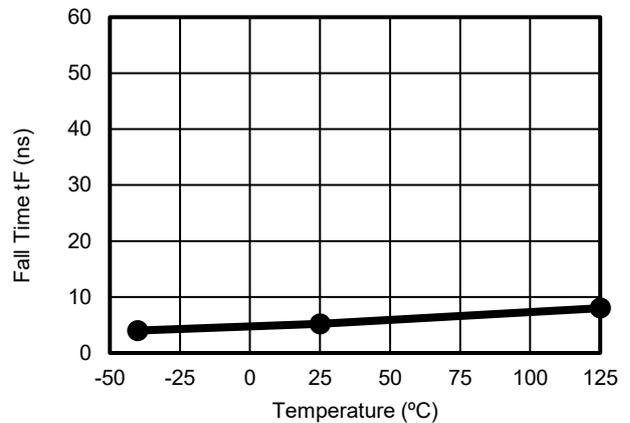


Fig. 8.10 Fall time tF
 $V_{IN(+)} = +100\text{mV to } -100\text{ mV}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 3.3\text{ V}$,
 $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$

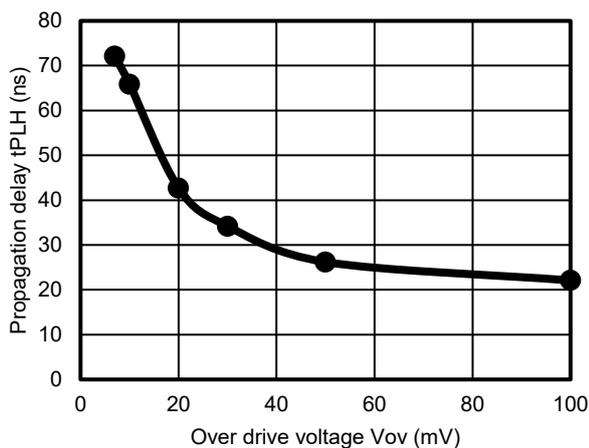


Fig. 8.11 Propagation delay time tPLH
 $V_{IN(+)} = -100\text{mV to } V_{ov}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 3.3\text{ V}$, $C_L = 50\text{ pF}$,
 $R_L = 10\text{ k}\Omega$, $T_a = 25\text{ }^\circ\text{C}$

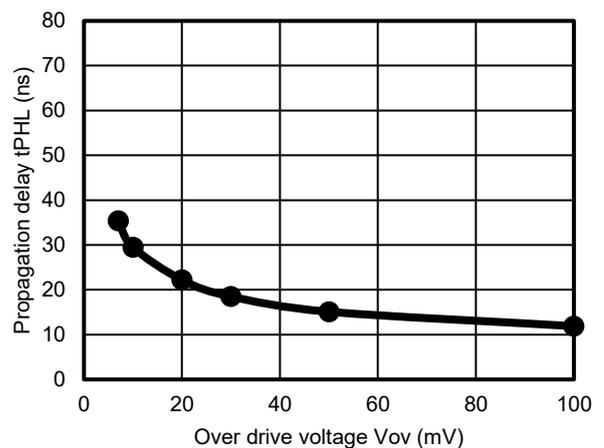


Fig. 8.12 Propagation delay time tPHL
 $V_{IN(+)} = +100\text{mV to } V_{ov}$, $V_{IN(-)} = V_{SS}$, $V_{DD} = 3.3\text{ V}$, $C_L = 50\text{ pF}$,
 $R_L = 10\text{ k}\Omega$, $T_a = 25\text{ }^\circ\text{C}$

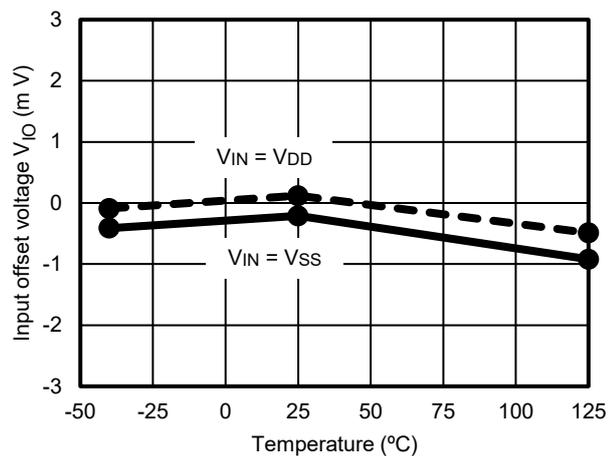


Fig. 8.13 Input offset voltage
 $V_{DD} = 3.3\text{ V}$

Note : The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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