Photocouplers GaAℓAs Infrared LED & Photo IC

TLP152

1. Applications

- Plasma Display Panels (PDPs)
- Industrial Inverters
- MOSFET Gate Drivers
- IGBT Gate Drivers

2. General

The TLP152 is a photocoupler in an SO6 package that consists of a GaAℓAs infrared light-emitting diode (LED) optically coupled to an integrated high-gain, high-speed photodetector IC chip. The photodetector IC chip has an internal shield to provide a high common-mode transient immunity of ±20 kV/μs and thus superior noise immunity between the input and output pins. The TLP152 has a totem-pole output that can both sink and source current. It is suitable for directly driving a small IGBT or power MOSFET.

3. Features

(1) Buffer logic type (totem pole output)

(2) Output peak current: ±2.5 A (max)

(3) Operating temperature: -40 to 100 ℃

(4) Supply current: 3.0 mA (max)

(5) Supply voltage: 10 to 30 V

(6) Threshold input current: 7.5 mA (max)

(7) Propagation delay time: t_{pHL} = 190 ns (max), t_{pLH} = 170 ns (max)

(8) Common-mode transient immunity: ±20 kV/μs (min)

(9) Isolation voltage: 3750 Vrms (min)

(10) Safety standards

UL-approved: UL1577, File No.E67349

cUL-approved: CSA Component Acceptance Service No.5A File No.E67349

VDE-approved: EN60747-5-5, EN60065 or EN60950-1 **(Note 1)**

: EN62368-1 (Pending) **(Note 1)**

CQC-approved: GB4943.1, GB8898 Thailand Factory

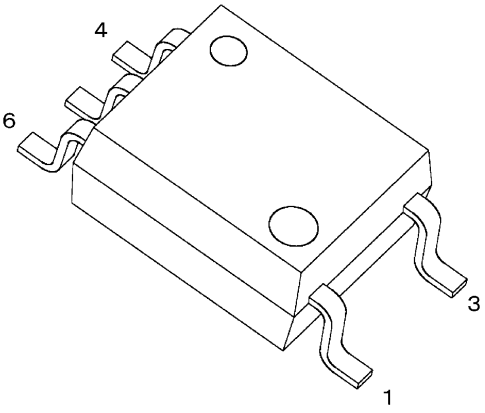
≤2000m CQC 仅适用于海拔 2000m 以下地区安全使用

Note 1: When a VDE approved type is needed, please designate the **Option (V4)**.

Start of commercial production

2012-06

4. Packaging and Pin Assignment



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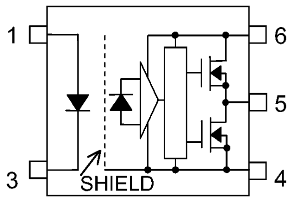
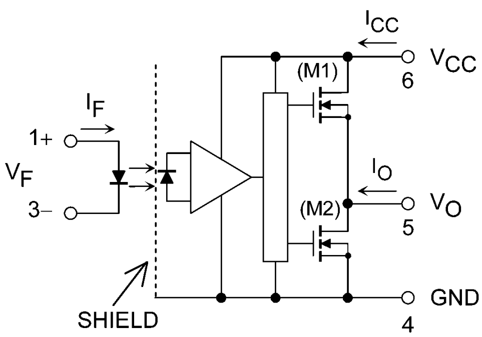


1: Anode
3: Cathode
4: GND
5: V_O
6: V_{CC}

5. Internal Circuit (Note)



Note: A 0.1-µF bypass capacitor must be connected between pin 6 and pin 4.

6. Principle of Operation

6.1. Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

6.2. Mechanical Parameters

Characteristics	Size	Unit
Creepage distances	5.0 (min)	mm
Clearance distances	5.0 (min)	
Internal isolation thickness	0.4 (min)	

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

	Characteristics		Symbol	Note	Rating	Unit
LED	Input forward current		I_F		20	mA
	Peak transient input forward current		I_{FPT}	(Note 1)	1	A
	Input reverse voltage		V_R		5	V
	Input power dissipation		P_D		40	mW
Detector	Peak high-level output current	(T_a = -40 to 100 °C)	I_{OPH}	(Note 2)	-2.5	A
	Peak low-level output current	(T_a = -40 to 100 °C)	I_{OPL}	(Note 2)	+2.5	
	Output voltage		V_O		35	V
	Supply voltage		V_{CC}		35	
	Output power dissipation		P_O		260	mW
	Output power dissipation derating	(T_a ≥ 85 °C)	$\Delta P_O/\Delta T_a$		-2.0	mW/°C
Common	Operating temperature		T_{opr}		-40 to 100	°C
	Storage temperature		T_{stg}		-55 to 125	
	Lead soldering temperature	(10 s)	T_{sol}	(Note 3)	260	
	Isolation voltage	(AC, 60 s, R.H. ≤ 60 %)	BV_S	(Note 4)	3750	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) ≤ 1 μs, 300 pps

Note 2: Exponential waveform. Pulse width ≤ 0.2 μs, f ≤ 15 kHz, V_{CC} = 20 V, T_a = -40 to 100 °C
Exponential waveform. Pulse width ≤ 0.08 μs, f ≤ 25 kHz, V_{CC} = 15 V, T_a = -40 to 100 °C

Note 3: ≥ 2 mm below seating plane.

Note 4: This device is considered as a two-terminal device: Pins 1 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

8. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	$I_{F(ON)}$	(Note 1)	10	—	15	mA
Input off-state voltage	$V_{F(OFF)}$		0	—	0.8	V
Peak high-level output current	I_{OPH}		—	—	-2.0	A
Peak low-level output current	I_{OPL}		—	—	+2.0	
Operating frequency	f	(Note 2)	—	—	250	kHz

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 6 and pin 4 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: The rise and fall times of the input on-current should be less than 0.5 μs.

Note 2: Exponential waveform. I_{OPH} ≥ -0.65 A (≤ 80 ns), I_{OPL} ≤ 0.65 A (≤ 80 ns), T_a = 100 °C, V_{CC} = 20 V

9. Electrical Characteristics (Note) (Unless otherwise specified, T_a = -40 to 100 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F		—	I_F = 10 mA, T_a = 25 °C	1.40	1.57	1.80	V
Input forward voltage temperature coefficient	$\Delta V_F/\Delta T_a$		—	I_F = 10 mA	—	-1.8	—	mV/°C
Input reverse current	I_R		—	V_R = 5 V, T_a = 25 °C	—	—	10	μA
Input capacitance	C_t		—	V = 0 V, f = 1 MHz, T_a = 25 °C	—	45	—	pF
Peak high-level output current	I_{OPH}	(Note 1)	Fig. 12.1.1	I_F = 10 mA, V_{CC} = 15 V, $V_{6\text{-}5}$ = 4 V	—	-2.2	-1.0	A
				I_F = 10 mA, V_{CC} = 15 V, $V_{6\text{-}5}$ = 10 V	—	-3.4	-2.0	
Peak low-level output current	I_{OPL}	(Note 1)	Fig. 12.1.2	I_F = 0 mA, V_{CC} = 15 V, $V_{5\text{-}4}$ = 2 V	1.0	2.4	—	
				I_F = 0 mA, V_{CC} = 15 V, $V_{5\text{-}4}$ = 10 V	2.0	3.5	—	
High-level output voltage	V_{OH}		Fig. 12.1.3	I_F = 10 mA, V_{CC} = 10 V, I_O = -100 mA	6.0	8.5	—	V
Low-level output voltage	V_{OL}		Fig. 12.1.4	V_F = 0.8 V, V_{CC} = 10 V, I_O = 100 mA	—	0.1	1.0	
High-level supply current	I_{CCH}		Fig. 12.1.5	I_F = 10 mA, V_{CC} = 10 to 30 V, V_O = Open	—	1.9	3.0	mA
Low-level supply current	I_{CCL}		Fig. 12.1.6	I_F = 0 mA, V_{CC} = 10 to 30 V, V_O = Open	—	1.8	3.0	
Threshold input current (L/H)	I_{FLH}		—	V_{CC} = 15 V, V_O > 1 V	—	1.5	7.5	
Threshold input voltage (H/L)	V_{FHL}		—	V_{CC} = 15 V, V_O < 1 V	0.8	1.47	—	V
Supply voltage	V_{CC}		—	—	10	—	30	
UVLO threshold voltage	V_{UVLO}+		—	I_F = 5 mA, V_O > 2.5 V	7.8	8.7	9.7	
	V_{UVLO}-			I_F = 5 mA, V_O < 2.5 V	7.5	8.4	9.4	
UVLO hysteresis	$UVLO_{HYS}$		—	I_F = 5 mA, V_O > 2.5 V	—	0.3	—	

Note: All typical values are at T_a = 25 °C.

Note: This device is designed for low power consumption, making it more sensitive to ESD than its predecessors. Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1: I_O application time ≤ 50 μs, single pulse.

10. Isolation Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	(Note 1)	V_S = 0 V, f = 1 MHz	—	0.35	—	pF
Isolation resistance	R_S	(Note 1)	V_S = 500 V, R.H. ≤ 60 %	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	(Note 1)	AC, 60 s	3750	—	—	Vrms
			AC, 1 s in oil	—	10000	—	
			DC, 60 s in oil	—	10000	—	Vdc

Note 1: This device is considered as a two-terminal device: Pins 1 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

11. Switching Characteristics (Note) (Unless otherwise specified, T_a = -40 to 100 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	Fig. 12.1.7	I_F = 0 → 10 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF, T_a = 25 °C	60	95	145	ns
Propagation delay time (H/L)	t_{pHL}	(Note 1)		I_F = 10 → 0 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF, T_a = 25 °C	60	110	165	
Propagation delay time (L/H)	t_{pLH}	(Note 1)		I_F = 0 → 10 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	50	95	170	
Propagation delay time (H/L)	t_{pHL}	(Note 1)		I_F = 10 → 0 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	50	110	190	
Propagation delay skew (device to device)	t_{psk}	(Note 1) (Note 4)		I_F = 0 ←→ 10 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	-85	—	85	
Pulse width distortion	$\|t_{pHL}-t_{pLH}\|$	(Note 1)		I_F = 0 ←→ 10 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	15	50	
Rise time	t_r	(Note 1)		I_F = 0 → 10 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	18	—	
Fall time	t_f	(Note 1)		I_F = 10 → 0 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	22	—	
Common-mode transient immunity at output high	CM_H	(Note 2)	Fig. 12.1.8	V_{CM} = 1000 V_{p-p}, I_F = 10 mA, V_{CC} = 30 V, T_a = 25°C, $V_{O(min)}$ = 26 V	±20	—	—	kV/μs
Common-mode transient immunity at output low	CM_L	(Note 3)		V_{CM} = 1000 V_{p-p}, I_F = 0 mA, V_{CC} = 30 V, T_a = 25°C, $V_{O(max)}$ = 1 V	±20	—	—	

Note: All typical values are at T_a = 25 °C.

Note 1: Input signal (f = 125 kHz, duty = 50 %, t_r = t_f = 5 ns or less).
CL is approximately 15 pF which includes probe and stray wiring capacitance.

Note 2: CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 26 V).

Note 3: CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 1 V).

Note 4: The propagation delay skew, t_{psk}, is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

12. Test Circuits and Characteristics Curves

12.1. Test Circuits

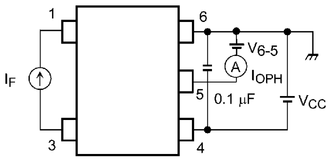


Fig. 12.1.1 I_{OPH} Test Circuit

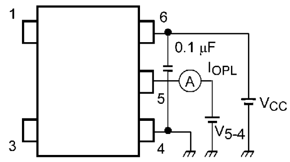


Fig. 12.1.2 I_{OPL} Test Circuit

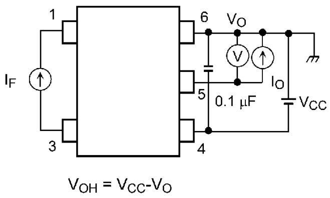


Fig. 12.1.3 V_{OH} Test Circuit

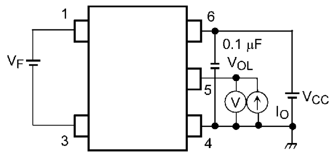


Fig. 12.1.4 V_{OL} Test Circuit

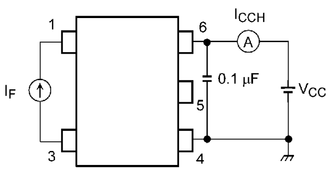


Fig. 12.1.5 I_{CCH} Test Circuit

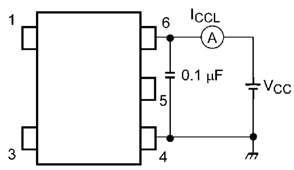


Fig. 12.1.6 I_{CCL} Test Circuit

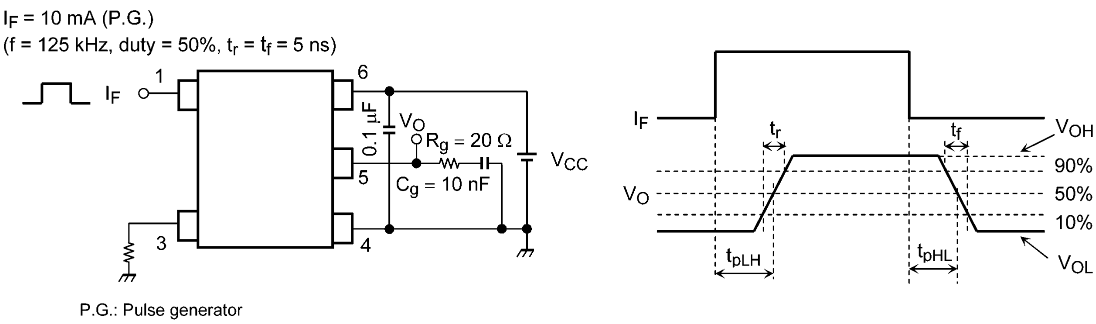


Fig. 12.1.7 Switching Time Test Circuit and Waveform

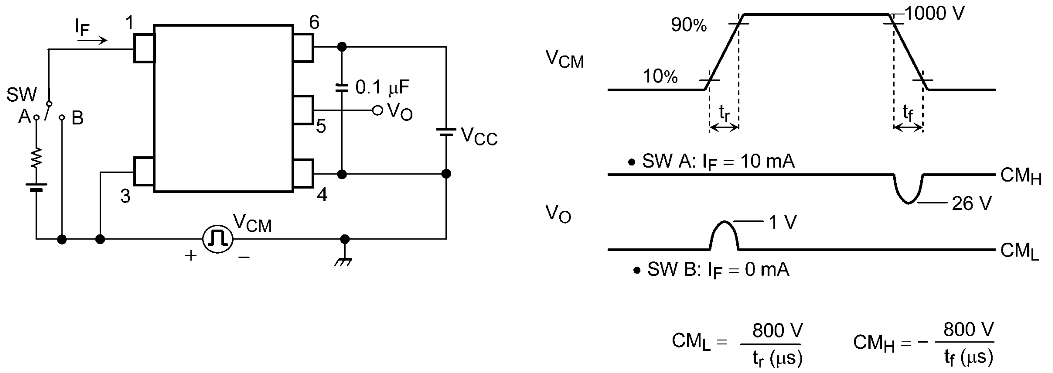


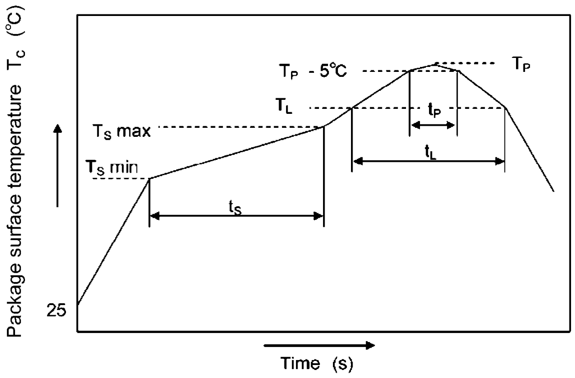
Fig. 12.1.8 Common-Mode Transient Immunity Test Circuit and Waveform

13. Soldering and Storage

13.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow.
  The soldering temperature profile is based on the package surface temperature.
  (See the figure shown below, which is based on the package surface temperature.)
  Reflow soldering must be performed once or twice.
  The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



	Symbol	Min	Max	Unit
Preheat temperature	T_S	150	200	°C
Preheat time	t_S	60	120	s
Ramp-up rate (T_L to T_P)			3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	150	s
Peak temperature	T_P		260	°C
Time during which T_c is between (T_P – 5) and T_P	t_P		30	s
Ramp-down rate (T_P to T_L)			6	°C/s

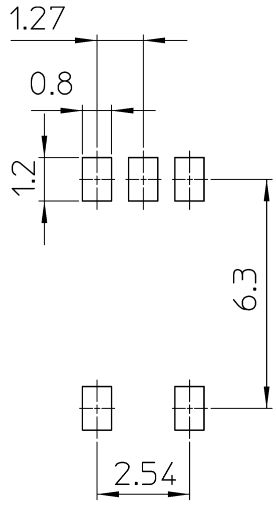
Fig. 13.1.1 An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used

- When using soldering flow
  Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
  Mounting condition of 260 °C within 10 seconds is recommended.
  Flow soldering must be performed once.
- When using soldering Iron
  Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C
  Heating by soldering iron must be done only once per lead.

13.2. Precautions for General Storage

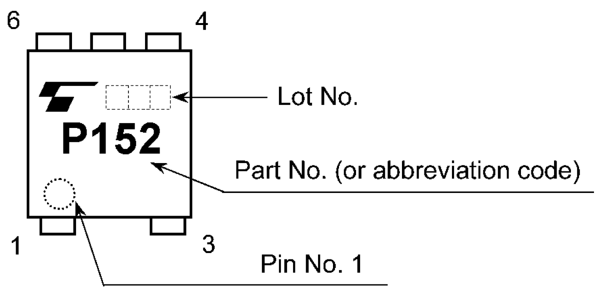
- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

14. Land Pattern Dimensions (for reference only)



Unit: mm

15. Marking



16. Specifications for Embossed-Tape Packing

16.1. Applicable Package

Package Name	Product Type
SO6	Mini flat coupler

16.2. Product Naming Conventions

Type of package used for shipment is denoted by a symbol suffix after a part number. The method of classification is as below.

Example) TLP152(TPL,E(T

Part number: TLP152
Tape type: TPL
[[G]]/RoHS COMPATIBLE: E **(Note 1)**
Domestic ID (Country/Region of origin: Thailand): T

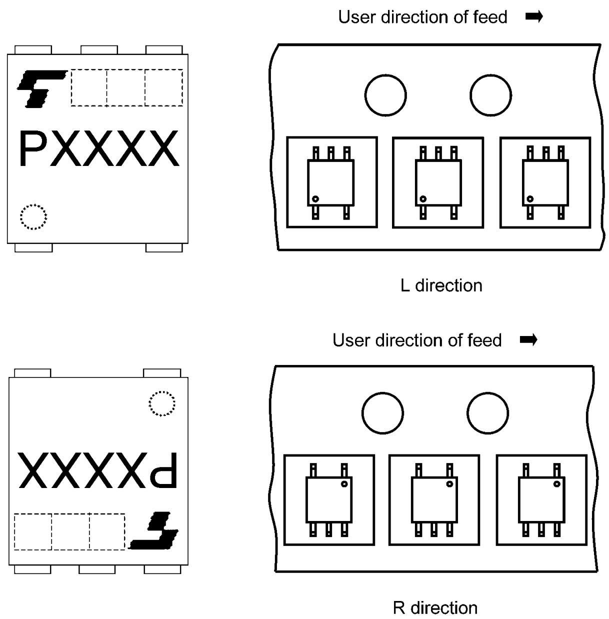
Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

16.3. Tape Dimensions Specification

Tape Type	Division	Packing Amount (A unit per reel)
TPL	L direction	3000
TPR	R direction	3000

16.3.1. Orientation of Device in Relation to Direction of Feed

Device orientation in the carrier cavities as shown in the following figure.



Device Orientation

16.3.2. Empty Cavities

Characteristics	Criterion	Remarks
Occurrences of 2 or more successive empty cavities	0 device	Within any given 40-mm section of tape, not including leader and trailer
Single empty cavity	6 devices (max) per reel	Not including leader and trailer

16.3.3. Tape Leader and Trailer

The start of the tape has 14 or more empty holes. The end of the tape has 34 or more empty holes and a cover tape of 30 mm or longer.

16.3.4. Tape Dimensions

Tape material: Plastic (for protection against static electricity)

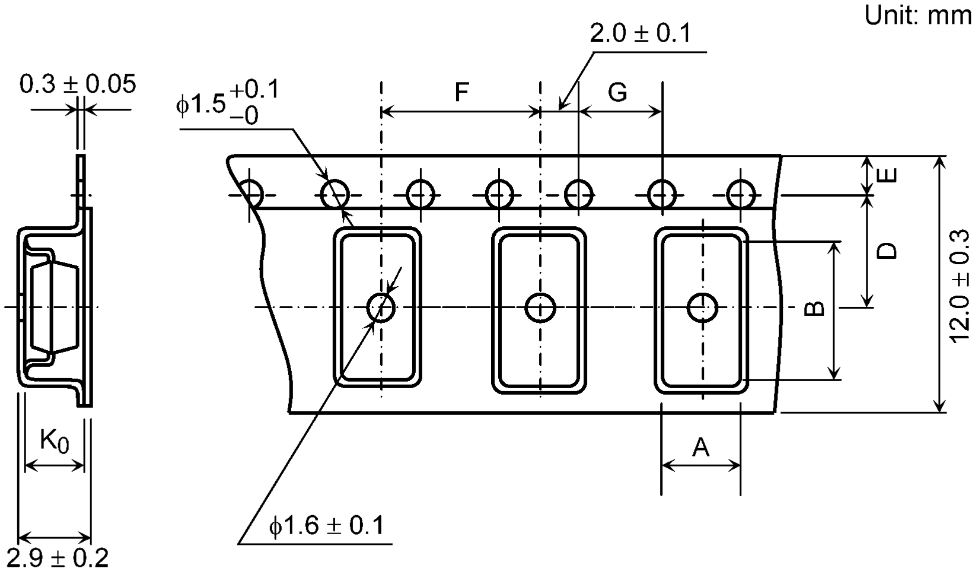


Table Tape Dimensions (unit: mm, tolerance: ±0.1)

Symbol	Dimension	Remark
A	4.0	—
B	7.6	—
D	5.5	Center line of embossed cavity and sprocket hole
E	1.75	Distance between tape edge and sprocket hole center
F	8.0	Cumulative error +0.1/-0.3 (max) per 10 empty cavities holes
G	4.0	Cumulative error +0.1/-0.3 (max) per 10 sprocket holes
K_0	2.6	Internal space

16.3.5. Reel Specification

Material: Plastic (for protection against static electricity)

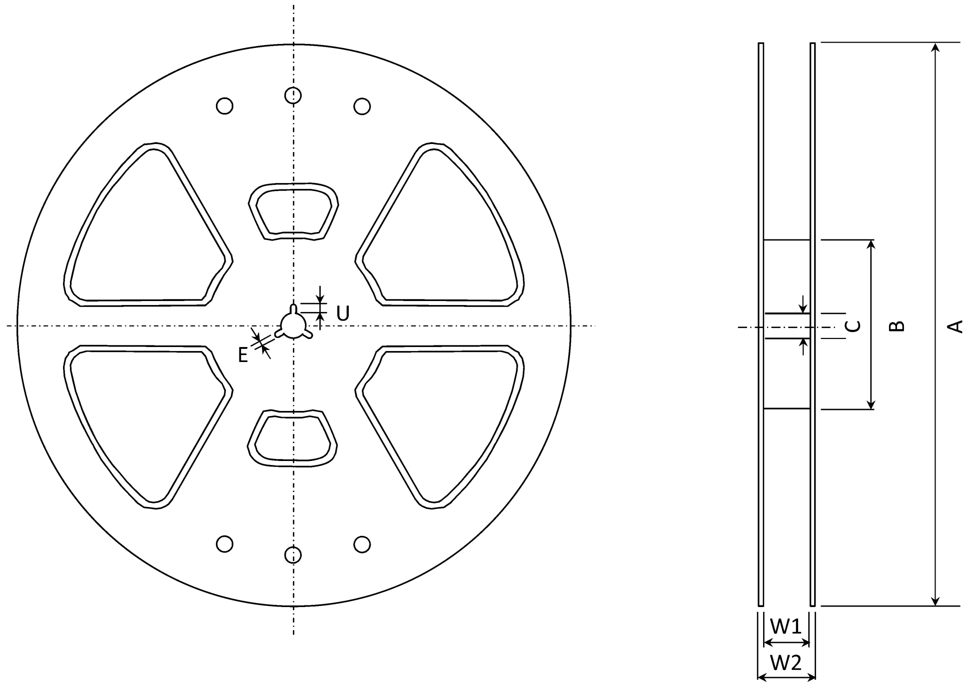
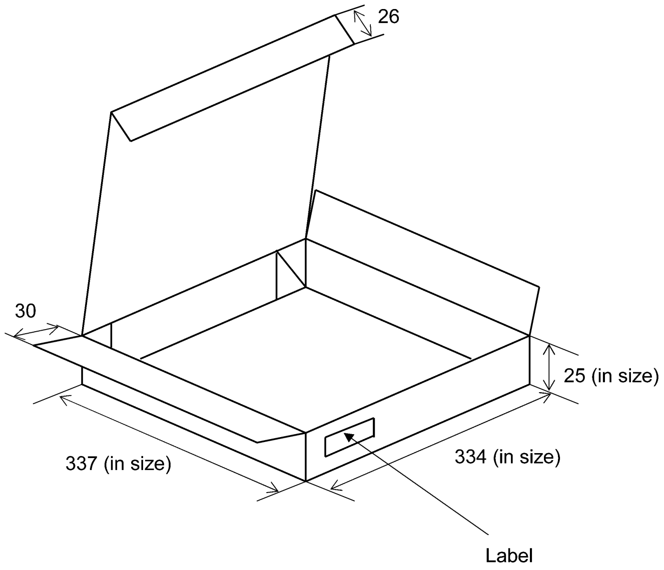


Table Reel Dimensions (unit: mm)

Symbol	Dimension
A	φ330 ± 2.0
B	φ80 ± 1.0
C	φ13 ± 0.5
E	2.0 ± 0.5
U	4.0 ± 0.5
W1	13.5 ± 0.5
W2	17.5 ± 1.0

16.3.6. Packing (Note)



1 reel/carton (unit: mm)

Note: Taping reel diameter: ϕ330 mm

16.3.7. Label Format

(1) Carton: The label provides the part number, quantity, lot number, the Toshiba logo, etc.

(2) Reel: The label provides the part number, the taping name, quantity, lot number, etc.

16.4. Ordering Information

When placing an order, please specify the part number, tape type and quantity as shown in the following example.

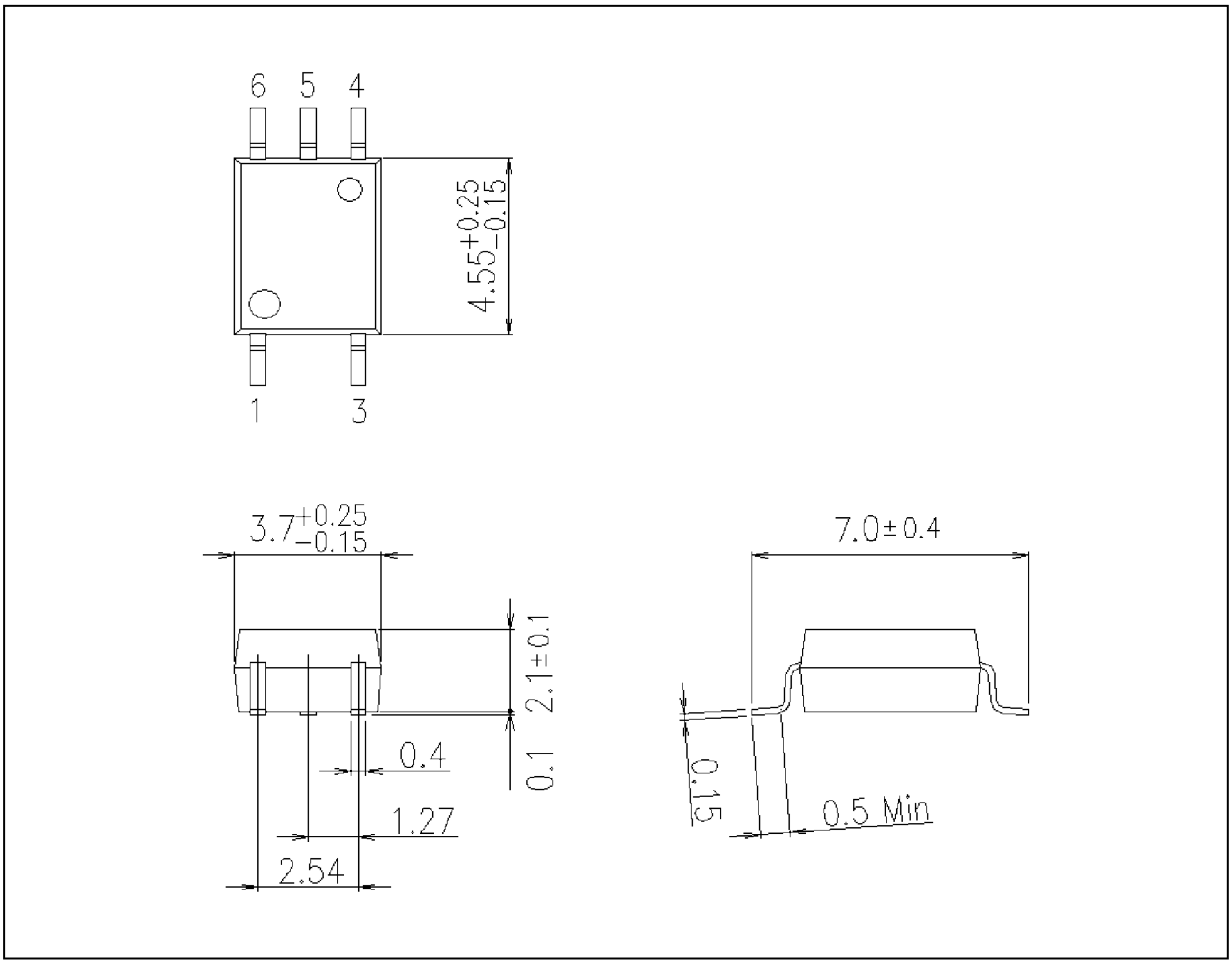
Example) TLP152(TPL,E(T 3000 pcs

Part number: TLP152
Tape type: TPL (8-mm pitch)
[[G]]/RoHS COMPATIBLE: E **(Note 1)**
Domestic ID (Country/Region of origin: Thailand): T
Quantity (must be a multiple of 3000): 3000 pcs

Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Package Dimensions

Unit: mm



Weight: 0.08 g (typ.)

Package Name(s)
TOSHIBA: 11-4L1S

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