

# TPC8408

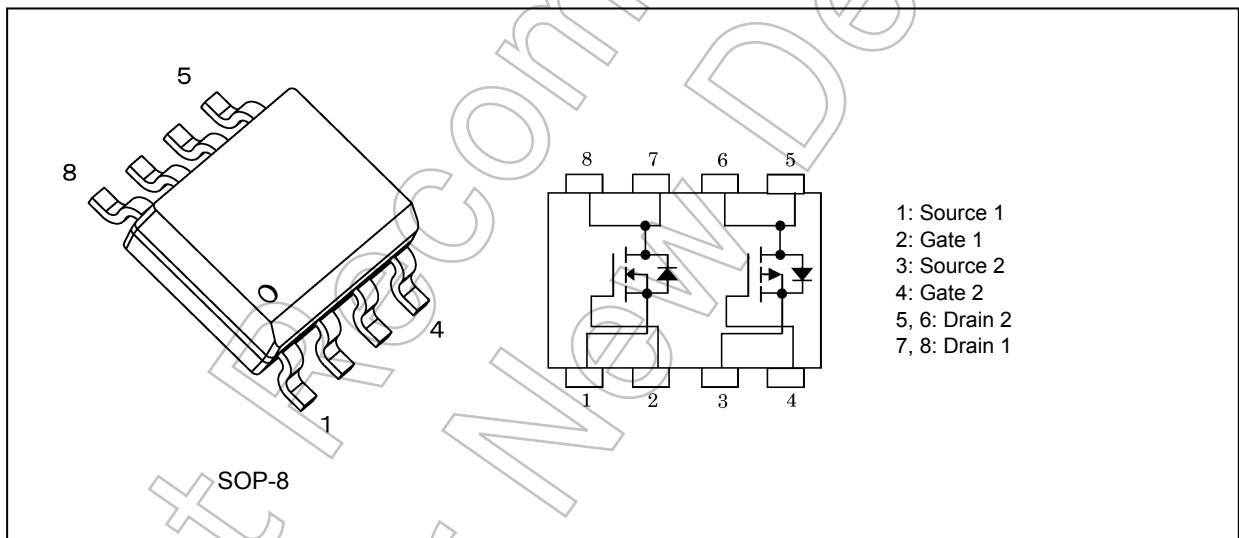
## 1. Applications

- Mobile Equipments
- Motor Drivers

## 2. Features

- (1) Small footprint due to a small and thin package
- (2) High speed switching
- (3) Low drain-source on-resistance  
 P-channel  $R_{DS(ON)} = 33 \text{ m}\Omega$  (typ.) ( $V_{GS} = -10 \text{ V}$ ),  
 N-channel  $R_{DS(ON)} = 24 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (4) Low leakage current  
 P-channel  $I_{DSS} = -10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = -40 \text{ V}$ ),  
 N-channel  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 40 \text{ V}$ )
- (5) Enhancement mode  
 P-channel  $V_{th} = -0.8 \text{ to } -2.0 \text{ V}$  ( $V_{DS} = -10 \text{ V}$ ,  $I_D = -0.1 \text{ mA}$ ),  
 N-channel  $V_{th} = 1.3 \text{ to } 2.3 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.1 \text{ mA}$ )

## 3. Packaging and Internal Circuit



Start of commercial production

2011-04

**4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	P/N	Symbol	Rating	Unit
Drain-source voltage	P-ch	$V_{DSS}$	-40	V
	N-ch		40	
Gate-source voltage	P-ch	$V_{GSS}$	$\pm 20$	
	N-ch		$\pm 20$	
Drain current (DC) (Note 1)	P-ch	$I_D$	-5.3	A
	N-ch		6.1	
Drain current (pulsed) (Note 1)	P-ch	$I_{DP}$	-21.2	A
	N-ch		24.4	
Power dissipation (single operation) (t = 10 s) (Note 2), (Note 4)	P-ch	$P_{D(1)}$	1.5	W
	N-ch		1.5	
Power dissipation (per device for dual operation) (t = 10 s) (Note 2), (Note 5)	P-ch	$P_{D(2)}$	1.1	W
	N-ch		1.1	
Power dissipation (single operation) (t = 10 s) (Note 3), (Note 4)	P-ch	$P_{D(1)}$	0.75	W
	N-ch		0.75	
Power dissipation (per device for dual operation) (t = 10 s) (Note 3), (Note 5)	P-ch	$P_{D(2)}$	0.45	W
	N-ch		0.45	
Single-pulse avalanche energy (Note 6)	P-ch	$E_{AS}$	18	mJ
	N-ch		24	
Avalanche current	P-ch	$I_{AR}$	-5.3	A
	N-ch		6.1	
Channel temperature	P-ch	$T_{ch}$	150	$^\circ\text{C}$
	N-ch		150	
Storage temperature	P-ch	$T_{stg}$	-55 to 150	$^\circ\text{C}$
	N-ch		-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**5. Thermal Characteristics**

Characteristics	Symbol	Max	Unit
Channel-to-ambient thermal resistance (single operation) (t = 10 s) (Note 2), (Note 4)	$R_{th(ch-a)(1)}$	83.3	°C/W
Channel-to-ambient thermal resistance (per device for dual operation) (t = 10 s) (Note 2), (Note 5)	$R_{th(ch-a)(2)}$	113	
Channel-to-ambient thermal resistance (single operation) (t = 10 s) (Note 3), (Note 4)	$R_{th(ch-a)(1)}$	166	
Channel-to-ambient thermal resistance (per device for dual operation) (t = 10 s) (Note 3), (Note 5)	$R_{th(ch-a)(2)}$	277	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1

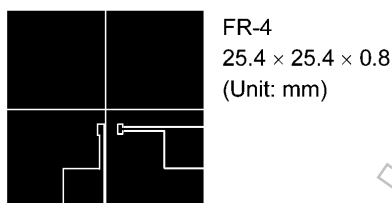
Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 4: Power dissipation and thermal resistance values per device with the other device being off (During single operation, power is supplied to only one of the two devices.)

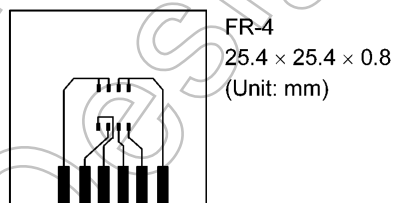
Note 5: Power dissipation and thermal resistance values per device for dual operation (During dual operation, power is evenly supplied to both devices.)

Note 6: P channel:  $V_{DD} = -32\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 0.5\text{ mH}$ ,  $R_G = 25\ \Omega$ ,  $I_{AR} = -5.3\text{ A}$

N channel:  $V_{DD} = 32\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 0.5\text{ mH}$ ,  $R_G = 25\ \Omega$ ,  $I_{AR} = 6.1\text{ A}$



**Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)**



**Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)**

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

**6. Electrical Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

**6.1. Static Characteristics**

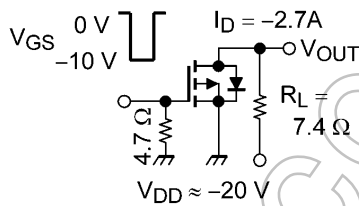
Characteristics	P/N	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	P-ch	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 0.1$	$\mu\text{A}$
	N-ch		$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 0.1$	
Drain cut-off current	P-ch	$I_{DSS}$	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$	—	—	-10	$\mu\text{A}$
	N-ch		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	P-ch	$V_{(BR)DSS}$	$I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$	-40	—	—	V
	N-ch		$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	40	—	—	
Drain-source breakdown voltage (Note 7)	P-ch	$V_{(BR)DSX}$	$I_D = -10\text{ mA}, V_{GS} = 10\text{ V}$	-30	—	—	V
	N-ch		$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	23	—	—	
Gate threshold voltage	P-ch	$V_{th}$	$V_{DS} = -10\text{ V}, I_D = -0.1\text{ mA}$	-0.8	—	-2.0	V
	N-ch		$V_{DS} = 10\text{ V}, I_D = 0.1\text{ mA}$	1.3	—	2.3	
Drain-source on-resistance	P-ch	$R_{DS(ON)}$	$V_{GS} = -4.5\text{ V}, I_D = -2.7\text{ A}$	—	41	53	$\text{m}\Omega$
			$V_{GS} = -10\text{ V}, I_D = -2.7\text{ A}$	—	33	43	
	N-ch		$V_{GS} = 4.5\text{ V}, I_D = 3.1\text{ A}$	—	28	36	
			$V_{GS} = 10\text{ V}, I_D = 3.1\text{ A}$	—	24	32	

Note 7: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Not Recommended for New Design

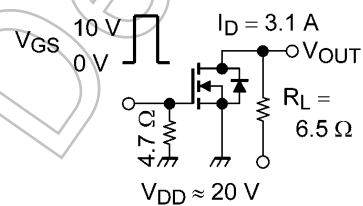
**6.2. Dynamic Characteristics**

Characteristics	P/N	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	P-ch	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	1105	—	pF
	N-ch		$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	850	—	
Reverse transfer capacitance	P-ch	$C_{rss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	135	—	pF
	N-ch		$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	40	—	
Output capacitance	P-ch	$C_{oss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	165	—	pF
	N-ch		$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	145	—	
Switching time (rise time)	P-ch	$t_r$	See Figure 6.2.1.	—	8.1	—	ns
	N-ch		See Figure 6.2.2.	—	2.0	—	
Switching time (turn-on time)	P-ch	$t_{on}$	See Figure 6.2.1.	—	16	—	ns
	N-ch		See Figure 6.2.2.	—	7.0	—	
Switching time (fall time)	P-ch	$t_f$	See Figure 6.2.1.	—	33	—	ns
	N-ch		See Figure 6.2.2.	—	2.3	—	
Switching time (turn-off time)	P-ch	$t_{off}$	See Figure 6.2.1.	—	131	—	ns
	N-ch		See Figure 6.2.2.	—	17	—	



Duty ≤ 1%,  $t_w = 10\ \mu\text{s}$

**Fig. 6.2.1 Switching Time Test Circuit (P-ch)**



Duty ≤ 1%,  $t_w = 10\ \mu\text{s}$

**Fig. 6.2.2 Switching Time Test Circuit (N-ch)**

**6.3. Gate Charge Characteristics**

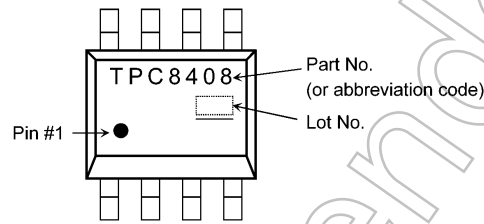
Characteristics	P/N	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	P-ch	$Q_g$	$V_{DD} \approx -32\text{ V}, V_{GS} = -10\text{ V},$ $I_D = -5.3\text{ A}$	—	24	—	nC
	N-ch		$V_{DD} \approx 32\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 6.1\text{ A}$	—	14	—	
Gate-source charge 1	P-ch	$Q_{gs1}$	$V_{DD} \approx -32\text{ V}, V_{GS} = -10\text{ V},$ $I_D = -5.3\text{ A}$	—	3.0	—	nC
	N-ch		$V_{DD} \approx 32\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 6.1\text{ A}$	—	2.6	—	
Gate-drain charge	P-ch	$Q_{gd}$	$V_{DD} \approx -32\text{ V}, V_{GS} = -10\text{ V},$ $I_D = -5.3\text{ A}$	—	5.3	—	nC
	N-ch		$V_{DD} \approx 32\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 6.1\text{ A}$	—	2.4	—	

**6.4. Source-Drain Characteristics**

Characteristics	P/N	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 8)	P-ch	$I_{DRP}$	—	—	—	-21.2	A
	N-ch			—	—	24.4	
Diode forward voltage	P-ch	$V_{DSF}$	$I_{DR} = -5.3 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	1.2	V
	N-ch		$I_{DR} = 6.1 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.2	

Note 8: Ensure that the channel temperature does not exceed 150°C.

**7. Marking (Note)**



**Fig. 7.1 Marking**

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined:  $[[Pb]]/INCLUDES > MCV$

Underlined:  $[[G]]/RoHS \text{ COMPATIBLE}$  or  $[[G]]/RoHS [[Pb]]$

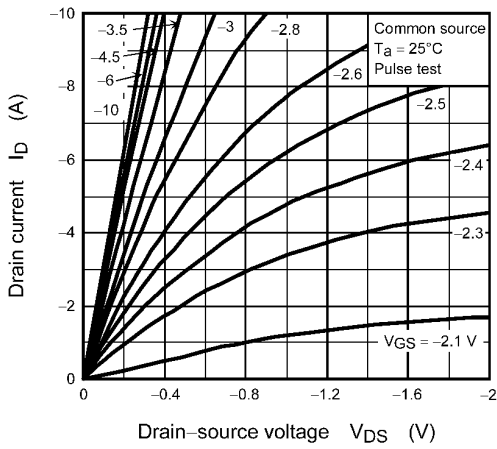
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

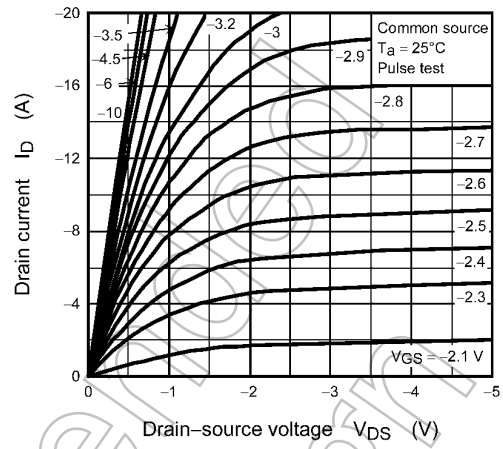
Not Recommended for New Design

**8. Characteristics Curves (Note)**

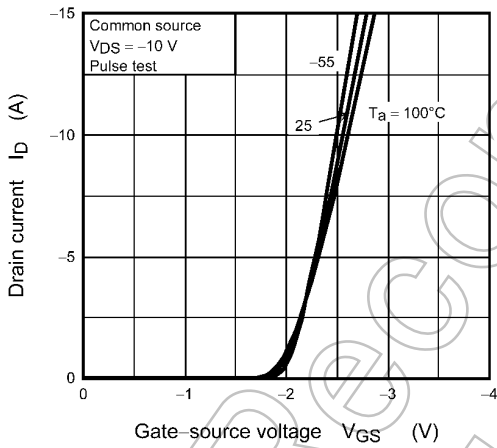
**8.1. P-Channel MOSFET**



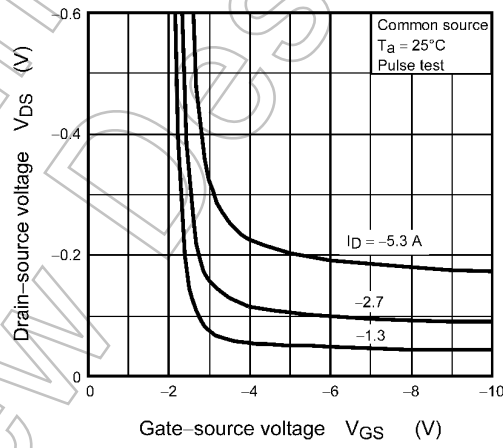
**Fig. 8.1.1 ID - VDS**



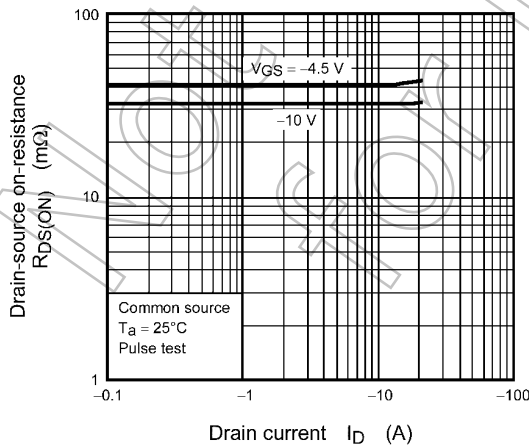
**Fig. 8.1.2 ID - VDS**



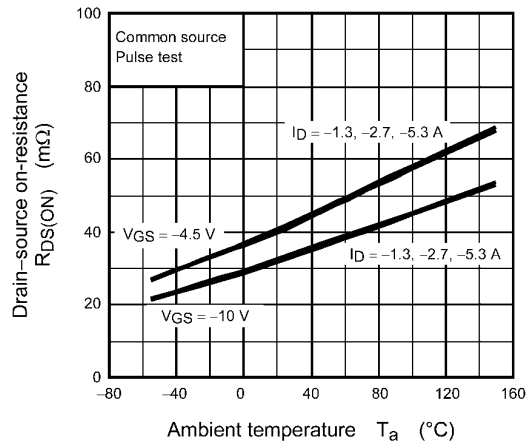
**Fig. 8.1.3 ID - VGS**



**Fig. 8.1.4 VDS - VGS**



**Fig. 8.1.5 RDS(ON) - ID**



**Fig. 8.1.6 RDS(ON) - Ta**

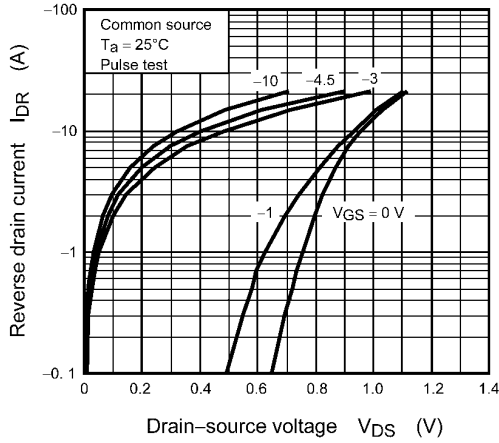


Fig. 8.1.7  $I_{DR} - V_{DS}$

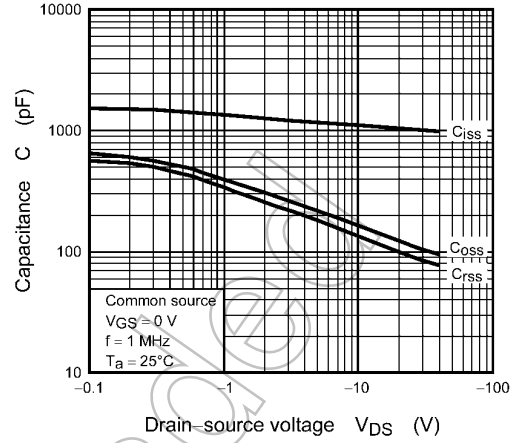


Fig. 8.1.8 Capacitance -  $V_{DS}$

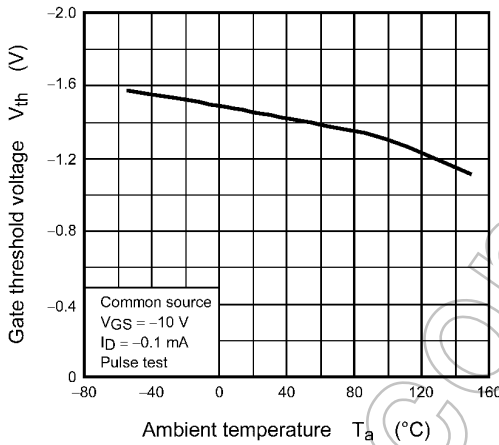


Fig. 8.1.9  $V_{th} - T_a$

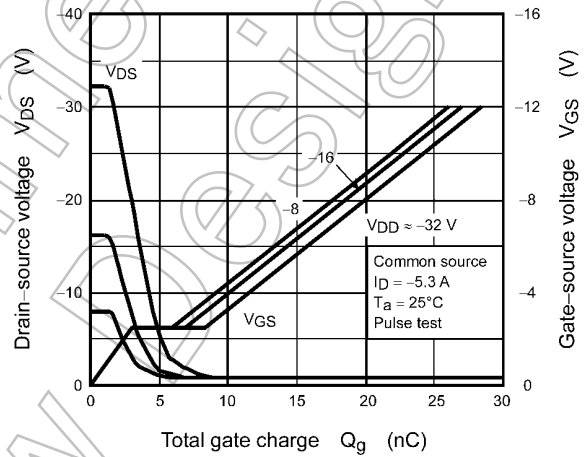


Fig. 8.1.10 Dynamic Input/Output Characteristics

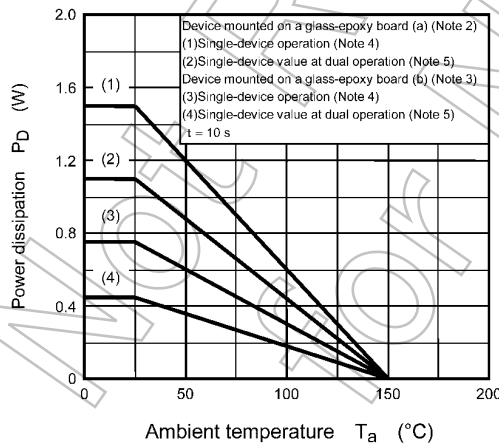
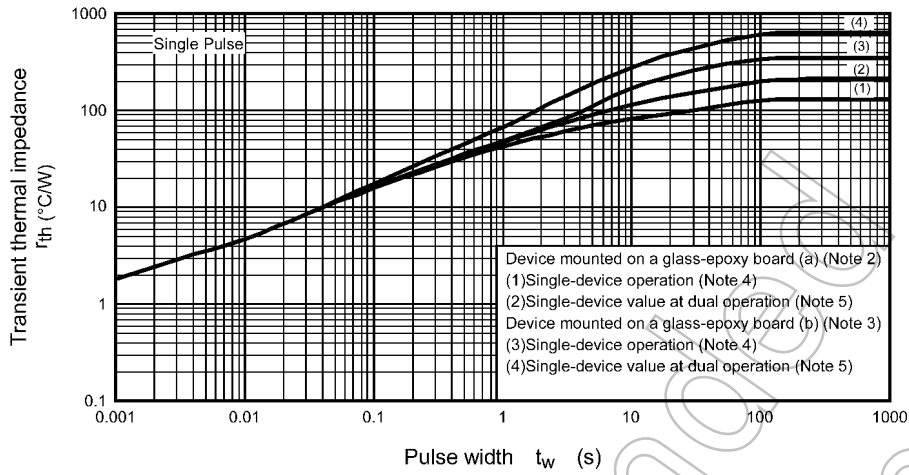
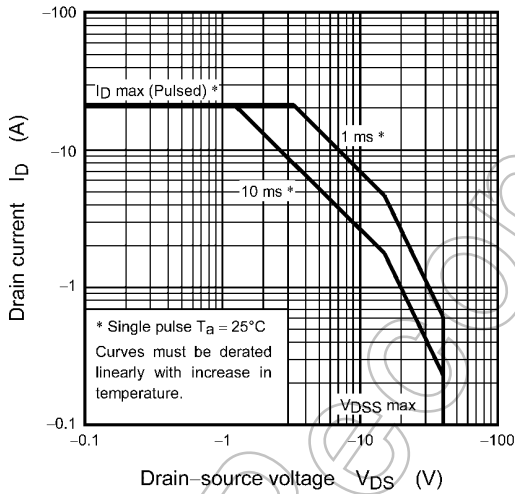


Fig. 8.1.11  $P_D - T_a$   
(Guaranteed Maximum)



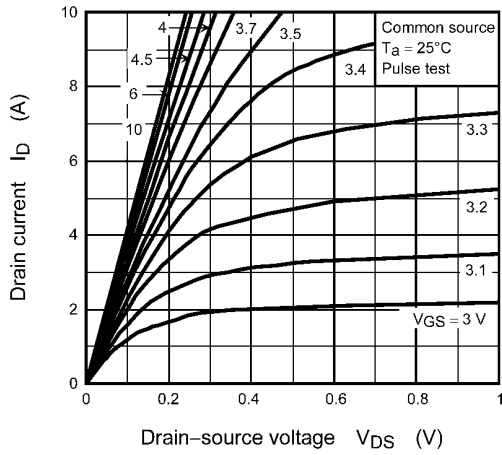


**Fig. 8.1.12  $r_{th} - t_w$**   
**(Guaranteed Maximum)**

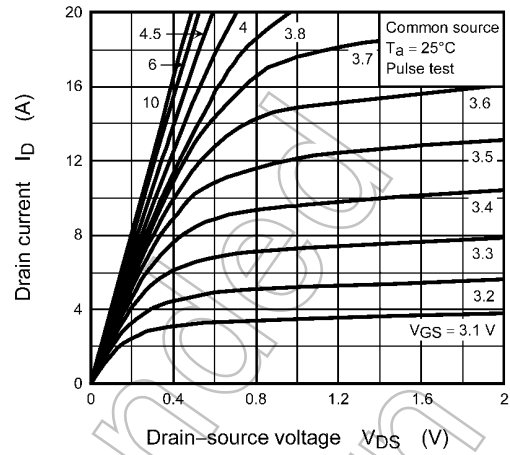


**Fig. 8.1.13 Safe Operating Area**  
**(Guaranteed Maximum)**

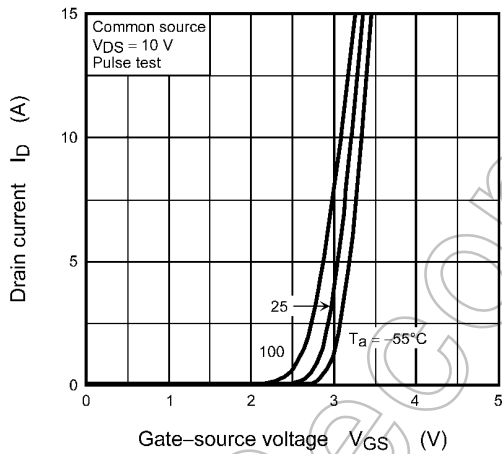
**8.2. N-Channel MOSFET**



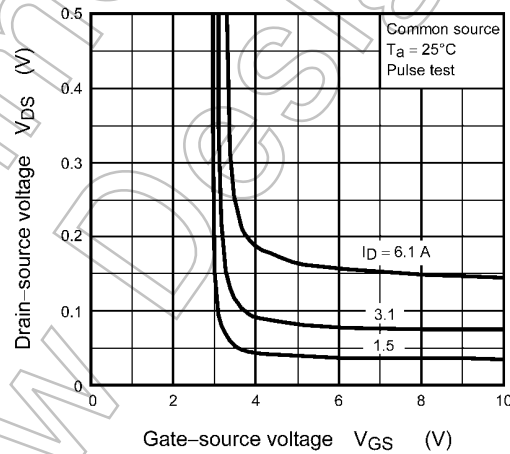
**Fig. 8.2.1  $I_D - V_{DS}$**



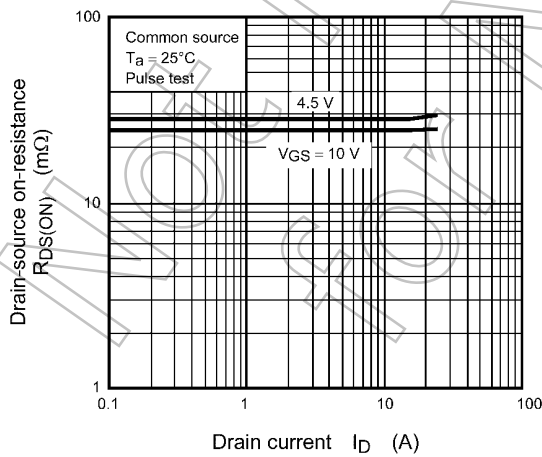
**Fig. 8.2.2  $I_D - V_{DS}$**



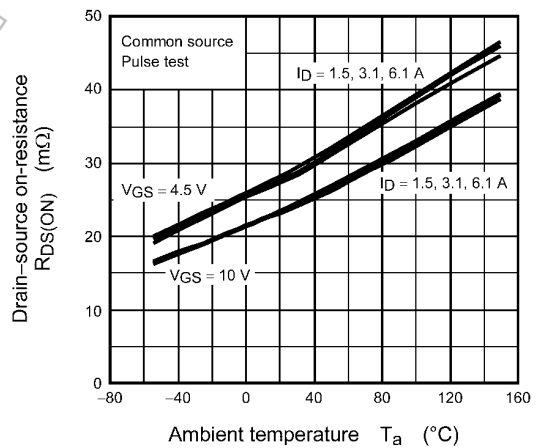
**Fig. 8.2.3  $I_D - V_{GS}$**



**Fig. 8.2.4  $V_{DS} - V_{GS}$**



**Fig. 8.2.5  $R_{DS(ON)} - I_D$**



**Fig. 8.2.6  $R_{DS(ON)} - T_a$**

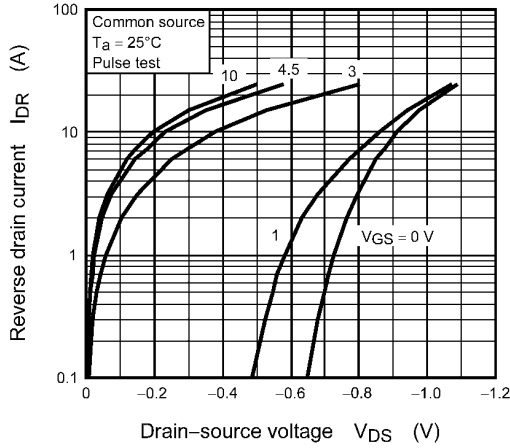


Fig. 8.2.7  $I_{DR} - V_{DS}$

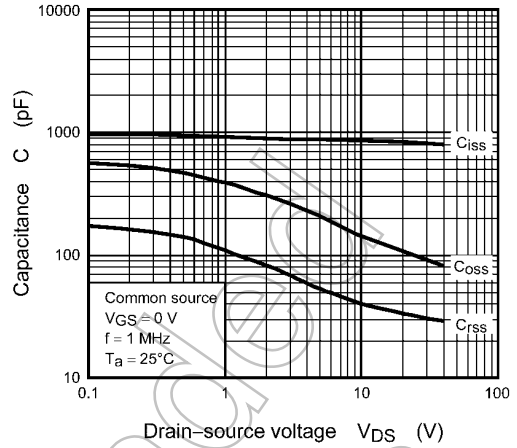


Fig. 8.2.8 Capacitance -  $V_{DS}$

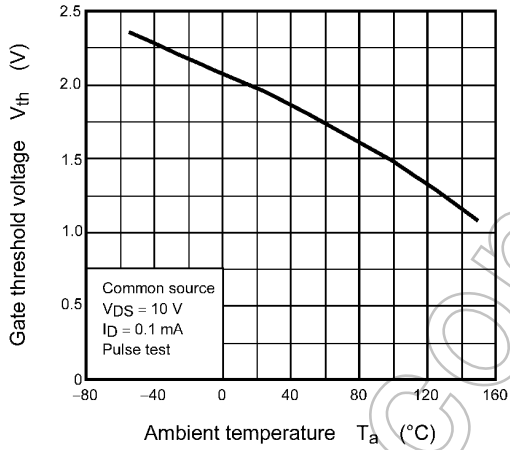


Fig. 8.2.9  $V_{th} - T_a$

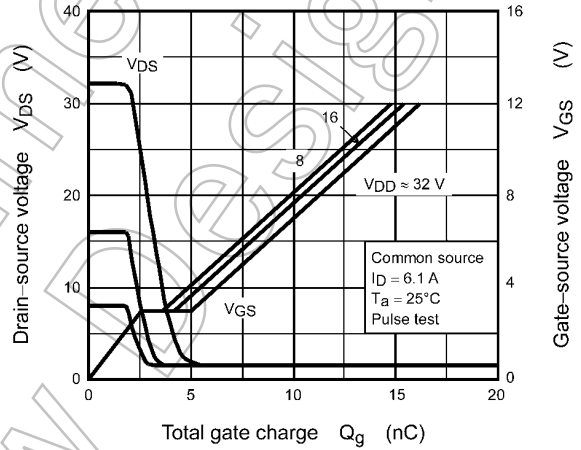


Fig. 8.2.10 Dynamic Input/Output Characteristics

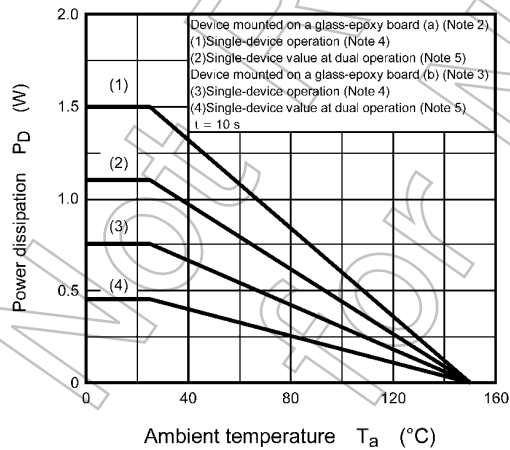


Fig. 8.2.11  $P_D - T_a$   
(Guaranteed Maximum)

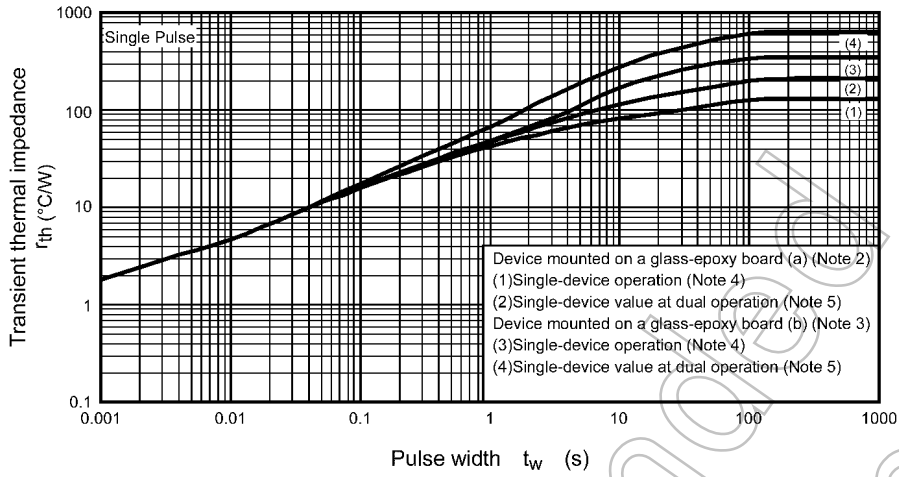


Fig. 8.2.12  $r_{th} - t_w$   
(Guaranteed Maximum)

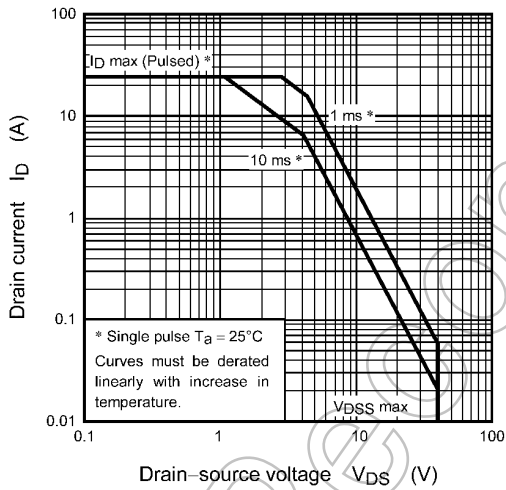
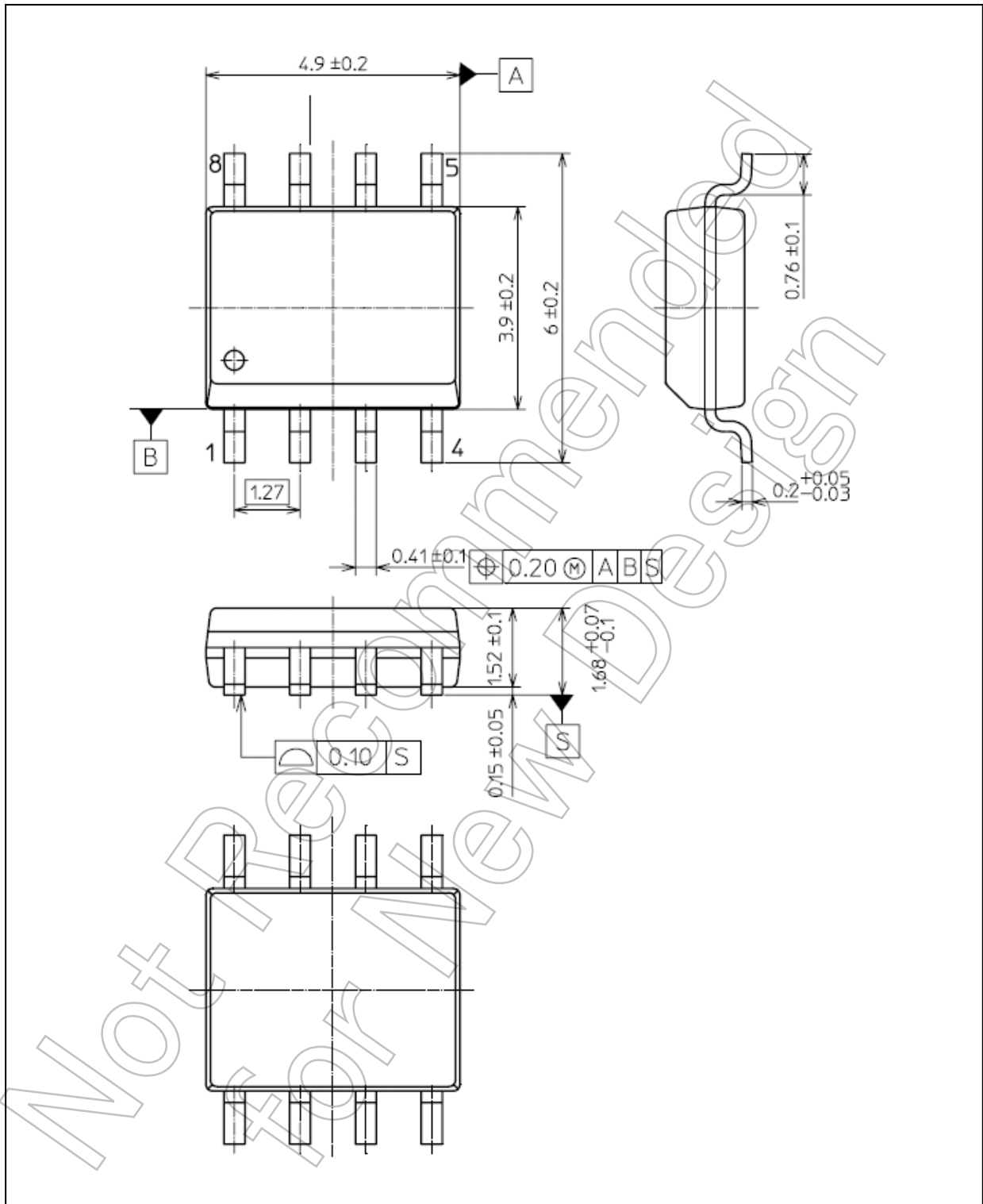


Fig. 8.2.13 Safe Operating Area  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.085 g (typ.)

Package Name(s)
TOSHIBA: 2-5R1S
Nickname: SOP-8

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