32-bit RISC Microcontroller

TXZ/TXZ+ Family

Reference Manual
Digital Noise Filter Circuit
(DNF-A)

Revision 2.1

2020-08

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

DNF	Digital Noise Filter Circuit
fc	Either selected high speed clock fosc or f_{PLL}
fosc	Clock generated by the high speed oscillator
f_{PLL}	Clock generated by the frequency multiplier

1. Outlines

The digital noise filter circuit can remove the noise of a predetermined width from the external interrupt pin input.

2. Configuration

The digital noise filter circuit consists of a clock control circuit, noise removal circuits and interrupt request selectors.

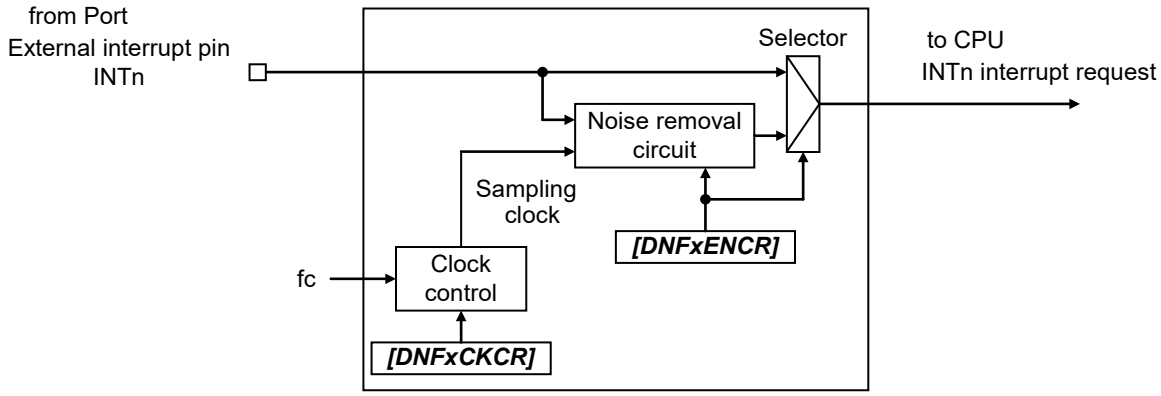

Figure 2.1 The digital noise filter circuit block diagram

Table 2.1 List of Signals

No	Signal name		I/O	Reference manual
1	fc	High speed clock	Input	Clock Control and Operation Mode
2	INTn	External interrupt pin(from Port)	Input	Product Information
3	INTn	Interrupt request signal(to CPU)	Output	Exception

3. Function and Operation

3.1. Clock Supply

When DNF is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB])***, fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***).

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to "Clock Control and Operation Mode" in Reference manual.

3.2. Operation

Both high and low level noises on the external interrupt signal INTn are removed.

The sampling clock is set in the ***[DNFxCKCR]***<NFCKS>. If the continuous period of the same level input is 7-clock long or less, input signal is determined as the noise. If the continuous period is 8-clock long or more, input signal is determined valid signal. In addition, the pulse whose width is between 7-clock long and 8-clock long is determined as either a noise or a valid signal. The digital noise filter circuit is enabled by setting the enable bit (<NFENn>) according to the external interrupt of ***[DNFxENCR]*** register (Note 1).

After the digital noise filter circuit removes the noise for the input signal (INTn) received from the external, each interrupt is detected on the rising edge, the falling edge or the level according to the setting of the interrupt control register (Note 2).

Note1: Before the external interrupt is enabled, the interrupt sources should be cleared and the digital noise filter circuit should be set to enable. For the external interrupt corresponding to each bit of ***[DNFxENCR]***, refer to "Product Information" of the reference manual.

Note2: Refer to "Exception" of the reference manual

3.3. Noise Removal Time

When the input signal keeps High or Low level for the period of 7-clock long or less, the noise removal circuit determine the input signal as the noise.

Table 3.1 Noise removal time (1)

[DNFxCKCR]<NFCKS>	fc [MHz]				Unit
	20	40	80	100	
001	0.7	0.35	0.175	0.14	μs
010	1.4	0.7	0.35	0.28	
011	2.8	1.4	0.7	0.56	
100	5.6	2.8	1.4	1.12	
101	11.2	5.6	2.8	2.24	
110	22.4	11.2	5.6	4.48	
111	44.8	22.4	11.2	8.96	

Note: Noises may not be removed from the pulses whose frequency is higher than the fc. Especially, it may occur when the fc frequency is low.

Table 3.2 Noise removal time (2)

[DNFxCKCR]<NFCKS>	fc [MHz]			Unit
	120	160	200	
001	0.116	0.0875	0.07	μs
010	0.233	0.175	0.14	
011	0.466	0.35	0.28	
100	0.933	0.7	0.56	
101	1.866	1.4	1.12	
110	3.733	2.8	2.24	
111	7.466	5.6	4.48	

Note: Noises may not be removed from the pulses whose frequency is higher than the fc. Especially, it may occur when the fc frequency is low.

3.4. Setting for Using STOP1/STOP2 Mode

When STOP1/STOP2 mode is used, the digital noise filter circuit is not available because the fc clock stops. If an external interrupt is used to release the STOP1/STOP2 mode, the following should be done. The interrupt enable bit should be disabled. And the noise filter enable bit in the ***[DNFxENCR]*** register should be disabled. Then the noise filter clock should be stopped by the setting of the ***[DNFxCKCR]*** register.

4. Registers

4.1. List of Registers

The control registers and their addresses are shown as follows.

Function name		Channel/Unit	Base address		
			TYPE1	TYPE2	TYPE3
Digital Noise Filter Circuit	DNF	A	0x400BB600	0x400A0200	0x40040200
		B	0x400BB700	0x400A0300	0x40040300
		C	0x400BE000	0x400A0800	-

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Address (Base+)
Noise Filter Control Register	***[DNFxCKCR]***	0x0000
Noise Filter Enable Register	***[DNFxENCR]***	0x0004

4.2. Details of Registers

4.2.1. *[DNFxCKCR]* (Noise Filter Control Register)

Bit	Bit Symbol	After Reset	Type	Function
31:3	-	0	R	Read as "0".
2:0	NFCKS[2:0]	000	R/W	Noise filter clock selection 000: Clock control circuit stop 001: fc/2 clock output 010: fc/4 clock output 011: fc/8 clock output 100: fc/16 clock output 101: fc/32 clock output 110: fc/64 clock output 111: fc/128 clock output

Note1: When ***[DNFxCKCR]***<NFCKS> is set, ***[DNFxENCR]***<NFENn>(n=0 to 15) should be all "0".

Note2: If the external interrupt pin is used to release the STOP1/STOP2 mode, the noise filter cannot be used. The noise filter enable bit in the ***[DNFxENCR]*** register should be disabled, and the ***[DNFxCKCR]*** register should stop the clock.

4.2.2. *[DNFxENCR]* (Noise Filter Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:16	-	0	R	Read as "0".
15	NFEN15	0	R/W	INTn noise filter enable(15) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
14	NFEN14	0	R/W	INTn noise filter enable(14): 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
13	NFEN13	0	R/W	INTn noise filter enable(13): 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
12	NFEN12	0	R/W	INTn noise filter enable(12): 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
11	NFEN11	0	R/W	INTn noise filter enable(11) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
10	NFEN10	0	R/W	INTn noise filter enable(10) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
9	NFEN9	0	R/W	INTn noise filter enable(9) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
8	NFEN8	0	R/W	INTn noise filter enable(8) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
7	NFEN7	0	R/W	INTn noise filter enable(7) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
6	NFEN6	0	R/W	INTn noise filter enable(6) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)

Bit	Bit Symbol	After Reset	Type	Function
5	NFEN5	0	R/W	INTn noise filter enable(5) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
4	NFEN4	0	R/W	INTn noise filter enable(4) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
3	NFEN3	0	R/W	INTn noise filter enable(3) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
2	NFEN2	0	R/W	INTn noise filter enable(2) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
1	NFEN1	0	R/W	INTn noise filter enable(1) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)
0	NFEN0	0	R/W	INTn noise filter enable(0) 0: Disabled (Output of the signal before the noise removal) 1: Enabled (Output of the signal after the noise removal)

Note: If the external interrupt is used to release the STOP1/STOP2 mode, the digital noise filter circuit is not available. The noise filter enable bit in the ***[DNFxENCR]*** register should be set to disable and the clock is stopped by the ***[DNFxCKCR]*** register.

5. Revision History

Table 5.1 Revision History

Revision	Date	Description
1.0	2017-09-07	First release
2.0	2018-03-27	- Added chapter "3.1.Clock Supply" - 3.4.Precaution for Using STOP Mode Title: Setting for Using STOP1/STOP2 Mode STOP(STOP1,STOP2)→STOP1/STOP2 - 4.1.List of Registers Added TYPE3 - 4.2.1 *[DNFxCKCR]* After RSET: 0→000
2.1	2020-08-31	- Revised Header&Footer (added New Family):Top Page - Revised chapter "3.1.Clock Supply" - Added table 3.2 - Revised chapter "3.4.Setting for Using STOP1/STOP2 Mode" - 4.1.List of Registers Added base address of Unit C/TYPE1

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