TOSHIBA

High-Frequency Semiconductors Power Devices

TOSHIBA CORPORATION
Semiconductor Company

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Preface

Thank you for choosing Toshiba semiconductor products. This is the year 2004 edition of the databook entitled High-Frequency Semiconductor Devices – Power Devices.

From this edition, the High-Frequency Semiconductor Devices is published in separate volumes: High-Frequency Semiconductor Devices – Diodes, High-Frequency Semiconductor Devices – Transistors, FETs and Cell Packs, and High-Frequency Semiconductor Devices – Power Devices. Please select the suitable databook for your application.

This databook is designed to be easily understood by engineers who are designing Toshiba high-frequency small-signal devices into their products for the first time. No special knowledge of these devices is assumed - the contents includes basic information about the high-frequency small-signal devices and the application fields in which they are used. In addition, complete technical specifications facilitate selection of the most appropriate high-frequency small-signal device for any given application.

Toshiba are continually updating technical publications. Any comments and suggestions regarding any Toshiba document are most welcome and will be taken into account when subsequent editions are prepared. To receive updates to the information in this databook, or for additional information about the products described in it, please contact your nearest Toshiba office or authorized Toshiba dealer.

March 2004

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[1] Part Number Index

[2] Main Characteristics

[2] Main Characteristics

1. Main Characteristics of High-Frequency Power Transistors

Application	Part Number	Maximum Ratings (T_C = 25°C)			P_O (W)			
						Test Conditions		
		V_{CBO} (V)	P_C (T_C = 25°C) (W)	I_C (A)	Min	V_{CC} (V)	f (MHz)	P_i (W)
27 to 50 MHz CB radio transmitter HAM radio transmitter	2SC2290	45	175	20	60PEP	12.5	28	4PEP
	2SC2879	45	250	25	80PEP	12.5	28	8PEP
	2SC2510	60	250	20	150PEP	28	28	9PEP
175 MHz Marine radio transmitter HAM radio transmitter Business-use radio transmitter	2SC2782	36	220	20	80	12.5	175	18

2. Main Characteristics of High-Frequency Power MOSFETs

Application		Part Number	Maximum Ratings (T_C = 25°C)			P_O			
							Test Conditions		
			V_{DSS} (V)	P_C (T_C = 25°C) (W)	I_D (A)	Min	V_{DD} (V)	f (MHz)	P_i
For TV broadcasting	VHF	2SK1310A	100	250	12	190 W	50	230	10 W
	UHF	2SK1739A	80	250	11	90 W	40	770	10 W
For cellular phone		2SK2854	10	0.5	0.5	0.2 W	6	849	0.02 W
		2SK2855	10	0.5	1	1.26 W	6	849	0.2 W
For radio transmitter		2SK3074	30	3	1	0.63 W	9.6	520	0.02 W
		2SK3075	30	20	5	7.5 W	9.6	520	0.5 W
For cellular phone		2SK3077	10	0.1	0.1	15.0dBmW	4.8	915	0dBmW
For radio transmitter		2SK3475	20	3	1	0.63 W	7.2	520	0.02 W
		2SK3476	20	20	3	7 W	7.2	520	0.5 W
For FRS/GMRS		2SK3078A	10	3	0.5	0.63 W	4.5	470	0.1 W
		2SK3079A	10	20	3	2.24 W	4.5	470	0.1 W
		2SK3656	7.5	3	0.5	0.5 W	3.6	470	0.02 W
		2SK3756	7.5	3	1	1.25 W	4.5	470	0.1 W

3. High-Frequency Power Module Product List by Part Number

Analog Application

Application		Part Number	Frequency Range	Characteristics			Test Conditions		Package Dimensions
			f	P_O	η_T	ρ_i	P_i	V_{CC}	
			(MHz)	(W)	(%)	(—)	(mW)	(V)	
VHF	50 W FM business-use radio transmitter	S-AV32	134~174	60	45	3	50	5/12.5	5-53P
	25 W FM business-use radio transmitter	S-AV33	134~174	32	45	3	50	5/12.5	5-53P
	25 W FM marine radio transmitter	S-AV35	154~162	32	50	3	10	5/12.5	5-32F
	65 W FM business-use radio transmitter	S-AV36	134~174	80	45	3	50	5/12.5	5-53P
UHF	5 W FM portable business-use radio transmitter	S-AU50L	400~430	7	40	3	50	4/9.6	5-23E
		S-AU50M	430~480	7	40	2.5	50	4/9.6	5-23E
		S-AU50H	470~520	6.5	40	4.5	50	4/9.6	5-23E
	5 W FM portable HAM radio transmitter	S-AU57	430~450	7	40	3	20	4/9.6	5-23E
	5 W FM portable business-use radio transmitter	S-AU68L	400~420	7	35	5	20	4/9.6	5-23E
		S-AU68M	450~470	7	40	2.5	20	4/9.6	5-23E
	50 W FM business-use radio transmitter	S-AU82VL	378~450	60	40	3	50	5/12.5	5-53P
		S-AU82L	400~470	60	40	3	50	5/12.5	5-53P
		S-AU82H	450~520	60	40	3	50	5/12.5	5-53P
	25 W FM business-use radio transmitter	S-AU83L	400~470	32	40	3	50	5/12.5	5-53P
		S-AU83H	450~520	32	40	3	50	5/12.5	5-53P
	2 W FM portable business-use radio transmitter	S-AU92	440~470	3	40	3	50	3.5/6	5-23E
	50 W FM business-use radio transmitter	S-AU93	430~500	60	40	3	50	5/12.5	5-53P

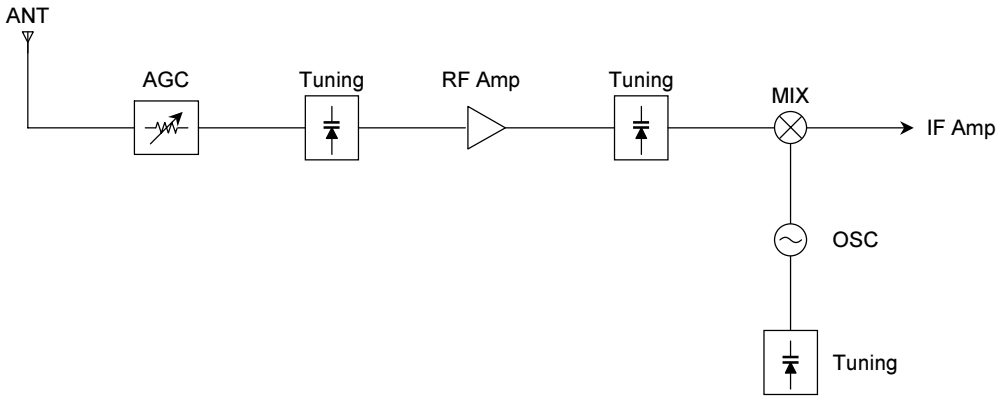
Digital Application

Application	Part Number	Frequency Range	Characteristics		Test Conditions		Package Dimensions
		f	P_O	ACP	V_{CC}	I_{CC}	
		(MHz)	(dBmW)	(dB)	(V)	(A)	
Business-use radio transmitter	S-AV34	150~165	39	−34	10.8	2.8	5-32G
Business-use radio transmitter (Japan Digital MCA)	S-AU86	889~915	35	−39	12	1.7	5-28C

[3] Block Diagrams for Suggested Applications

[3] Block Diagrams for Suggested Applications

1. High-Frequency Devices for AM Tuners



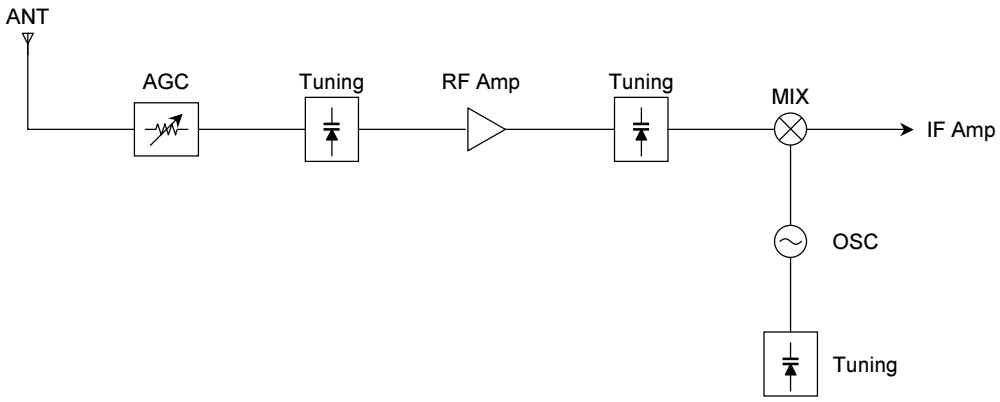
Application	Type		Package Type	Part Number
AGC	PIN Diode	Single	S-MINI	1SV128
			USC	1SV271 1SV307
			ESC	1SV308 JDP2S01E JDP2S04E
			TESC	JDP2S01T JDP2S02T
		Double	S-MINI	1SV172
			SMQ	1SV237
			USM	1SV252
			USQ	1SV312 JDP4P02U

Application	Type	Package Type	Part Number
Tuning	Tuning Varicap	MINI	1SV102 1SV149-B
		FM8	HN1V01H HN1V02H HN2V02H

Application	Type	Package Type	Part Number
MIX	Bipolar transistor	TO-92	2SC380TM 2SC941TM
		MINI	2SC2669 2SC2670
		S-MINI	2SC2715 2SC2716

Application	Type	Package Type	Part Number
AGC	Bipolar transistor	MINI	2SC2458
		S-MINI	2SC2712
RF Amp	J-FET	TO-92	2SK709
		MINI	2SK710
		S-MINI	2SK711
		USM	2SK1875
	Multi-chip-transistor	SMV	HN3G01J

2. High-Frequency Devices for FM Tuners



Application	Type		Package Type	Part Number
AGC	PIN Diode	Single	S-MINI	1SV128
			USC	1SV271 1SV307
			ESC	1SV308 JDP2S01E JDP2S04E
			TESC	JDP2S01T JDP2S02T
		Double	S-MINI	1SV172
			SMQ	1SV237
			USM	1SV252
			USQ	1SV312 JDP4P02U

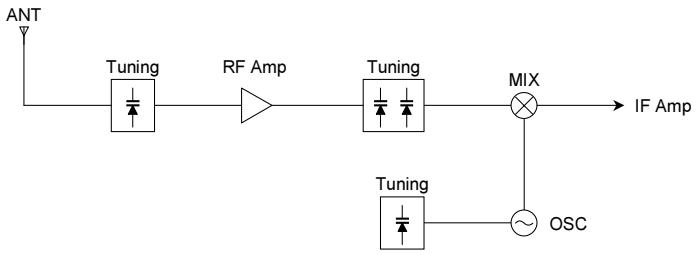
Application	Type		Package Type	Part Number
RF Amp	Dual Gate MOSFET		SMQ	3SK195
				3SK225 3SK226
			USQ	3SK257 3SK258
	Single Gate MOSFET		MINI	2SK241
			S-MINI	2SK302
			USM	2SK882
			SMQ	2SK1771
	Bipolar transistor		MINI	2SC2668
			S-MINI	2SC2714
			USM	2SC4215
	J-FET		MINI	2SK161 2SK192A
			S-MINI	2SK211 2SK210
			USM	2SK881

Application	Type		Package Type	Part Number
Tuning	Tuning Varicap Diode	Single	MINI	1SV101
		Double	S-MINI	1SV225 1SV228 JDV3C11
	AFC Varicap Diode	Single	S-MINI	1SV160

Application	Type	Package Type	Part Number
MIX	Dual Gate MOSFET	USQ	3SK260
	Bipolar transistor	MINI	2SC2668
		S-MINI	2SC2714
		USM	2SC4215
		SSM	2SC4915

Application	Type	Package Type	Part Number
OSC	J-FET	MINI	2SK192A
		S-MINI	2SK210
	Bipolar transistor	MINI	2SC2668 2SC2995
		S-MINI	2SC2714 2SC2996
		USM	2SC4215
		SSM	2SC4915

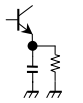
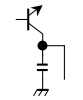
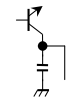
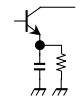
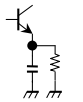
3. High-Frequency Devices for TV and VTR Tuners



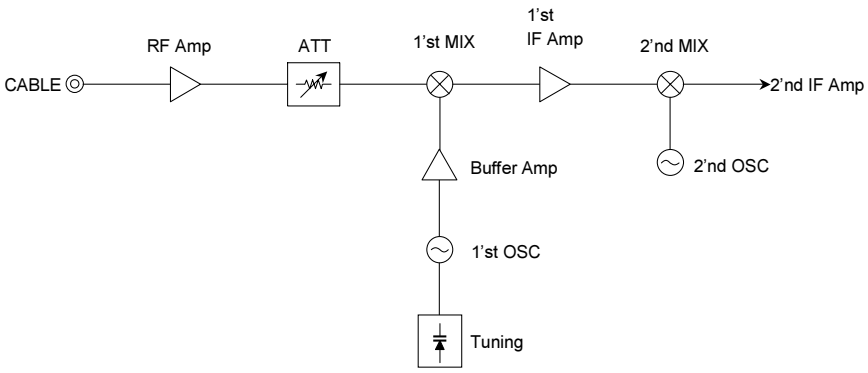
Application	Type	Band	Package Type	Part Number
Tuning	Varicap Diode	Wide Band VHF	USC	1SV215 1SV217 1SV262 1SV288 1SV231 1SV232 1SV269 1SV302
			ESC	1SV282 1SV290 1SV283 1SV303
			S-MINI (double type)	1SV242
		UHF	USC	1SV214
			ESC	1SV278
	AFC Diode	VHF to UHF	USC	1SV216
RF Amp	Dual Gate FET	VHF (wide band)	SMQ	3SK195 3SK225 3SK226 3SK292
			USQ	3SK259 3SK257 3SK258 3SK294
		UHF	SMQ	3SK199 3SK207 3SK232 3SK291
			USQ	3SK256 3SK249 3SK293
MIX	Dual Gate FET	VHF and Wide Band VHF	USQ	3SK260 3SK259
	Schottky Diode	UHF	S-MINI	1SS295 (double)
			USC	1SS315
			TESC	JDH2S01T
			SSM	JDH3D01S* (double)
			fSC	JDH2S01FS

*: New products

Application	Type		Band	Internal Connections	Package Type	Part Number
Tuning	Band SW	Single	VHF and Wide Band VHF		USC	1SS314
					ESC	1SS381
					sESC	JDS2S03S
		Double		ANODE COMMON	S-MINI	1SS269
						1SS268
					USM	1SS313
				CATHODE COMMON	USM	1SS312
					SSM	1SS364

Application	Type	Band	Circuit Diagram	Package Type	Part Number
RF Amp	Bipolar transistor	VHF	 EMITTER COMMON	USM	2SC4249
				SM	2SC3122
		UHF	 BASE COMMON	USM	2SC4244
				SMQ	2SC4214
OSC	Bipolar transistor	VHF (wide band)	 COLLECTOR COMMON	USM	2SC4251 2SC4246 2SC4252
				S-MINI	2SC3124 2SC3121
		UHF	 BASE COMMON	USM	2SC4246
				S-MINI	2SC3121
			 COLLECTOR COMMON	USM	2SC4247
				S-MINI	2SC3547A
MIX	Bipolar transistor	VHF (wide band)		USM	2SC4250 2SC4245
				S-MINI	2SC3123 2SC3120
				USM	2SC4253 2SC4251 2SC4246
				S-MINI	2SC3125 2SC3124 2SC3121
		UHF	 EMITTER COMMON	S-MINI	2SC3120 2SC3862
				S-MINI	2SC3547A
			 BASE COMMON	USM	2SC4245
				USM	2SC4247

4. High-Frequency Devices for CATV Converters



Application	Type	Package Type	Part Number
RF Amp	Bipolar transistor	SMQ	2SC5087 MT4S03A MT4S04A
		USQ	MT4S03AU MT4S04AU MT4S100U MT4S101U *MT4S102U *MT4S104U
		TESQ	MT4S100T MT4S101T *MT4S102T *MT4S104T

Application	Type		Package Type	Part Number
ATT	Pin Diode	Single	S-MINI	1SV128
			USC	1SV271 1SV307
			ESC	1SV308 JDP2S01E JDP2S04E
			TESC	JDP2S01T JDP2S02T
		Double	S-MINI	1SV172
			SMQ	1SV237
			USM	1SV252
			USQ	1SV312 JDP4P02U
			TESQ	JDP4P02AT

Application	Type		Package Type	Part Number
1'st MIX	Schottky Diode	Single	S-MINI	1SS154
			fSC	JDH2S01FS
		Double	S-MINI	1SS271
			SSM	*JDH3D01S

Application	Type	Package Type	Part Number
1'st IF Amp	Bipolar transistor	S-MINI	MT3S03A MT3S04A
		SMQ	MT4S03A MT4S04A MT4S06 MT4S07
		USQ	MT4S03AU MT4S04AU MT4S06U MT4S07U
	Si Dual Gate MOSFET	SMQ	3SK199 3SK232 3SK291 3SK292
		USQ	3SK249 3SK293 3SK294

Application	Type	Package Type	Part Number
2'nd MIX	Schottky Diode	SMQ	1SS239
		S-MINI	1SS154 (single) 1SS271 (double)
	Si Dual Gate MOSFET	SMQ	3SK199 3SK232 3SK291
		USQ	3SK249 3SK293
	Cell Pack	SM8	TA4107F

Application	Type	Package Type	Part Number
Buffer Amp	Bipolar transistor	S-MINI	MT3S03A MT3S04A
		SMQ	MT4S03A MT4S04A MT4S06 MT4S07
		USQ	MT4S03AU MT4S04AU MT4S06U MT4S07U

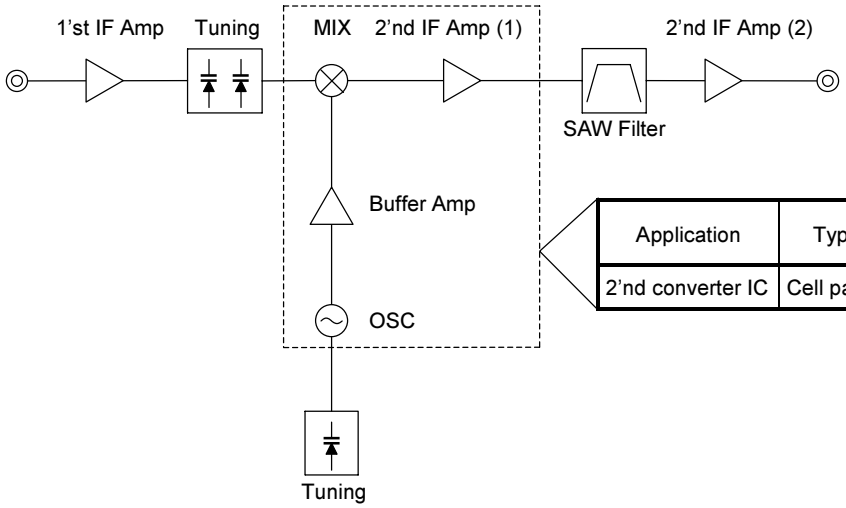
Application	Type	Package Type	Part Number
1'st OSC	Bipolar transistor	S-MINI	2SC5084 MT3S03A MT3S04A
		USM	MT3S03AU MT3S03AU

Application	Type	Package Type	Part Number
Tuning	Tuning Varicap	USC	1SV214 1SV230
		ESC	1SV278

Application	Type	Package Type	Part Number
2'nd OSC	Bipolar transistor	USM	2SC4246
		S-MINI	2SC3121

*: New products

5. High-Frequency Devices for SHF 2nd Converters



Application	Type	Package Type	Part Number
2'nd converter IC	Cell pack	SSOP20-P-225	TA4303F

Application	Type	Package Type	Part Number
1'st IF Amp	Bipolar transistor	SMQ	MT4S03A MT4S04A MT4S06 MT4S07 2SC5092
		USQ	2SC5088 2SC5093 2SC5319 MT4S06U MT4S07U MT4S100U MT4S101U *MT4S102U *MT4S104U
		TESQ	MT4S100T MT4S101T *MT4S102T *MT4S104T

Application	Type	Package Type	Part Number
Tuning	Preselector and Tuning Varicap Diode	USC	1SV245 1SV287
		ESC	1SV309 1SV291

Application	Type	Package Type	Part Number
MIX	Bipolar transistor	SMQ	2SC5087 2SC5092
	Schottky Diode	S-MINI	1SS154 (single) 1SS271 (double)
		SSM	*JDH3D01S (Duble)
		fSC	JDH2S01FS
	Cell Pack	SM8	*TA4107F

Application	Type	Package Type	Part Number
2'nd IF Amp (1)	Bipolar transistor	SMQ	2SC5092
		S-MINI	2SC5089
	Cell Pack	SMQ	TA4002F
		SMV	TA4003F

Application	Type	Package Type	Part Number
2'nd IF Amp (2)	Cell Pack	SM6	TA4000F
		TU6	TA4017FT
		SM8	TA4018F
		SM8	TA4019F

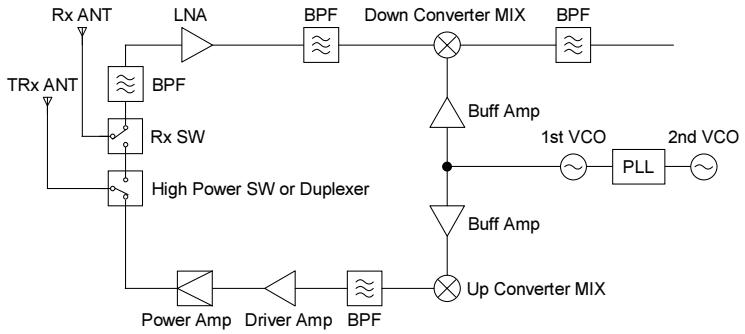
Application	Type	Package Type	Part Number
Buffer Amp	Bipolar transistor	SMQ	2SC5092
		USQ	2SC5088 2SC5093 2SC5319

Application	Type	Package Type	Part Number
OSC	Bipolar transistor	S-MINI	2SC5089

*: New products

Package type: SMV (SSOP5-P-0.95)

6. High-Frequency Devices for 800 MHz Band Analog and Digital Cellular Phones



Application	Type	Package Type	Part Number
Power Amp (JAPAN CDMA)	Module	5-6B	S-AU84
Power Amp (US CDMA)	Module	5-6B	S-AU85

Application	Type	Package Type	Part Number
Power Amp	Si MOSFET	PW-MINI	2SK2854
			2SK2855

Application	Type	Package Type	Part Number
Rx SW	GaAs Cell Pack	TU6	TG2210FT
			TG2211FT
	PIN Diode	USC	ISS314
		ESC	ISS381
		fSC	JDP2S02AFS
			*JDP2S05FS
		sESC	JDS2S03S

Application	Type	Package Type	Part Number
Buff Amp	Si Cell Pack	SMV	TA4003F
			TA4004F
		ESV	TA4011AFE
			TA4012AFE

Application \ Package Type	Type	USC	TESC
Detector	SBD	1SS315	JDH2S01T

Application \ Package Type	TESM	fSM	SMQ	USQ
LNA, Buff Amp	2SC5066FT			
	2SC5086FT		2SC5087	2SC5088
	2SC5091FT		2SC5092	2SC5093
	2SC5096FT		2SC5097	2SC5098
	MT3S03AT	MT3S03AFS		
	MT3S06T	MT3S06FS	MT4S06	MT4S06U
	MT3S07T	MT3S07FS	MT4S07	MT4S07U
	MT3S14T	*MT3S14FS		
	MT3S17T	*MT3S17FS		
	MT3S18T	*MT3S18FS		
	MT3S35T	MT3S35FS		
	MT3S36T	MT3S36FS		
	MT3S37T	MT3S37FS		
	MT3S38T	MT3S38FS		
	MT3S40T	MT3S40FS		
	MT3S41T	MT3S41FS		
				MT4S32U
MIX	2SC5066FT			
	2SC5086FT	—	2SC5087	2SC5088
	2SC5108FT			
	2SC5111FT			
VCO	2SC5086FT			
	2SC5464FT			
	2SC5066FT			
	2SC5108FT			
	2SC5111FT			
	MT3S03AT	MT3S03AFS		
	MT3S04AT	MT3S04AFS		
	MT3S05T	MT3S05FS		
	MT3S06T	MT3S06FS		
	MT3S07T	MT3S07FS		
	MT3S08T	MT3S08FS	—	—
	MT3S11T	*MT3S11FS		
	MT3S12T	*MT3S12FS		
	MT3S14T	*MT3S14FS		
	*MT3S18T	*MT3S18FS		
	MT3S35T	MT3S35FS		
	MT3S36T	MT3S36FS		
	MT3S37T	MT3S37FS		
	MT3S38T	MT3S38FS		
	MT3S40T	MT3S40FS		
	MT3S41T	MT3S41FS		
	MT3S45T	MT3S45FS		

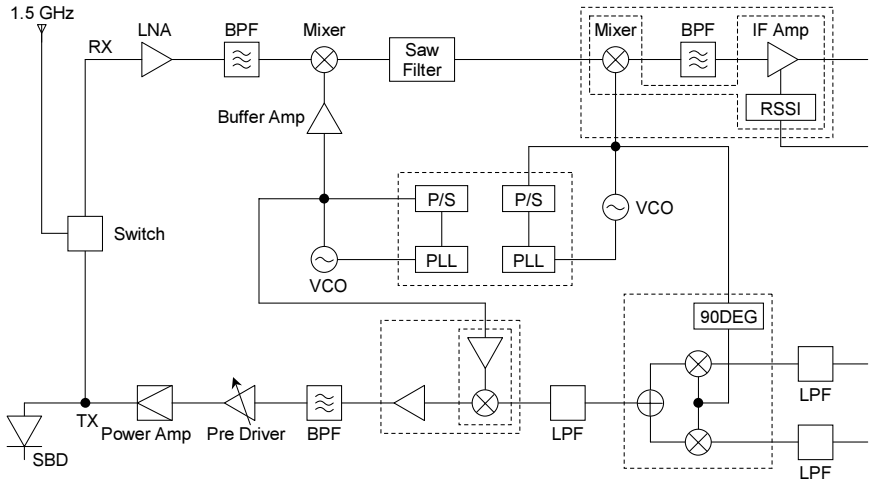
*: New products

Varicap Diode

Application \ Package Type	USC	ESC	sESC	fSC
VCO	1SV229	1SV279		
	1SV270	1SV281		
	1SV276	1SV284	JDV2S06S	JDV2S06FS
	1SV304	1SV305	JDV2S08S	JDV2S08FS
	1SV310	1SV311	JDV2S09S	JDV2S09FS

*: New products

7. High-Frequency Devices for PDC (1.5 GHz)



Application	Package Type / Type	TESM	fSM	USQ	TESQ
LNA, Buff Amp	Bipolar transistor	2SC5317FT 2SC5322FT MT3S06T MT3S07T MT3S14T MT3S17T MT3S18T MT3S35T MT3S36T MT3S37T MT3S38T MT3S40T MT3S41T MT3S45T	MT3S06FS MT3S07FS *MT3S14FS *MT3S17FS *MT3S18FS MT3S35FS MT3S36FS MT3S37FS MT3S38FS MT3S40FS MT3S41FS MT3S45FS	2SC5319 MT4S06U MT4S07U MT4S100U MT4S101U	MT4S100T MT4S101T
Mixer (down)	Bipolar transistor	2SC5317FT 2SC5322FT 2SC5086FT			
VCO	Bipolar transistor	MT3S03AT MT3S04AT MT3S05T MT3S06T MT3S07T MT3S08T MT3S11T MT3S12T MT3S14T *MT3S18T MT3S35T MT3S36T MT3S37T MT3S38T MT3S40T MT3S41T MT3S45T	MT3S03AFS MT3S04AFS MT3S05FS MT3S06FS MT3S07FS MT3S08FS *MT3S11FS *MT3S12FS *MT3S14FS *MT3S18FS MT3S35FS MT3S36FS MT3S37FS MT3S38FS MT3S40FS MT3S41FS MT3S45FS		

*: New products

Application	Package Type / Type	ESC	sESC	fSC
VCO	VCD	JDV2S05E 1SV285 1SV305 1SV311 1SV314 1SV329	JDV2S05S JDV2S07S JDV2S08S JDV2S09S JDV2S10S JDV2S13S	JDV2S05FS JDV2S07FS JDV2S08FS JDV2S09FS JDV2S10FS JDV2S13FS

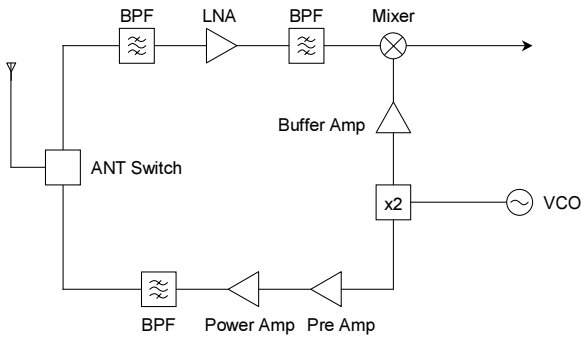
Application	Package Type / Type	ESV
Buff Amp	Si Cell pack	TA4011AFE TA4012AFE

Application	Package Type / Type	TU6
RF Switch	GaAs Cell pack	TG2211FT

Application	Package Type / Type	USC	TESC	fSC	SSM
Detector	SBD	1SS315	JDH2S01T	JDH2S01FS	*JDH3D01S

*: New products

8. High-Frequency Devices for 900 MHz, 2.4 GHz and 5.8 GHz Band Cordless Phone

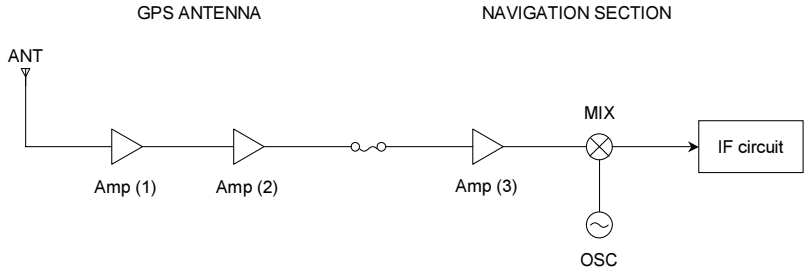


Application \ Package Type / Frequency Band	USC	ESC	sESC	fSC	CST2	USM	SSM	TESM	SMQ	USQ	TESQ
ANT Switch — 900 MHz	1SV271 1SV307 1SS314	JDP2S04E 1SV308 1SS381	JDP2S02AS JDS2S03S	JDP2S02AFS	*JDP2S02ACT						
ANT Switch — 2.4 GHz	1SV271 1SV307	JDP2S04E 1SV308	JDP2S02AS	JDP2S02AFS *JDP2S05FS	**JDP2S05CT						
ANT Switch — 5.8 GHz				*JDP2S05FS	**JDP2S05CT						
VCO — 900 MHz	1SV214 1SV229 1SV276 1SV304 1SV310 1SV313	1SV278 1SV279 1SV284 1SV305 1SV311 1SV314	JDV2S06S JDV2S08S JDV2S09S	JDV2S06FS JDV2S08FS JDV2S09FS							
VCO — 2.4 GHz		JDV2S01E JDV2S02E JDV2S05E	JDV2S01S JDV2S02S JDV2S05S JDV2S16S JDV2S19S JDV2S20S	JDV2S01FS JDV2S02FS JDV2S05FS JDV2S16FS JDV2S19FS JDV2S20FS							
VCO — 5.8 GHz		JDV2S02E	JDV2S02S *JDV2S17S JDV2S20S *JDV2S22S	JDV2S02FS *JDV2S17FS JDV2S20FS *JDV2S22FS							
VCO Buffer Amp Mixer Power Amp Pre Amp LAN — 900 MHz						2SC5065 2SC5085 MT3S06U *MT3S16U	2SC5066 2SC5086 MT3S06S	2SC5066FT 2SC5086FT MT3S06T *MT3S16T *MT3S17T *MT3S18T	2SC5087 MT4S06	2SC5088 MT4S06U	
VCO Buffer Amp Mixer Power Amp Pre Amp LAN — 2.4 GHz						MT3S06U	2SC5317 MT3S06S	2SC5317FT MT3S06T *MT3S17T *MT3S18T *MT3S35T	MT4S06	2SC5319 MT4S06U MT4S32U	
VCO Buffer Amp Mixer Power Amp Pre Amp LAN — 5.8 GHz								MT3S35T MT3S37T		MT4S100U MT4S101U *MT4S102U *MT4S104U	MT4S100T MT4S101T *MT4S102T *MT4S104T

*: New products

**: Under development

9. High-Frequency Devices for GPS LNB



GPS Antenna Section

Application	Package Type / Type	ES6	USQ	TESQ
Amp (2)	Bipolar transistor		2SC5319 MT4S32U *MT4S100U *MT4S101U *MT4S102U *MT4S104U	*MT4S100T *MT4S101T *MT4S102T *MT4S104T
	Si Cell-Pack	*TA4016AFE		

*: New products

Navigation Section

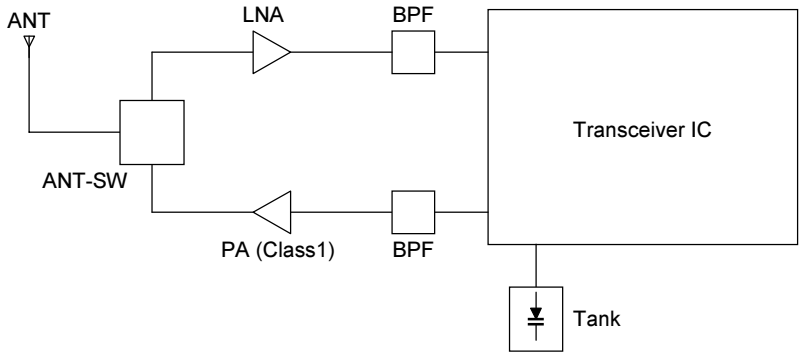
Application	Package Type / Type	USQ	TESQ
Amp (3)	Bipolar transistor	2SC5319 MT4S06U MT4S32U *MT4S100U *MT4S101U *MT4S102U *MT4S104U	*MT4S100T *MT4S101T *MT4S102T *MT4S104T
Mixer, OSC	Bipolar transistor	2SC5319 MT4S06U	

*: New products

Application	Package Type / Type	ESC	sESC	fSC
OSC	Varicap Diode	1SV314	JDV2S10S	JDV2S10FS
		1SV329	JDV2S13S	JDV2S13FS
		JDV2S01E JDV2S02E JDV2S05E	JDV2S01S JDV2S02S JDV2S05S JDV2S16S *JDV2S17S JDV2S19S JDV2S20S *JDV2S22S	JDV2S01FS JDV2S02FS JDV2S05FS JDV2S16FS *JDV2S17FS JDV2S19FS JDV2S20FS *JDV2S22FS

*: New products

10. 2.4 GHz Wireless LAN and Bluetooth



ANT-SW

	Type	Part Number
For Class 1	GaAs MMIC	TG2216TU
For Class 2, 3	GaAs MMIC	TG2210FT
	GaAs MMIC	◎TG2211FT
	GaAs MMIC	TG2213S
	GaAs MMIC	TG2214S
All Class	Pin Diode	JDP2S01AFS
	Pin Diode	JDP2S02AFS

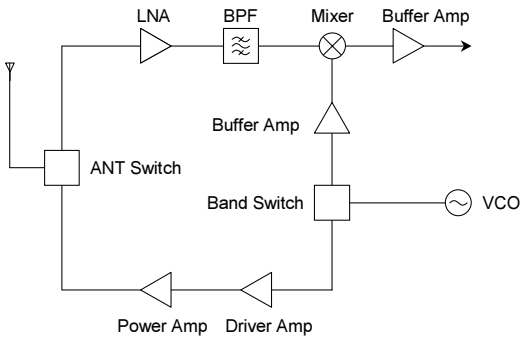
◎: Built-in inverter

Application \ Package Type	USQ	TESQ
Type		
LNA / Bipolar transistor	2SC5319 MT4S32U MT4S100U MT4S101U *MT4S102U *MT4S104U	MT4S100T MT4S101T *MT4S102T *MT4S104T

*: New products

Application \ Package Type	Type	ESC	sESC	fSC
VCO	Varicap Diode	1SV314	JDV2S10S	JDV2S10FS
		1SV329	JDV2S13S	JDV2S13FS
		JDV2S01E JDV2S02E JDV2S05E	JDV2S01S JDV2S02S JDV2S05S JDV2S16S JDV2S19S JDV2S20S	JDV2S01FS JDV2S02FS JDV2S05FS JDV2S16FS JDV2S19FS JDV2S20FS

11. High-Frequency Devices for FRS, GMRS



Application \ Package	Type	USC	ESC	sESC	fSC	CST2	USM	SSM	TESM	SMQ	USQ
ANT Switch	FRS, GMRS	1SS314 1SV271 1SV307	1SS381 JDP2S04E 1SV308	JDS2S03S JDP2S02AS	JDP2S02AFS *JDP2S05FS	*JDP2S02ACT					
VCO		1SV214 1SV229 1SV276 1SV304	1SV278 1SV279 1SV284 1SV305 1SV282A	JDV2S06S JDV2S08S	JDV2S06FS JDV2S08FS						
VCO Driver Buffer Amp Mixer LAN							2SC5065 2SC5085 MT3S06U *MT3S16U	2SC5066 2SC5086 MT3S06S	2SC5066FT 2SC5086FT MT3S06T *MT3S16T *MT3S17T *MT3S18T	2SC5087 MT4S06	2SC5088 MT4S06U

*: New products

Application \ Package	Type	PW-MINI	PW-X
Power Amp	FRS	2SK3078A *2SK3656	
	GMRS		2SK3079A *2SK3756

*: New products

[4] Maximum Ratings and Electrical Characteristics

[4] Maximum Ratings and Electrical Characteristics

1. Definition of Maximum Ratings

1.1 Maximum Ratings (for high-frequency bipolar transistors)

1) Collector-base voltage (V_{CBO})

Maximum permissible value of voltage between collector and base with emitter open at the specified ambient temperature

2) Collector-emitter voltage (V_{CES})

Maximum permissible value of voltage between collector and emitter with base-emitter short at the specified ambient temperature

3) Collector-emitter voltage (V_{CEO})

Maximum permissible value of voltage between collector and emitter with base open at the specified ambient temperature

4) Emitter-base voltage (V_{EBO})

Maximum permissible value of voltage between emitter and base with collector open at the specified ambient temperature

5) Collector current (I_C)

Maximum permissible value of collector current at the specified ambient temperature.

Regardless of the states of base and emitter, a current exceeding the rated value cannot flow through the collector.

6) Collector power dissipation (P_C)

Maximum permissible power dissipation at the specified ambient temperature. Normally the value is specified for room temperature. P_C decreases with increase in ambient temperature. If a device dissipates power in excess of the P_C rating, it may be damaged electrically or thermally due to the generation of heat. Note also that the specified P_C value is the value for the device alone. If the device is mounted on a PCB, its P_C value will differ substantially.

7) Junction temperature (T_j)

Permissible junction temperature range for device operation. The device's maximum power consumption and operating temperature levels must be set so that the junction temperature always remains within the T_j range.

8) Storage temperature range (T_{stg})

Ambient temperature range within which the device must be stored while not being used. Toshiba guarantees that the device will not be degraded if it is stored at a temperature within the T_{stg} range.

1.2 Maximum Ratings (for MOSFETs)

1) Drain-source voltage (V_{DSS})

Maximum voltage that can be applied between drain and source when gate and source are connected directly at the specified temperature

2) Gate-source voltage (V_{GSS})

Maximum voltage that can be applied between gate and source when drain and source are connected directly at the specified temperature

3) Drain current (I_D)

Maximum forward current that can flow in drain pin at the specified temperature

4) Reverse drain current (I_{DR})

Maximum reverse current that can flow in drain pin at the specified temperature

5) Power dissipation (P_D)

Maximum power dissipation at the specified temperature

6) Channel temperature (T_{ch})

Maximum junction temperature during device operation

7) Storage temperature (T_{stg})

Specified ambient temperature range for while MOSFET is not in use

1.3 Maximum Ratings (for MOS modules)

1) Power supply voltage (V_{dd})

Maximum voltage that can be applied between V_{dd} pin and GND at the specified temperature

2) Control voltage (V_{gg})

Maximum voltage that can be applied between V_{gg} pin and GND at the specified temperature

3) Current consumption (I_t)

Maximum current that can flow in all voltage pins at the specified temperature

4) Input power (P_i)

Maximum high-frequency power that can be applied to P_i pin at the specified temperature and under the specified conditions

5) Output power (P_o)

Maximum high-frequency power that can be measured at P_o pin at the specified temperature and under the specified conditions

6) Operating temperature (T_C (opr))

Theoretical case temperature range for module operation. Toshiba guarantees that the module will operate properly if the case temperature remains within this range while the module is being used.

7) Storage temperature (T_{stg})

Specified ambient temperature range for while module is not in use

1.4 Maximum Ratings (for bipolar modules)

1) Power supply voltage (V_{CC})

Maximum voltage that can be applied between V_{CC} pin and GND at the specified temperature

2) Control voltage (V_{con})

Maximum voltage that can be applied between V_{con} pin and GND at the specified temperature

3) Current dissipation (I_t)

Maximum current that can flow in all voltage pins at the specified temperature

4) Input power (P_i)

Maximum high-frequency power that can be applied to P_i pin at the specified temperature and under the specified conditions

5) Output power (P_o)

Maximum high-frequency power that can be measured at P_o pin at the specified temperature and under the specified conditions

6) Operating temperature (T_C (opr))

Theoretical case temperature range for module operation. Toshiba guarantees that the module will operate properly if the case temperature remains within this range while the module is being used.

7) Storage temperature (T_{stg})

Ambient temperature range within which the module must be stored while not being used

2. Definition of Electrical Characteristics

2.1 Electrical Characteristics (for high-frequency bipolar transistors)

Parameter	Symbol	Description
Collector-emitter breakdown voltage	$V_{(BR)\ CEO}$	Breakdown voltage between collector and emitter when the specified voltage is applied between collector and emitter with emitter common and base open
Collector-emitter breakdown voltage	$V_{(BR)\ CES}$	Breakdown voltage between collector and emitter when the specified collector current flows with emitter common, and base and emitter shorted.
Emitter-base breakdown voltage	$V_{(BR)\ EBO}$	Breakdown voltage between emitter and base when the specified emitter current flows with base common and collector open.
DC current gain	h_{FE}	Ratio of collector current to base current when device is operating at the specified collector-emitter voltage and collector current and with emitter common
Output capacitance	C_{ob}	Capacitance between collector and base at the specified collector-base voltage with base common
Input power	P_i	High-frequency input power required to achieve the specified high-frequency output power under the specified operating conditions in the specified test circuit.
Output power	P_o	High-frequency output power when the specified high-frequency power is applied under the specified operating conditions in the specified test circuit.

2.2 Electrical Characteristics (for MOSFETs)

Parameter	Symbol	Description
Gate leakage current	I_{GSS}	Gate current when the specified gate voltage is applied with source common, and drain and source shorted
Drain current, Drain cut-off current	I_{DSS}	Drain current when the specified drain voltage is applied with gate and source shorted and source common
Source-drain breakdown voltage	$V_{(BR)\ DSS}$	Breakdown voltage between source and drain when the specified drain current flows with source common, and gate and source shorted.
Gate threshold voltage	V_{th}	Gate voltage when the specified drain current flows with source common, and the specified drain voltage applied.
Drain-source On resistance	$R_{DS\ (ON)}$	Drain-source resistance when the specified drain current flows with source common, and the specified gate voltage applied.
Drain-source On voltage	$V_{DS\ (ON)}$	Drain-source voltage when the specified drain current flows with source common, and the specified gate voltage applied.
Forward transfer admittance	$\|Y_{fS}\|$	Admittance obtained at $\Delta I_D/\Delta V_{GS}$ when the device is operating at the specified frequency with source common and with the specified drain current and drain voltages applied
Input capacitance	C_{iss}	Equivalent capacitance between gate and source when the device is operating at the specified frequency with source common, drain and source common and with the specified drain current and drain voltages applied
Output capacitance	C_{oss}	Equivalent capacitance between drain and source when the device is operating at the specified values of gate voltage, drain voltage and frequency, with source common, and gate and source shorted (AC shorted).
Reverse transter capacitance	C_{rss}	Equivalent capacitance between gate and drain when the device is operating at the specified frequency with source common and with the specified drain current and drain voltages applied
Output power	P_o	High-frequency output power when the specified high-frequency power is applied under the specified operating conditions in the specified test circuit.
Drain efficiency	ηD	Ratio, expressed in percentage, between high-frequency output power and DC drain input power when the specified high-frequency power is applied under the specified operating conditions in the specified test circuit.
Power gain	G_p	Power gain when the specified high-frequency power is applied under the specified operating conditions in the specified test circuit.

2.3 Electrical Characteristics (for modules)

Parameter	Symbol	Description
Frequency range	f_{RANGE}	Frequency range for high-frequency device operation
Power output	P_o	High-frequency power under the specified conditions
Power gain	G_p	High-frequency gain under the specified conditions
Overall efficiency	η_t	Conversion efficiency of device under the specified conditions ηt is defined as: $\eta t = P_o \times 100/P_i + V_{con} \times I_{con} + V_{CC} \times I_{CC}$.
Input VSWR	$VSWR_{in}$	Standing-wave ratio for input side of device under the specified conditions $VSWR_{in}$ is defined as: $VSWR_{in} = 1 + (\sqrt{Pi/Pr})/1 - (\sqrt{Pi/Pr})$.
Harmonics	HRM	Difference between fundamental harmonic and secondary frequency under the specified conditions
Load-resistance characteristics	—	Device will not be destroyed under the specified conditions.
Stability	—	Device will not oscillate abnormally under the specified conditions.

[5] Device Features in Detail

[5] Device Features in Detail

1. High-Frequency Transistor Parameter

The main design parameters of a transistor include the device parameters which closely respond to the internal operating mechanism of the transistor, and the circuit parameters which comprise a matrix obtained by regarding the transistor as a terminal circuit network.

These latter-mentioned parameters are further divided into one group corresponding to small-signal equivalent circuits (analog circuits), and another group describing large-signal equivalent circuits (digital circuits); the demarcation between these two groups being made according to the amplitude of signals to be handled by each.

Equivalent circuits have undergone very rapid development recently. Circuit designers pay close attention to the application ranges and operating limits of the device being simulated in selecting an appropriate equivalent circuit. Table 1.1 lists equivalent circuits presently employed in small-signal applications.

The descriptions in this section will emphasize small-signal equivalent circuits they are used.

Table 1.1 List of Transistor Equivalent Circuits

Transistor equivalent circuits	Small-signal equivalent circuits (general linear circuits for purposes such as amplification, oscillation, modulation, and demodulation)	Device parameters	Early's T-type equivalent circuits (common base circuits) Giacoletto's π-type equivalent circuits (emitter and collector common circuits)
		Circuit parameters	Matrices showing the relations among the inputs and outputs by voltage and current a, b matrices; g, h matrices (low frequency); y, z matrices (high frequency) Matrices showing the relations among inputs and outputs by power s matrices (high frequency)
	Large-signal equivalent circuits (nonlinear circuits such as pulse, digital, and switching circuits)		Current control model by Evers-Moll; Current control model by Beaufoy-Sparkes; Current control model by Linville; other nonlinear models

1.1 Device Parameters

1.1.1 Early's T-Type Equivalent Circuits

Figure 1.1 shows an Early's T-type equivalent circuit.

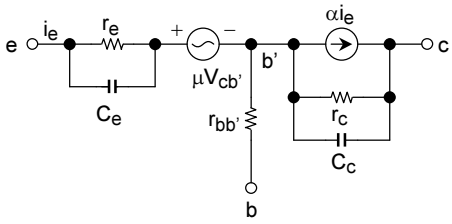


Figure 1.1 Early's T-Type Equivalent Circuit

In this circuit,

r_e: Emitter resistance

Since this is a forward-biased resistance associated with the base-to-emitter junction, represented by the following equation:

$$r_e = \frac{kT}{qI_E}(\Omega) \quad \text{.....(1)}$$

where

k: Boltzman's constant (1.38×10^{-23} J/K)

T: Absolute temperature (K)

q: Electric charge of electron (1.60×10^{-19} C)

I_E: Emitter current (A)

Equation (1) is changed as follows at normal temperature (300 K) if the emitter current is represented by mA in:

$$r_e = \frac{26}{I_E(\mathrm{mA})}(\Omega) \quad \text{.....(2)}$$

where C_e: Emitter capacitance ($C_{T_e} + C_{D_e}$)

The emitter capacitance is represented as a sum of the depletion layer capacitance and the diffusion capacitance. Because the depletion layer capacitance in an emitter-to-base junction is normally far smaller than the diffusion capacitance, it can in most cases be ignored. The depletion layer capacitance C_{T_e} and the diffusion capacitance C_{D_e} are represented as:

$$C_{T_e} = A_e\sqrt{\frac{\frac{1}{2}\varepsilon q n_N}{\phi_0 - V_{b'e}}}(\mathrm{F}) \quad \text{.....(3)}$$

where,

A_e: Emitter junction area (m^2)

ε: permittivity

n_N: Majority carrier density (m^{-3}) on the side of higher specific resistance side (NPN in this case)

ϕ_0: Contact potential difference (potential fault ck. term when balanced) (V)

$V_{b'e}$: Potential applied to both ends of the base-to-emitter junction (1)

$$C_{D_e} = \frac{qI_E W^2}{2kTD}(\mathrm{F}) \quad \text{.....(4)}$$

where,

W: Base width (m)

D : Diffusion coefficient of minority carrier in the base region (m^2/s)

μ: Voltage feedback ratio (early constant)

This constant, measuring what is known as the Early effect, is a base-width modulation parameter,

$$\mu = \frac{kTd_c}{3qW(\phi_0 - V_{b'e})} \quad \text{.....(5)}$$

where,

d_c: Width of collector depletion lay (m)

r_c: Collector resistance

This is a kind of base-width modulation parameter, represented as follows:

$$r_c = \frac{1}{I_E\left(\frac{\partial\alpha}{\partial V_{b'c}}\right)}(\Omega) \quad \text{.....(6)}$$

The value of rc is usually 1 to 2 MΩ or so.

C_c: Collector capacitance

Calculated similarly to emitter capacitance, this is shown as the sum of depletion layer capacitance and diffusion capacitance of the collector-to-base junction. However, since the diffusion capacitance of the collector-to-base junction is far smaller than the depletion layer capacitance, it can be ignored. The depletion layer capacitance is represented as

$$C_{TC} = A_C\sqrt[3]{\frac{\frac{\varepsilon^2 qa}{12}}{\phi_0 - V_{b'c}}}\,(F) \quad \text{.....(7)}$$

where,

A_C: Collector junction area (m^2)

a: Impurity concentration gradient (m^{-4})

$V_{b'e}$: Potential applied to both ends of the base-to-collector junction (V)

Usually the value of C_c is one to ten pF.

α: DC forward current transfer ratio

This is the only parameter that depends on frequency, among the several related to an Early's T-type equivalent circuit, and it is represented by the equation

$$\alpha = \frac{\alpha_0}{1 + j\omega C_e r_e}$$

$$f_\alpha = \frac{1}{2\pi C_e r_e}$$

therefore,

$$\alpha = \frac{\alpha_0}{1 + j\frac{f}{f_\alpha}} \quad \text{.....(8)}$$

where,

α_0: Value of α at low frequency

f_α : α-interrupting frequency (frequency at which α is reduced to a level 3dB less than α_0)

Figure 1.2 shows the frequency locus of α. When actually measuring α, the difference between theoretical and measured values increases as the frequency approaches f_α. This is because the Early's equivalent circuit is based on an first approximation of physical phenomena.

To correct it, Thomas-Moll introduced excess phase m and offered the equation.

$$\alpha = \frac{\alpha_0}{1 + j\frac{f}{f_\alpha}} \exp\left(-jm\frac{f}{f_\alpha}\right) \quad \text{.....(9)}$$

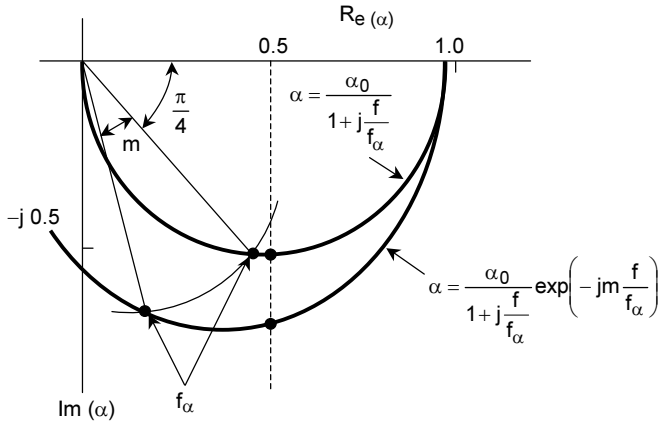


Figure 1.2 Frequency Locus of α

The above equation agrees well with measured values in frequencies less than f_α.

$r_{bb'}$: Base diffusion resistance

This is resistance from the center of the base area to the external base terminal, which actually contributes to transistor action. It is determined according to the shape and dimensions of the transistor, and the base specific resistance.

$$r_{bb'} \simeq \frac{q_B}{8\pi W}(\Omega) \quad \text{.....(10)}$$

where,

q_B: Specific resistance of base area (Ω・m)

DC Current gain (β) at the common emitter is represented as follows:

$$\beta = \frac{\alpha_0}{1-\alpha_0}\frac{1}{1 + j\omega C_{b'e} r_{b'e}} = \frac{\beta_0}{1 + j\omega C_{b'e} r_{b'e}}$$

The β-interrupting frequency f_β is defined as the frequency at which the absolute value of β becomes $\beta_0/\sqrt{2}$. f_β is represented similarly to f_α, as:

$$f_\beta = \frac{1}{2\pi C_{b'e} r_{b'e}}$$

therefore,

$$\beta = \frac{\beta_0}{1 + j\frac{f}{f_\beta}} \quad \text{.....(11)}$$

1.1.2 Giacoletto's π-Type Equivalent Circuit

Figure 1.3 shows the π-type equivalent circuit. This equivalent circuit is in itself the same as an Early's T-type equivalent circuit mentioned above. The only thing distinguishing the π-type circuit from an Early's T-type equivalent circuit is that in principle each parameter has no frequency response.

Table 1.2 Relationship between Parameters of the π-Type and T-Type Equivalent Circuits

π-Type Equivalent Circuit Parameters	T-Type Equivalent Circuit Parameters
$C_{b'e}$	C_e
$r_{be'}$	$\frac{r_e}{1-\alpha_0}$
$C_{b'c}$	C_c
$\frac{1}{r_{b'c}}$	$\frac{1}{r_c}-\frac{\mu(1-\alpha_0)}{r_e}$
r_{ce}	$\frac{r_e}{\mu}$
g_m	$\frac{\alpha_0}{r_e}$
$r_{bb'}$	$r_{bb'}$

Parameters of the T-type equivalent circuit and those of the π-type have the correlation shown Table 1.2.

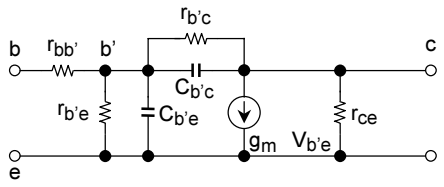


Figure 1.3 π-Type Equivalent Circuit

Because the physical meaning of each parameter is easy to understand, this circuit is popularly employed. When actually employed for circuit calculation, it will prove convenient if the basic style shown in Figure 1.3 is slightly simplified by restricting the frequency range to that which is anticipated for performance of the device actually being simulated.

1.1.3 Types and Structures of Field Effect Transistors (FETs)

Field Effect Transistors (FETs) can be classified into the following two types according to their gates:

- Junction FET (junction gate)
- MOSFET (insulated gate)

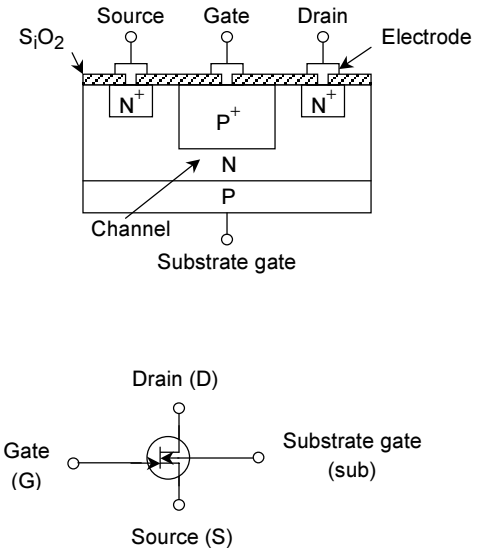
Figure 1.4 shows the structures of both types.

A junction FET is one whose gate-to-channel portion is composed of a PN junction; but a FET whose gate-to-channel portion is composed of Metal, Oxide, and a Semiconductor is termed a MOSFET. FETs are also classified into P-channel and N-channel types according to the type (P or N) of the semiconductor layer through which drain current flows.

The structural drawings shown in Figure 1.4 are all N-channel type.

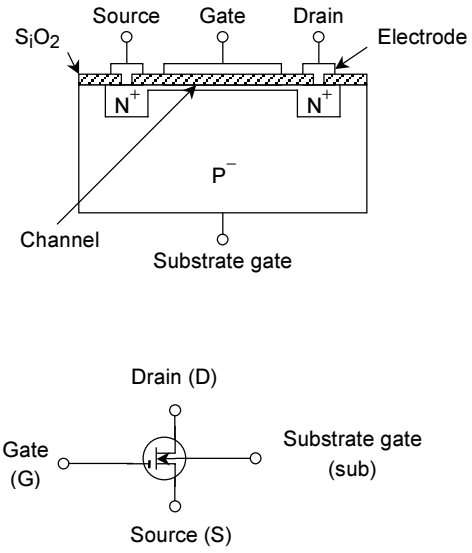
Both junction and MOSFETs have their merits and disadvantages. A MOSFET is much more easily broken down by static electricity. Extreme care must be exercised, and suitable protective measures taken, when handling a MOSFET.

(1) Junction FET



*: The substrate gate is usually connected to the source.

(2) MOSFET



*: The substrate gate is usually connected to the source.

Figure 1.4 Structures and Symbols of Field Effect Transistors (FETs)

However, almost all MOSFETs incorporate a protective diode at the gate to prevent such breakdowns, and it is very rare for them to degenerate when handled in a careful manner.

Nevertheless, junction FETs are considerably more robust, and are usually not damaged even if they are handled in the same manner as bipolar transistors.

Almost all MOSFETs are used for high-frequency circuits and chopper circuits. This is because, compared with the junction type, the MOS type is superior in cross-modulation and inter-modulation characteristics, and that when used in a chopper circuit, there is less spike and switching speed is higher.

When using FETs for a high-frequency circuit, it is necessary to reduce the internal feedback capacitance to as low a level as possible, so that stable gain can be obtained. FETs with a cascode connection are employed by adopting for this purpose.

In recent years, this problem has been solved in two different ways: by producing a cascode FET in which two FETs are cascode-connected in the interior, as well as by development of dual-gate MOSFETs.

Figure 1.5 illustrates the structure of a cascode FET, and a drawing of an equivalent connection for it. A cascode FET has two junction gates, the one near the drain being connected to the substrate gate. Thereby two FETs are produced, a common source FET and a common gate FET.

This structure causes feedback from the drain to be grounded as alternate current, producing a FET with small reverse transfer capacitance.

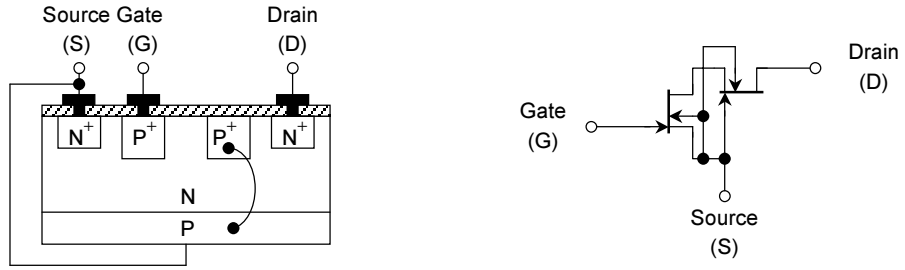


Figure 1.5 Structure and Equivalent Connection Drawing of Cascode FET

Figure 1.6 shows the structure and equivalent connection drawings of a dual-gate MOSFET. As far as the operating principle is concerned, this FET is identical with a cascode FET. In the dual-gate MOSFET, gate 2 is lead out to be grounded for AC and to be supplied with positive bias voltage for DC, when the FET is used in a high-frequency amplifier circuit. It is possible to use gate 2 as an injection terminal when using the MOSFET in a mixing circuit.

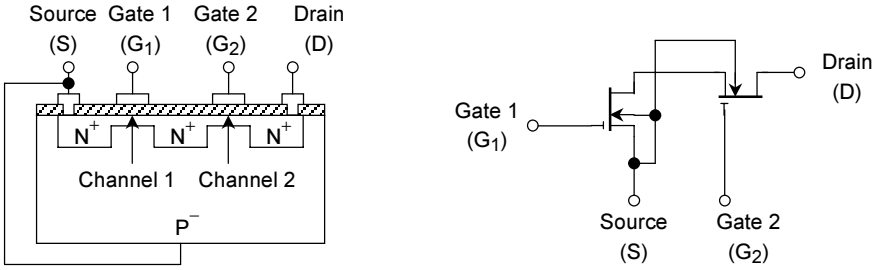


Figure 1.6 Structure and Equivalent Connection Drawings of Dual-Gate MOSFET

The symbols used for a junction cascode FET and for a dual-gate MOSFET are illustrated in Figure 1.7.

(1) Junction cascode FET

(2) Dual-gate MOS FET

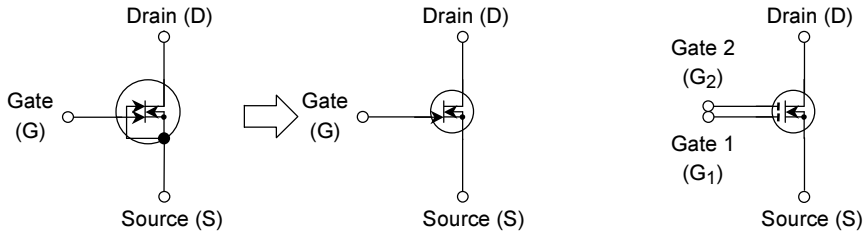


Figure 1.7 Symbols Used for Junction Cascode FET and Dual-Gate MOSFET

Other available FETs, in addition to those already described, include a power FET and a GaAs FET.

1.1.4 FET Equivalent Circuit

As in the case of bipolar transistors, a FET can be simulated by means of an equivalent circuit. Figure 1.8 is a schematic diagram of the equivalent circuit's structure.

This diagram is rewritten into an equivalent circuit in Figure 1.9 (a), and further rewritten into a practical, simplified equivalent circuit in Figure 1.9 (b).

C_{GD}, C_{GS}, and C_{DS} shown here are parasitic capacitances. Since their values are relatively small, it is possible to ignore them unless this circuit is used in VHF regions.

However, when using transistors whose capacitances between electrodes are large, such as a power FET and a high-g_m FET in low-frequency regions, these capacitances must be considered fully.

For a FET to be used in chopper circuits, it is necessary to keep the difference between C_{GD} and C_{GS} small to prevent spikes.

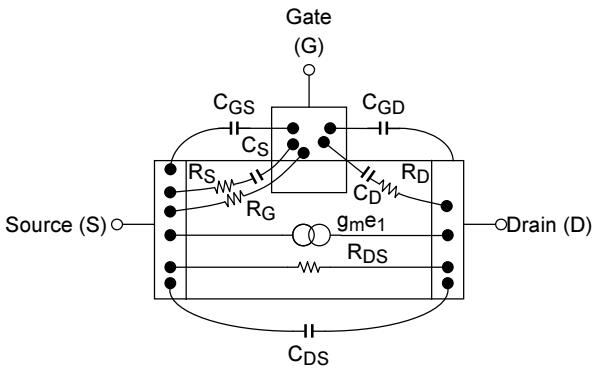
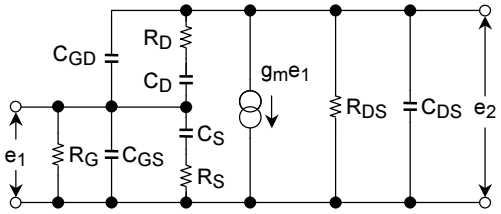


Figure 1.8 Equivalent Circuit in Relation to Structure of a FET

(a) Equivalent circuit



(b) Simplified equivalent circuit

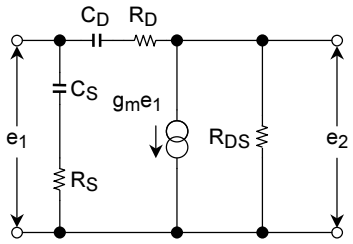


Figure 1.9 Equivalent Circuit

This simplified equivalent circuit shows the main characteristics of a FET very well, because it is related to the structure of the FET and it is portrayed with basic parameters not depending on frequency. For example, here it is understood that DC input resistance (which is infinity) can be practically ignored and that C_D (internal feedback capacitance) is an unstable factor at high frequency.

Furthermore, at low frequency it is possible to ignore capacitance; and input resistance is infinity, while output resistance = R_{DS}. With these simplifications this is almost an equivalent circuit of a vacuum tube

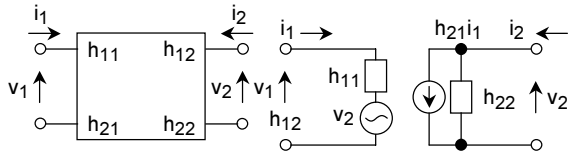
1.2 Circuit Parameters

1.2.1 Matrices Showing the Relations Among Inputs and Outputs by Voltage and Current

This is a method used to describe a transistor by regarding it as a four-terminal circuit network, and by using the electrical characteristic of terminals irrespective of the physical characteristics of the transistor.

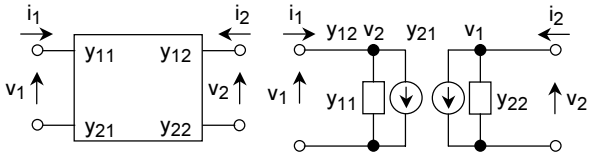
The resulting matrices are of six types as shown in Table 1.1 (a, b, g, h, y and z matrices). Among these, both the "h" and "y" matrices are used comparatively often.

Figure 1.10 and Figure 1.11 show the definitions of "h" and "y" matrices. Differentiation between the common emitter and the common base is shown by using suffixes e or b after i, r, f, or o.



$$\begin{pmatrix} v_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \begin{pmatrix} i_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} h_i & h_r \\ h_f & h_o \end{pmatrix} \begin{pmatrix} i_1 \\ v_2 \end{pmatrix}$$

Figure 1.10 Circuit Network Depicted by "h" Matrix



$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} y_i & y_r \\ y_f & y_o \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix}$$

Figure 1.11 Circuit Network Depicted by "y" Matrix

The physical meanings of each parameter in Figure 1.10 and Figure 1.11 are as follows:

h_i: input impedance

h_r: voltage feedback ratio

h_f: current gain

h_o: output admittance

y_i: input admittance

y_r: reverse transfer admittance

y_f: forward transfer admittance

y_o: output admittance

The h matrix is often used for low-frequency regions, and the y matrix for high-frequency regions.

1.2.2 Matrix Showing the Relations Among Inputs and Outputs by Power

Such phenomena as the reflection and transfer of waves in a microwave circuit (for example, in waveguides and cavity resonators) are usually indicated by an "S" matrix (scattering matrix).

As the frequency limits for semiconductor products expand, the "S" matrix itself is occasionally used as a circuit parameter.

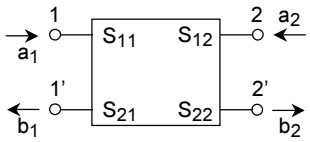
The definition of the "S" matrix is shown in Figure 1.12; the physical meanings of each parameter are as follows:

S_{11}: input reflection coefficient

S_{12}: reverse transfer coefficient

S_{21}: forward transfer coefficient

S_{22}: output reflection coefficient



$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} = \begin{pmatrix} S_i & S_r \\ S_f & S_o \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

Figure 1.12 Circuit Network Depicted by "S" Matrix

Suffix b or e is used to indicate the common base or the common emitter in the same manner as y parameters and h parameters.

Table 1.3 Conversion of Parameters

	[H]	[Y]	[S]
[H]	h_i h_r h_f h_o	$\frac{1}{y_i}$ $-\frac{y_r}{y_i}$ $\frac{y_f}{y_i}$ $\frac{y_i y_o - y_r y_f}{y_i}$	$\frac{(1+S_i)(1+S_o)-S_r S_f}{(1-S_i)(1+S_o)+S_r S_f}$ $\frac{2S_r}{(1-S_i)(1+S_o)+S_r S_f}$ $\frac{-2S_f}{(1-S_i)(1+S_o)+S_r S_f}$ $\frac{(1-S_o)(1-S_i)-S_r S_f}{(1-S_i)(1+S_o)+S_r S_f}$
[Y]	$\frac{1}{h_i}$ $-\frac{h_r}{h_i}$ $\frac{h_f}{h_i}$ $\frac{h_i h_o - h_r h_f}{h_i}$	y_i y_r y_f y_o	$\frac{(1+S_o)(1-S_i)+S_r S_f}{(1+S_i)(1+S_o)-S_r S_f}$ $\frac{-2S_r}{(1+S_i)(1+S_o)-S_r S_f}$ $\frac{-2S_f}{(1+S_i)(1+S_o)-S_r S_f}$ $\frac{(1+S_i)(1-So)+S_r S_f}{(1+S_i)(1+S_o)-S_r S_f}$
[S]	$\frac{(h_i-1)(h_o+1)-h_r h_f}{(h_i+1)(h_o+1)-h_r h_f}$ $\frac{2h_r}{(h_i+1)(h_o+1)-h_r h_f}$ $\frac{-2h_f}{(h_i+1)(h_o+1)-h_r h_f}$ $\frac{(1+h_i)(1-h_o)+h_r h_f}{(h_i+1)(h_o+1)-h_r h_f}$	$\frac{(1-y_i)(1+y_o)+y_r y_f}{(1+y_i)(1+y_o)-y_r y_f}$ $\frac{-2y_r}{(1+y_i)(1+y_o)-y_r y_f}$ $\frac{-2y_f}{(1+y_i)(1+y_o)-y_r y_f}$ $\frac{(1+y_i)(1-y_o)+y_r y_f}{(1+y_i)(1+y_o)-y_r y_f}$	S_i S_r S_f S_o

Table 1.4 Conversion Formulas for "h" Parameters

Known "h" Parameters		Converted "h" Parameters					
		Common Base		Common Emitter		Common Collector	
Common Base				$\frac{h_{ib}}{1+h_{fb}}$	$\frac{\Delta h_b - h_{rb}}{1+h_{fb}}$	$\frac{h_{ib}}{1+h_{fb}}$	1
				$\frac{-h_{fb}}{1+h_{fb}}$	$\frac{h_{oh}}{1+h_{fb}}$	$\frac{-1}{1+h_{fb}}$	$\frac{h_{ob}}{1+h_{fb}}$
Common Emitter		$\frac{h_{ie}}{1+h_{fe}}$	$\frac{\Delta h_e - h_{re}}{1+h_{fe}}$			h_{ie}	$1 - h_{re}$
		$\frac{-h_{fe}}{1+h_{fe}}$	$\frac{h_{oe}}{1+h_{fe}}$			$-(1 + h_{fe})$	h_{oe}
Common Collector		$\frac{-h_{ic}}{h_{fc}}$	$\frac{-\Delta h_c}{h_{fc}} - 1$	h_{ic}	$1 - h_{rc}$		
		$\frac{-(1+h_{fc})}{h_{fc}}$	$\frac{h_{oc}}{h_{fc}}$	$-(1 + h_{fc})$	h_{oc}		

$\Delta h_e = h_{ie} \cdot h_{oe} - h_{re} \cdot h_{fe}$, $\Delta h_b = h_{ib} \cdot h_{ob} - h_{rb} \cdot h_{fb}$, $\Delta h_c = h_{ic} \cdot h_{oc} - h_{rc} \cdot h_{fe}$

Table 1.5 Conversion Formulas for "y" Parameters

Known "y" Parameters		Converted "y" Parameters					
		Common Base		Common Emitter		Common Collector	
Common Base				Σ_{yb}	$-(y_{rb} + y_{ob})$	Σ_{yb}	$-(y_{ib} + y_{ob})$
				$-(y_{fb} + y_{ob})$	y_{ob}	$-(y_{ib} + y_{rb})$	y_{ib}
Common Emitter		Σ_{ye}	$-(y_{re} + y_{oe})$			y_{ie}	$-(y_{ie} + y_{re})$
		$-(y_{fe} + y_{oe})$	y_{oe}			$-(y_{ie} + y_{fe})$	Σ_{ye}
Common Collector		y_{oc}	$-(y_{fc} + y_{oc})$	y_{ic}	$-(y_{ic} + y_{rc})$		
		$-(y_{rc} + y_{oc})$	Σ_{yc}	$-(y_{ic} + y_{rc})$	Σ_{yc}		

$\Sigma y_e = y_{ie} + y_{re} + y_{fe} + y_{oe}$

$\Sigma y_b = y_{ib} + y_{rb} + y_{fb} + y_{ob}$

$\Sigma y_c = y_{ic} + y_{rc} + y_{fc} + y_{oc}$

Table 1.6 "h" Parameters Converted by Early's T-Type Device Parameters

	Common Base		Common Emitter
h_{ib}	$\dfrac{r_e + r_{bb'}\left((1-\alpha_0) + j\dfrac{f}{f_\alpha}\right)}{1 + j(f/f_\alpha)}$	h_{ie}	$r_{bb'} + \dfrac{r_e}{(1-\alpha_0) + j(f/f_\alpha)}$
h_{rb}	$j2\pi f C_c r_{bb'}$	h_{re}	$2\pi f_\alpha C_c r_e \dfrac{j\dfrac{f}{f_\alpha}}{(1-\alpha_0) + j(f/f_\alpha)}$
h_{fb}	$\dfrac{-\alpha_0}{1 + j(f/f_\alpha)}$	h_{fe}	$\dfrac{\alpha_0}{(1-\alpha_0) + j(f/f_\alpha)}$
h_{ob}	$j2\pi f C_c$	h_{oe}	$2\pi f_\alpha C_c \dfrac{j\dfrac{f}{f_\alpha}\left(1 + j\dfrac{f}{f_\alpha}\right)}{(1-\alpha_0) + j(f/f_\alpha)}$

Table 1.7 "y" Parameters Converted by Early's T-Type Device Parameters

	Common Base		Common Emitter
y_{ib}	$\dfrac{1 + j\dfrac{f}{f_\alpha}}{r_e + jr_{bb'}\dfrac{f}{f_\alpha}}$	y_{ie}	$\dfrac{(1-\alpha_0) + j\dfrac{f}{f_\alpha}}{r_e + jr_{bb'}\dfrac{f}{f_\alpha}}$
y_{rb}	$-2\pi f_\alpha C_c \dfrac{j\dfrac{f}{f_\alpha}\left(1 + j\dfrac{f}{f_\alpha}\right)}{\dfrac{r_e}{r_{bb'}} + j\dfrac{f}{f_\alpha}}$	y_{re}	$-2\pi f_\alpha C_c \dfrac{r_e}{r_{bb'}} \dfrac{j\dfrac{f}{f_\alpha}}{\dfrac{r_e}{r_{bb'}} + j\dfrac{f}{f_\alpha}}$
y_{fb}	$-\dfrac{\alpha_0}{r_e + jr_{bb'}\dfrac{f}{f_\alpha}}$	y_{fe}	$\dfrac{\alpha_0}{r_e + jr_{bb'}\dfrac{f}{f_\alpha}}$
y_{ob}	$2\pi f_\alpha C_c \dfrac{j\dfrac{f}{f_\alpha}\left(1 + \dfrac{r_e}{r_{bb'}} + j\dfrac{f}{f_\alpha}\right)}{\dfrac{r_e}{r_{bb'}} + j\dfrac{f}{f_\alpha}}$	y_{oe}	$2\pi f_\alpha C_c \dfrac{j\dfrac{f}{f_\alpha}\left(1 + \dfrac{r_e}{r_{bb'}} + j\dfrac{f}{f_\alpha}\right)}{\dfrac{r_e}{r_{bb'}} + j\dfrac{f}{f_\alpha}}$

Note: The common base parameter y_{ob} and the common emitter parameter y_{oe} are identical.

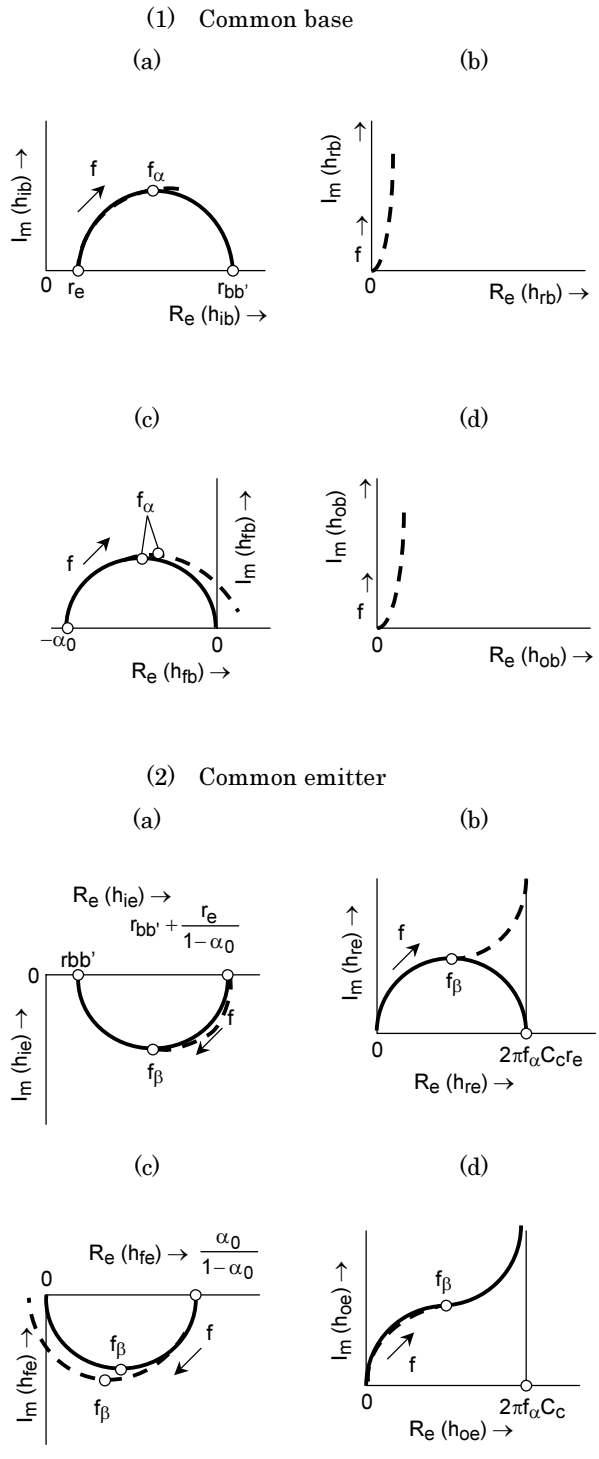


Figure 1.13 Frequency Locus of "h" Parameters

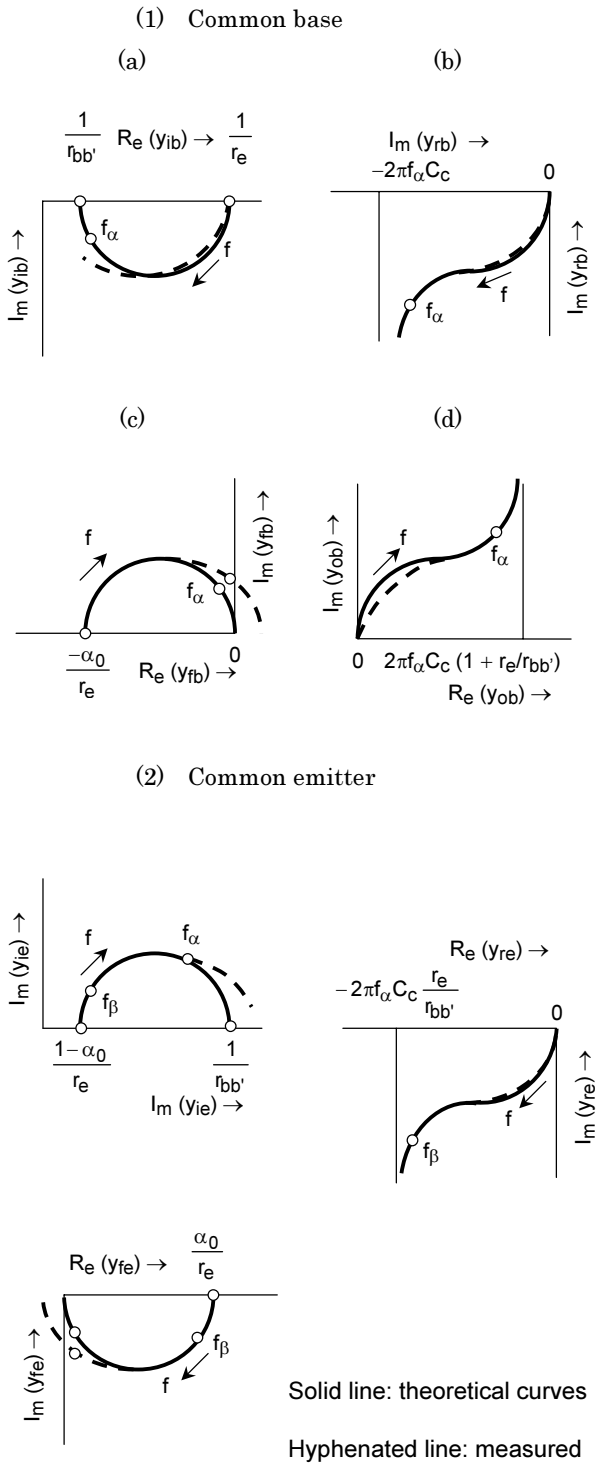


Figure 1.14 Frequency Locus of "y" Parameters

Please refer to Table 1.3, Table 1.4, and Table 1.5 for the correlation and conversion among circuit parameters of common base and common emitter. Figure 1.13, and Figure 1.14 show the frequency locuses of "h" and "y" parameters obtained from Table 1.6, and Table 1.7.

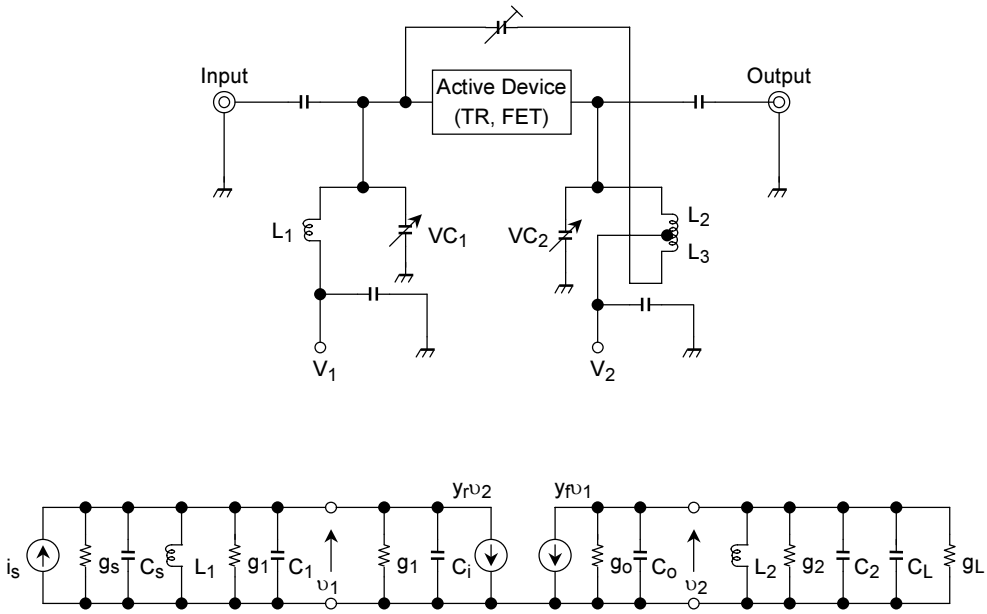
The above-mentioned parameters vary according to the operating points and temperature, and circuit designers must allow for such variations.

2. Gain and Stability

Figure 2.1 shows the basic high-frequency amplification circuit of a transistor/FET and the FET's equivalent circuit.

When this amplification circuit is tuned to the center frequency, the capacitance is removed and only the conductance remains, as shown in the equivalent circuit in Figure 2.2.

In this circuit, if both the capacitance and the conductance are neutralized, it can be assumed that $|yr| \simeq 0$. The same assumption that $|yr| \simeq 0$ can also be made for active devices with small reverse transfer capacitance, such as cascaded FETs. Also, when the unloaded Q in the I/O coil is large, and when the loss conductances g_1 and g_2 are ignored, a circuit of simple configuration can be constructed as shown in Figure 2.3.



i_s: constant signal current source

g_s, C_s: signal source conductance, capacitance

g_i, C_i: input conductance, capacitance

L_1, L_2: I/O tuning inductance

g_o, C_o: output conductance, capacitance

g_1, g_2: power loss conductance of an I/O coil

g_L, C_L: load conductance, capacitance

C_1, C_2: load conductance in external I/O

Figure 2.1 Basic High-Frequency Amplifier Circuit and its Equivalent Circuit

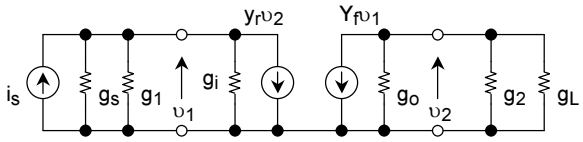


Figure 2.2 Equivalent Circuit (tuned frequency)

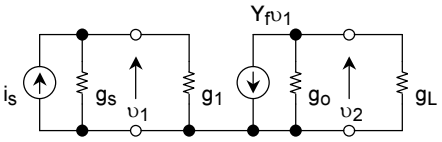


Figure 2.3 Unidirectional Equivalent Circuit

We now find the power gain of the equivalent circuit.

$$G_p = \frac{P_o}{P_i\ (max)} = \frac{|\upsilon_2|^2 g_L}{|i_s|^2/4g_s} \quad \text{..... (1)}$$

Combining with

$$\upsilon_2 = \frac{yf\,\upsilon_1}{g_o + g_L},\ i_s = -\upsilon_1(g_s + g_i)$$

we obtain

$$G_p = \frac{4|y_f|^2 g_s g_L}{(g_s + g_i)^2(g_o + g_L)^2} \quad \text{..... (2)}$$

When $g_s = g_i$, and $g_L = g_o$ the power gain becomes maximum; these conditions are met when the input and the output are matched.

$$G_p(max) = \frac{|y_{fs}|^2}{4g_i g_o} \quad \text{..... (3)}$$

Gp (max) is the Maximum Available Gain (MAG) that can be achieved when the circuit and device impedance are matched at both the input and output interfaces, while input-to-output signal transfer is unidirectional.

Therefore, in practice, stability gain must be considered as well as power gain.

The active device stability coefficient s is

$$S = \frac{2g_i \cdot g_o}{1 + \cos(\phi_r + \phi_f)|y_r| \cdot |y_f|} \quad \text{..... (4)}$$

Where ϕ is the phase angle of the y parameter

$$\begin{cases} \phi_r = \tan^{-1}(b_r/g_r) \\ \phi_f = \tan^{-1}(b_f/g_f) \end{cases}$$

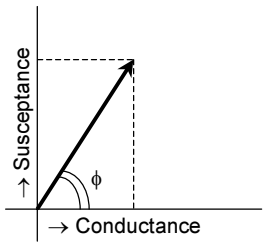


Figure 2.4 Phase Angle Diagram

The stability coefficient is calculated from the device's y parameter, and, if s > 1, the device can be deemed stable without considering the I/O circuit; however, when s ≦ 1, there is a danger that the I/O circuit may cause oscillation.

In a high-frequency amplifier circuit, total stability S is expressed in terms of Gi and Go.

$$S = \frac{2}{1+\cos(\phi_r+\phi_f)} \cdot \frac{G_i \cdot G_o}{|y_r||y_f|} \quad \cdots\cdots (5)$$

Where $G_i = g_s + g_1 + g_i$

$G_0 = g_0 + g_2 + g_L$

The relationship between S and the stability coefficient of a device (s) can be expressed as follows

$$S = \frac{G_i G_o}{g_i g_o} \cdot s$$

$$= \left(1+\frac{g_s+g_1}{g_1}\right)\left(1+\frac{g_L+g_2}{g_o}\right) \cdot s \quad \cdots\cdots (6)$$

$S \geqq s$

In other words, the circuit stability can be increased by selecting larger g_s, g_L, g_1, or g_2.

When the input and output are matched, even though the loss conductance of the coil is (g_1, g_2) = 0,

$$\begin{cases} G_i = g_s + g_i = 2g_i \\ G_o = g_o + g_L = 2g_o \end{cases}$$

$S = 4\ s$

and total circuit stability four times greater than that of the device alone can be attained.

Power gain G_p can be expressed as a function of S:

$$G_p = \frac{1}{S} \cdot \frac{2}{1+\cos(\phi_r+\phi_f)} \cdot \frac{|y_f|}{|y_f|} \quad \cdots\cdots (7)$$

This formula can be changed to

$$G_p = \frac{4}{S} \cdot \frac{2}{1+\cos(\phi_r+\phi_f)} \cdot \frac{g_i \cdot g_o}{|y_r||y_f|} \cdot \frac{|y_f|^2}{4g_i g_o} \quad \cdots\cdots (8)$$

$$= \frac{4s}{S} \cdot G_p(\max) \quad \cdots\cdots (9)$$

An S value of at least 4 ($S \geqq 4$) indicates good circuit stability.

$G_p \leqq s \cdot G_p\ (\max)$ ..... (10)

If $S \leqq 1$, indicating poor device stability the MAG of the device is upper limit of the power gain which can be attained in the circuit.

Table 2.1 shows the G_p of a high-frequency transistor/FET when MAG and S = 4.

Table 2.1 Gain and Stability (example)

f = 100 MHz

		MAG (dB)	s	G_{ps} (dB)
TR	2SC1923	34.9	0.030	19.6
J-FET	2SK192A	26.9	0.023	10.5
	2SK161	26.4	0.265	20.7
MOS FET	2SK241	34.0	0.120	24.8

Several methods are available for achieving stable gain in high-frequency circuits. The most popular circuit-design-based method is to avoid feedback by installing a neutralized circuit. Figure 2.5 shows an example.

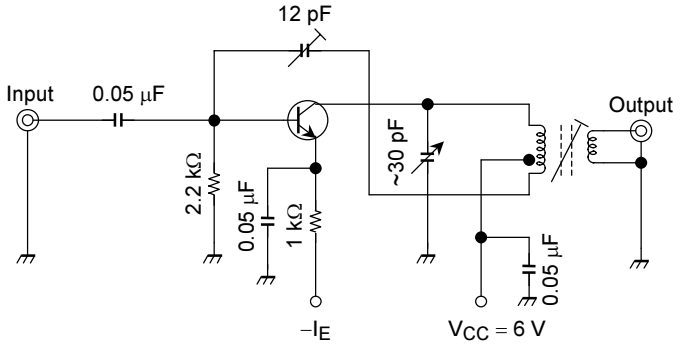


Figure 2.5 2SC380TM 10.7 MHz Amplifier Circuit

Another method is to lower the feedback capacitance by means of a cascode connection. Figure 2.6 is a typical example of a cascode-connected circuit.

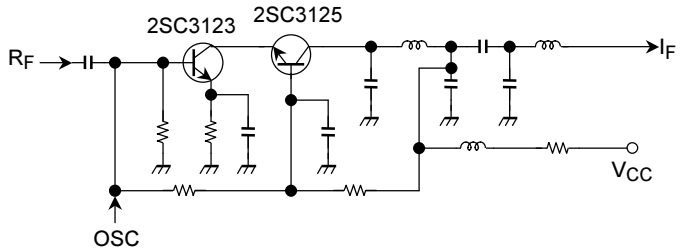


Figure 2.6 TV Tuner VHF Mixer Circuit

The Faraday shield (electrostatic screen) method is used to protect transistors from interference generated by other active devices.

In the case of FETs, construction of devices with cascode connections inside the devices such as cascode FETs and dual MOSFETs are equivalent to the Faraday shield method.

3. Hight-Freguency 3-Pin MOSFET

This 3-pin MOSFET is a new device that leads current electronics technology.

Prior to introduction of this further innovation, the dual-gate MOSFET has been the most popular type of conventional high-frequency MOSFET.

In this device, Gate 2 already had features offering several advantages when compared to junction-type FETs or bipolar transistors.

Generally, Gate 2 can be used as the local oscillation signal injector terminal for mixer circuits, and an AGC terminal.

However, there is an alternative application technique for dual-gate MOSFETs, as shown in Figure 3.1. This shows a typical high-frequency amplifier in a Hi-Fi tuner. In the circuit depicted by this figure, Gate 2 is used only as a DC fixed-bias terminal, in order to achieve power gain.

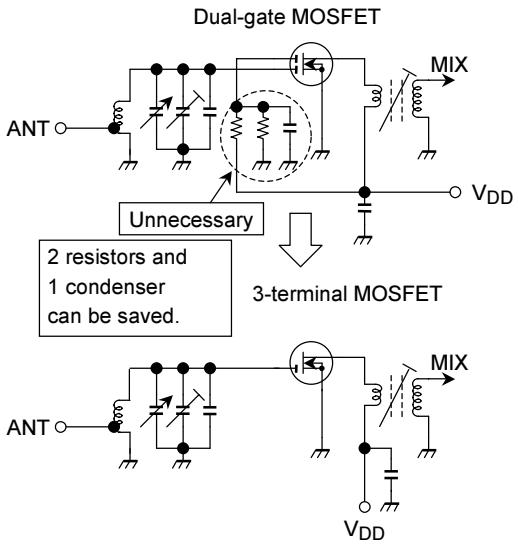


Figure 3.1

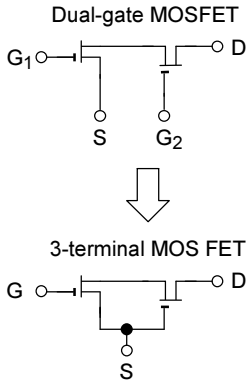


Figure 3.2

Assuming that a dual-gate MOSFET can achieve good performance when the Gate 2 bias voltage is zero, Gate 2 only needs to be grounded; however, in practice, in this device Gate 2 has to be biased in a voltage range of 3 to 5 V.

Passive components required for this purpose are at least two resistors and one capacitor.

However, a 3-terminal MOSFET does not require such components, yet can achieve the same characteristics as a dual-gate MOSFET.

The 3-terminal MOSFET is a cascode-connected device, in which Gate 2 of the dual-gate MOSFET is connected to the source.

In addition, special consideration has been given to maintaining excellent performance even when Gate 2 is zero biased: this is achieved by using the channel control from the Gate 2 side.

Moreover, our original manufacturing technique allows reliability is improved by a decrease in the amount of bonding.

Three types of packages are available, suitable for current compact FM tuners: Mini Mold (2SK241), Super Mini (2SK302), and Ultra Super Mini (2SK882).

4. AGC for Dual-Gate MOSFET

4.1 Typical AGC Circuit in Dual-Gate MOSFETs

Dual-gate MOSFET AGC (automatic gain control) is achieved by changing the bias of Gate 2. This type of control is used mainly for the RF stage in TVs (VHF/UHF) and in FM tuners. Figure 4.1 shows a typical example of a bias circuit.

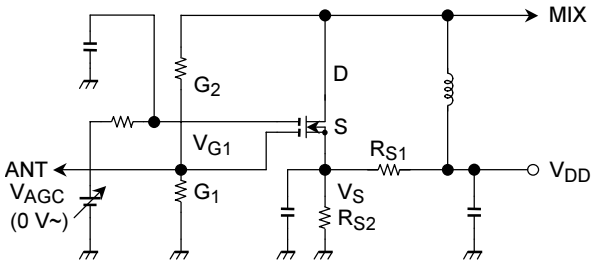


Figure 4.1 Typical AGC Circuit in a Dual-Gate MOSFET

One point requiring particular attention in the design of this circuit, shown in the figure, is the proper setting of V_{G1} and V_S. Briefly, the I_D-V_{G1S} operation point locus in Gate 2, V_{AGC}, is determined by the setting of V_{G1} and V_S. This is because there is a close relationship between the I_D-V_{G1S} operation point locus, and the device's gain reduction and cross-modulation characteristics. The I_D-V_{G1S} operation point and the cross modulation characteristics are described below.

4.2 Relationship Between V_{G1S} and Cross Modulation, $|y_{fs}|$, I_D

The characteristics shown as a representative example in Figure 4.2 relate both forward conductance $|y_{fs}|$ and cross-modulation (undesired signal level) to the Gate 1-to-source voltage V_{G1S}.

Three "good" points corresponding to peaks of the cross-modulation curve (D, E, F) of the 1% cross modulation characteristic in the $|y_{fs}|$-versus-V_{G1S} characteristics can be seen; and three "bad" points corresponding to off-peak cross-modulation values (A, B, C) can also be seen.

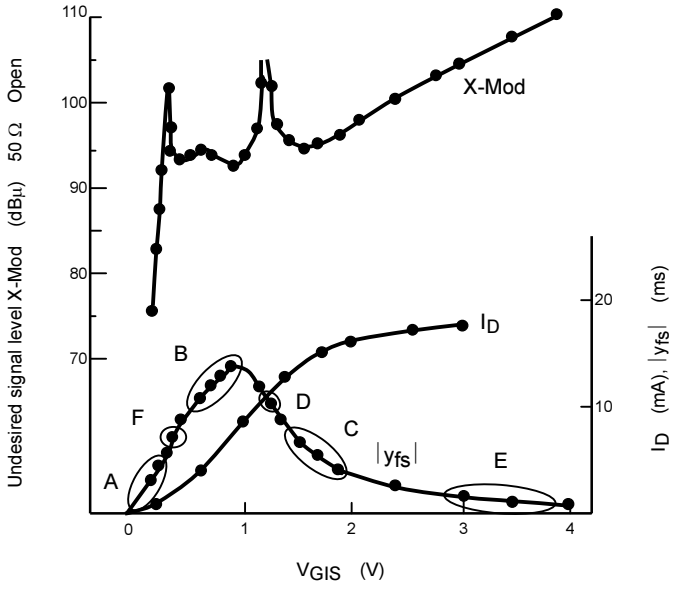


Figure 4.2 I_D, $|y_{fs}|$, X-Mod–V_{G1S} Characteristics

In short, the figure shows that in a region with a sharp $|y_{fs}|$–V_{G1S} curve, the second-order $|y_{fs}|$ (third-order I_D) term is large, and therefore is bad; regions of the $|y_{fs}|$ curve which are nearly linear are good since secondary $|y_{fs}|$ is small. Explanation of each point is as follows.

4.2.1 Point A

This point is that in a dual-gate MOSFET, in the section close to the OFF state of the front-stage FET, which is similar to that of a single-gate FET or to a bipolar transistor's reverse AGC, the place where GR (gain reduction) is large actually has very poor cross-modulation characteristics. Therefore, in a dual-gate FET, it is strongly advisable not to allow Gate 1's operation point, having a large GR, to fall in the A range in which AGC is applied at Gate 2.

4.2.2 Point B

From the viewpoint of the I_D–V_{G1S} (or $|y_{fs}|$–V_{G1S}) characteristic, this is the point where the rear-stage FET starts to have an effect (the front-stage FET, however, is controlled by the A and F points). This is a point that exists at all times if the device is a dual-gate FET. The V_{G1S} at this point is characterized by V_{G2S} becoming smaller, as V_{G2S} moves close to the V_{G1S} (OFF) state, and the cross-modulation tends to worsen. However, this point is passed through when the actual GR is small (V_{G2S} is large). Therefore, mounting the device on a tuner is not a problem since the cross-modulation of the FET is buried by the cross modulation (of the mixer) which follows the RF amplifier stage.

4.2.3 Point C

From point B which is affected by the rear-stage FET, I_D–V_{G1S} characteristics is one step before being more affected by the rear-stage FET. It's like point B, this point exists if a device is the dual-gate FET. The point's position on V_{G1S}. The cross-modulation shows bad same as point B. However, this problem that is different form point B arises. If the cross-modulation is bad on this point, that affects tuner characteristics to be bad because the GR (gain reduction) is passing through GR = 10 to 30dB.

4.2.4 Point D, F

Between the "bad" points A and B with poor cross-modulation, and similarly between B and C, there must exist two "good" points D and F. In other words, when I_D is taken as a Taylor series expansion of V_{G1S}, the third-and first-order terms, exhibit counter-action changes in magnitude, and being opposite in sign inevitably a point is eventually reached at which the sum of the third-and first-order terms equals zero. These points of inflection are in principle very desirable as operating points. However, in practice it is difficult to use them in design because they are difficult to locate precisely.

4.2.5 Point E

With respect to I_D–V_{G1S} (or $|y_{fs}|$–V_{G1S}) characteristics, this is a point strongly affected by the rear-stage FET characteristics. One feature of this section is that GR is relatively large and cross modulation is good (This is the most advantageous feature of a dual-gate FET). Note that for lower V_{G2S} values, the $|y_{fs}|$ curve becomes flatter and the ranges of V_{G1S} corresponding to desirable nearly-linear segments of the curve become wider gain reduction.

When applied AGC is to V_{G2S}, the device must be designed to place its operating point at point E which corresponds to V_{G1S} values where gain reduction is high, in order to make best use of the advantages of a dual-gate FET.

4.3 AGC Circuit Design in Dual-Gate FET

In short considering the dual-gate FET's cross-modulation characteristic, good AGC circuit design requires careful selection of the I_D-V_{G1S} operation point locus. The relationship between the I_D-V_{G1S} operation point locus and the cross modulation characteristic is given below, based on the actual test data. A dual-gate MOSFET for TV/VHF tuner RF, the 3SK126, was used for this illustration.

Operation point locus [1] in Figure 4.3 shows an example of a poor design which does not reach point E when V_{G2S} is small (GR is large); the 1% cross modulation characteristic in Figure 4.4 shows the poor result where GR is large. On the other hand, operation point loci [2] and [3] reach Point E where V_{G2S} is small, and the 1% cross modulation characteristic is better where GR is large. Also, for Point B (near GR = 4dB in Figure 4.4) and Point C (near GR = 15dB in Figure 4.4), the operating point loci [2] and [3] are better when compared to [1]. This is because in each of these cases the operating point locus passes through Points B and C where V_{G2S} is large, in the order [3], [2], [1]. Therefore when designing a circuit, if the operation point locus is placed on Point E where GR is large and cross modulation is in good condition (for [2] and [3]), the cross modulation characteristic at Point GR will automatically be good.

We now have sufficient information to derive the values of V_{G1}, V_S, R_{S1} and R_{S2} for the 3SK126, with reference to the circuit shown in Figure 4.1.

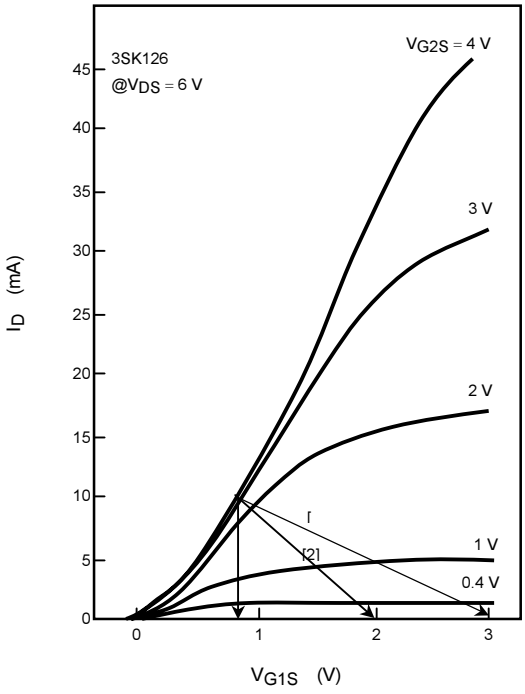


Figure 4.3 I_D vs. V_{G1S}

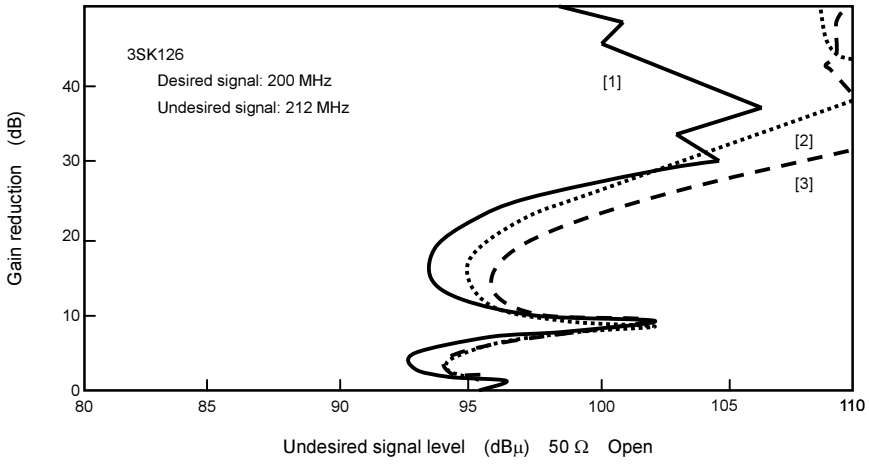


Figure 4.4 1% Cross Modulation Characteristics

First, the FET must be completely in the OFF state, with V_{AGC} = 0 V; Some allowance must be made for variation in $V_{S|I_D}$ = 0.

$V_{S|I_{D\,=\,0}} = 1 - V_{G2S\ (OFF)}$ (V)..... (1)

Next for V_{G1}, V_{G1S} (= $V_{G1} - V_{S|I_{D\,=\,0}}$) is required to be at Point E, under the conditions of V_{AGC} = 0 and $V_{S|I_D}$ = 0 = 1 − $V_{G2S\ (OFF)}$. When operation locus [3] in Figure 4.3 is used, V_{G1} becomes

$V_{G1S} = V_{G1S\ (OFF)} + 3$ V..... (2)

Therefore,

$V_{G1} = V_{G1S\ (OFF)} + V_{S|I_D\,=\,0} + 3$ V..... (3)

When equation (1) is substituted in (3),

$V_{G1} = 4$ V + $V_{G1S\ (OFF)}$ (V)..... (4)

Also when GR = 0dB, V_{G2S} = 3 V, and I_D = 10 mA, one can determine V_{AGC} max, R_{S1}, and R_{S2} as follows:

$R_S = R_{S1}\,R_{S2}/(R_{S1} + R_{S2})$..... (5)

$V_{G1S|V_{G2S}\,=\,3\ V}$, I_D = 10 mA = $V_{G1} - (V_{S|I_{D\,=\,0}} + R_S \times 10$ mA)..... (6)

$V_{G2S} = V_{AGC}$ max − $(V_{S|I_{D\,=\,0}} + R_S \times 10$ mA) = 3 (V)..... (7)

and the design is completed by setting

$R_S = (V_{G1} - V_{S|I_{D\,=\,0}} - V_{G1S|V_{G2S}\,=\,3\ V}$, I_D = 10 mA)/10 mA (Ω)..... (8)

V_{AGC} max = 3 + $V_{S|I_{D\,=\,0}} + R_S \times 10$ mA (V)..... (9)

Using Figure 4.3 as a reference, when $V_{G1S\ (OFF)} = 0$ V, $V_{G2S\ (OFF)} = 0$ V, $V_{GIS \mid V_{G2S}} = 3$ V, and $I_D = 10$ mA = 0.92 V, the $V_{S \mid I_{D=0}}$, V_{G1}, R_S, V_{AGC} range becomes

$V_{S \mid I_{D=0}} = 1$ V

$V_{G1} = 4$ V

$R_S = 208\ \Omega$

$V_{AGC} = 0$ V to 6.08 V

Also, when V_{DS} is under 6 V, GR = 0dB ($V_{G2S} = 3$ V、 $I_D = 10$ mA), the value of V_{DD} is found as follows:

$V_{DD} = V_{S \mid I_{D=0}} + R_S \times 10\ mA + V_{DS \mid V_{GS=3\ V}}$, $I_D = 10$ mA

$= 1\ V + 2.08\ V + 6\ V$

$= 9.08$ V

Finally, R_{S1} and R_{S2} must be found:

$R_S = R_{S1}\ R_{S2}/(R_{S1} + R_{S2}) = 208\ \Omega$ ..... (10)

$V_{S \mid I_{D=0}} = V_{DD}\ R_{S2}/(R_{S1} + R_{S2}) = 9.08 \times R_{S2}/(R_{S1} + R_{S2}) = 1$ V .....(11)

When equation (10) is divided by equation (11),

$R_{S1}/9.08 = 208$

$\therefore R_{S1} = 208 \times 9.08 = 1.89\ k\Omega$

Therefore, $R_{S2} = 234\ \Omega$

This completes the AGC circuit design for the dual-gate FET. Note that the cross-modulation characteristics have been considered at each step.

5. Inter-Modulation and Cross Modulation

In general, output current and input voltage for semiconductor amplifiers (bipolar transistors, FETs) are related as follows:

$$I_C = a_0 + a_1V_{be} + a_2V_{be}^2 + a_3V_{be}^3 + a_4V_{be}^4 + a_5V_{be}^5 + \cdots \quad (1)$$

(For FETs, $I_C \Rightarrow I_d$, $V_{be} \Rightarrow V_{gs}$)

Here, when two signals of angular frequencies ω_1, and ω_2 are input, the output signal frequency will be complex, comprised of several different components including V_{be}^2, V_{be}^3, etc.

The input signal is calculated as follows.

$$V_{be} = V_1\sin\omega_1 t + V_2\sin\omega_2 t \quad (2)$$

Then, equation (1) is substituted in equation (2). But to simplify the resulting formula, terms of higher order then V_{be}^3 can be ignored.

$$I_C = a_0 + a_1 (V_1\sin\omega_1 t + V_2\sin\omega_2 t)$$

$$+\frac{1}{2}a_2\left(V_1^2 + V_2^2\right) - \frac{1}{2}a_2\left(V_1^2\cos 2\omega_1 t + V_2^2\cos 2\omega_2 t\right) \pm a_2V_1V_2\cos\left(\omega_1 \mp \omega_2\right)t$$

$$+\frac{3}{4}a_3\left(V_1^3\sin\omega_1 t + V_2^3\sin\omega_2 t\right) - \frac{1}{4}a_3\left(V_1^3\sin 3\omega_1 t + V_2^3\sin 3\omega_2 t\right)$$

$$+\frac{3}{4}a_3\left\{V_1^2V_2\sin\left(\mp 2\omega_1 - \omega_2\right)t + V_1V_2^2\sin\left(\mp 2\omega_2 - \omega_1\right)t\right\}$$

$$+\frac{3}{2}a_3\left\{V_1^2V_2\sin\omega_2 t + V_1V_2^2\sin\omega_1 t\right\} \quad (3)$$

In equation (3), ⬚ represents the inter-modulation term and ▭ represents the cross modulation. Figure 5.1 shows a spectrum diagram equation (3) figure.

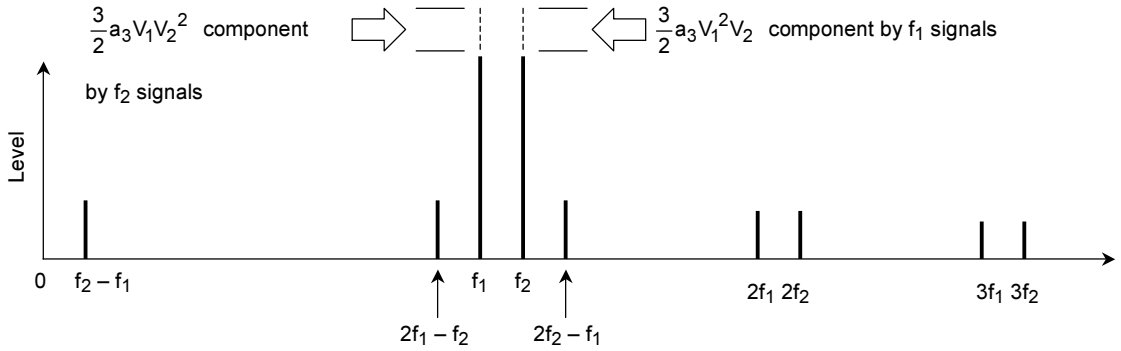


Figure 5.1

5.1 Inter-Modulation

On both sides of two neighboring signals f_1 and f_2, two frequency components ($2f_1 - f_2$, $2f_2 - f_1$) appear in a region equal in width to the difference between the two desired signals. This is generally called IMD third-order distortion.

In transmitters, inter-modulation problems occur mainly because in SSB and FM-modulation transmitters, signals may interfere with neighboring channels when inter modulation is severe.

In tuners, inter-modulation problems occur because, if there are three broadcasting stations (f_1, f_2, f_3), and if a tuner is tuned to f_1, the f_1 signals are affected by f_2 and f_3 signals in the relations of $f_1 = 2f_2 - f_3$ or $f_1 = 2f_3 - f_2$.

Measurement and expression of inter-modulation are as follows.

(1) Input signals f_1 and f_2 are derived with the same power level.

(2) IMD third-order distortion is expressed by the difference (mdB) between the f_1 (or f_2) output level and the $2f_1 - f_2$ (or $2f_2 - f_1$) output level. The IMD third-order distortion becomes worse with increasing input or output power levels.

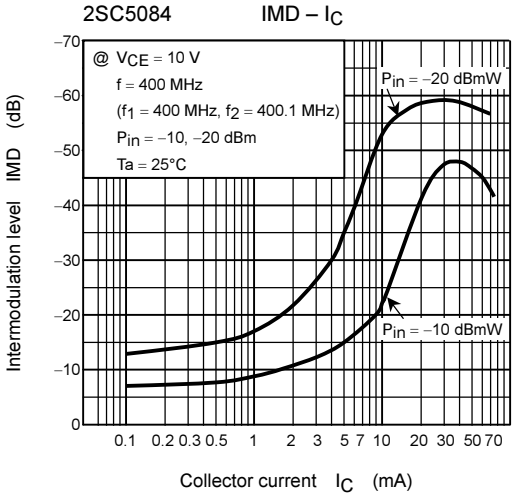


Figure 5.2 Inter-Modulation Characteristics (2SC5084)

5.2 Cross Modulation

When there are two neighboring signals f_1 and f_2, the f_2 (or f_1) signal affects f_1 (or f_2). For example, when tuned by a non-modulated signal f_1, the modulated f_2 signal affects the f_1 signal and creates f_2 modulated signals in wave-detection output.

This problem arises in TV tuners when there are neighboring broadcasting stations f_1 and f_2. When tuned to station f_1, its video and audio signals are affected by the powerful station f_2 video and audio signals.

All illustration of measurement and expression of cross modulation follows:

(1) Example conditions: The desired signal is f_1 and the undesired signal is f_2, the f_1 signal is unmodulated and the f_2 signal has 30% AM modulation at 1 kHz.

$e_1 = E_1 \sin\omega_1 t$

$e_2 = E_2 (1 + m_2 \cos\omega m_2 t) \sin\omega_2 t$

in which m2: undesired signal modulation ratio (0.3)

$\omega m2$: modulation angular frequency (fm_2 = 1 kHz)

(2) When signals e_1 and e_2 defined above are input, cross-modulation appears on the same frequency as the desired signal, as shown by equation 3.

$$I_C \approx a_1 E_1 \left(1 + 3 \cdot \frac{a_3}{a_1} \cdot m_2 {E_2}^2 \cos\omega m_2 t\right) \sin\omega_1 t$$

As shown by the above equation, the required f_1 signal (originally unmodulated) is modulated by the undesired signal f_2. The modulation ratio m_K' is defined by (or some such see next question below) the following equation.

$$m_K = 3 \cdot \frac{a_3}{a_1} \cdot m_2 \cdot {E_2}^2 \cdot (\text{percent})$$

The modulated signal is expressed by

$I_C = a_1 E_1 \{1 + m_1 \cos\omega m_1\} \sin\omega_1 t$

in which m_1: desire signal modulation ratio (0.3)

ωm_1: modulation angular frequency (fm_1 = 1 kHz)

Therefore, the cross modulation exponent is

$$K_C = \frac{m_K}{m_1} = \frac{3 a_3 m_2 {E_2}^2}{a_1 m_1}$$

In general, cross modulation is expressed by the level of the undesired signal E_2 where $K_C = 0.01$. Therefore, when $m_1 = 0.3$, $m_2 = 0.3$,

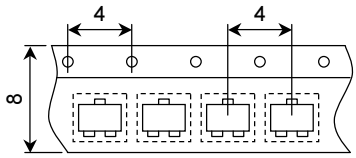
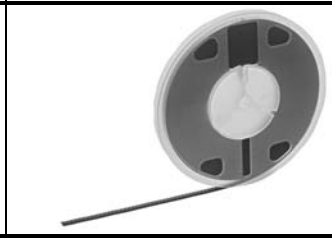
$$E_2 = \sqrt{\frac{1}{300} \cdot \frac{a_1}{a_3}}$$

This shows that E_2 becomes larger if the distortion component is smaller (smaller a_3), thus lessening the interference problem.

6. Tape Packing Specifications

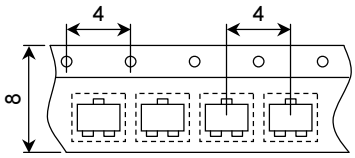
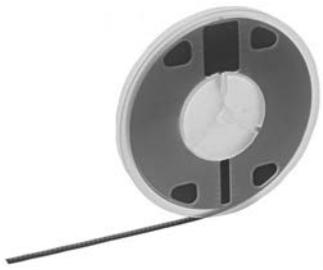
6.1 Tape Specifications by Type of Device Package

6.1.1 ○ Super-Mini Package Group: S-MINI, SMQ, SMV (SSOP5-P-0.95) and SM6 (SSOP6-P-0.95)
○ Ultra-Super-Mini Package Group: USM, USQ, USV US6
○ Small Super-Mini (SSM)
○ Extremely Thin Super-Mini Package (TESM)
○ Ultra-Super-Mini and Thin Package (TU6)

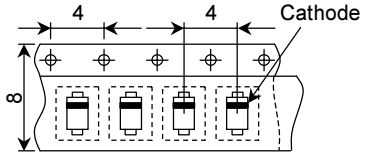
Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Packing Quantity
Embossed tape	TE85L			3000 per reel (Note 1)
	TE85L2 (only for s-mini, SMV and USM)			10000 per reel

Note 1: TESM: 4000 per reel.

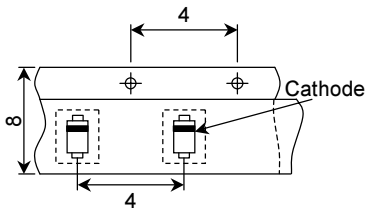
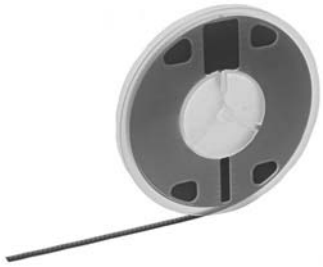
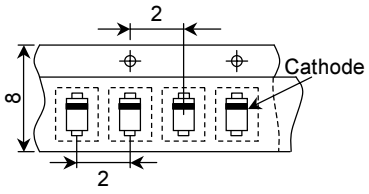
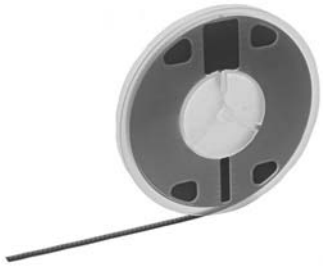
6.1.2 Super-Mini Package for Varicap Diode

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Pair	Packing Quantity
Embossed tape	TPH2			○	3000 per reel
	TPH3			×	
	TPH4			○	
	TPH6			○	600 to 3000 per reel
	TPH7			○	3000 per reel

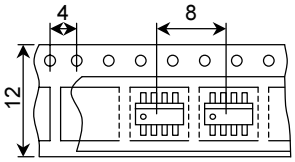
6.1.3 Ultra-Super-Mini Coaxial Package (USC)

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Pair	Packing Quantity
Embossed tape	TPH2			○	2400 to 3000 per reel
	TPH3			×	3000 per reel
	TPH4			○	2400 to 3000 per reel

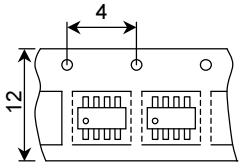
6.1.4 Extreme-Super-Mini Coaxial Package (ESC)
Extremely Thin Super-Mini Coaxial Package (TESC)

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Pair	Packing Quantity
Embossed tape	TPH2			○	3200 to 4000 per reel
	TPH3			×	4000 per reel
	TPL2			○	6400 to 8000 per reel
	TPL3			×	8000 per reel

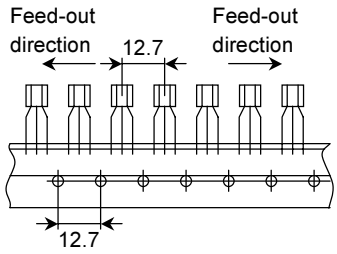
6.1.5 Flat-Mini Package (FM8)

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Packing Quantity
Embossed tape	TE12L			1000 per reel

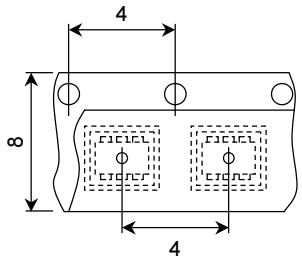
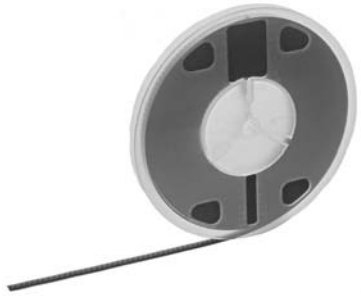
6.1.6 Flat-Super-Mini Package (SM8) (SSOP8-P-0.65)

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Packing Quantity
Embossed tape	TE12L			3000 per reel

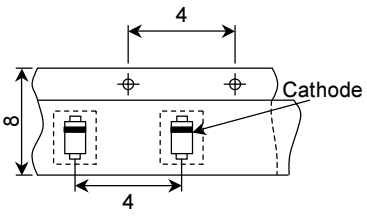
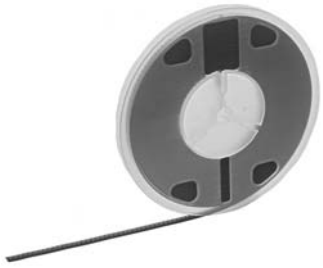
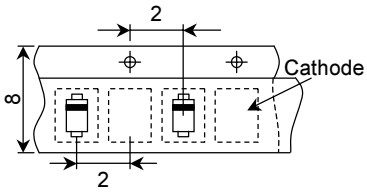
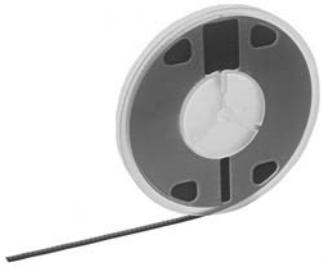
6.1.7 Mini Package (MINI)

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Packing Quantity
Ammo pack	TPE4			5000 per carton

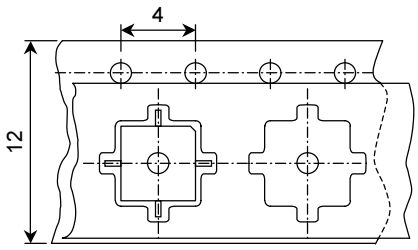
6.1.8 Extreme-Super-Mini Package (ES6)
sES6

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Packing Quantity
Embossed tape	TE85L			4000 per reel

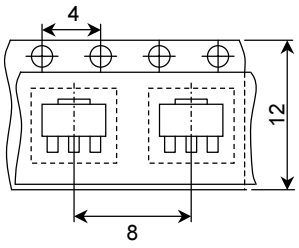
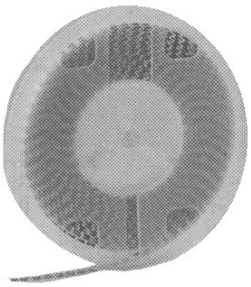
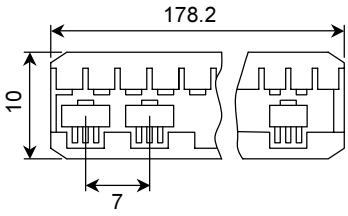
6.1.9 Extreme-Super-Mini Coaxial Package (sESC)

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Pair	Packing Quantity
Embossed tape	TPH3			×	5000 per reel
	TPL3			×	10000 per reel

6.1.10 PW-X Package

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Packing Quantity
Embossed tape	TE12L			1000 per reel

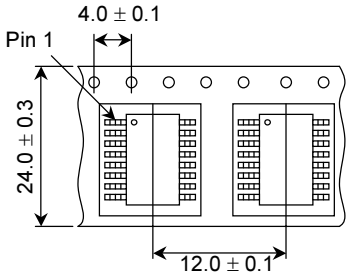
6.1.11 Power Mini Transistor Package (PW-MINI)

Packing Type		Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Packing Quantity
Tape	Pack type	TE12L			1000 per reel
Magazine	Stick type	—			25 per magazine

6.1.12 TO-92/Mini Devices

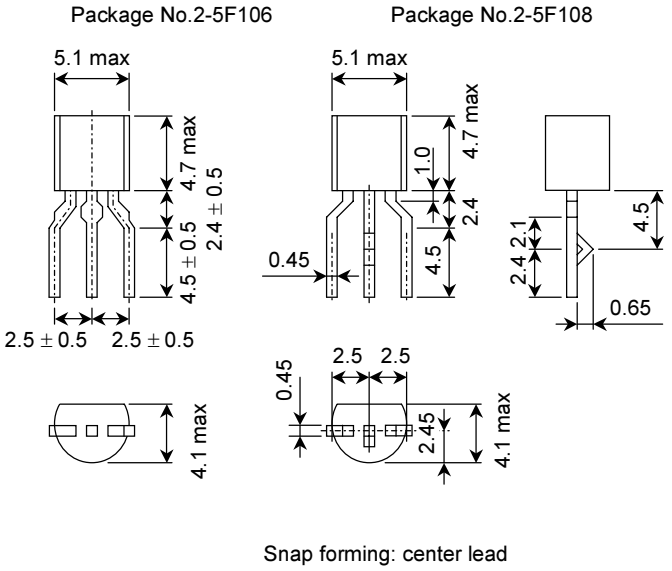
Tape Type Suffix	Applied Package Type	Packing Type	Packing Quantity	Reel Appearance
TPE2	TO-92 (2-5F)	Ammo pack	3000 pcs	
TPE4	MINI (2-4E)	Ammo pack	5000 pcs	

6.1.13 Shrink Small Outline Package (SSOP20-P-225-1.0)

Packing Type	Tape Type Suffix	Tape Dimensions (unit: mm)	Reel Appearance	Packing Quantity
Embossed tape	EL			2000 per reel

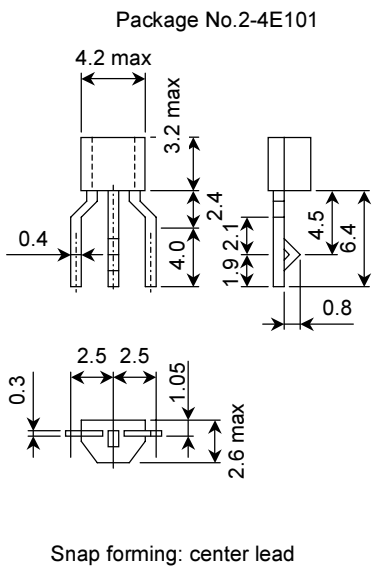
6.2 Lead Formed TO-92 and Mini Transistor Package Dimensions

Unit: mm



Snap forming: center lead

Figure 6.1 Lead-Formed TO-92 Transistor Package Dimensions



Snap forming: center lead

Figure 6.2 Lead-Formed Mini Transistor Package Dimensions

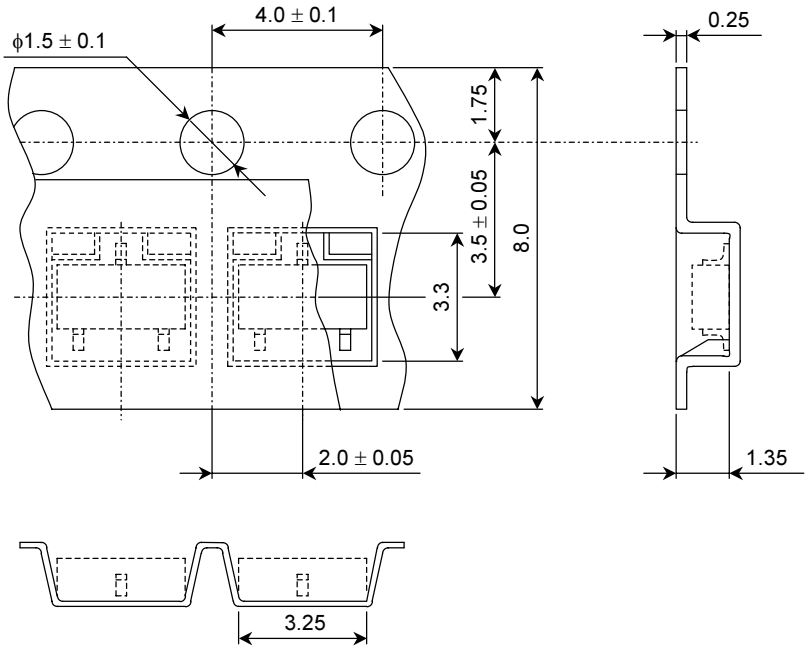
6.3 Tape Dimensions

6.3.1 Tape Layout for 3-Pin Super-Mini Package…(S-MINI)

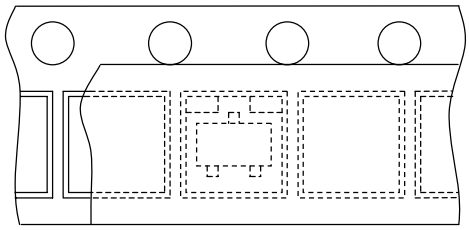
This is a tape specification for 3-pin super mini-FETs and diodes. The diagram below shows the TE85L tape specification.

New Tape Dimensions for Super-Mini Package Dimension Example: TE85L

Unit: mm

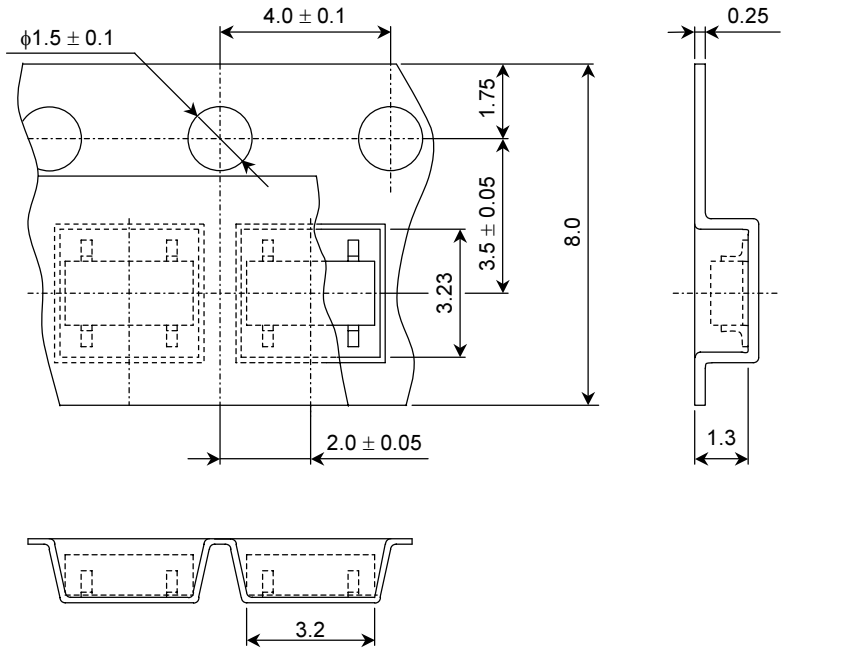


Device Orientation

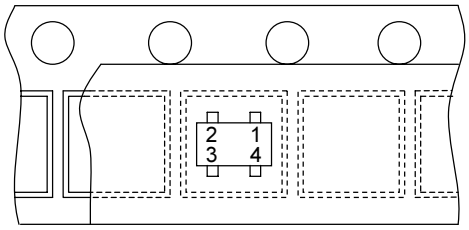


6.3.2 Tape Layout for 4-Pin Super-Mini Package…(SMQ)

Unit: mm

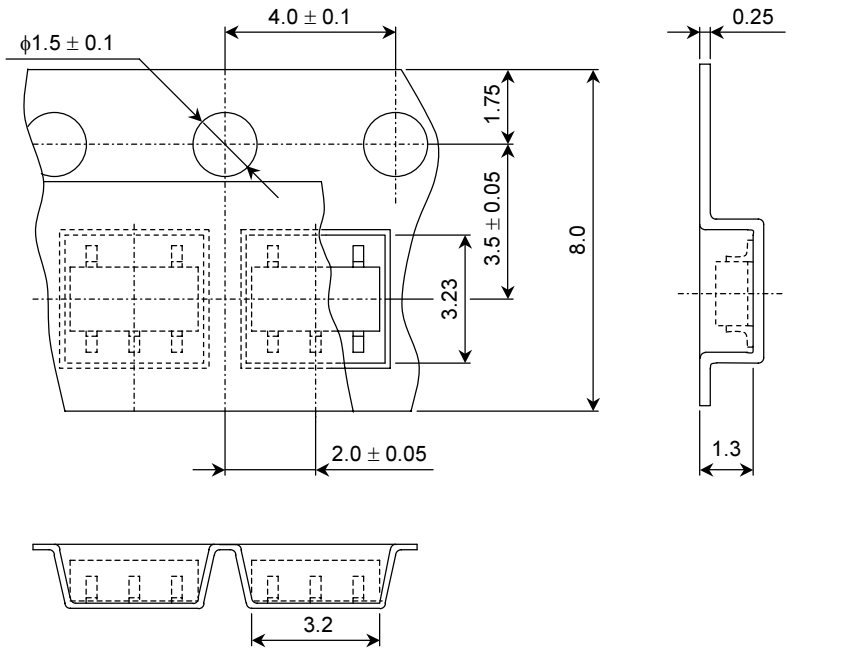


Device Orientation

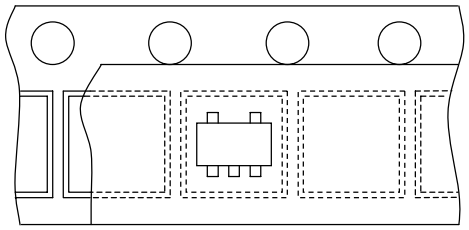


6.3.3 Tape Layout for 5-Pin Super-Mini Package…(SMV) (SSOP5-P-0.95)

Unit: mm

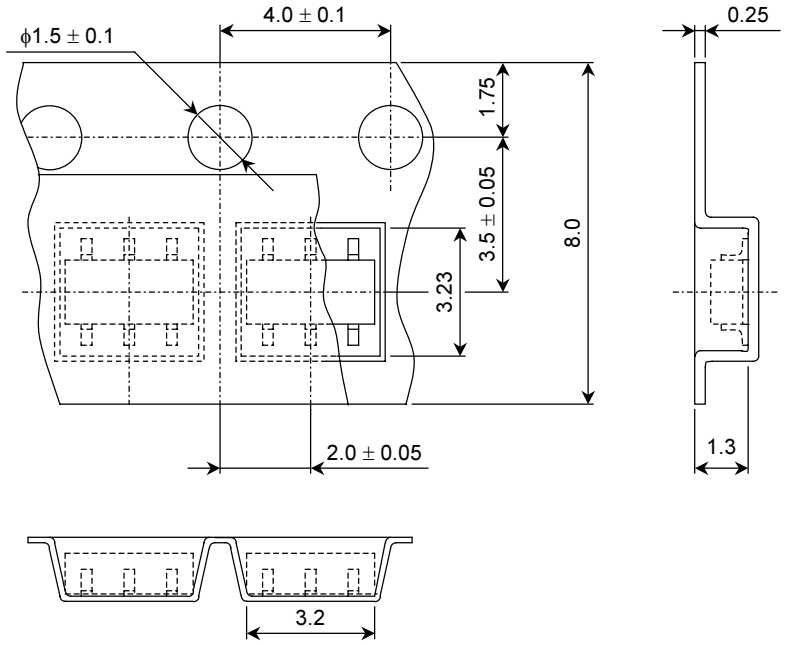


Device Orientation



6.3.4 Tape Layout for 6-Pin Super-Mini Package…(SM6) (SSOP6-P-0.95)

Unit: mm

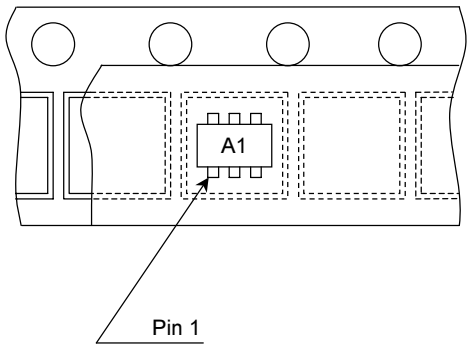


Device Orientation

L: TE85L

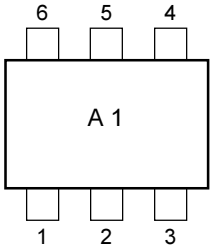
N: TE85N when there is no direction (Note)

Note: TE85N is tape packing of products which are symmetrical in both their internal components and external leads, so that device orientation is unimportant.



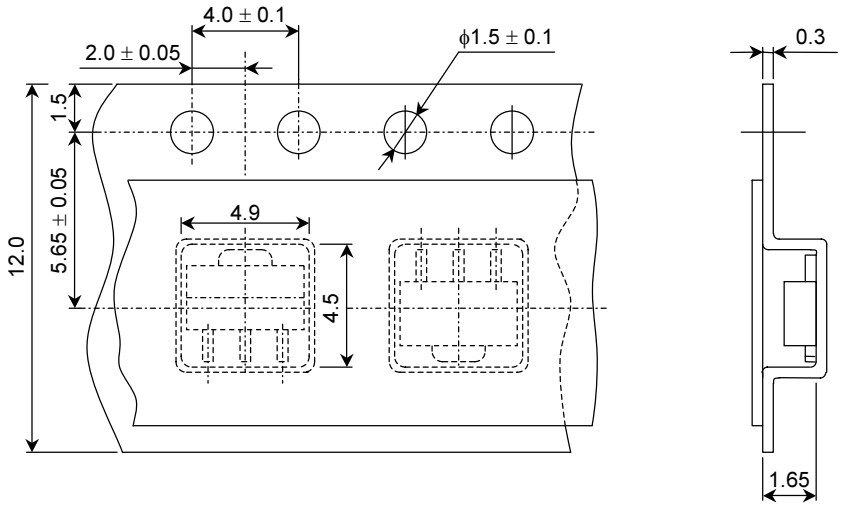
Pin 1 is on lower left of the marking.

Example: Top View

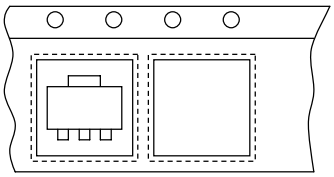


6.3.5 Tape Layout for Power Mini Package…(PW-MINI)

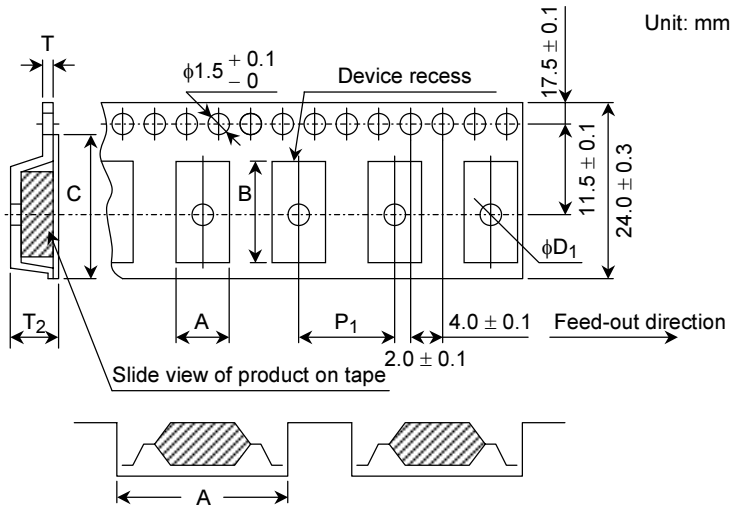
Unit: mm



Device Orientation



6.3.6 Tape Layout for Shrink Small Outline Package…(SSOP20-P-225)



A : 6.9 ± 0.2 mm

B : 10.5 ± 0.2 mm

C : 21.0 mm

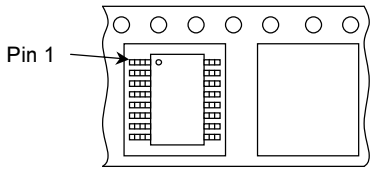
D_1 : 16.5 ± 0.1 mm

P_1 : 12.0 ± 0.1 mm

T : 0.3 ± 0.1 mm

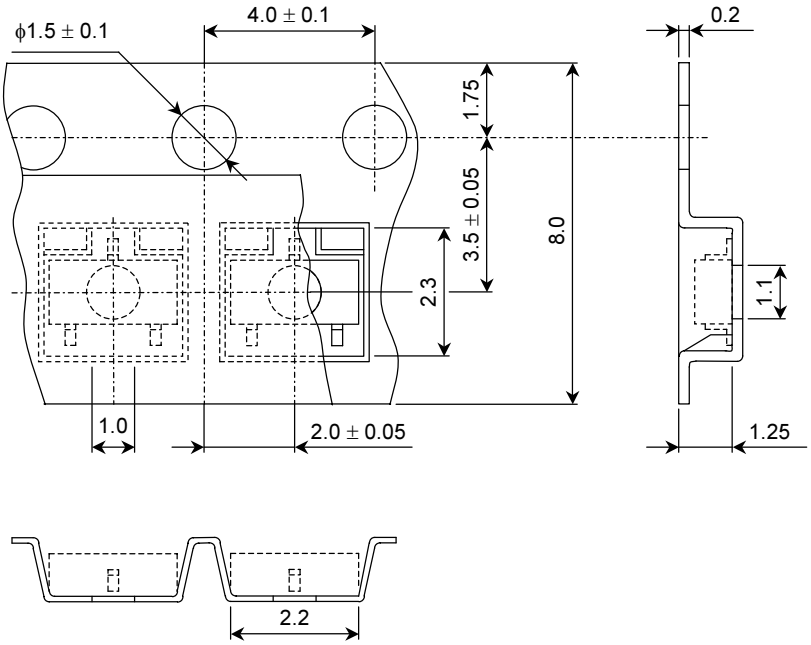
T_1 : 2.2 ± 0.1 mm

Device Orientation

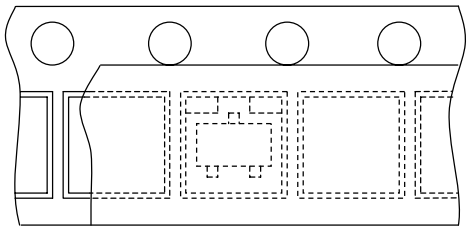


6.3.7 Tape Layout for 3-Pin Ultra-Super-Mini Package…(USM)

Unit: mm

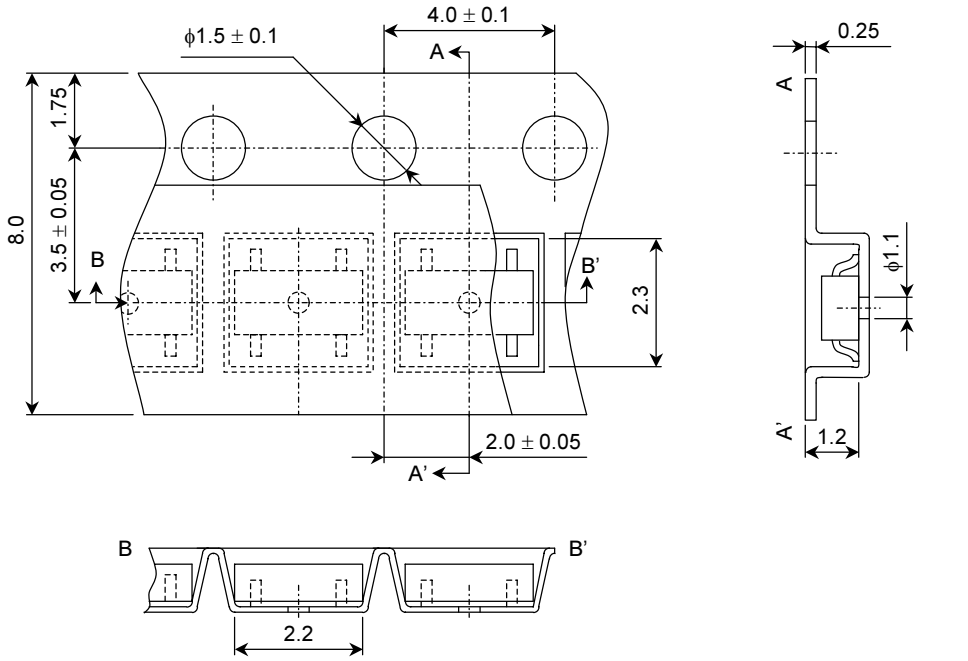


Device Orientation

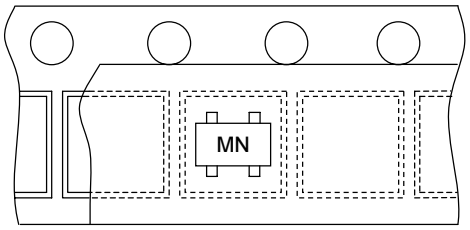


6.3.8 Tape Layout for 4-Pin Ultra-Super-Mini Package…(USQ)

Unit: mm

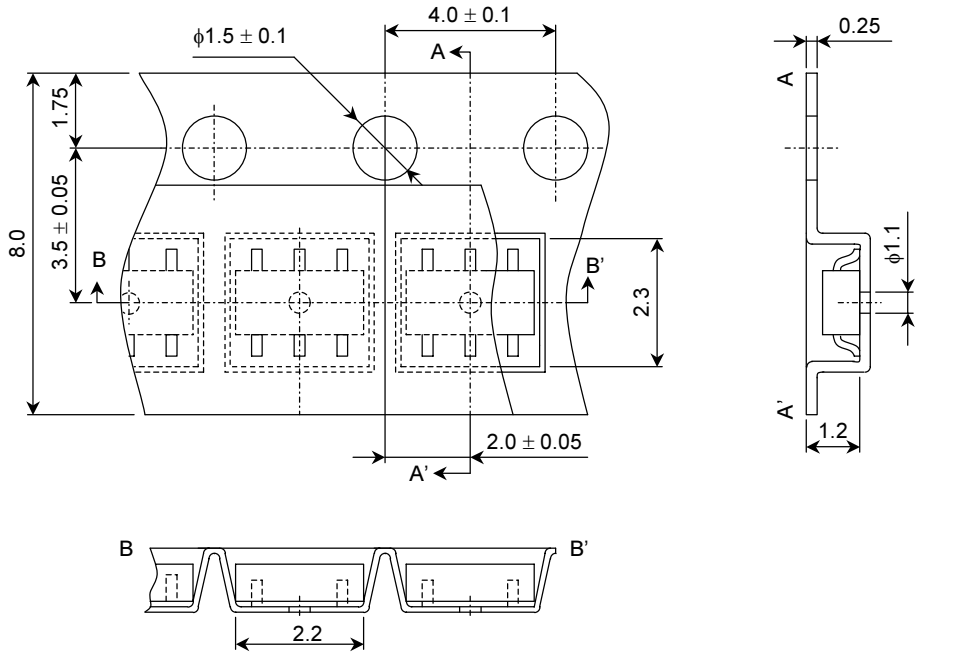


Device Orientation

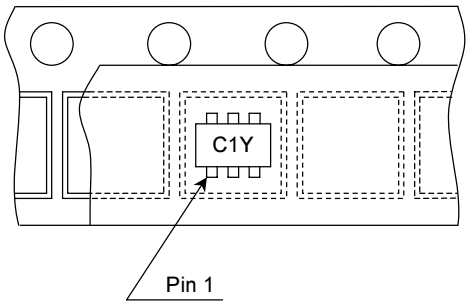


6.3.9 Tape Layout for 6-Pin Ultra-Super-Mini Package…(US6)

Unit: mm



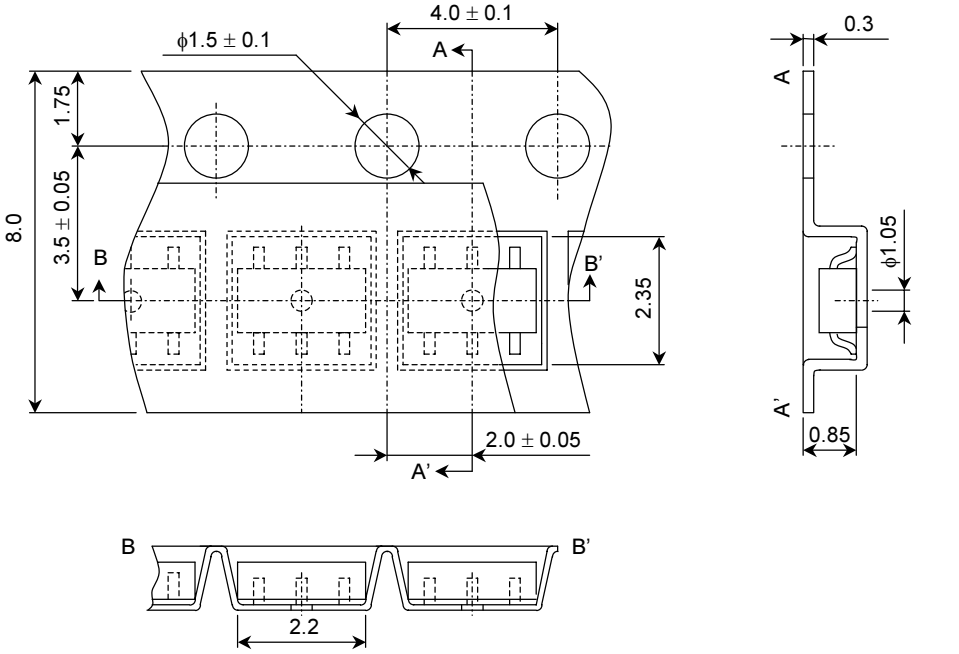
Device Orientation



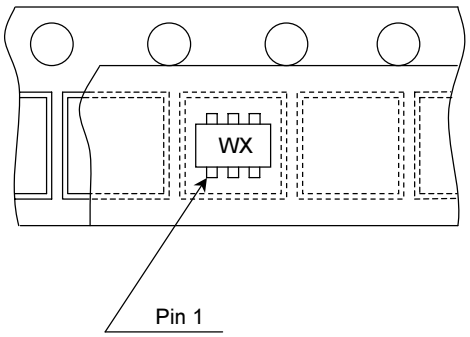
Note: TE85N is tape packing of products which are symmetrical in both their internal components and external leads, so that device orientation is unimportant.

6.3.10 Tape Layout for 6-Pin Ultra-Thin-Super-Mini Package…(TU6)

Unit: mm

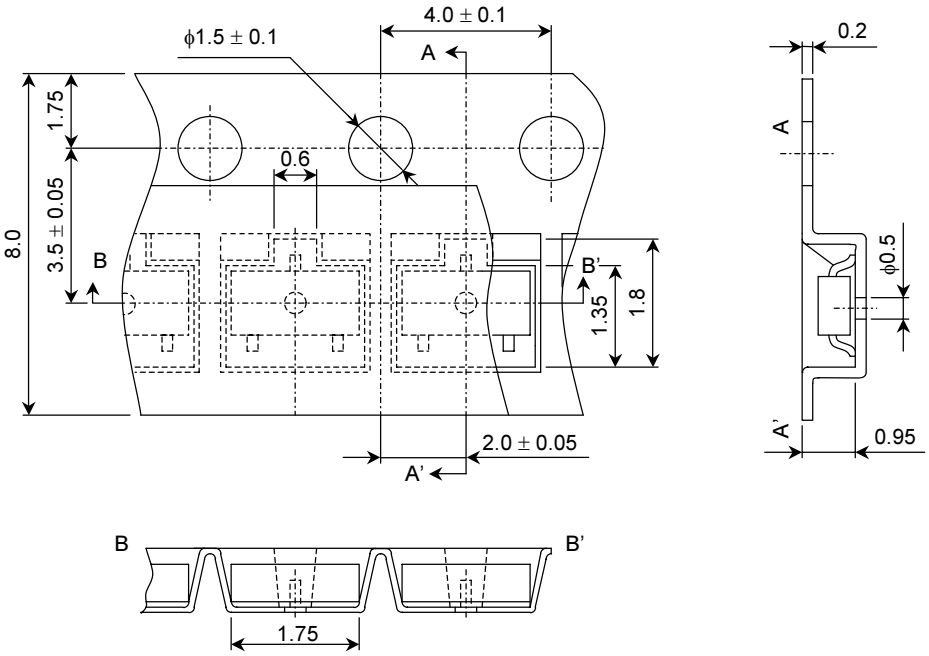


Device Orientation

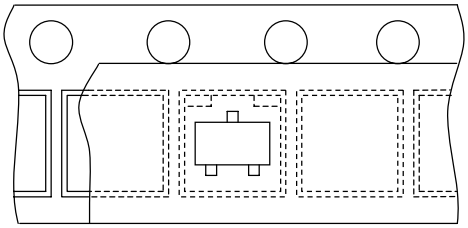


6.3.11 Tape Layout for Small-Super-Mini Package…(SSM)

Unit: mm

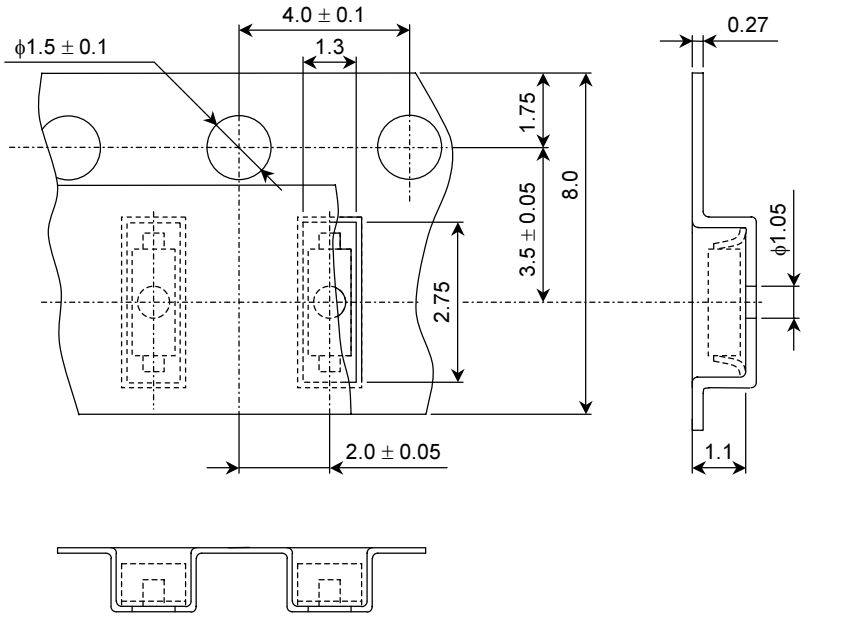


Device Orientation

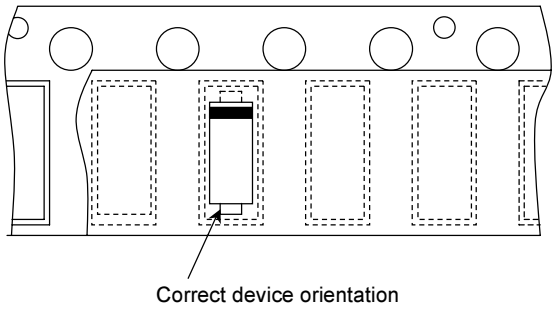


6.3.12 Tape Layout for Ultra-Super-Mini Coaxial Package…(USC)

Unit: mm

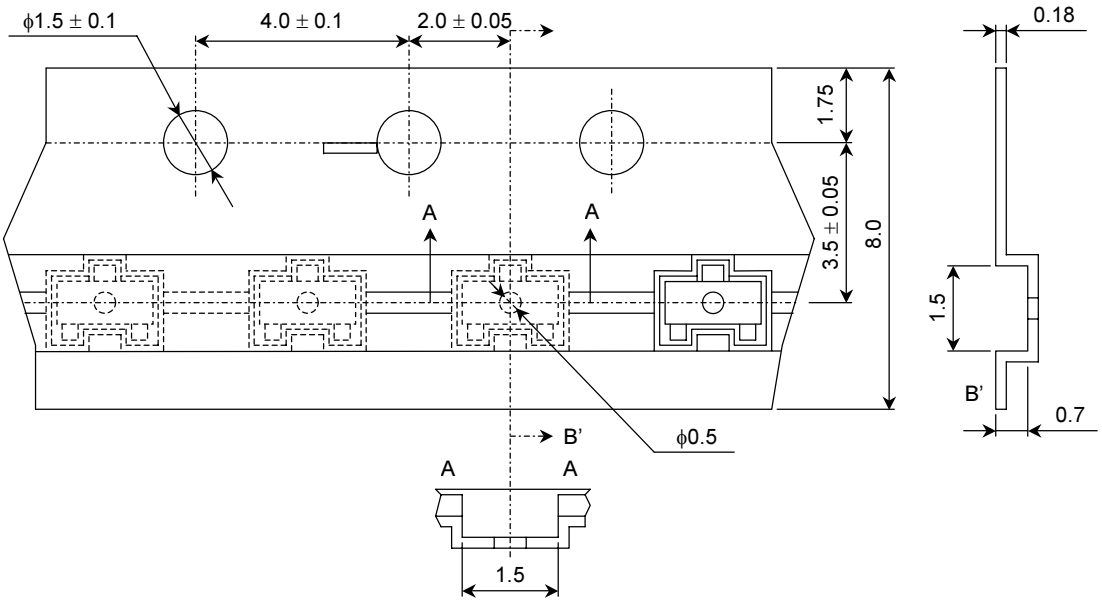


Device Orientation

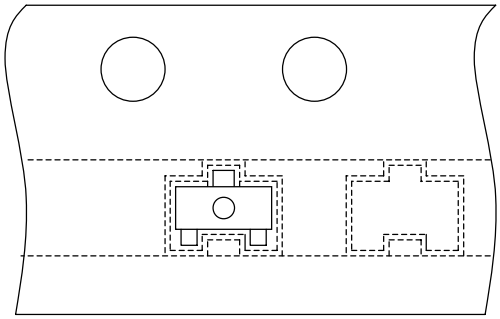


6.3.13 Tape Layout for Extremely Thin Super-Mini Package…(TESM)

Unit: mm



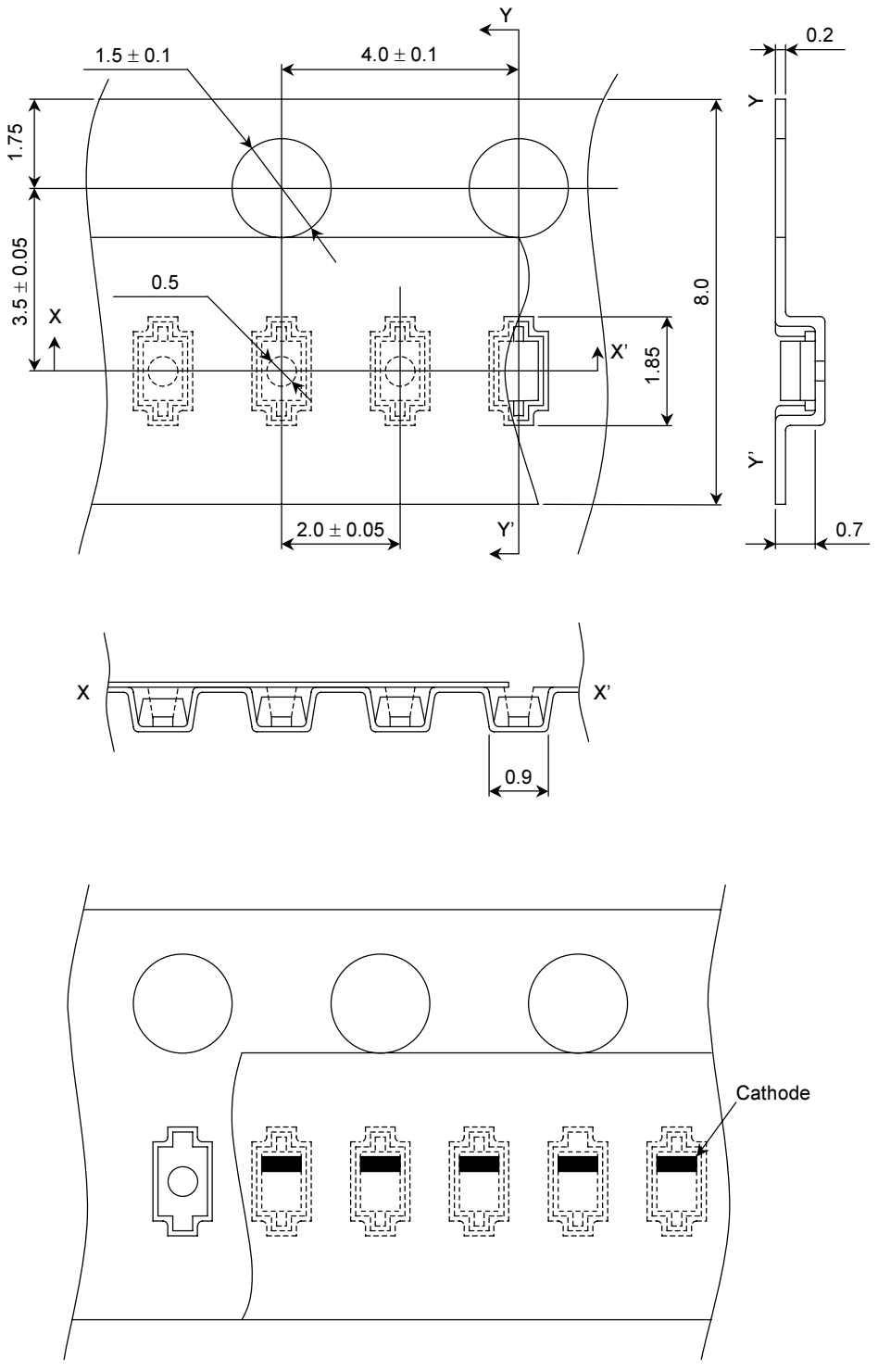
Device Orientation



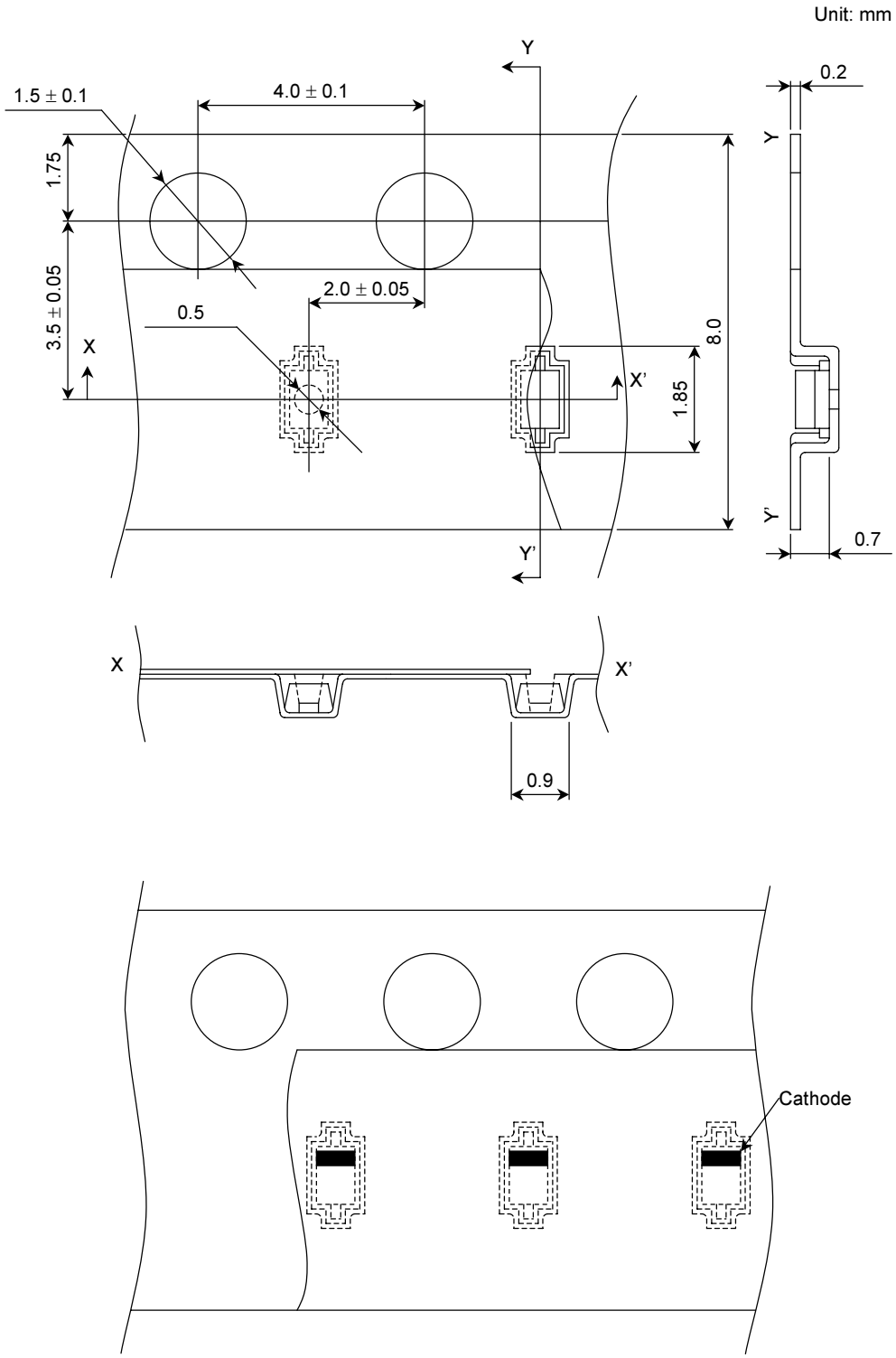
6.3.14 Tape Layout for Extreme-Super-Min Coaxial Package…(ESC)
Tape Layout for Extremely Thin Super-Mini Coaxial Package…(TESC)

2-mm Pitch Type

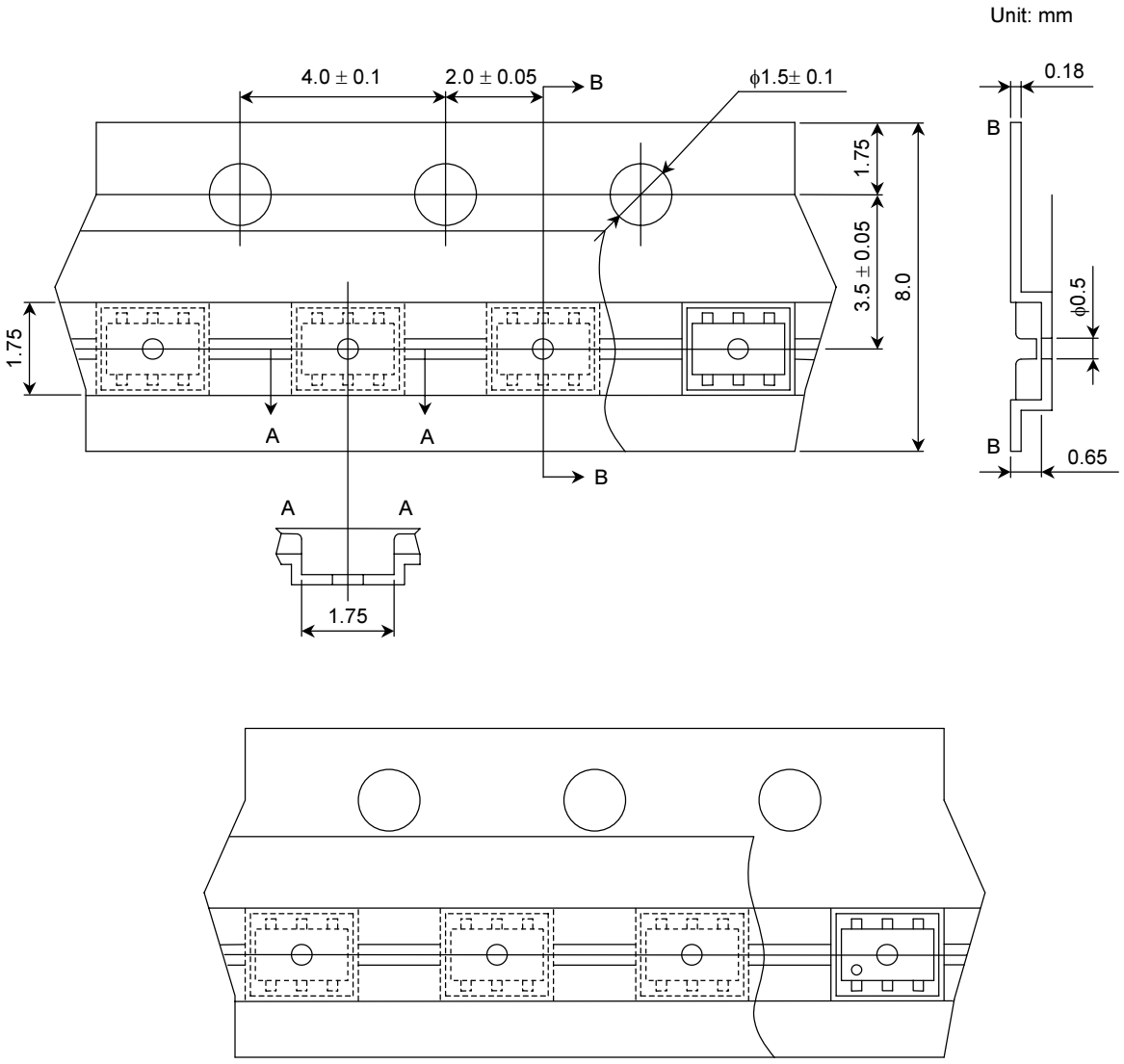
Unit: mm



4-mm Pitch Type

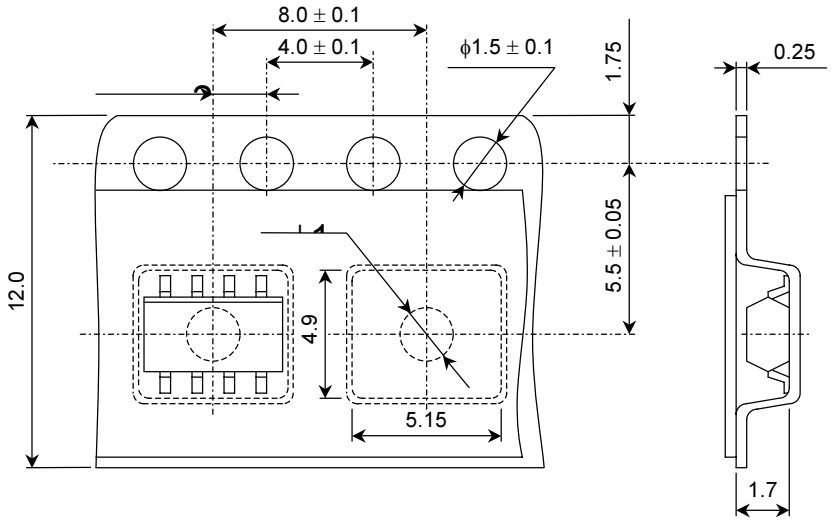


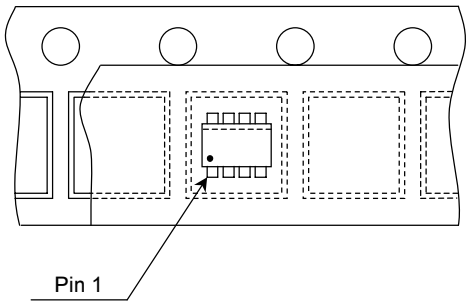
6.3.15 Tape Layout for Extreme-Super-Mini Package…(ES6)



6.3.16 Tape Layout for 8-Pin FM Package…(FM8)

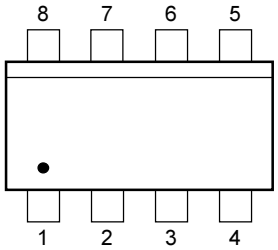
Unit: mm





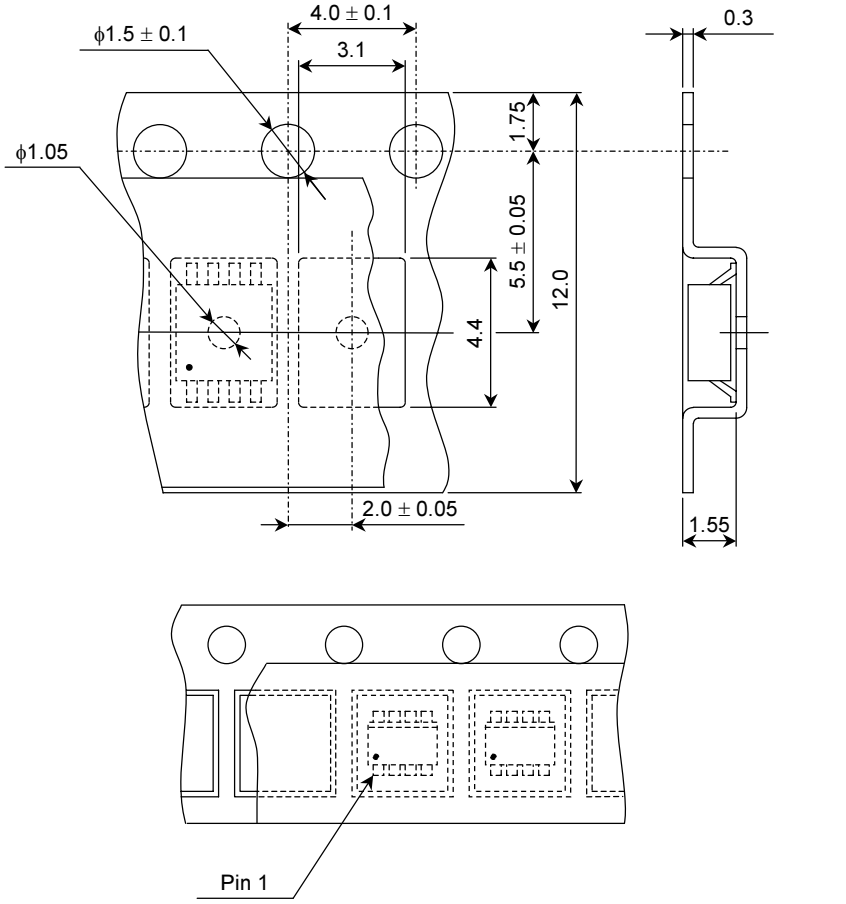
Pin 1 is on lower left of the marking.

Example: Top View

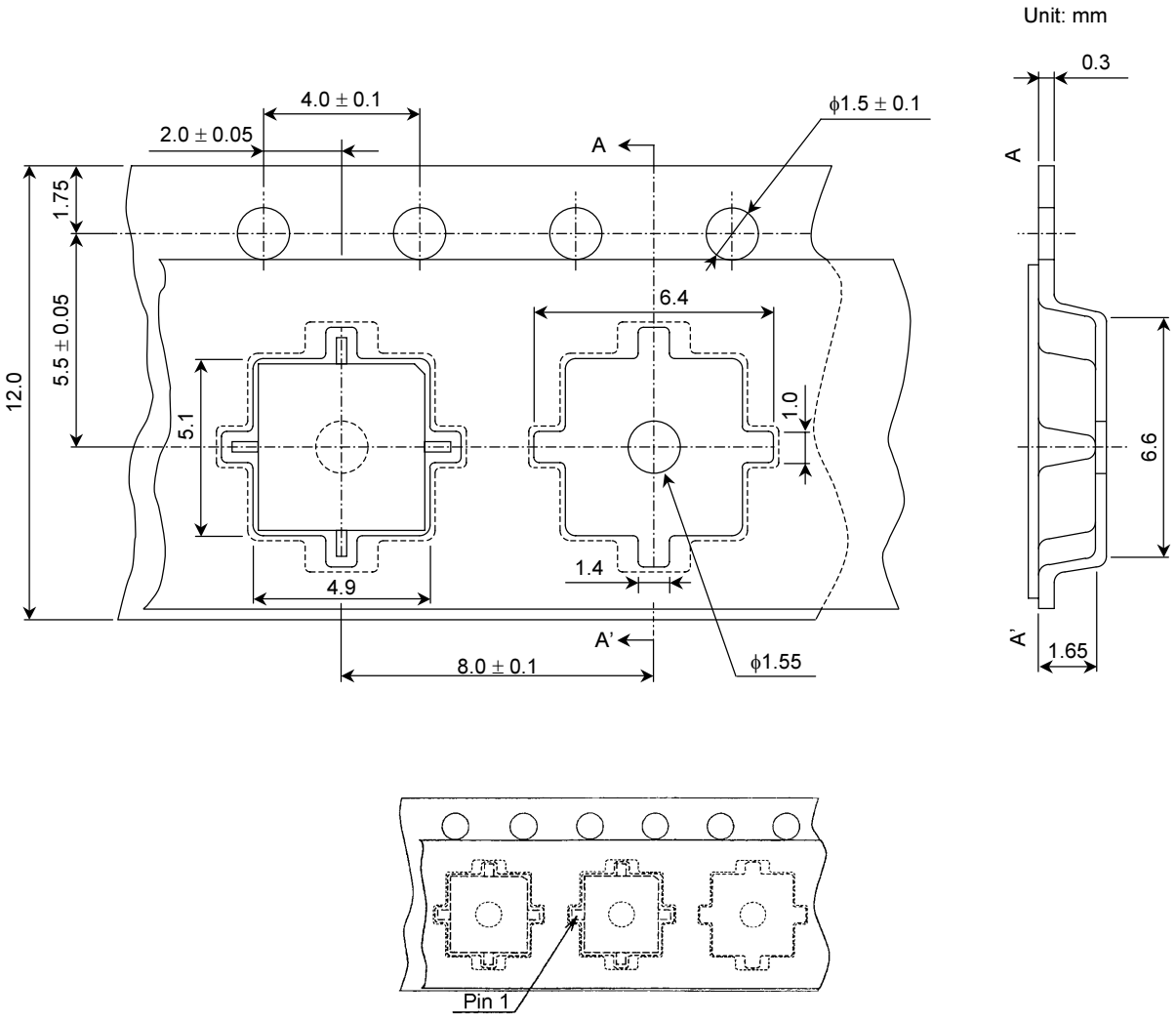


6.3.17 Tape Layout for 8-Pin SM Package…(SM8)

Unit: mm

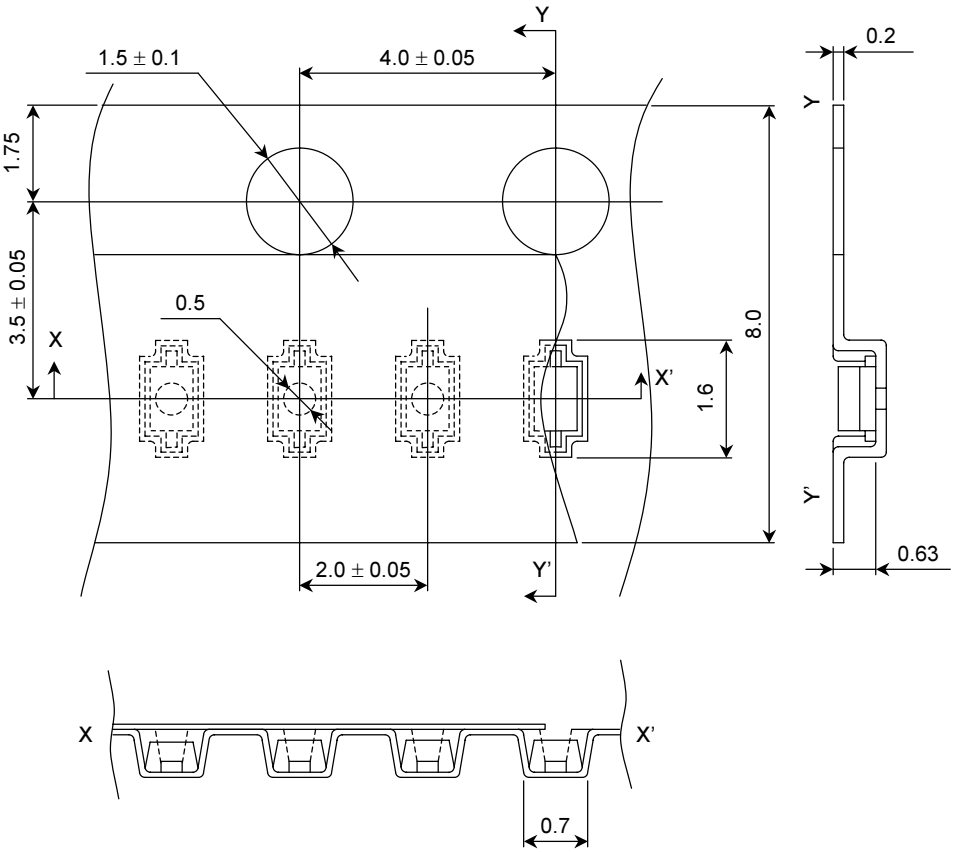


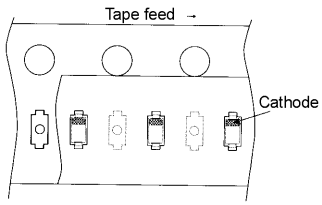
6.3.18 Tape Layout for PW-X Package…(PW-X)



6.3.19 Tape Layout for Small-Extreme-Super-Mini Coaxial Package…(sESC)

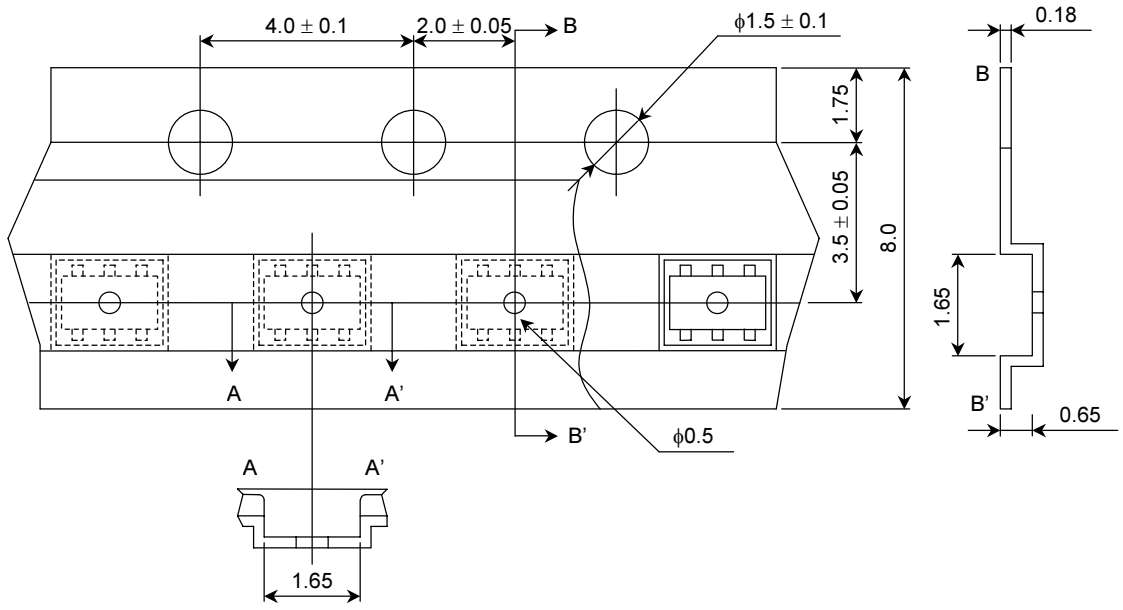
Unit: mm





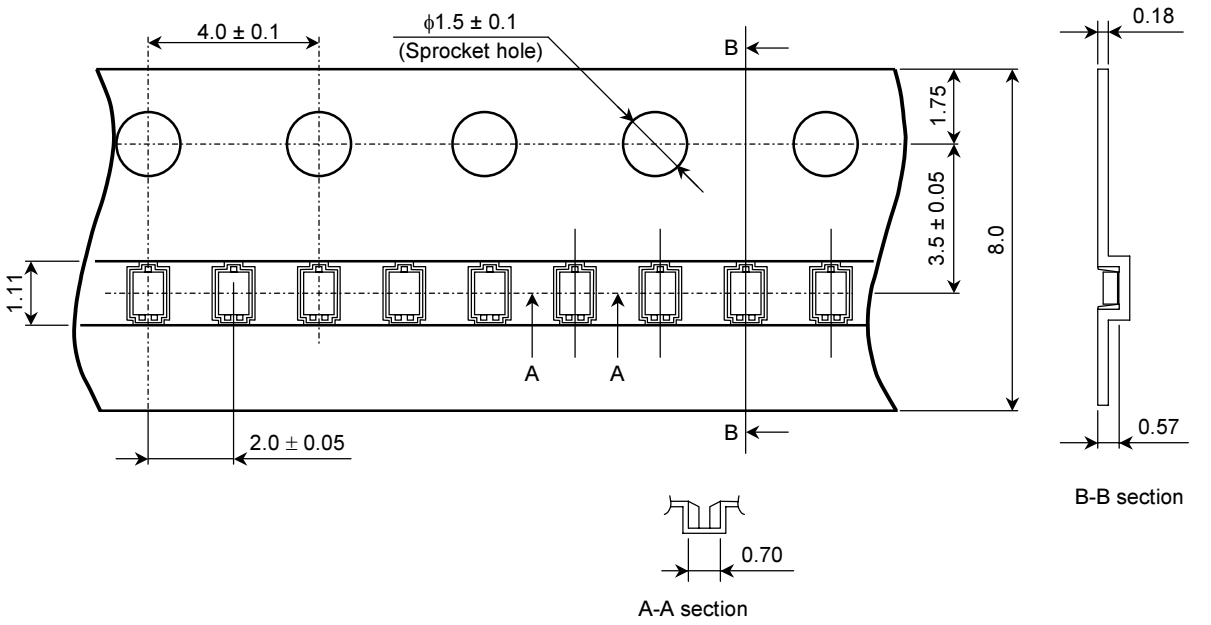
6.3.20 Tape Layout for Small-Extreme-Super-Mini Package…(sES6)

Unit: mm



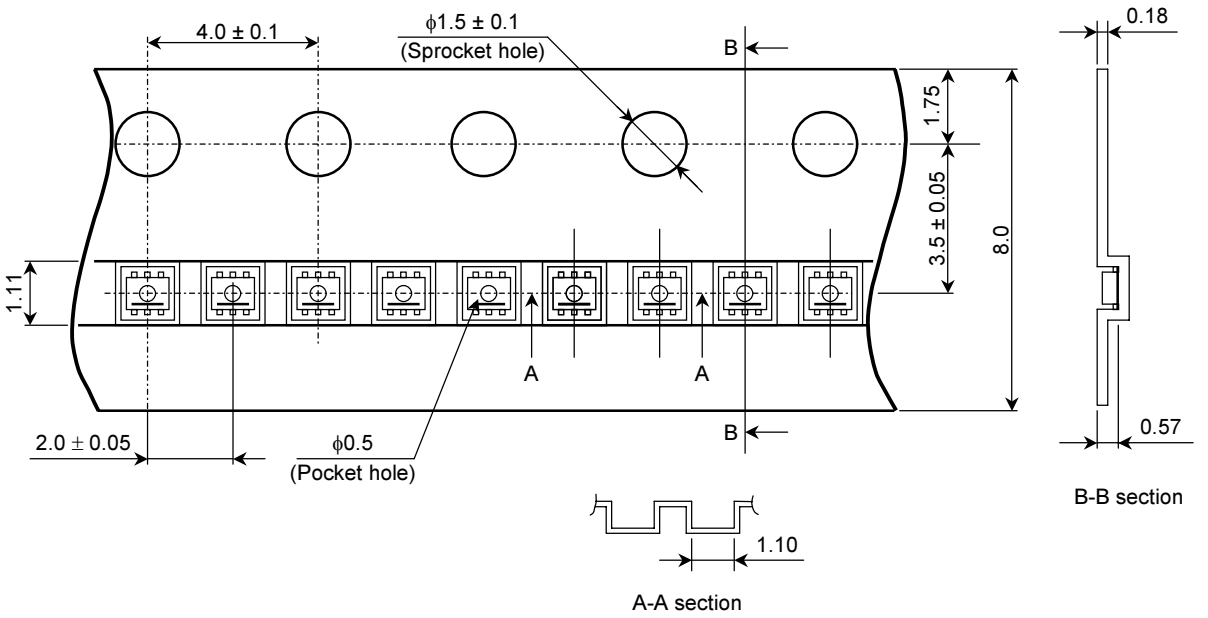
6.3.21 Tape Layout for fSM Package

Unit: mm



6.3.22 Tape Layout for fS6 Package

Unit: mm



6.3.23 Tape Layout for fSC Package

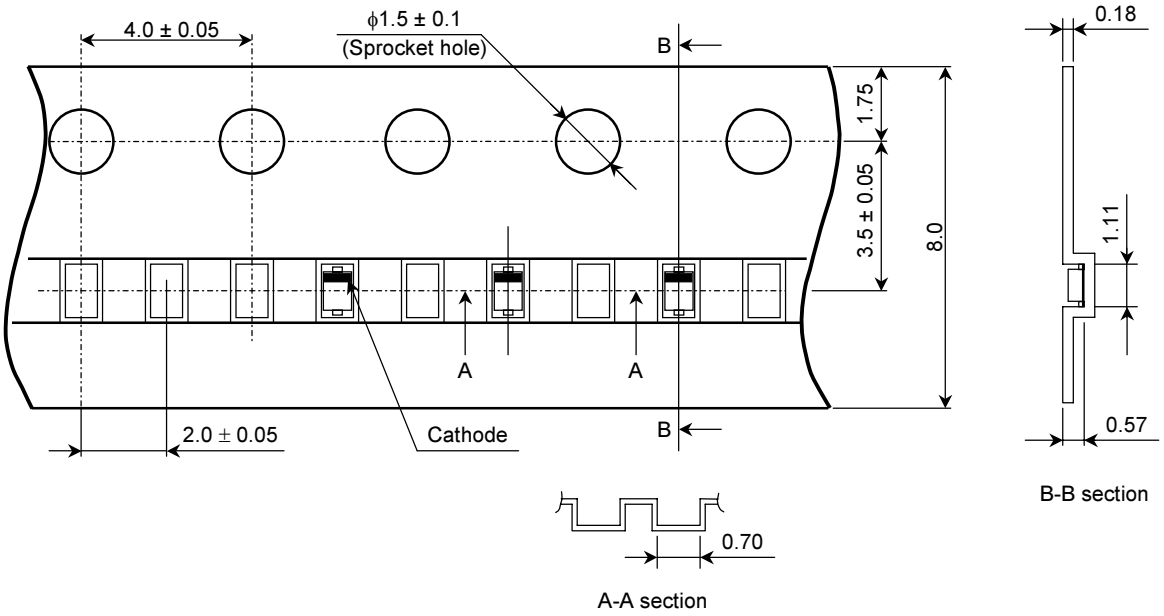
Tape Specifications

1 Cumulative pitch error tolerance is ±0.2 mm/10 devices.

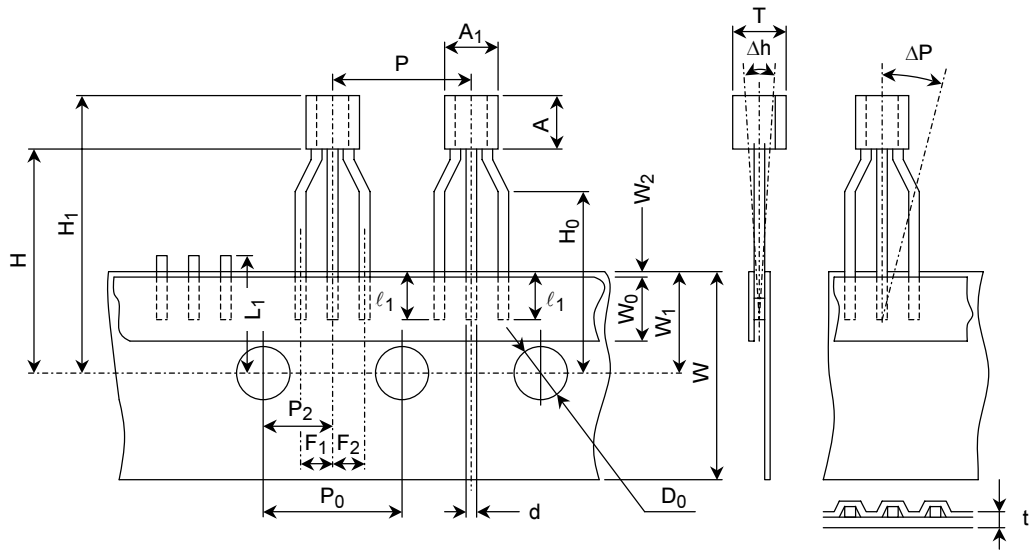
2 Tape meterial is plastic (anti-electrostatic).

3 Tape dimensions.

Unit: mm

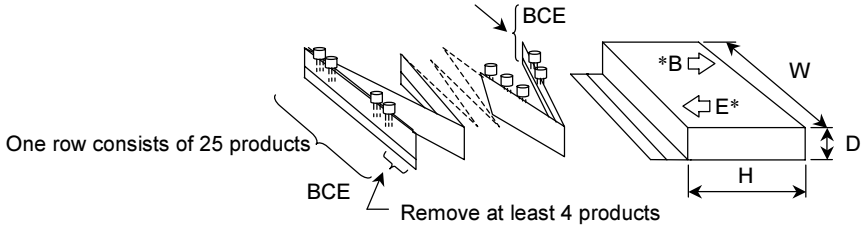


6.3.24 Radial Tape Layout for TO-92 and Mini Package



Measurement	Symbol	Dimensions				Unit: mm	Remarks
		TO-92 (SC-43)	MINI	TO-92MOD	MSTM		
Product Width	A_1	6.0 max	4.5 max	5.1 max	7.1 max		Please refer to each technical datasheet for more details
Product Height	A	9.0 max	3.5 max	8.2 max	4.7 max		
Product Thickness	T	6.0 max	2.6 max	4.1 max	2.7 max		
Lead Width	d	0.45□ typ.	0.4□ typ.	0.67□ max	0.45□ typ.		
Attached Lead Length	ℓ_1	2.5 min		3.5 min	2.6 min		
Pitch Between Products	P	12.7 ± 1.0			12.7 ± 0.5		
Feed Hole Pitch	P_0	12.7 ± 0.3			12.7 ± 0.2		Cumulative pitch error rate: ±1 mm/20 pitches
Feed Hole Center to Lead Center	P_2	6.35 ± 0.4					
Lead Spacing	F_1/F_2	$2.5^{+0.6}_{-0.3}$			$2.54^{+0.3}_{-0.2}$		
Vertical Skew	Δh	0 ± 2.0			0 ± 1.0		
Tape Width	W	$18.0^{+1.0}_{-0.5}$					
Sealing Tape Width	W_0	6.0 ± 0.3					
Tape Edge to Feed Hole Center	W_1	$9.0^{+0.75}_{-0.5}$		9.0 ± 0.5			
Carrier Tape Edge to Sealing Tape Edge	W_3	0.5 max					
Package to Feed Hole Center	H	20 max	$20^{+0.75}_{-0.5}$	20 max	19 ± 0.5		
Lead Clinch to Feed Hole Center	H_0	16.0 ± 0.5			—		
Product Protrusion from Feed Hole Center	H_1	32.25 max			25.0 max		
Feed Hole Diameter	D_0	4.0 ± 0.2					
Tape Thickness	t	0.6 ± 0.2					
Length of Shipped Lead	L_1	11.0 max					
Horizontal Skew	ΔP	0 ± 1.0					

Ammo Pack and Ammo Pack Dimensions



Unit: mm

Package Type	W	H	D
TO-92 (SC-43)	336 ± 3	250 ± 3	47 ± 3
MINI	336 ± 3	260 ± 3	47 ± 3
TO-92MOD	336 ± 3	190 ± 3	47 ± 3
MSTM	336 ± 3	230 ± 3	47 ± 3

*: Indicate the first electrode of a lead

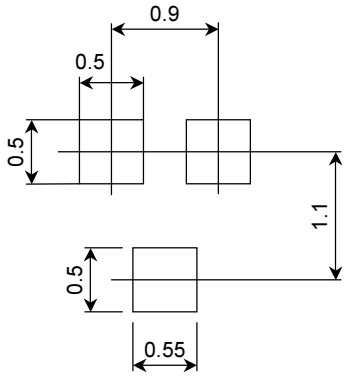
Example: E: Emitter

B: Base

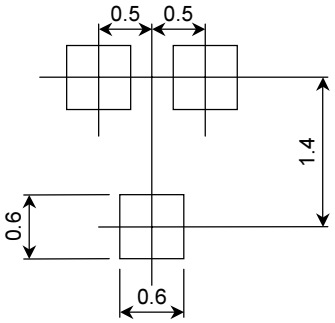
7. Reference Pad Dimensions

The following shows reference pad dimensions when a device mounted on a board. Unit: mm

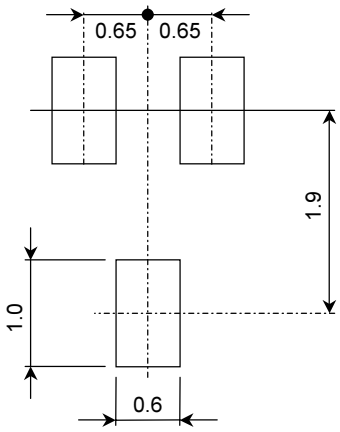
(1) 3-pin extremely thin super-mini package (TESM)



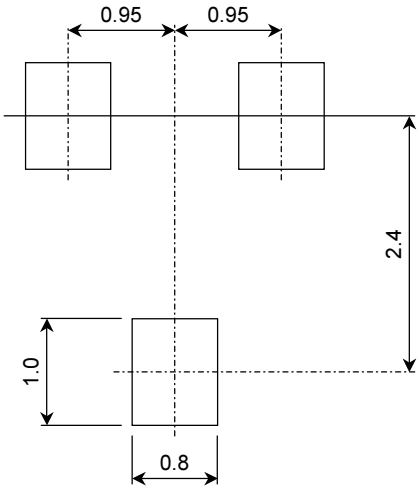
(2) 3-pin small-super-mini package (SSM)



(3) 3-pin ultra-super-mini package (USM) (JEITA: SC-70)

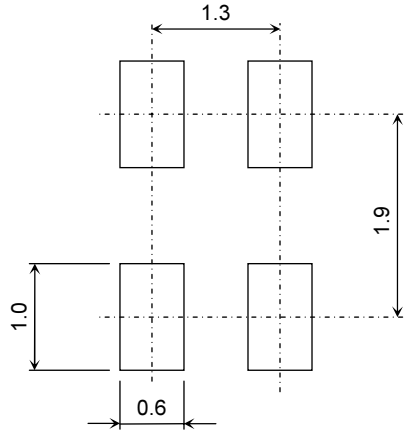


(4) 3-pin super-mini package (SM) (JEITA: SC-59)

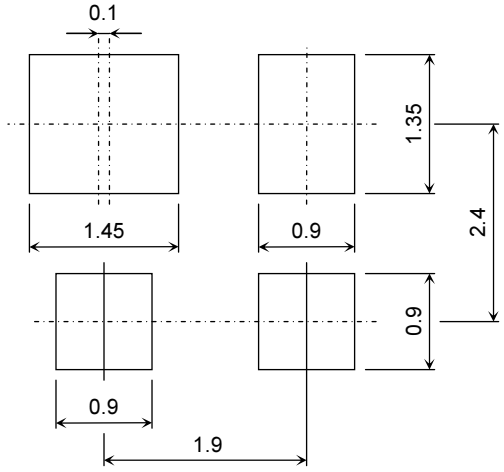


Unit: mm

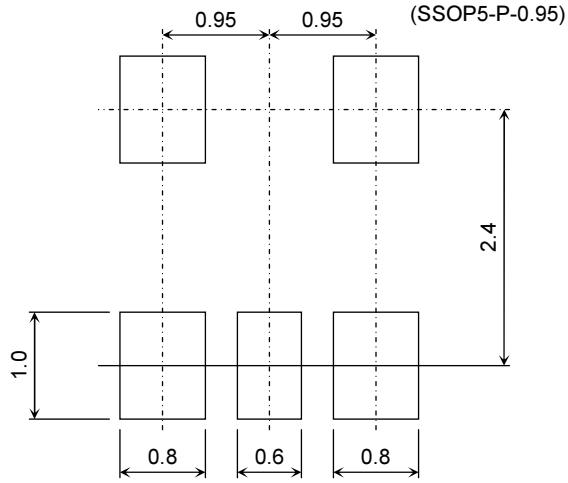
(5) 4-pin ultra-super-mini package (USQ)



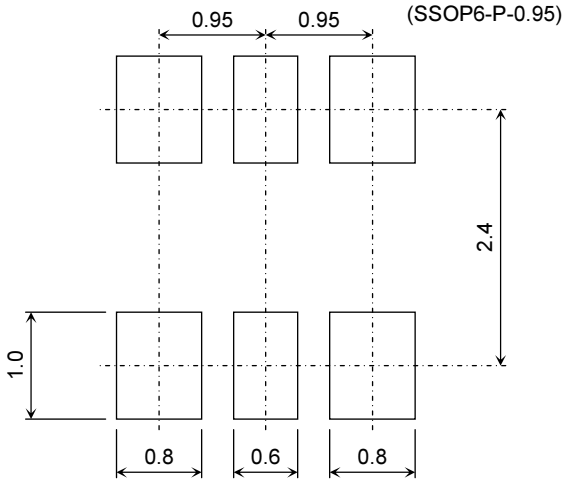
(6) 4-Pin super-mini package (SMQ)
(JEITA: SC-61B)



(7) 5-pin super-mini package (5LEAD)
(SMV)

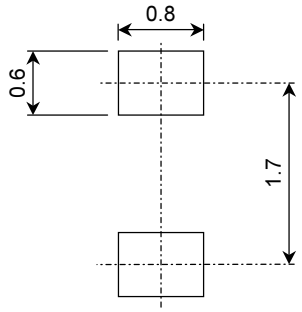


(8) 6-pin super-mini (SM6)

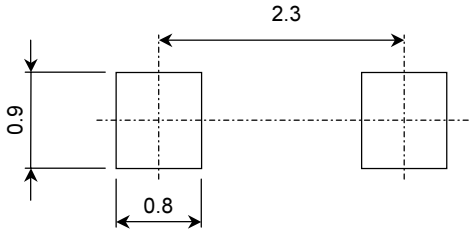


Unit: mm

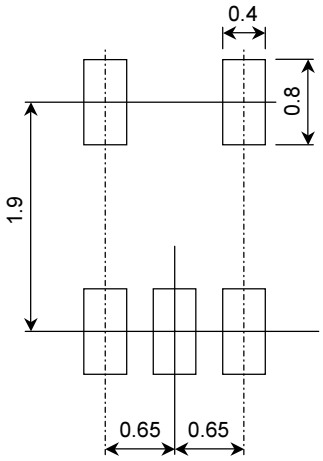
(9) Extreme-super-mini package (ESC)
extremely thin super-mini package
(TESC)



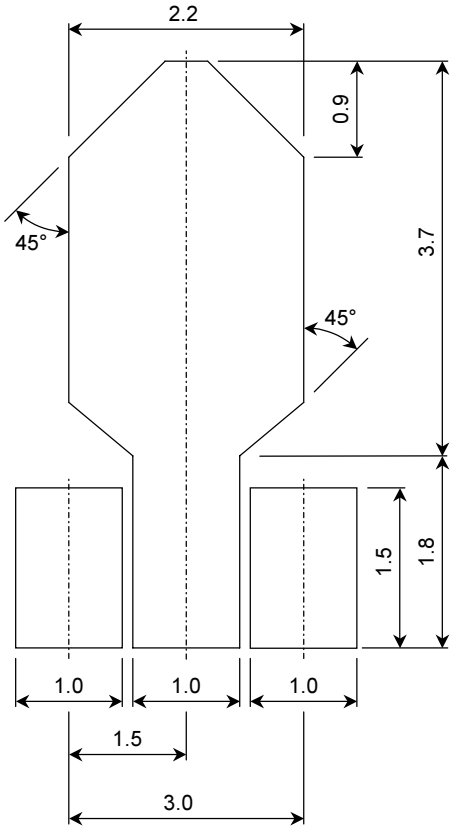
(10) 2-pin ultra-super-mini package (USC)



(11) 5-Pin ultra-super-mini package (USV)

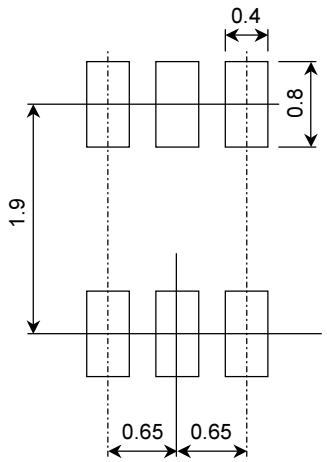


(12) Power mini package (JEITA: SC-62)

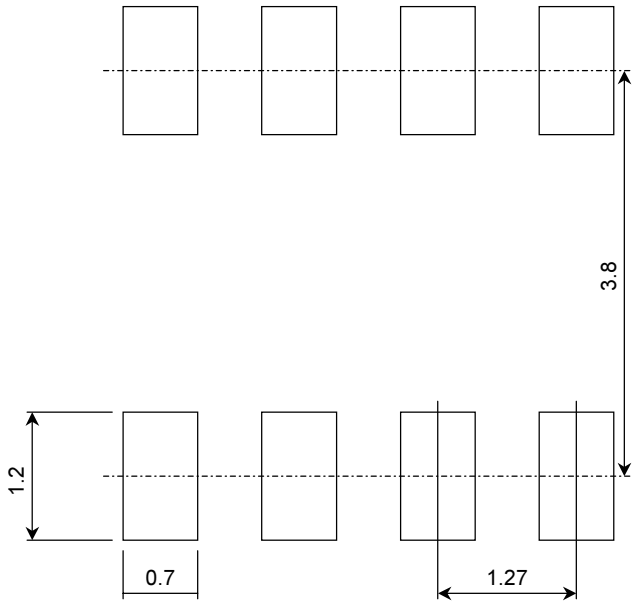


Unit: mm

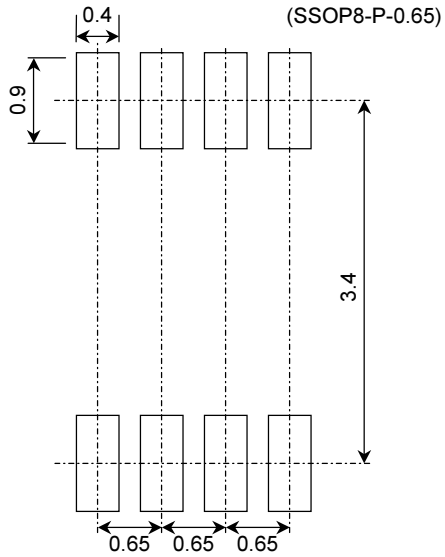
(13) 6-pin ultra-super-mini and 6-pin thin ultra-super-mini package (US6/TU6/UF6)



(14) 8-pin flat mini (FM8)

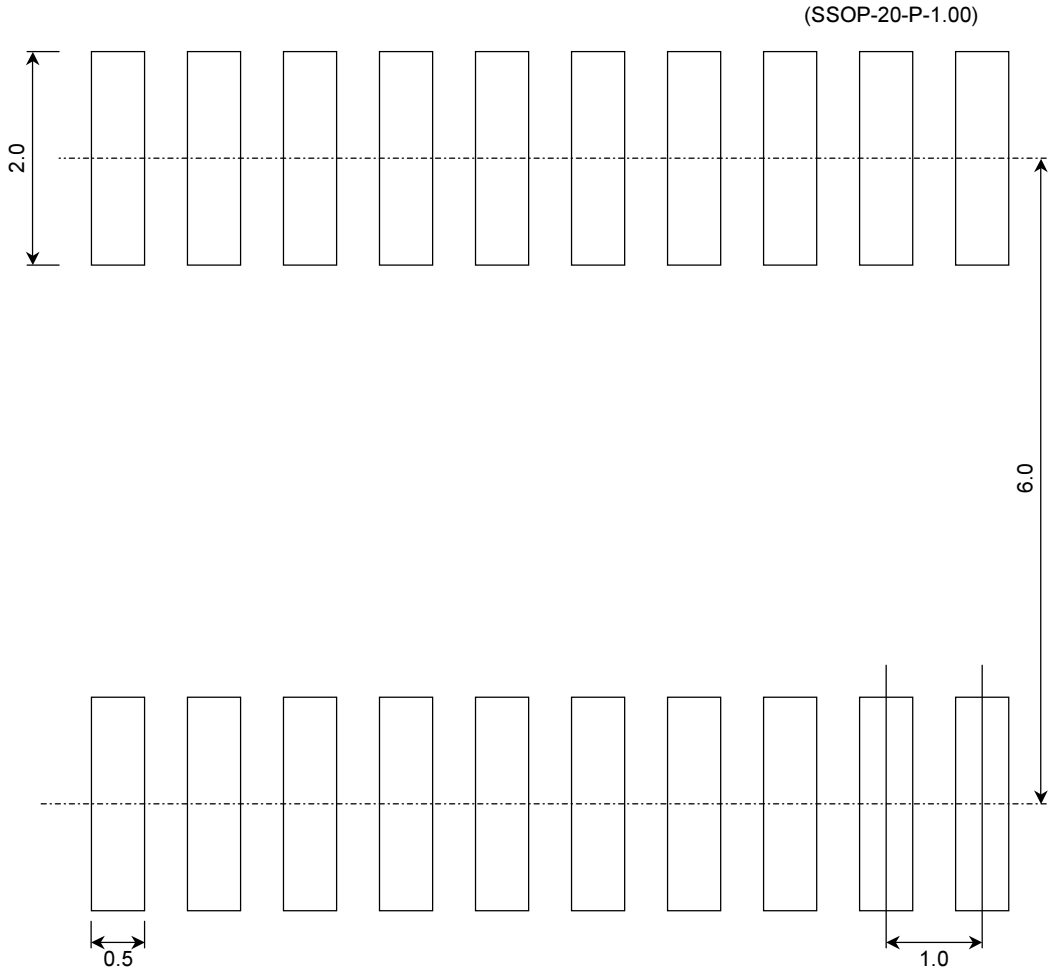


(15) 8-pin small-flat-mini (SM8)

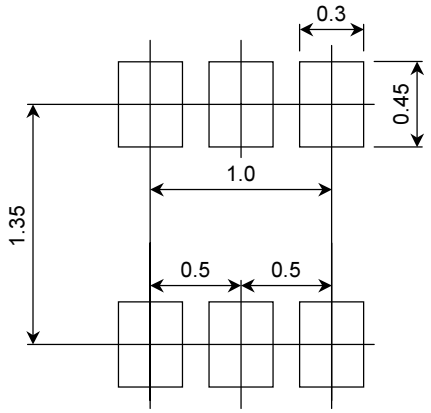


Unit: mm

(16) Shrink small outline package

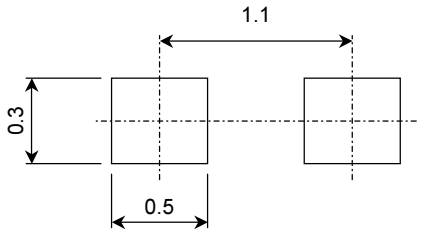


(17) 6-pin extreme-super-mini package (ES6)

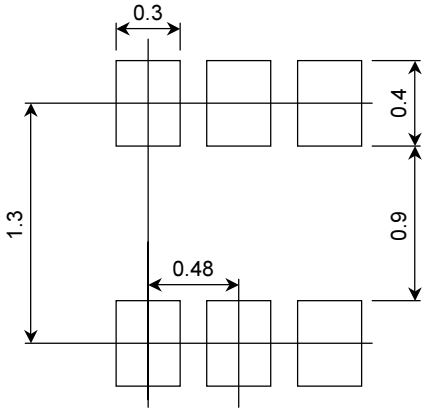


Unit: mm

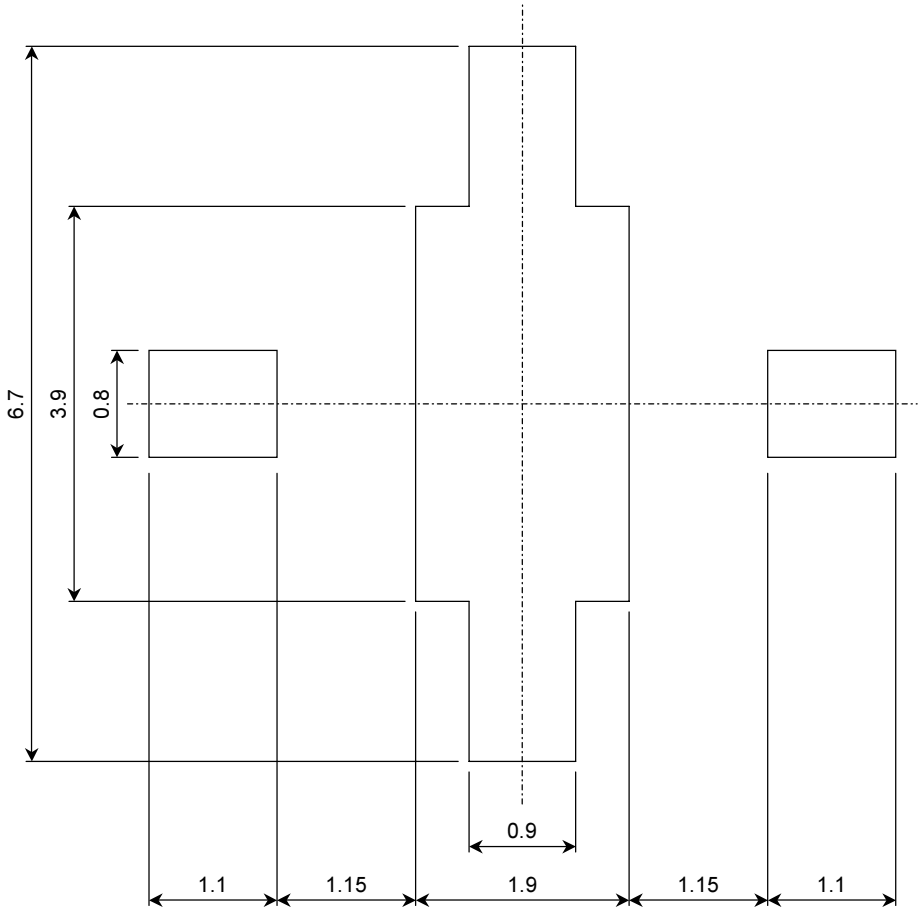
(18) Extreme-super-mini package (sESC)



(19) 6-pin extreme-super-mini package (sES6)

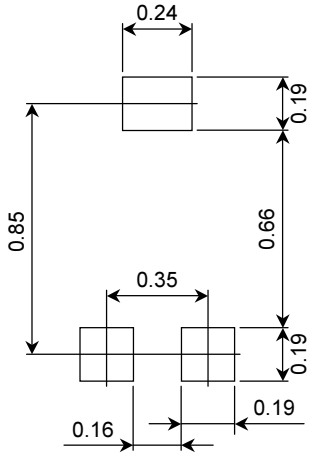


(20) PW-X

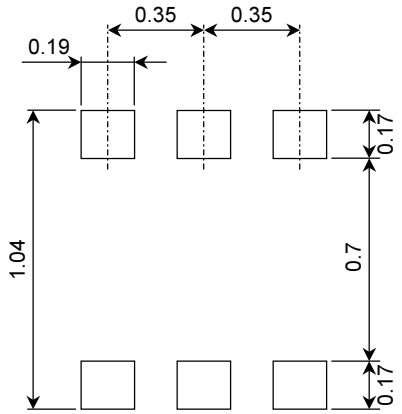


The following shows reference pad dimensions when a device mounted on a board. Unit: mm

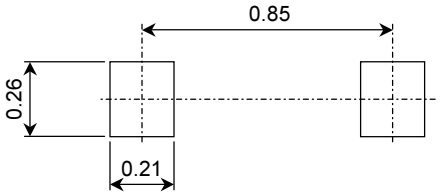
(21) fSM



(22) fS6



(23) fSC



[6] Handling Precautions

[6] Handling Precautions

1. Using Toshiba Semiconductors Safely

TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.

In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..

The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.

2. Safety Precautions

This section lists important precautions which users of semiconductor devices (and anyone else) should observe in order to avoid injury and damage to property, and to ensure safe and correct use of devices.

Please be sure that you understand the meanings of the labels and the graphic symbol described below before you move on to the detailed descriptions of the precautions.

[Explanation of Labels]

⚠DANGER	Indicates an imminently hazardous situation which will result in death or serious injury if you do not follow instructions.
⚠WARNING	Indicates a potentially hazardous situation which could result in death or serious injury if you do not follow instructions.
⚠CAUTION	Indicates a potentially hazardous situation which if not avoided, may result in minor injury or moderate injury.

2.1 General Precautions Regarding Semiconductor Devices

⚠CAUTION
Do not use devices under conditions exceeding their absolute maximum ratings (e.g. current, voltage, power dissipation or temperature). This may cause the device to break down, degrade its performance, or cause it to catch fire or explode resulting in injury. Do not insert devices in the wrong orientation. Make sure that the positive and negative terminals of power supplies are connected correctly. Otherwise the rated maximum current or power dissipation may be exceeded and the device may break down or undergo performance degradation, causing it to catch fire or explode and resulting in injury. When power to a device is on, do not touch the device's heat sink. Heat sinks become hot, so you may burn your hand. Do not touch the tips of device leads. Because some types of device have leads with pointed tips, you may prick your finger. When conducting any kind of evaluation, inspection or testing, be sure to connect the testing equipment's electrodes or probes to the pins of the device under test before powering it on. Otherwise, you may receive an electric shock causing injury. Before grounding an item of measuring equipment or a soldering iron, check that there is no electrical leakage from it. Electrical leakage may cause the device which you are testing or soldering to break down, or could give you an electric shock. Always wear protective glasses when cutting the leads of a device with clippers or a similar tool. If you do not, small bits of metal flying off the cut ends may damage your eyes.

2.2 Bipolar ICs (for use in automobiles)

⚠CAUTION
If your design includes an inductive load such as a motor coil, incorporate diodes or similar devices into the design to prevent negative current from flowing in. The load current generated by powering the device on and off may cause it to function erratically or to break down, which could in turn cause injury. Ensure that the power supply to any device which incorporates protective functions is stable. If the power supply is unstable, the device may operate erratically, preventing the protective functions from working correctly. If protective functions fail, the device may break down causing injury to the user.

3. General Safety Precautions and Usage Considerations

This section is designed to help you gain a better understanding of semiconductor devices, so as to ensure the safety, quality and reliability of the devices which you incorporate into your designs.

3.1 From Incoming to Shipping

3.1.1 Electrostatic Discharge (ESD)

When handling individual devices (which are not yet mounted on a printed circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects which come into direct contact with devices should be made of anti-static materials and should be grounded to earth via an 0.5- to 1.0-MΩ protective resistor.

Please follow the precautions described below; this is particularly important for devices which are marked “Be careful of static.”.

(1) Work environment

- When humidity in the working environment decreases, the human body and other insulators can easily become charged with static electricity due to friction. Maintain the recommended humidity of 40% to 60% in the work environment, while also taking into account the fact that moisture-proof-packed products may absorb moisture after unpacking.
- Be sure that all equipment, jigs and tools in the working area are grounded to earth.
- Place a conductive mat over the floor of the work area, or take other appropriate measures, so that the floor surface is protected against static electricity and is grounded to earth. The surface resistivity should be 10^4 to 10^8 Ω/sq and the resistance between surface and ground, 7.5×10^5 to 10^8 Ω
- Cover the workbench surface also with a conductive mat (with a surface resistivity of 10^4 to 10^8 Ω/sq, for a resistance between surface and ground of 7.5×10^5 to 10^8 Ω). The purpose of this is to disperse static electricity on the surface (through resistive components) and ground it to earth. Workbench surfaces must not be constructed of low-resistance metallic materials that allow rapid static discharge when a charged device touches them directly.
- Pay attention to the following points when using automatic equipment in your workplace:
  (a) When picking up ICs with a vacuum unit, use a conductive rubber fitting on the end of the pick-up wand to protect against electrostatic charge.
  (b) Minimize friction on IC package surfaces. If some rubbing is unavoidable due to the device’s mechanical structure, minimize the friction plane or use material with a small friction coefficient and low electrical resistance. Also, consider the use of an ionizer.
  (c) In sections which come into contact with device lead terminals, use a material which dissipates static electricity.
  (d) Ensure that no statically charged bodies (such as work clothes or the human body) touch the devices.

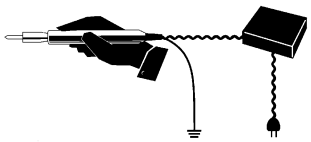
(e) Make sure that sections of the tape carrier which come into contact with installation devices or other electrical machinery are made of a low-resistance material.

(f) Make sure that jigs and tools used in the assembly process do not touch devices.

(g) In processes in which packages may retain an electrostatic charge, use an ionizer to neutralize the ions.

- Make sure that CRT displays in the working area are protected against static charge, for example by a VDT filter. As much as possible, avoid turning displays on and off. Doing so can cause electrostatic induction in devices.
- Keep track of charged potential in the working area by taking periodic measurements.
- Ensure that work chairs are protected by an anti-static textile cover and are grounded to the floor surface by a grounding chain. (suggested resistance between the seat surface and grounding chain is 7.5×10^5 to 10^{12} Ω.)
- Install anti-static mats on storage shelf surfaces. (suggested surface resistivity is 10^4 to 10^8 Ω/sq; suggested resistance between surface and ground is 7.5×10^5 to 10^8 Ω.)
- For transport and temporary storage of devices, use containers (boxes, jigs or bags) that are made of anti-static materials or materials which dissipate electrostatic charge.
- Make sure that cart surfaces which come into contact with device packaging are made of materials which will conduct static electricity, and verify that they are grounded to the floor surface via a grounding chain.
- In any location where the level of static electricity is to be closely controlled, the ground resistance level should be Class 3 or above. Use different ground wires for all items of equipment which may come into physical contact with devices.

(2) Operating environment

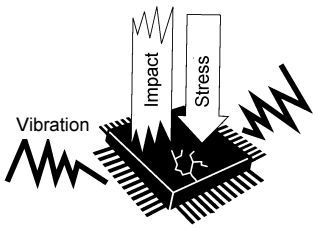


- Operators must wear anti-static clothing and conductive shoes (or a leg or heel strap).
- Operators must wear a wrist strap grounded to earth via a resistor of about 1 MΩ.
- Soldering irons must be grounded from iron tip to earth, and must be used only at low voltages (6 V to 24 V).
- If the tweezers you use are likely to touch the device terminals, use anti-static tweezers and in particular avoid metallic tweezers. If a charged device touches a low-resistance tool, rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pat to the tip, and connect it to a dedicated ground used especially for anti-static purposes (suggested resistance value: 10^4 to 10^8 Ω).
- Do not place devices or their containers near sources of strong electrical fields (such as above a CRT).
- When storing printed circuit boards which have devices mounted on them, use a board container or bag that is protected against static charge. To avoid the occurrence of static charge or discharge due to friction, keep the boards separate from one other and do not stack them directly on top of one another.
- Ensure, if possible, that any articles (such as clipboards) which are brought to any location where the level of static electricity must be closely controlled are constructed of anti-static materials.

- In cases where the human body comes into direct contact with a device, be sure to wear anti-static finger covers or gloves (suggested resistance value: 10^8 Ω or less).
- Equipment safety covers installed near devices should have resistance ratings of 10^9 Ω or less.
- If a wrist strap cannot be used for some reason, and there is a possibility of imparting friction to devices, use an ionizer.
- The transport film used in TCP products is manufactured from materials in which static charges tend to build up. When using these products, install an ionizer to prevent the film from being charged with static electricity. Also, ensure that no static electricity will be applied to the product's copper foils by taking measures to prevent static occurring in the peripheral equipment.

3.1.2 Vibration, Impact and Stress

Handle devices and packaging materials with care. To avoid damage to devices, do not toss or drop packages. Ensure that devices are not subjected to mechanical vibration or shock during transportation. Ceramic package devices and devices in canister-type packages which have empty space inside them are subject to damage from vibration and shock because the bonding wires are secured only at their ends.



Plastic molded devices, on the other hand, have a relatively high level of resistance to vibration and mechanical shock because their bonding wires are enveloped and fixed in resin. However, when any device or package type is installed in target equipment, it is to some extent susceptible to wiring disconnections and other damage from vibration, shock and stressed solder junctions. Therefore when devices are incorporated into the design of equipment which will be subject to vibration, the structural design of the equipment must be thought out carefully.

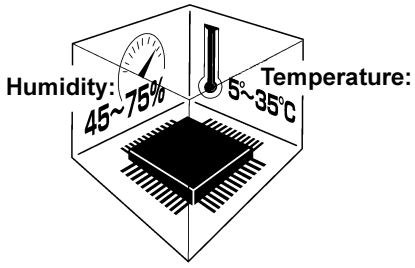
If a device is subjected to especially strong vibration, mechanical shock or stress, the package or the chip itself may crack. In products such as CCDs which incorporate window glass, this could cause surface flaws in the glass or cause the connection between the glass and the ceramic to separate.

Furthermore, it is known that stress applied to a semiconductor device through the package changes the resistance characteristics of the chip because of piezoelectric effects. In analog circuit design attention must be paid to the problem of package stress as well as to the dangers of vibration and shock as described above.

3.2 Storage

3.2.1 General Storage

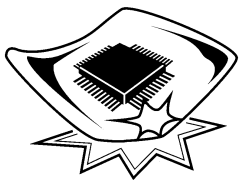
- Avoid storage locations where devices will be exposed to moisture or direct sunlight.
- Follow the instructions printed on the device cartons regarding transportation and storage.
- The storage area temperature should be kept within a temperature range of 5°C to 35°C, and relative humidity should be maintained at between 45% and 75%.



- Do not store devices in the presence of harmful (especially corrosive) gases, or in dusty conditions.
- Use storage areas where there is minimal temperature fluctuation. Rapid temperature changes can cause moisture to form on stored devices, resulting in lead oxidation or corrosion. As a result, the solderability of the leads will be degraded.
- When repacking devices, use anti-static containers.
- Do not allow external forces or loads to be applied to devices while they are in storage.
- If devices have been stored for more than two years, their electrical characteristics should be tested and their leads should be tested for ease of soldering before they are used.

3.2.2 Moisture-Proof Packing

Moisture-proof packing should be handled with care. The handling procedure specified for each packing type should be followed scrupulously. If the proper procedures are not followed, the quality and reliability of devices may be degraded. This section describes general precautions for handling moisture-proof packing. Since the details may differ from device to device, refer also to the relevant individual datasheets or databook.



(1) General precautions

Follow the instructions printed on the device cartons regarding transportation and storage.

- Do not drop or toss device packing. The laminated aluminum material in it can be rendered ineffective by rough handling.
- The storage area temperature should be kept within a temperature range of 5°C to 30°C, and relative humidity should be maintained at 90% (max). Use devices within 12 months of the date marked on the package seal.

- If the 12-month storage period has expired, or if the 30% humidity indicator shown in Figure 3.1 is pink when the packing is opened, it may be advisable, depending on the device and packing type, to back the devices at high temperature to remove any moisture. Please refer to the table below. After the pack has been opened, use the devices in a 5°C to 30°C. 60% RH environment and within the effective usage period listed on the moisture-proof package. If the effective usage period has expired, or if the packing has been stored in a high-humidity environment, back the devices at high temperature.

Packing	Moisture Removal
Tray	If the packing bears the "Heatproof" marking or indicates the maximum temperature which it can withstand, bake at 125°C for 20 hours. (some devices require a different procedure.)
Tube	Transfer devices to trays bearing the "Heatproof" marking or indicating the temperature which they can withstand, or to aluminum tubes before baking at 125°C for 20 hours.
Tape	Deviced packed on tape cannot be baked and must be used within the effective usage period after unpacking, as specified on the packing.

- When baking devices, protect the devices from static electricity.
- Moisture indicators can detect the approximate humidity level at a standard temperature of 25°C. 6-point indicators and 3-point indicators are currently in use, but eventually all indicators will be 3-point indicators.

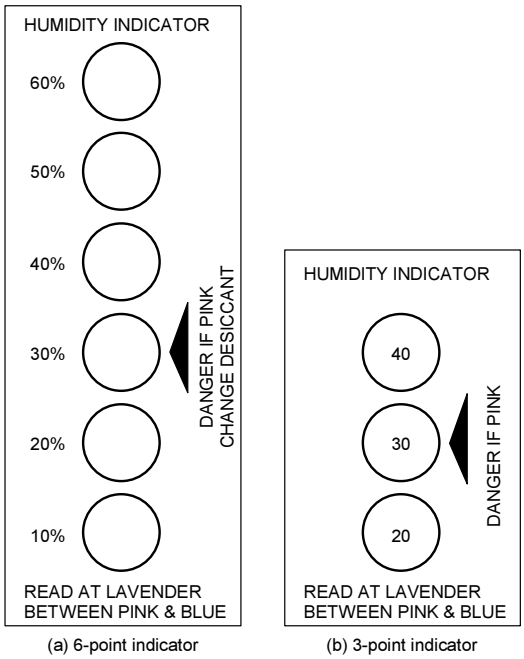


Figure 3.1 Humidity Indicator

3.3 Design

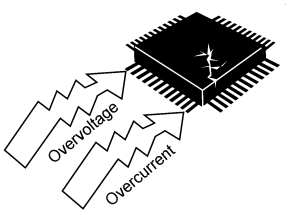
Care must be exercised in the design of electronic equipment to achieve the desired reliability. It is important not only to adhere to specifications concerning absolute maximum ratings and recommended operating conditions, it is also important to consider the overall environment in which equipment will be used, including factors such as the ambient temperature, transient noise and voltage and current surges, as well as mounting conditions which affect device reliability. This section describes some general precautions which you should observe when designing circuits and when mounting devices on printed circuit boards.

For more detailed information about each product family, refer to the relevant individual technical datasheets available from Toshiba.

3.3.1 Absolute Maximum Ratings

⚠CAUTION Do not use devices under conditions in which their absolute maximum ratings (e.g. current, voltage, power dissipation or temperature) will be exceeded. A device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user.

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Although absolute maximum ratings differ from product to product, they essentially concern the voltage and current at each pin, the allowable power dissipation, and the junction and storage temperatures.



If the voltage or current on any pin exceeds the absolute maximum rating, the device's internal circuitry can become degraded. In the worst case, heat generated in internal circuitry can fuse wiring or cause the semiconductor chip to break down.

If storage or operating temperatures exceed rated values, the package seal can deteriorate or the wires can become disconnected due to the differences between the thermal expansion coefficients of the materials from which the device is constructed.

3.3.2 Recommended Operating Conditions

The recommended operating conditions for each device are those necessary to guarantee that the device will operate as specified in the datasheet.

If greater reliability is required, derate the device's absolute maximum ratings for voltage, current, power and temperature before using it.

3.3.3 Derating

When incorporating a device into your design, reduce its rated absolute maximum voltage, current, power dissipation and operating temperature in order to ensure high reliability.

Since derating differs from application to application, refer to the technical datasheets available for the various devices used in your design.

3.3.4 Unused Pins

If unused pins are left open, some devices can exhibit input instability problems, resulting in malfunctions such as abrupt increase in current flow. Similarly, if the unused output pins on a device are connected to the power supply pin, the ground pin or to other output pins, the IC may malfunction or break down.

Since the details regarding the handling of unused pins differ from device to device and from pin to pin, please follow the instructions given in the relevant individual datasheets or databook.

CMOS logic IC inputs, for example, have extremely high impedance. If an input pin is left open, it can easily pick up extraneous noise and become unstable. In this case, if the input voltage level reaches an intermediate level, it is possible that both the P-channel and N-channel transistors will be turned on, allowing unwanted supply current to flow. Therefore, ensure that the unused input pins of a device are connected to the power supply (V_{CC}) pin or ground (GND) pin of the same device. For details of what to do with the pins of heat sinks, refer to the relevant technical datasheet and databook.

3.3.5 Latch-Up

Latch-up is an abnormal condition inherent in CMOS devices, in which V_{CC} gets shorted to ground. This happens when a parasitic PN-PN junction (thyristor structure) internal to the CMOS chip is turned on, causing a large current of the order of several hundred mA or more to flow between V_{CC} and GND, eventually causing the device to break down.

Latch-up occurs when the input or output voltage exceeds the rated value, causing a large current to flow in the internal chip, or when the voltage on the V_{CC} (V_{DD}) pin exceeds its rated value, forcing the internal chip into a breakdown condition. Once the chip falls into the latch-up state, even though the excess voltage may have been applied only for an instant, the large current continues to flow between V_{CC} (V_{DD}) and GND (V_{SS}). This causes the device to heat up and, in extreme cases, to emit gas fumes as well. To avoid this problem, observe the following precautions:

(1) Do not allow voltage levels on the input and output pins either to rise above V_{CC} (V_{DD}) or to fall below GND (V_{SS}). Also, follow any prescribed power-on sequence, so that power is applied gradually or in steps rather than abruptly.
(2) Do not allow any abnormal noise signals to be applied to the device.
(3) Set the voltage levels of unused input pins to V_{CC} (V_{DD}) or GND (V_{SS}).
(4) Do not connect output pins to one another.

3.3.6 Input/Output Protection

Wired-AND configurations, in which outputs are connected together, cannot be used, since this short-circuits the outputs. Outputs should, of course, never be connected to V_{CC} (V_{DD}) or GND (V_{SS}).

Furthermore, ICs with tri-state outputs can undergo performance degradation if a shorted output current is allowed to flow for an extended period of time. Therefore, when designing circuits, make sure that tri-state outputs will not be enabled simultaneously.

3.3.7 Load Capacitance

Some devices display increased delay times if the load capacitance is large. Also, large charging and discharging currents will flow in the device, causing noise. Furthermore, since outputs are shorted for a relatively long time, wiring can become fused.

Consult the technical information for the device being used to determine the recommended load capacitance.

3.3.8 Thermal Design

The failure rate of semiconductor devices is greatly increased as operating temperatures increase. As shown in, Figure 3.2 the internal thermal stress on a device is the sum of the ambient temperature and the temperature rise due to power dissipation in the device. Therefore, to achieve optimum reliability, observe the following precautions concerning thermal design:

(1) Keep the ambient temperature (Ta) as low as possible.

(2) If the device's dynamic power dissipation is relatively large, select the most appropriate circuit board material, and consider the use of heat sinks or of forced air cooling. Such measures will help lower the thermal resistance of the package.

(3) Derate the device's absolute maximum ratings to minimize thermal stress from power dissipation.

$\theta ja = \theta jc + \theta ca$

$\theta ja = (Tj - Ta)/P$

$\theta jc = (Tj - Tc)/P$

$\theta ca = (Tc - Ta)/P$

in which θja = thermal resistance between junction and surrounding air (°C/W)

θjc = thermal resistance between junction and package surface, or internal thermal resistance (°C/W)

θca = thermal resistance between package surface and surrounding air, or external thermal resistance (°C/W)

Tj = junction temperature or chip temperature (°C)

Tc = package surface temperature or case temperature (°C)

Ta = ambient temperature (°C)

P = power dissipation (W)

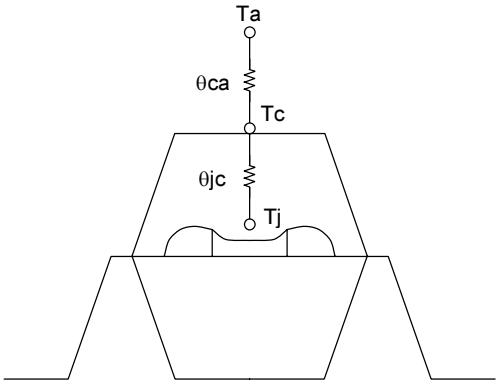


Figure 3.2 Thermal Resistance of Package

3.3.9 Interfacing

When connecting inputs and outputs between devices, make sure input voltage (V_{IL}/V_{IH}) and output voltage (V_{OL}/V_{OH}) levels are matched. Otherwise, the devices may malfunction. When connecting devices operating at different supply voltages, such as in a dual-power-supply system, be aware that erroneous power-on and power-off sequences can result in device breakdown. For details of how to interface particular devices, consult the relevant technical datasheets and databooks. If you have any questions or doubts about interfacing, contact your nearest Toshiba office or distributor.

3.3.10 Decoupling

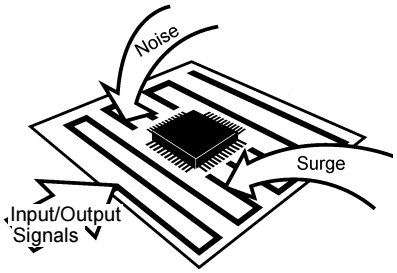
Spike currents generated during switching can cause V_{CC} (V_{DD}) and GND (V_{SS}) voltage levels to fluctuate, causing ringing in the output waveform or a delay in response speed. (the power supply and GND wiring impedance is normally 50 Ω to 100 Ω.) For this reason, the impedance of power supply lines with respect to high frequencies must be kept low. This can be accomplished by using thick and short wiring for the V_{CC} (V_{DD}) and GND (V_{SS}) lines and by installing decoupling capacitors (of approximately 0.01 μF to 1 μF capacitance) as high-frequency filters between V_{CC} (V_{DD}) and GND (V_{SS}) at strategic locations on the printed circuit board.

For low-frequency filtering, it is a good idea to install a 10- to 100-μF capacitor on the printed circuit board (one capacitor will suffice). If the capacitance is excessively large, however, (e.g. several thousand μF) latch-up can be a problem. Be sure to choose an appropriate capacitance value.

An important point about wiring is that, in the case of high-speed logic ICs, noise is caused mainly by reflection and crosstalk, or by the power supply impedance. Reflections cause increased signal delay, ringing, overshoot and undershoot, thereby reducing the device's safety margins with respect to noise. To prevent reflections, reduce the wiring length by increasing the device mounting density so as to lower the inductance (L) and capacitance (C) in the wiring. Extreme care must be taken, however, when taking this corrective measure, since it tends to cause crosstalk between the wires. In practice, there must be a trade-off between these two factors.

3.3.11 External Noise

Printed circuit boards with long I/O or signal pattern lines are vulnerable to induced noise or surges from outside sources. Consequently, malfunctions or breakdowns can result from overcurrent or overvoltage, depending on the types of device used. To protect against noise, lower the impedance of the pattern line or insert a noise-canceling circuit. Protective measures must also be taken against surges.



For details of the appropriate protective measures for a particular device, consult the relevant databook.

3.3.12 Electromagnetic Interference

Widespread use of electrical and electronic equipment in recent years has brought with it radio and TV reception problems due to electromagnetic interference. To use the radio spectrum effectively and to maintain radio communications quality, each country has formulated regulations limiting the amount of electromagnetic interference which can be generated by individual products.

Electromagnetic interference includes conduction noise propagated through power supply and telephone lines, and noise from direct electromagnetic waves radiated by equipment. Different measurement methods and corrective measures are used to assess and counteract each specific type of noise.

Difficulties in controlling electromagnetic interference derive from the fact that there is no method available which allows designers to calculate, at the design stage, the strength of the electromagnetic waves which will emanate from each component in a piece of equipment. For this reason, it is only after the prototype equipment has been completed that the designer can take measurements using a dedicated instrument to determine the strength of electromagnetic interference waves. Yet it is possible during system design to incorporate some measures for the prevention of electromagnetic interference, which can facilitate taking corrective measures once the design has been completed. These include installing shields and noise filters, and increasing the thickness of the power supply wiring patterns on the printed circuit board. One effective method, for example, is to devise several shielding options during design, and then select the most suitable shielding method based on the results of measurements taken after the prototype has been completed.

3.3.13 Peripheral Circuits

In most cases semiconductor devices are used with peripheral circuits and components. The input and output signal voltages and currents in these circuits must be chosen to match the semiconductor device's specifications. The following factors must be taken into account.

(1) Inappropriate voltages or currents applied to a device's input pins may cause it to operate erratically. Some devices contain pull-up or pull-down resistors. When designing your system, remember to take the effect of this on the voltage and current levels into account.

(2) The output pins on a device have a predetermined external circuit drive capability. If this drive capability is greater than that required, either incorporate a compensating circuit into your design or carefully select suitable components for use in external circuits.

3.3.14 Safety Standards

Each country has safety standards which must be observed. These safety standards include requirements for quality assurance systems and design of device insulation. Such requirements must be fully taken into account to ensure that your design conforms to the applicable safety standards.

3.3.15 Other Precautions

(1) When designing a system, be sure to incorporate fail-safe and other appropriate measures according to the intended purpose of your system. Also, be sure to debug your system under actual board-mounted conditions.

(2) If a plastic-package device is placed in a strong electric field, surface leakage may occur due to the charge-up phenomenon, resulting in device malfunction. In such cases take appropriate measures to prevent this problem, for example by protecting the package surface with a conductive shield.

(3) With some microcomputers and MOS memory devices, caution is required when powering on or resetting the device. To ensure that your design does not violate device specifications, consult the relevant databook for each constituent device.

(4) Ensure that no conductive material or object (such as a metal pin) can drop onto and short the leads of a device mounted on a printed circuit board.

3.4 Inspection, Testing and Evaluation

3.4.1 Grounding

⚠CAUTION

Ground all measuring instruments, jigs, tools and soldering irons to earth.
Electrical leakage may cause a device to break down or may result in electric shock.

3.4.2 Inspection Sequence

⚠CAUTION

1) Do not insert devices in the wrong orientation. Make sure that the positive and negative electrodes of the power supply are correctly connected. Otherwise, the rated maximum current or maximum power dissipation may be exc0eeded and the device may break down or undergo performance degradation, causing it to catch fire or explode, resulting in injury to the user.

2) When conducting any kind of evaluation, inspection or testing using AC power with a peak voltage of 42.4 V or DC power exceeding 60 V, be sure to connect the electrodes or probes of the testing equipment to the device under test before powering it on. Connecting the electrodes or probes of testing equipment to a device while it is powered on may result in electric shock, causing injury.

(1) Apply voltage to the test jig only after inserting the device securely into it. When applying or removing power, observe the relevant precautions, if any.

(2) Make sure that the voltage applied to the device is off before removing the device from the test jig. Otherwise, the device may undergo performance degradation or be destroyed.

(3) Make sure that no surge voltages from the measuring equipment are applied to the device.

(4) The chips housed in tape carrier packages (TCPs) are bare chips and are therefore exposed. During inspection take care not to crack the chip or cause any flaws in it.
Electrical contact may also cause a chip to become faulty. Therefore make sure that nothing comes into electrical contact with the chip.

3.5 Mounting

There are essentially two main types of semiconductor device package: lead insertion and surface mount. During mounting on printed circuit boards, devices can become contaminated by flux or damaged by thermal stress from the soldering process. With surface-mount devices in particular, the most significant problem is thermal stress from solder reflow, when the entire package is subjected to heat. This section describes a recommended temperature profile for each mounting method, as well as general precautions which you should take when mounting devices on printed circuit boards. Note, however, that even for devices with the same package type, the appropriate mounting method varies according to the size of the chip and the size and shape of the lead frame. Therefore, please consult the relevant technical datasheet and databook.

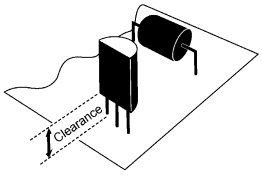
3.5.1 Lead Forming

⚠CAUTION

1) Always wear protective glasses when cutting the leads of a device with clippers or a similar tool. If you do not, small bits of metal flying off the cut ends may damage your eyes.
2) Do not touch the tips of device leads. Because some types of device have leads with pointed tips, you oay prick your finger.

Semiconductor devices must undergo a process in which the leads are cut and formed before the devices can be mounted on a printed circuit board. If undue stress is applied to the interior of a device during this process, mechanical breakdown or performance degradation can result. This is attributable primarily to differences between the stress on the device's external leads and the stress on the internal leads. If the relative difference is great enough, the device's internal leads, adhesive properties or sealant can be damaged. Observe these precautions during the lead-forming process (this does not apply to surface-mount devices):

(1) Lead insertion hole intervals on the printed circuit board should match the lead pitch of the device precisely.
(2) If lead insertion hole intervals on the printed circuit board do not precisely match the lead pitch of the device, do not attempt to forcibly insert devices by pressing on them or by pulling on their leads.
(3) For the minimum clearance specification between a device and a printed circuit board, refer to the relevant device's datasheet and databook. If necessary, achieve the required clearance by forming the device's leads appropriately. Do not use the spacers which are used to raise devices above the surface of the printed circuit board during soldering to achieve clearance. These spacers normally continue to expand due to heat, even after the solder has begun to solidify; this applies severe stress to the device.



(4) Observe the following precautions when forming the leads of a device prior to mounting.

- Use a tool or jig to secure the lead at its base (where the lead meets the device package) while bending so as to avoid mechanical stress to the device. Also avoid bending or stretching device leads repeatedly.
- Be careful not to damage the lead during lead forming.
- Follow any other precautions described in the individual datasheets and databooks for each device and package type.

3.5.2 Mounting on Printed Circuit Board

When soldering the leads on the printed circuit board, be careful not to leave stress on the leads.

Leads must be shaped and aligned to the hole size, and space must be left between the device and the board (Figure 3.6). If leads are not shaped but forced into holes or stress is applied by a tool, corrosion or whiskers may occur where stress is applied, resulting in cutout or shorting of leads. Thus, hole size must be aligned to the lead interval.

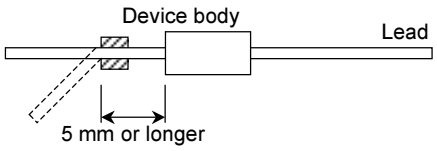


Figure 3.3 How to Bend Leads

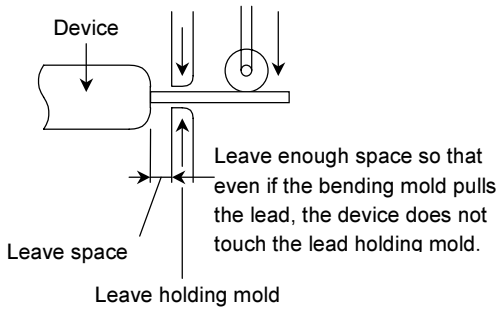


Figure 3.4 How to Bend Leads Using Metal Mold

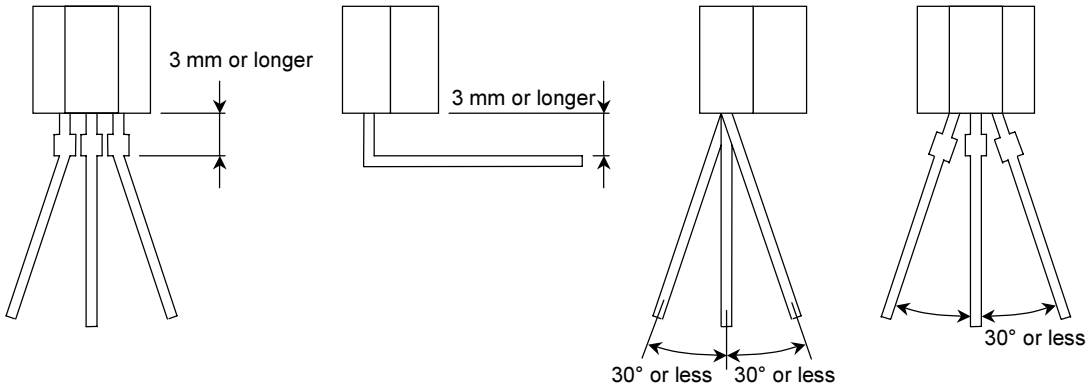


Figure 3.5 How to Bend Leads

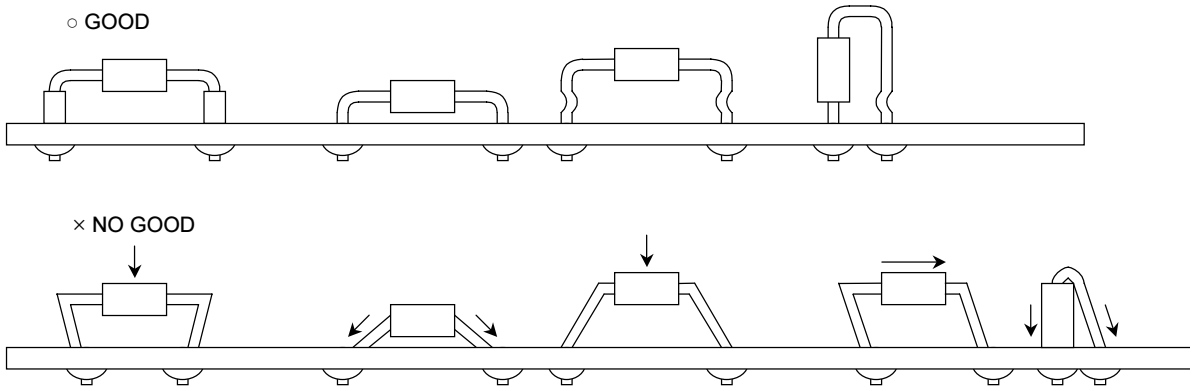


Figure 3.6 Example of Mounting on Printed-Circuit Board

3.5.3 Socket Mounting

(1) When socket mounting devices on a printed circuit board, use sockets which match the inserted device's package.

(2) Use sockets whose contacts have the appropriate contact pressure. If the contact pressure is insufficient, the socket may not make a perfect contact when the device is repeatedly inserted and removed; if the pressure is excessively high, the device leads may be bent or damaged when they are inserted into or removed from the socket.

(3) When soldering sockets to the printed circuit board, use sockets whose construction prevents flux from penetrating into the contacts or which allows flux to be completely cleaned off.

(4) Make sure the coating agent applied to the printed circuit board for moisture-proofing purposes does not stick to the socket contacts.

(5) If the device leads are severely bent by a socket as it is inserted or removed and you wish to repair the leads so as to continue using the device, make sure that this lead correction is only performed once. Do not use devices whose leads have been corrected more than once.

(6) If the printed circuit board with the devices mounted on it will be subjected to vibration from external sources, use sockets which have a strong contact pressure so as to prevent the sockets and devices from vibrating relative to one another.

3.5.4 Soldering Temperature Profile

The soldering temperature and heating time vary from device to device. Therefore, when specifying the mounting conditions, refer to the individual datasheets and databooks for the devices used.

(1) Using a soldering iron

Complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

(2) Using medium infrared ray reflow

- Heating top and bottom with long or medium infrared rays is recommended (see Figure 3.7).

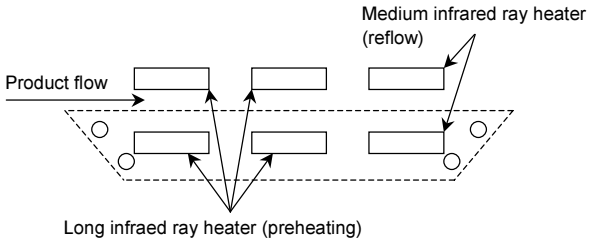


Figure 3.7 Heating Top and Bottom with Long or Medium Infrared Rays

- Complete the infrared ray reflow process within 30 seconds at a package surface temperature of between 210°C and 240°C.
- Refer to Figure 3.8 for an example of a good temperature profile for infrared or hot air reflow.

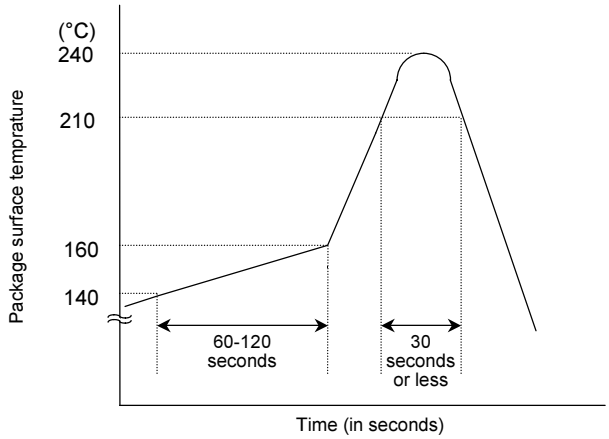


Figure 3.8 Sample Temperature Profile for Infrared or Hot Air Reflow

(3) Using hot air reflow

- Complete hot air reflow within 30 seconds at a package surface temperature of between 210°C and 240°C.
- For an example of a recommended temperature profile, refer to Figure 3.8 above.

(4) Using solder flow

- Apply preheating for 60 to 120 seconds at a temperature of 150°C.
- For lead insertion-type packages, complete solder flow within 10 seconds with the temperature at the stopper (or, if there is no stopper, at a location more than 1.5 mm from the body) which does not exceed 260°C.
- For surface-mount packages, complete soldering within 5 seconds at a temperature of 250°C or less in order to prevent thermal stress in the device.

- Figure 3.9 shows an example of a recommended temperature profile for surface-mount packages using solder flow.

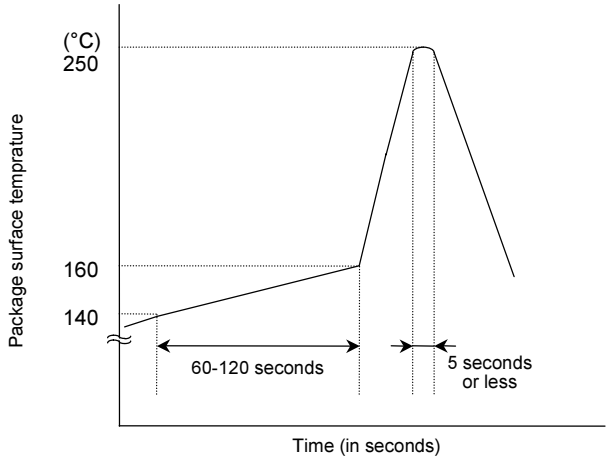


Figure 3.9 Sample Temperature Profile for Solder Flow

3.5.5 Flux Cleaning and Ultrasonic Cleaning

(1) When cleaning circuit boards to remove flux, make sure that no residual reactive ions such as Na or Cl remain. Note that organic solvents react with water to generate hydrogen chloride and other corrosive gases which can degrade device performance.

(2) Washing devices with water will not cause any problems. However, make sure that no reactive ions such as sodium and chlorine are left as a residue. Also, be sure to dry devices sufficiently after washing.

(3) Do not rub device markings with a brush or with your hand during cleaning or while the devices are still wet from the cleaning agent. Doing so can rub off the markings.

(4) The dip cleaning, shower cleaning and steam cleaning processes all involve the chemical action of a solvent. Use only recommended solvents for these cleaning methods. When immersing devices in a solvent or steam bath, make sure that the temperature of the liquid is 50°C or below, and that the circuit board is removed from the bath within one minute.

(5) Ultrasonic cleaning should not be used with hermetically-sealed ceramic packages such as a leadless chip carrier (LCC), pin grid array (PGA) or charge-coupled device (CCD), because the bonding wires can become disconnected due to resonance during the cleaning process. Even if a device package allows ultrasonic cleaning, limit the duration of ultrasonic cleaning to as short a time as possible, since long hours of ultrasonic cleaning degrade the adhesion between the mold resin and the frame material. The following ultrasonic cleaning conditions are recommended:

Frequency: 27 kHz to 29 kHz

Ultrasonic output power: 300 W or less (0.25 W/cm^2 or less)

Cleaning time: 30 seconds or less

Suspend the circuit board in the solvent bath during ultrasonic cleaning in such a way that the ultrasonic vibrator does not come into direct contact with the circuit board or the device.

3.5.6 No Cleaning

If analog devices or high-speed devices are used without being cleaned, flux residues may cause minute amounts of leakage between pins. Similarly, dew condensation, which occurs in environments containing residual chlorine when power to the device is on, may cause between-lead leakage or migration. Therefore, Toshiba recommends that these devices be cleaned.

However, if the flux used contains only a small amount of halogen (0.05 W% or less), the devices may be used without cleaning without any problems.

3.5.7 Mounting Tape Carrier Packages (TCPs)

(1) When tape carrier packages (TCPs) are mounted, measures must be taken to prevent electrostatic breakdown of the devices.

(2) If devices are being picked up from tape, or outer lead bonding (OLB) mounting is being carried out, consult the manufacturer of the insertion machine which is being used, in order to establish the optimum mounting conditions in advance and to avoid any possible hazards.

(3) The base film, which is made of polyimide, is hard and thin. Be careful not to cut or scratch your hands or any objects while handling the tape.

(4) When punching tape, try not to scatter broken pieces of tape too much.

(5) Treat the extra film, reels and spacers left after punching as industrial waste, taking care not to destroy or pollute the environment.

(6) Chips housed in tape carrier packages (TCPs) are bare chips and therefore have their reverse side exposed. To ensure that the chip will not be cracked during mounting, ensure that no mechanical shock is applied to the reverse side of the chip. Electrical contact may also cause a chip to fail. Therefore, when mounting devices, make sure that nothing comes into electrical contact with the reverse side of the chip.
If your design requires connecting the reverse side of the chip to the circuit board, please consult Toshiba or a Toshiba distributor beforehand.

3.5.8 Mounting Chips

Devices delivered in chip form tend to degrade or break under external forces much more easily than plastic-packaged devices. Therefore, caution is required when handling this type of device.

(1) Mount devices in a properly prepared environment so that chip surfaces will not be exposed to polluted ambient air or other polluted substances.

(2) When handling chips, be careful not to expose them to static electricity.
In particular, measures must be taken to prevent static damage during the mounting of chips. With this in mind, Toshiba recommend mounting all peripheral parts first and then mounting chips last (after all other components have been mounted).

(3) Make sure that PCBs (or any other kind of circuit board) on which chips are being mounted do not have any chemical residues on them (such as the chemicals which were used for etching the PCBs).

(4) When mounting chips on a board, use the method of assembly that is most suitable for maintaining the appropriate electrical, thermal and mechanical properties of the semiconductor devices used.

*: For details of devices in chip form, refer to the relevant device's individual datasheets.

3.5.9 Circuit Board Coating

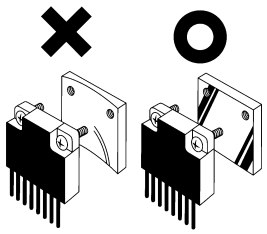
When devices are to be used in equipment requiring a high degree of reliability or in extreme environments (where moisture, corrosive gas or dust is present), circuit boards may be coated for protection. However, before doing so, you must carefully consider the possible stress and contamination effects that may result and then choose the coating resin which results in the minimum level of stress to the device.

3.5.10 Heat Sinks

(1) When attaching a heat sink to a device, be careful not to apply excessive force to the device in the process.

(2) When attaching a device to a heat sink by fixing it at two or more locations, evenly tighten all the screws in stages (i.e. do not fully tighten one screw while the rest are still only loosely tightened). Finally, fully tighten all the screws up to the specified torque.

(3) Drill holes for screws in the heat sink exactly as specified. Smooth the surface by removing burrs and protrusions or indentations which might interfere with the installation of any part of the device.



(4) A coating of silicone compound can be applied between the heat sink and the device to improve heat conductivity. Be sure to apply the coating thinly and evenly; do not use too much. Also, be sure to use a non-volatile compound, as volatile compounds can crack after a time, causing the heat radiation properties of the heat sink to deteriorate.

(5) If the device is housed in a plastic package, use caution when selecting the type of silicone compound to be applied between the heat sink and the device. With some types, the base oil separates and penetrates the plastic package, significantly reducing the useful life of the device. Two recommended silicone compounds in which base oil separation is not a problem are YG6260 from Toshiba Silicone.

(6) Heat-sink-equipped devices can become very hot during operation. Do not touch them, or you may sustain a burn.

3.5.11 Tightening Torque

(1) Make sure the screws are tightened with fastening torques not exceeding the torque values stipulated in individual datasheets and databooks for the devices used.

(2) Do not allow a power screwdriver (electrical or air-driven) to touch devices.

3.5.12 Repeated Device Mounting and Usage

Do not remount or re-use devices which fall into the categories listed below; these devices may cause significant problems relating to performance and reliability.

(1) Devices which have been removed from the board after soldering
(2) Devices which have been inserted in the wrong orientation or which have had reverse current applied
(3) Devices which have undergone lead forming more than once

3.6 Protecting Devices in the Field

3.6.1 Temperature

Semiconductor devices are generally more sensitive to temperature than are other electronic components. The various electrical characteristics of a semiconductor device are dependent on the ambient temperature at which the device is used. It is therefore necessary to understand the temperature characteristics of a device and to incorporate device derating into circuit design. Note also that if a device is used above its maximum temperature rating, device deterioration is more rapid and it will reach the end of its usable life sooner than expected.

3.6.2 Humidity

Resin-molded devices are sometimes improperly sealed. When these devices are used for an extended period of time in a high-humidity environment, moisture can penetrate into the device and cause chip degradation or malfunction. Furthermore, when devices are mounted on a regular printed circuit board, the impedance between wiring components can decrease under high-humidity conditions. In systems which require a high signal-source impedance, circuit board leakage or leakage between device lead pins can cause malfunctions. The application of a moisture-proof treatment to the device surface should be considered in this case. On the other hand, operation under low-humidity conditions can damage a device due to the occurrence of electrostatic discharge. Unless damp-proofing measures have been specifically taken, use devices only in environments with appropriate ambient moisture levels (i.e. within a relative humidity range of 40% to 60%).

3.6.3 Corrosive Gases

Corrosive gases can cause chemical reactions in devices, degrading device characteristics.

For example, sulphur-bearing corrosive gases emanating from rubber placed near a device (accompanied by condensation under high-humidity conditions) can corrode a device's leads. The resulting chemical reaction between leads forms foreign particles which can cause electrical leakage.

3.6.4 Radioactive and Cosmic Rays

Most industrial and consumer semiconductor devices are not designed with protection against radioactive and cosmic rays. Devices used in aerospace equipment or in radioactive environments must therefore be shielded.

3.6.5 Strong Electrical and Magnetic Fields

Devices exposed to strong magnetic fields can undergo a polarization phenomenon in their plastic material, or within the chip, which gives rise to abnormal symptoms such as impedance changes or increased leakage current. Failures have been reported in LSIs mounted near malfunctioning deflection yokes in TV sets. In such cases the device's installation location must be changed or the device must be shielded against the electrical or magnetic field. Shielding against magnetism is especially necessary for devices used in an alternating magnetic field because of the electromotive forces generated in this type of environment.

3.6.6 Interference from Light (ultraviolet rays, sunlight, fluorescent lamps and incandescent lamps)

Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases the device can malfunction. This is especially true for devices in which the internal chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. This problem is not limited to optical semiconductors and EPROMs. All types of device can be affected by light.

3.6.7 Dust and Oil

Just like corrosive gases, dust and oil can cause chemical reactions in devices, which will adversely affect a device's electrical characteristics. To avoid this problem, do not use devices in dusty or oily environments. This is especially important for optical devices because dust and oil can affect a device's optical characteristics as well as its physical integrity and the electrical performance factors mentioned above.

3.6.8 Fire

Semiconductor devices are combustible; they can emit smoke and catch fire if heated sufficiently. When this happens, some devices may generate poisonous gases. Devices should therefore never be used in close proximity to an open flame or a heat-generating body, or near flammable or combustible materials.

3.7 Disposal of Devices and Packing Materials

When discarding unused devices and packing materials, follow all procedures specified by local regulations in order to protect the environment against contamination.

4. Precautions and Usage Considerations Specific to Each Product Group

This section describes matters specific to each product group which need to be taken into consideration when using devices.

4.1 Bipolar Ics

4.1.1 ICs for Use in Automobiles

(1) Design

⚠CAUTION

1) If your design includes an inductive load such as a motor coil, incorporate diodes into your design to prevent negative current from flowing in. Otherwise the device may malfunction or break down due to rush currents or counter electromotive force generated when the device is powered on and off. For information on how to connect the diodes, refer to the relevant individual datasheets for automobile ICs. Breakdown of the devices may result in injury.
2) Ensure that the power supply to any device which incorporates protective functions is stable. If the power supply is unstable, the device may operate erratically, preventing the protective functions from working correctly.
If protective functions fail, the device may break down, causing the device to explode and resulting in injury to the user.

- Heat radiation

  System power supply and driver ICs generate heat. When using these devices, refer to the technical databooks entitled Bipolar ICs for Use in Automobiles and General-Purpose Bipolar IC Databook, and incorporate sufficient heat radiation for the devices used into your design, so that the heat generated will not exceed the stipulated junction temperature (Tj) at which the ICs' internal heat-isolating protective circuits are activated.
- Power supply fuses

  These ICs contain various protective circuits to prevent them from breaking down due to faulty wiring or when pulses of noise are input to the power supply. However, should the IC break down, a large current may continue to flow. To prevent this, use a fuse of the appropriate capacity for the power supply.
  For information about the various types of protective circuit incorporated into the ICs, refer to the individual datasheets for the devices used.
- Power supply

  Do not abruptly increase or decrease the power supply to a device.

(2) Mounting

- Heat sinks

  Depending on the type of package used (e.g. an HSIP7-P-2.54), a device's characteristics may be degraded if the package is attached to a heat sink using screws. In such cases please consult Toshiba or a Toshiba distributor.

4.1.2 Communication Equipment ICs

(1) Design

When using these devices in power amps or system power supplies, be aware that since the effective current capacity of the output pins is 100 mA or higher, a device's DC output current may increase if there is any problem caused by an external component (in particular, leak current from a feedback resistor or a negative feedback capacitor). In some cases this will cause the product to generate heat or to catch fire. Take this into account when designing your product and choosing which components to use. For more detailed information, please refer to the individual datasheets or databooks.

(2) Mounting

Trends toward lightweight and compact design in mobile communications have resulted in the device-mounting board becoming vulnerable to distortion or deformation due to a lack of strength. This causes the devices to be imperfectly connected when mounted on the board. Therefore, carefully examine the board design and mounting methods to ensure that device pins are firmly connected to the board.

4.1.3 Audio/Video Equipment ICs

These devices are designed for use in consumer electronics, typically in television and audio equipment. When using these devices in low-frequency audio amps, system power supply ICs, driver ICs or power ICs, pay attention to the following points:

(1) Design

- Circuit design

  Large leakage current in input or negative feedback capacitors causes the DC output voltage of power ICs to increase. In this case, if the speaker's DC input withstand voltage is low, the speaker may emit smoke or catch fire.

  This must be fully taken into account when selecting the types of capacitor and speaker to use, especially in the case of power ICs of the BTL (bridge-tied load) connection type, in which the DC output voltage is input directly to the speaker.

- Heat radiation

  Power ICs, system power supply ICs and driver ICs generate heat. When using these devices, and incorporate sufficient heat radiation for the devices used into your design, so that the heat generated will not exceed the stipulated junction temperature (Tj = 150°C) at which the ICs' internal thermal shutdown protective circuits are activated. For more detailed information, refer to the individual product datasheets and to the general audio/car audio LSI databooks.

  Also, take into account the operating temperature ranges and characteristics of the peripheral components used with power ICs.

- Power supply fuses

  These ICs contain various protective circuits to prevent them from breaking down due to faulty wiring or noise pulses on the power supply input. However, should the IC break down, a large current may continue to flow. To prevent this, use a fuse of the appropriate capacity for the power supply.

4.1.4 ICs for Motors

(1) Design

- When designing a circuit incorporating a motor, be sure to incorporate a diode to act as a current-limiting resistance and to absorb any counter electromotive force so that the starting current or counter electromotive force does not cause any malfunction or breakdown in the IC. For detailed information concerning this type of design, refer to the relevant individual datasheets or databooks for ICs for motors.
- Circuits which are used to protect ICs from excessive current do not always work. If an IC is used outside its absolute maximum ratings, the IC may break down before the protective circuit is activated.
- Be sure to use a stable power supply for the IC. If the power supply is unstable, the internal circuits of the IC may function erratically, possibly causing the IC to break down.

(2) Heat radiation

- When using a driver IC, be sure to incorporate heat radiation so that the junction temperature (Tj) will never exceed 150°C. Since ICs generate considerable heat, ICs may break down if adequate heat radiation is not provided.
- Circuits which are used to protect devices from excessive heat do not always work. If an IC is used outside its absolute maximum ratings, it may break down before the protective circuit is activated.
- When attaching a heat sink to the driver IC, avoid excessive mechanical stress. Also note that some ICs inhibit the action of silicone rubber.
- When incorporating heat radiation or attaching heat sinks, refer to the relevant individual datasheets or databooks for ICs for motors.

(3) Power supply fuses

In order to prevent excessive current from flowing continuously when the IC breaks down, use a power supply fuse of an appropriate capacity. An IC may break down when used outside its absolute maximum ratings, or when wires or loads induce unusual pulse noise. The fuse capacity must be carefully determined in order to minimize any negative effect in the case of an IC breakdown and the resulting large current flow.

4.1.5 Cautions about Power Dissipation (Constant State)

A transistor by itself will often differ from a board- mounted transistor in its power dissipation characteristics. Changes in power dissipation for representative package types, due to board mounting, are described below.

Each representative package type and the power dissipation change is explained below.

4.1.5.1 Super-Mini Transistors

Allowable power dissipation of a super-mini transistor is 100 to 150 mW as a single unit.

However, when it is mounted on a ceramic board, this value increases depending on the board size. this is shown in Figure 4.1 (transistors used: 2SA1162 and 2SC2712).

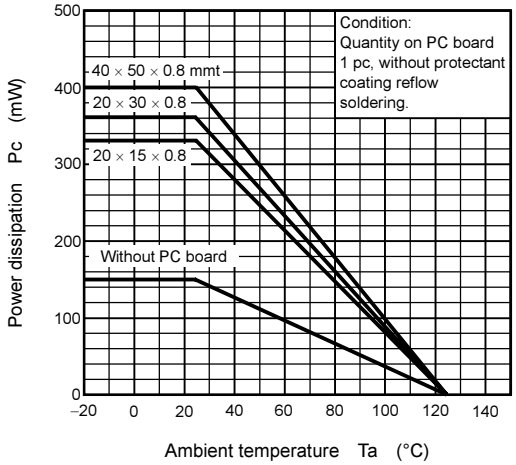


Figure 4.1 Pc (max) when Mounted on Alumi-Ceramic Board Ta Characteristic (2SA1162, 2SC2712)

4.1.5.2 Power-Mini Transistors

Since power-mini transistors are of compact size, Pc_{max} is only 500 mW; however, when they are mounted on a circuit board, thermal diffusion from a drain fin to the board will be high. The drain power dissipation will then range from 1.0 W to 2.0 W, and a circuit design capability equivalent to that of the TO-92MOD (800 to 900 mW) or TO-126 (1.0 to 1.2 W) is possible. Figure 4.2 shows the drain power dissipation for a typical case of circuit-board mounting of a 2SC2873 or 2SA1213.

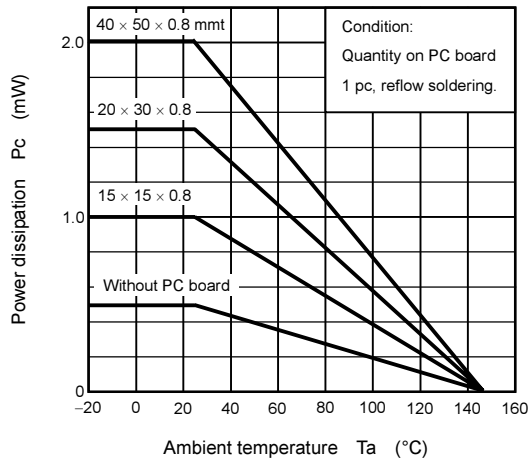


Figure 4.2 Pc (max) when Mounted on Alumi-Ceramic Board Ta Characteristic (2SC2873, 2SA1213)

4.1.5.3 Power-Mold Transistors

For straight-type power-mold transistors, the power dissipation (Pc) = 1 W However, when LB-type transistors have a drain-fin, their installed power dissipation increases significantly. When a power-mold transistor is soldered to an alumina-ceramic board, Pc (1) (1,000 mm^2) = 2 W, Pc (2) (2,500 mm^2) = 3 W Figure 4.3 show the relationship between drain power dissipation Pc and ambient temperature Ta for the transistors 2SC3074 and 2SA1244.

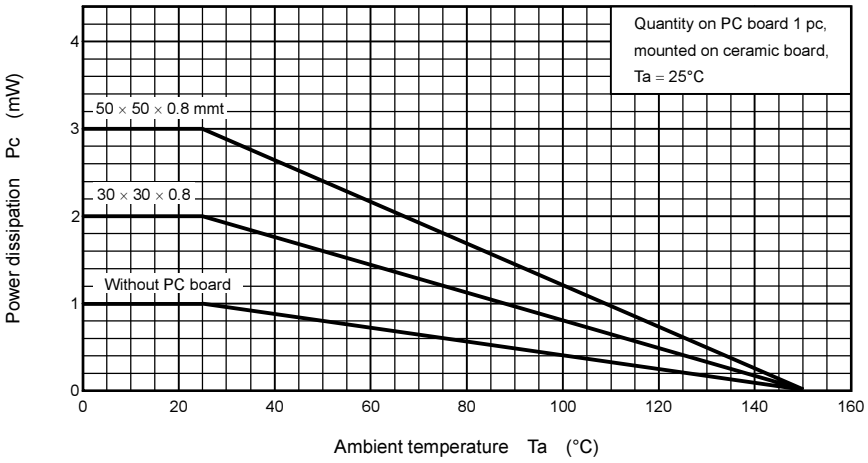


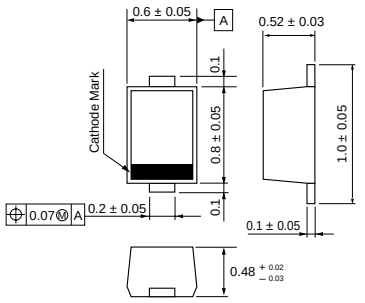
Figure 4.3 Power Dissipation Pc and Ambient Temperature Ta when Transistors are Mounted on Alumina-Ceramic Boards (for 2SC3074 and 2SA1244 devices)

[8] Package Dimensions

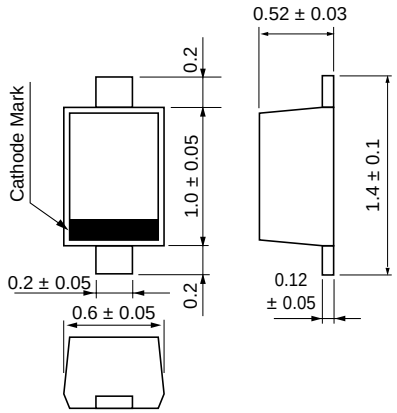
[8] Package Dimensions

Unit: mm

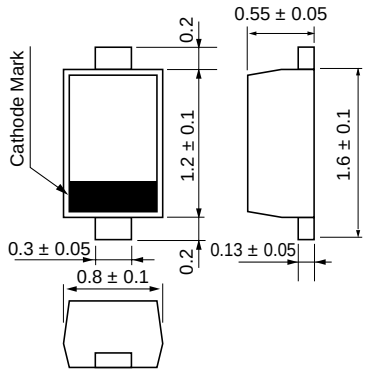
fSC



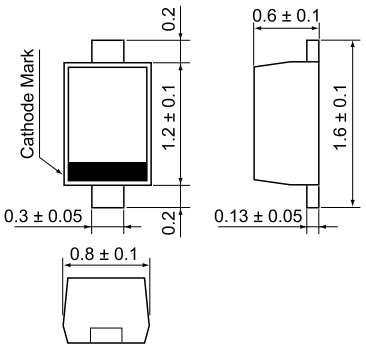
sESC



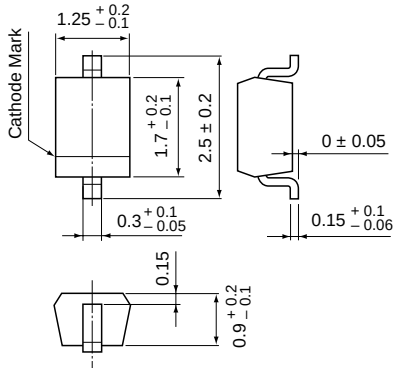
TESC



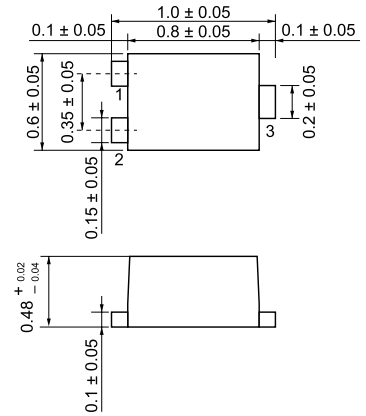
ESC



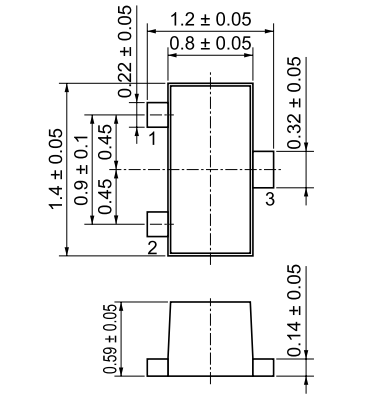
USC



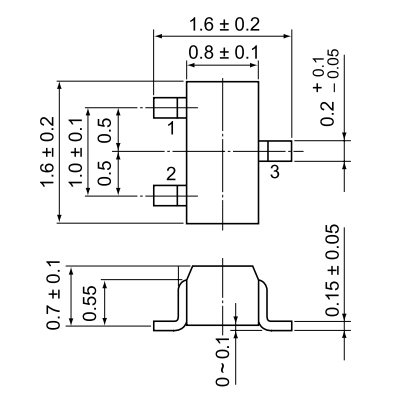
fSM



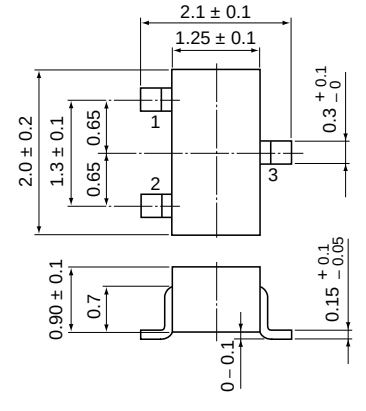
TESM



SSM

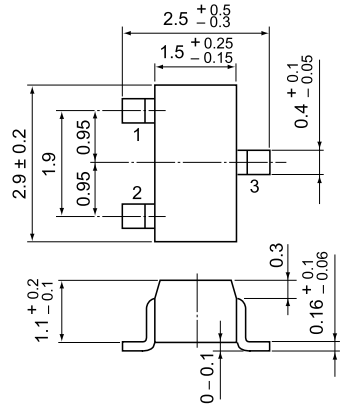


USM

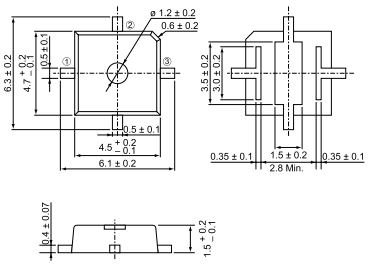


Unit: mm

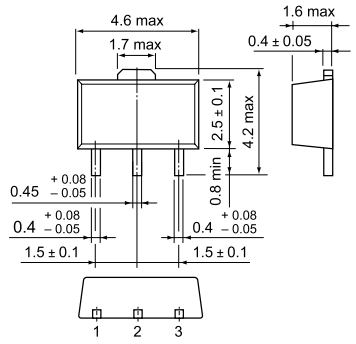
S-MINI



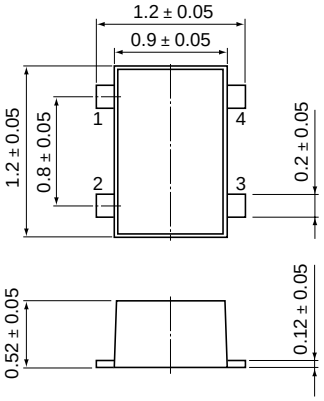
PW-X



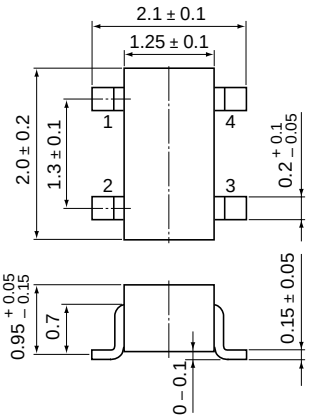
PW-MINI



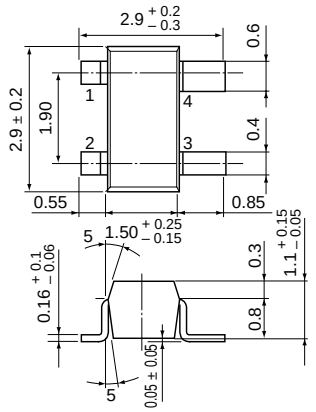
TESQ



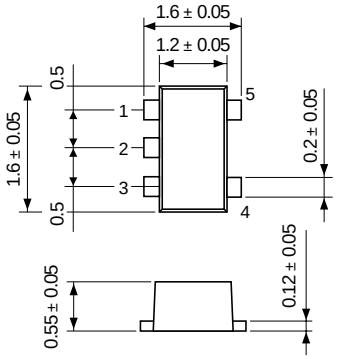
USQ



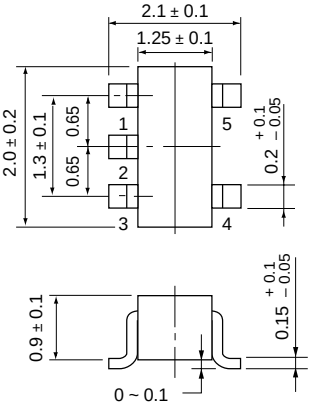
SMQ (ESOP4-P-1.90)



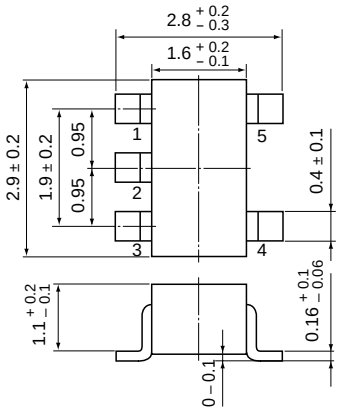
ESV (SON5-P-0.50)



USV (SSOP5-P-0.65)

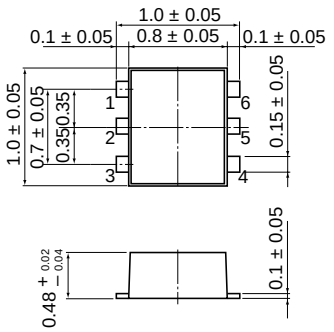


SMV (SSOP5-P-0.95)

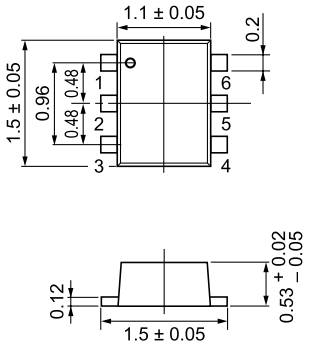


Unit: mm

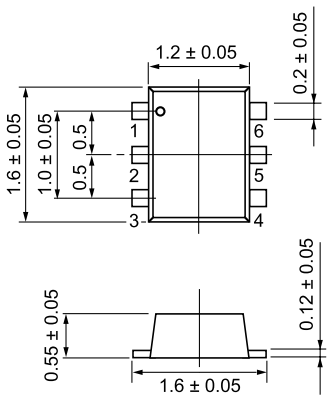
fS6



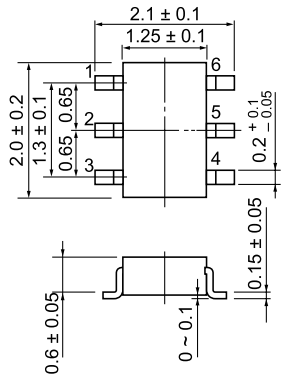
sES6



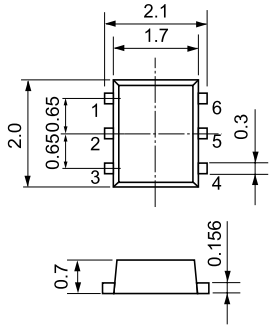
ES6 (SSOP6-P-0.5)



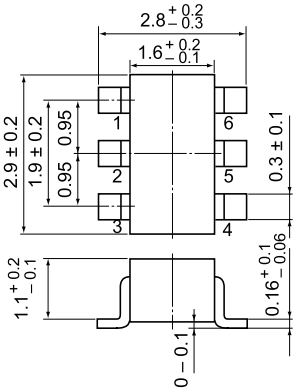
TU6 (SSOP6-P-0.65)



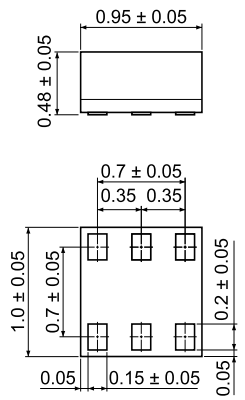
UF6



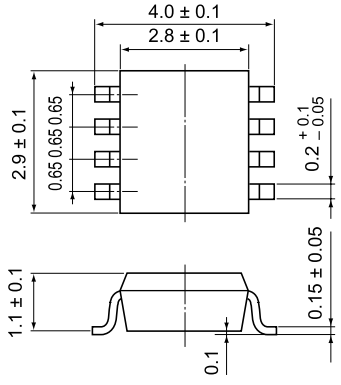
SM6 (SSOP5-P-0.95)



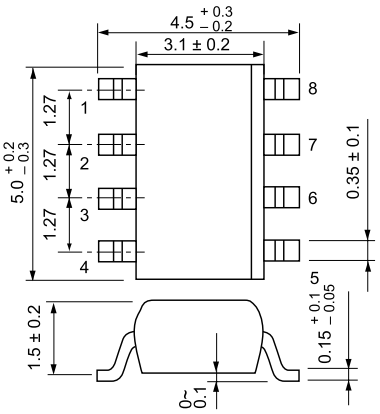
CS6



SM8 (SSOP8-P-0.65)

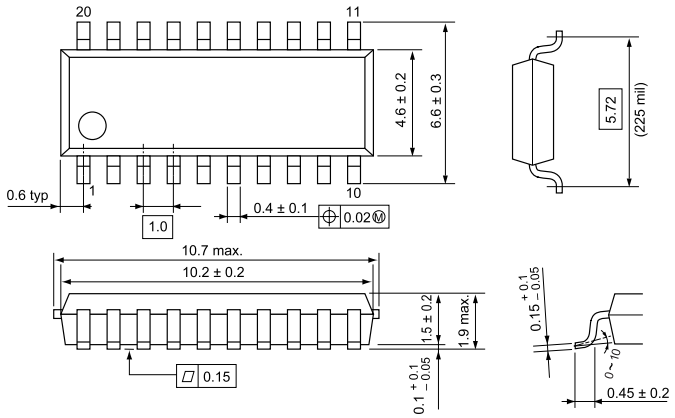


FM8

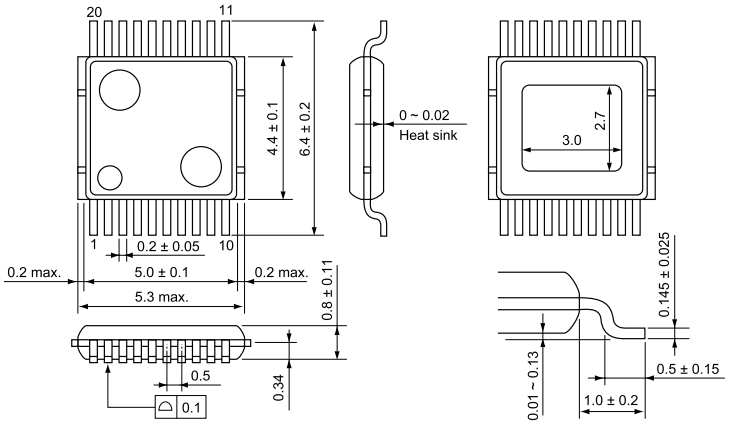


Unit: mm

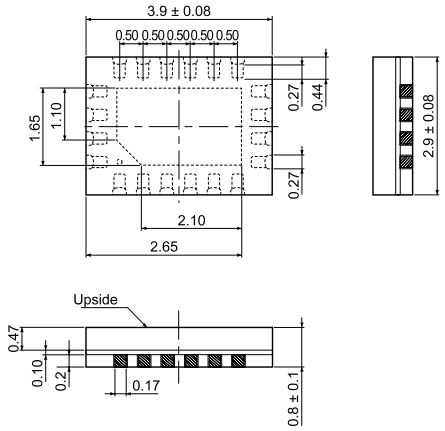
SSOP20



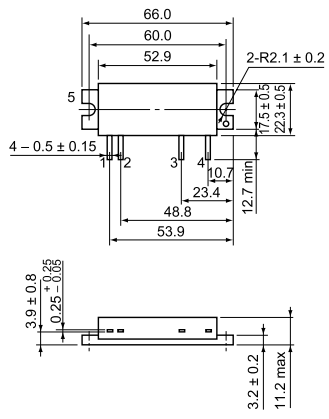
HSOP20



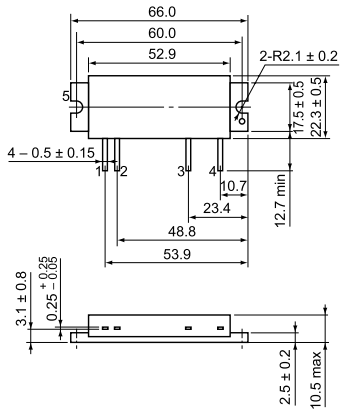
CS20



5-53L

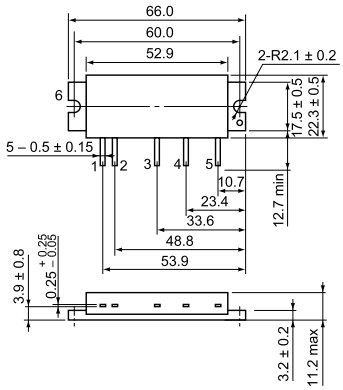


5-53P

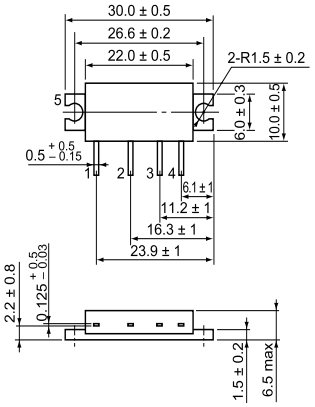


Unit: mm

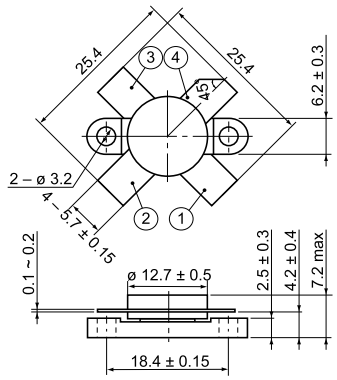
5-53Q



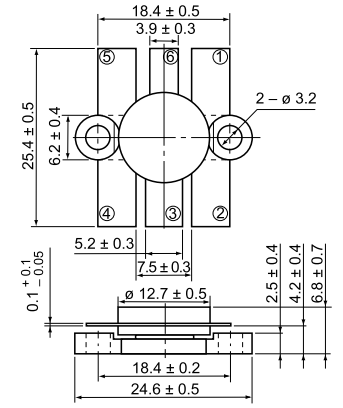
5-23E



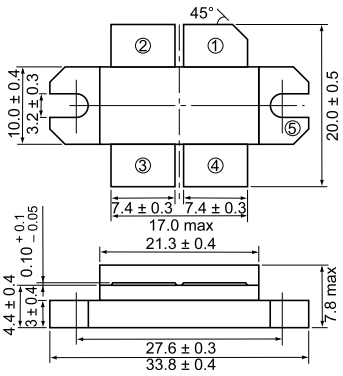
2-13B1A



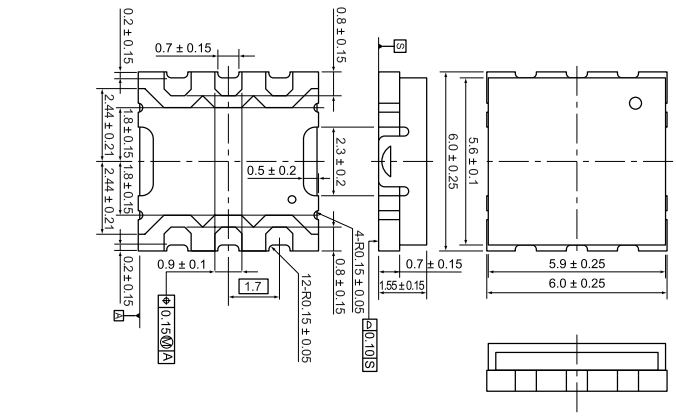
2-13C1A



2-22C2A



S-AU84/S-AU85



[9] List of Final-Phase Products

[9] List of Final-Phase Products

The following listed products will soon be discontinued. Please refer to the recommended replacement devices.

Final-Phase Products

Part Number	Recommended Replacement	Part Number	Recommended Replacement	Part Number	Recommended Replacement
1S2186	1SS341	HN3C08F	—	S-AU27AM	S-AU83H
1S2236	1SV160	HN3C10F	—	S-AU27AH	S-AU83H
1SS238	1SS312, 1SS314	HN3C13FU	—	S-AU35AH	—
1SS239	1SS154, 1SS271	HN3C14FT	—	S-AV6	S-AV35
1SS241	1SS314, 1SS381	HN9C02FT	—	S-AV7	S-AV33
1SS242	1SS315, 1SS295	HN9C03FT	—	S-AV10L	S-AV33
1SV149	—	HN9C07FT	—	S-AV10H	S-AV33
1SV153	1SV214	HN9C10FT	—	S-AV17	S-AV36
1SV153A	—	HN9C13FT	—	S-AV22A	—
1SV161	1SV215	HN9C16FT	—	TA4006F	—
1SV186	1SV245	HN9C18FT	—	TA4007F	—
1SV204	1SV216	HN9C19FT	—	TA4008F	TA4011FU, TA4011AFE
1SV211	1SV262	HN9C21FT	—	TA4009F	TA4012FU, TA4012AFE
1SV212	1SV229	HN9C22FT	—	TA4011F	TA4011FU, TA4011AFE
1SV224	1SV230	MT3S31T	—	TA4012F	TA4012FU, TA4012AFE
2SC2509	—	MT3S46T	—	TA4013FU	—
2SC4255	2SC4252	MT3S46FS	—	TA4102F	—
2SC4392	2SC5107	MT4S34U	—	TA4103F	—
2SC5312	—	MT6L69FS	—	TA4300F	—
2SC5313	—	MT6L70FS	—	TA4301F	—
2SC5317	MT3S07T	MT6P03AE	—	TG2000F	—
3SK250	—	MT6P03AT	—	TG2003V	—
3SK283	3SK240	MT6P04AE	—	TG2202F	—
3SK284	3SK320	MT6P04AT	—	TG2205F	TG2216TU
3SK59	3SK126	S-AU26	—	TG2206F	TG2216TU
HN3C07F	—	S-AU27AL	S-AU83L		

[10] List of Discontinued Products

[10] List of Discontinued Products

The following listed products have been discontinued. Please refer to the recommended replacement devices.

Discontinued Products

Part Number	Recommended Replacement	Part Number	Recommended Replacement	Part Number	Recommended Replacement
1S2094	—	2SC389A	2SC1923	2SC2783	—
1S2187	1SS315	2SC390	2SC2347	2SC2805	2SC3121
1SS42	—	2SC391	2SC2347	2SC2876	2SC5087
1SS148	—	2SC391A	2SC2347	2SC3006	—
1SS155	1SS314	2SC392	2SC2498	2SC3147	—
1SS240	—	2SC392A	2SC2347	2SC3301	2SC3607
1SV100	—	2SC393	—	2SC3302	2SC5087
1SV123	1SV214	2SC396	2SC1923	2SC3445	2SC5084
1SV158	1SV215	2SC397	2SC2347	2SC3608	MT4S04
1SV226	1SV288	2SC784	2SC1923	2SC4316	2SC5089
1SV238	1SV269	2SC784TM	2SC1923	2SC4318	—
1SV255	—	2SC784TMA	2SC1923	2SC4319	MT4S03
1SV256	1SV216	2SC785	2SC1923	2SC4323	2SC5097
1SV257	1SV279	2SC786	2SC1923	2SK19	2SK192A
1SV258	—	2SC787	—	2SK19TM	2SK192A
1SV260	1SV280	2SC864	2SC383TM	2SK61	2SK161
1SV261	1SV309	2SC941	2SC941TM	2SK61LV	2SK161
1SV274	1SV282	2SC1236	2SC5084	2SK192	2SK192A
1SV275	1SV283	2SC1558	2SC5087	2SK1028	—
2SC381TM	2SC1923	2SC1559	2SC5087	2SK1310	2SK1310A
2SC381TMA	2SC1923	2SC1743	2SC5087	2SK1739	2SK1739A
2SC382	—	2SC2099	—	2SK2496	—
2SC382TM	—	2SC2114	—	2SK2497	2SK3179
2SC384	2SC1923	2SC2115	—	2SK2856	2SK3179
2SC385	2SC2349	2SC2328	—	2SK3276	—
2SC385A	2SC2349	2SC2395	—	3SK22	—
2SC385ATM	2SC2349	2SC2531	—	3SK23	2SK192A
2SC386	2SC2349	2SC2638	—	3SK28	2SK192A
2SC386A	2SC2349	2SC2639	—	3SK73	3SK195
2SC387	2SC2347	2SC2640	—	3SK77	—
2SC387A	2SC2347	2SC2641	—	3SK78	3SK195
2SC387A (G)	2SC2347	2SC2642	—	3SK90	—
2SC387A (G) TM	2SC2347	2SC2643	—	3SK101	3SK195
2SC387ATM	2SC2347	2SC2652	—	3SK102	—
2SC389	2SC1923	2SC2663	2SC5087	3SK112	3SK240

Part Number	Recommended Replacement	Part Number	Recommended Replacement	Part Number	Recommended Replacement
3SK114	3SK126	S1255	2SC2644	2-AV24	—
3SK115	3SK291	S1256	2SC2644	2-AV26H	—
3SK121	3SK240	S1297	2SC2498	2-AV28	—
3SK140	3SK240	S2531	2SC2498	2-AV29H	—
3SK145	3SK291	S2676	—	2-AV30H	—
3SK146	3SK232	S9A61	—	TG2002V	—
3SK152	3SK292	2-AU6L	—	TG2005F	TG2006F
3SK159	3SK292	2-AU6VL	—	TG2200AF	TG2216TU
3SK160	3SK225	2-AU39	—	TG2200F	TG2216TU
3SK198	3SK291	2-AU64	—	TG2203F	TG2210FT
DLP238	1SS314	2-AU80	—	TG2204F	TG2216TU