

TLP716

**Plasma display panel
High Speed Interface
Factory Automation**

The TOSHIBA TLP716 consists of an infrared emitting diode and a high speed photodetector. This unit is 6-lead SDIP. TLP716 is 50% smaller than 8PIN DIP and has suited the safety standard reinforced insulation class. So, mounting area in safety standard required equipment can be reduced.

- Inverter Logic (totempole output)
- Package Type : SDIP6
- Guaranteed Performance Over Temperature : -40 to 100°C
- Power Supply Voltage: 4.5 to 5.5 V
- Input Thresholds Current: IFHL = 6.5 mA (max)
- Propagation delay Time (tpHL/tpLH): 75 ns (max)
- Switching speed: 15 MBd (typ.)
- Common mode transient immunity: ±10 kV/μs (min)
- Isolation voltage: 5000 Vrms (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved : EN 60747-5-5 , EN 62368-1 (Note 1)

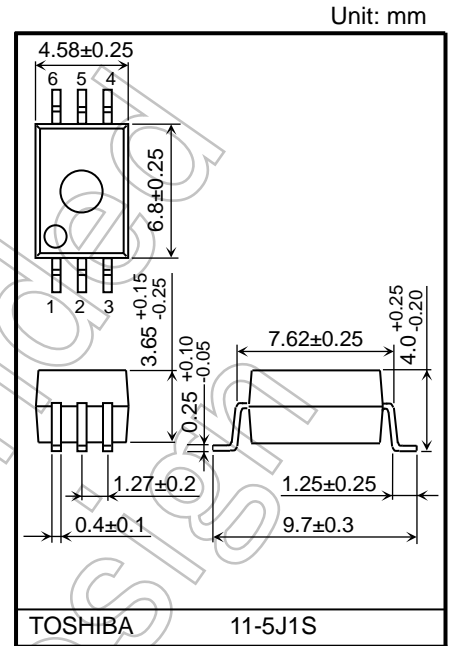
Note 1: When a VDE approved type is needed, please designate the **Option(D4)**.

- Construction Mechanical Rating

Creepage Distance	7.0 mm (min)
Clearance	7.0 mm (min)
Insulation Thickness	0.4 mm (min)

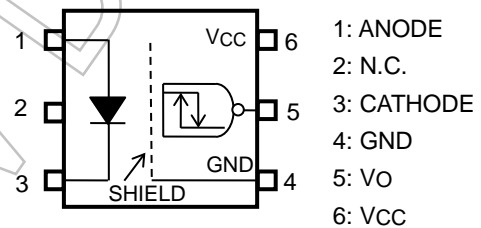
Truth Table

Input	LED	M1	M2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

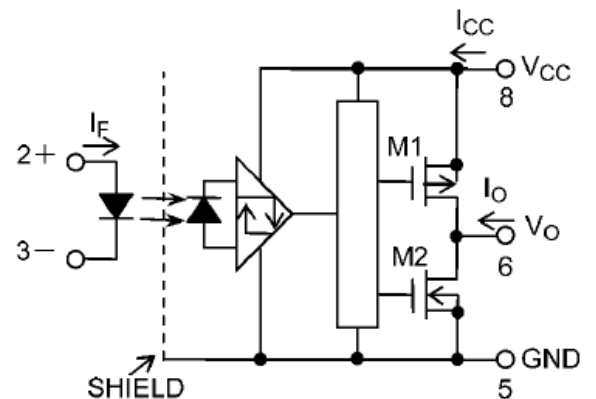


Weight: 0.26 g (typ.)

Pin Configuration (Top View)



Schematic



Note: 0.1 μF bypass capacitor must be connected between pins 6 and 4.

Start of commercial production
2006-06

Absolute Maximum Ratings (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 85°C)	I _F	20	mA
	Forward Current Derating (Ta > 85°C)	ΔI _F /ΔTa	-0.5	mA/°C
	Peak Transient Forward Current (Note1)	I _{FPT}	1	A
	Reverse Voltage	V _R	5	V
	Diode power dissipation	P _D	40	mW
	Diode power dissipation derating (Ta > 85°C)	ΔP _D /ΔTa	-1.0	mW/°C
	Junction Temperature	T _j	125	°C
DETECTOR	Output Current (Ta ≤ 85°C)	I _O	10	mA
	Output Current Derating (Ta > 85°C)	ΔI _O /ΔTa	-0.25	mA/°C
	Output Voltage (V _O ≤ V _{CC})	V _O	-0.5 to 6	V
	Supply Voltage	V _{CC}	-0.5 to 6	V
	Power Dissipation (Ta ≤ 85°C)	P _C	40	mW
	Power Dissipation Derating (Ta > 85°C)	ΔP _C /ΔTa	-1.0	mW/°C
	Junction Temperature	T _j	125	°C
Operating Temperature Range		T _{opr}	-40 to 100	°C
Storage Temperature Range		T _{stg}	-55 to 125	°C
Lead Solder Temperature(10 s)		T _{sol}	260	°C
Isolation Voltage (AC, 60 s, R.H. ≤ 60 %) (Note2)		BV _s	5000	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width PW ≤ 1 μs, 300 pps.

Note 2: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON	I _F (ON)	8	12	18	mA
Input Voltage, OFF	V _F (OFF)	0	—	0.8	V
Supply Voltage (Note1)(Note2)(Note 3)	V _{CC}	4.5	5	5.5	V

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: This item denotes operating ranges, not meaning of recommended operating conditions.

Note 2: The detector of this product requires a power supply voltage (V_{CC}) of 4.5 V or higher for stable operation. If the V_{CC} is lower than this value, an I_{CC} may increase, or an output may be unstable. Be sure to use the product after checking the supply current, and the operation of a power-on/-off.

Note 3: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

The correlation between input current and switching speed and drive circuit (reference information)

Input Current (I _F)	TEST CIRCUIT (Psg 4)	Typical Switching Speed
12mA	1	14 – 16 MBd
8mA	1	11 – 13 MBd
8mA	2 (with Speed up capacitor)	16 – 20 MBd

Electrical Characteristics

(Unless otherwise specified, Ta = -40 to 100°C, V_{CC} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Input Forward Voltage	V _F	I _F = 10 mA, Ta = 25 °C	—	1.65	1.8	V
Temperature Coefficient of Forward Voltage	ΔV _F /ΔTa	I _F = 10 mA	—	-2.0	—	mV/°C
Input Reverse Current	I _R	V _R = 5 V, Ta = 25 °C	—	—	10	μA
Input Capacitance	C _T	V = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
Logic Low Output Voltage	V _{OL}	I _{OL} = 1.6 mA, I _F = 12 mA V _{CC} = 5 V	—	—	0.4	V
Logic High Output Voltage	V _{OH}	I _{OH} = -0.02 mA, V _F = 1.05 V V _{CC} = 5 V	4.0	—	—	V
Logic Low Supply Current	I _{CCL}	I _F = 12 mA	—	—	5.0	mA
Logic High Supply Current	I _{CCH}	V _F = 0 V	—	—	5.0	mA
Input Current Logic Low Output	I _{FHL}	I _O = 1.6 mA, V _O < 0.4 V	—	—	6.5	mA
Input Voltage Logic High Output	V _{FLH}	I _O = -0.02 mA, V _O > 4.0 V	0.8	—	—	V

Note: All typical values are at Ta = 25°C, V_{CC} = 5 V, I_{F(ON)} = 12 mA unless otherwise specified

Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance input to output	C _s	V _S = 0 V, f = 1 MHz	—	0.8	—	pF
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 V	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 60 s	5000	—	—	V _{rms}

Note : Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

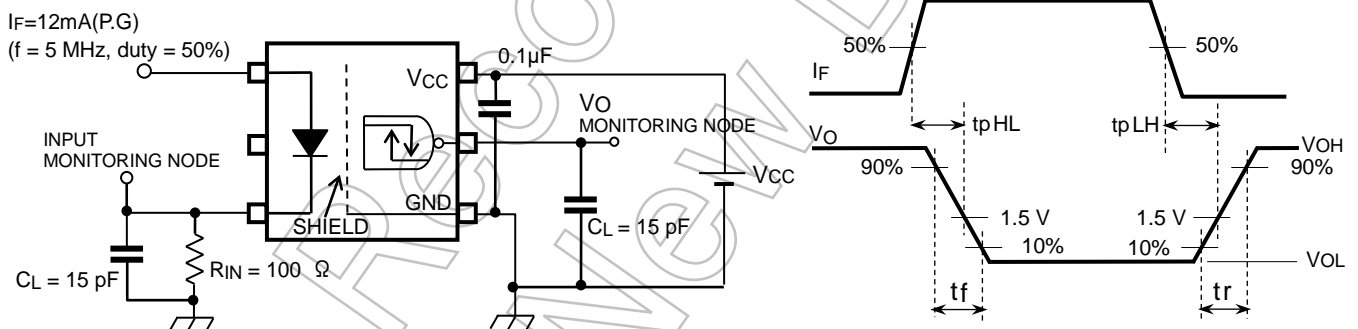
Switching Characteristics (Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 5.5 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT
propagation Delay Time to Logic Low output	t_{pHL}	1	$I_F = 0 \rightarrow 12$ mA	—	—	75	ns
propagation Delay Time to Logic High output	t_{pLH}		$I_F = 12 \rightarrow 0$ mA				
propagation Delay Time to Logic Low output	t_{pHL}	2	$V_{IN} = 0 \rightarrow 5$ V ($I_F = 0 \rightarrow 8$ mA)	—	—	65	ns
propagation Delay Time to Logic High output	t_{pLH}		$V_{IN} = 5 \rightarrow 0$ V ($I_F = 8 \rightarrow 0$ mA)				
Switching Time Dispersion between ON and OFF	$ t_{pLH} - t_{pHL} $	1	$I_F = 12$ mA, $R_{IN} = 100 \Omega$, $C_L = 15$ pF (Note 1)	—	—	45	ns
Output Fall Time (90 to 10%)	t_f		$I_F = 0 \rightarrow 12$ mA				
Output Rise Time (10 to 90%)	t_r		$I_F = 12 \rightarrow 0$ mA				
Common Mode transient Immunity at High Level Output	CMH	3	$V_{CM} = 1000$ Vp-p, $I_F = 0$ mA, $V_{O(\text{Min})} = 4$ V, $T_a = 25^\circ\text{C}$	10000	—	—	V/ μs
Common Mode transient Immunity at Low Level Output	CML		$V_{CM} = 1000$ Vp-p, $I_F = 12$ mA, $V_{O(\text{Max})} = 0.4$ V, $T_a = 25^\circ\text{C}$	-10000	—	—	V/ μs

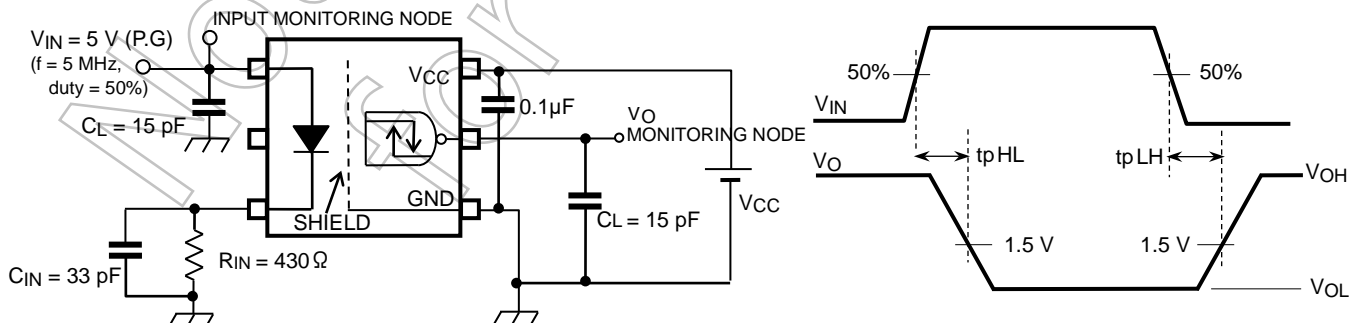
Note: All typical values are at $T_a = 25^\circ\text{C}$

Note 1: C_L is approximately 15 pF which includes probe and Jig/stray wiring capacitance.

TEST CIRCUIT 1: t_{pLH} , t_{pHL}

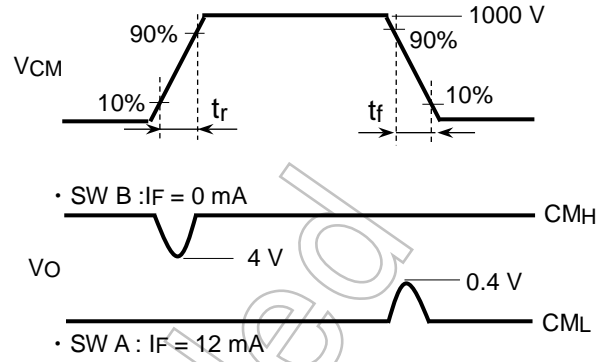
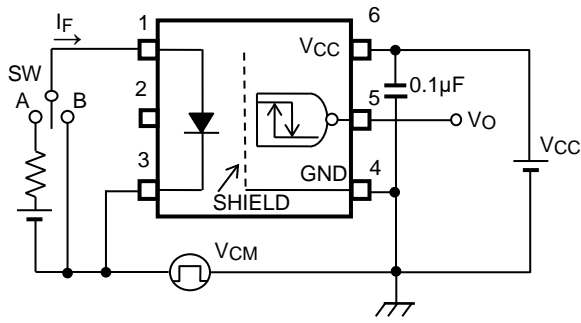


TEST CIRCUIT 2: t_{pLH} , t_{pHL}



The PROBE and JIG capacitances are included in C_L .
(P.G) : Pulse Generator

TEST CIRCUIT 3: Common-Mode Transient Immunity Test Circuit



$$CMH = \frac{800(V)}{tr(\mu s)} \quad CML = - \frac{800(V)}{tf(\mu s)}$$

Note: CML (CMH) is the maximum rate of fall (rise) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

Not Recommended for New Designs

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