

SSM3J314T

○ High Speed Switching Applications

- 4.0V drive
- Low ON-resistance: $R_{ON} = 100\text{m}\Omega$ (max) (@ $V_{GS} = -4.0\text{ V}$)
 $R_{ON} = 54\text{m}\Omega$ (max) (@ $V_{GS} = -10\text{ V}$)

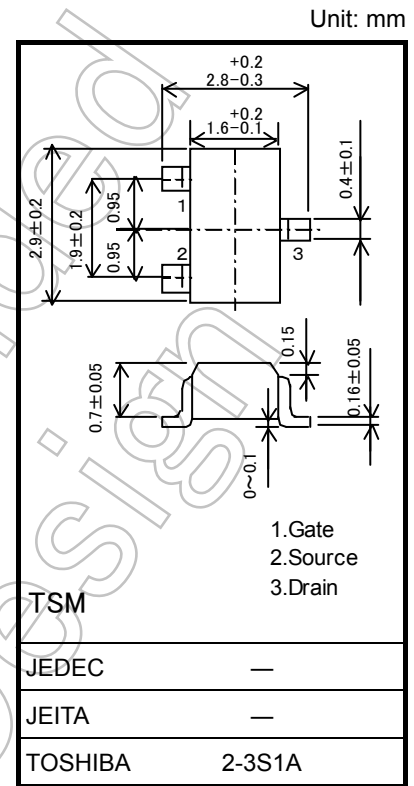
Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DSS}	-30	V
Gate-Source voltage	V_{GSS}	± 20	V
Drain current	DC	I_D	-3.5
	Pulse	I_{DP}	-7.0
Drain power dissipation	P_D (Note 1)	700	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board.
 (25.4 mm × 25.4 mm × 1.6mm, Cu Pad: 645 mm²)



Weight: 10 mg (typ.)

Electrical Characteristics (Ta = 25°C)

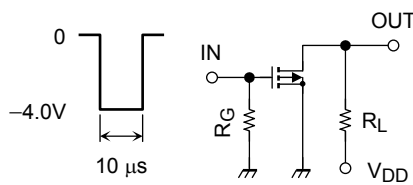
Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0\text{ V}$	-30	—	—	V
	$V_{(BR)DSX}$	$I_D = -1\text{ mA}, V_{GS} = 20\text{ V}$	-15	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	—	—	-10	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -5\text{ V}, I_D = -1\text{ mA}$	-0.8	—	-2.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -5\text{ V}, I_D = -2.0\text{ A}$ (Note2)	3.7	7.4	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -2.0\text{ A}, V_{GS} = -10\text{ V}$ (Note2)	—	38	54	mΩ
		$I_D = -2.0\text{ A}, V_{GS} = -4.0\text{ V}$ (Note2)	—	69	100	
Input capacitance	C_{iss}	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	505	—	pF
Output capacitance	C_{oss}		—	138	—	
Reverse transfer capacitance	C_{rss}		—	105	—	
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}, I_D = -3.5\text{ A}$ $V_{GS} = -10\text{ V}$	—	11.5	—	nC
Gate-Source Charge	Q_{gs}		—	8.9	—	
Gate-Drain Charge	Q_{gd}		—	2.6	—	
Switching time	Turn-on time	t_{on}	$V_{DD} = -15\text{ V}, I_D = -1.0\text{ A},$ $V_{GS} = 0\text{ to }-4.0\text{ V}, R_G = 10\ \Omega$	—	20	ns
	Turn-off time	t_{off}		—	20	
Drain-Source forward voltage	V_{DSF}	$I_D = 3.5\text{ A}, V_{GS} = 0\text{ V}$ (Note2)	—	0.8	1.2	V

Note2: Pulse test

Start of commercial production
 2007-03

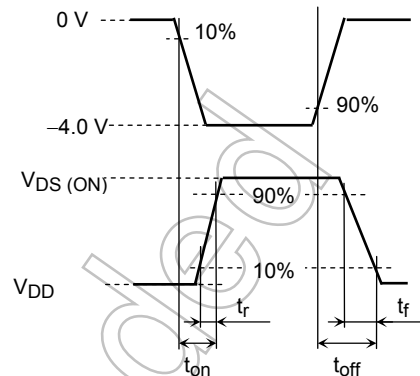
Switching Time Test Circuit

(a) Test Circuit



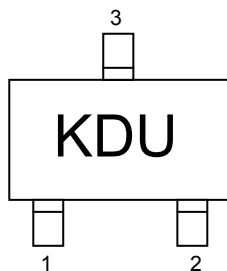
$V_{DD} = -15\text{ V}$
 $R_G = 10\ \Omega$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5\text{ ns}$
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}

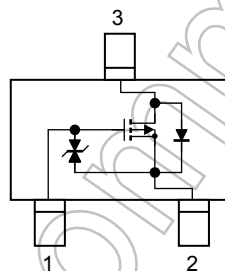


(c) V_{OUT}

Marking



Equivalent Circuit (top view)



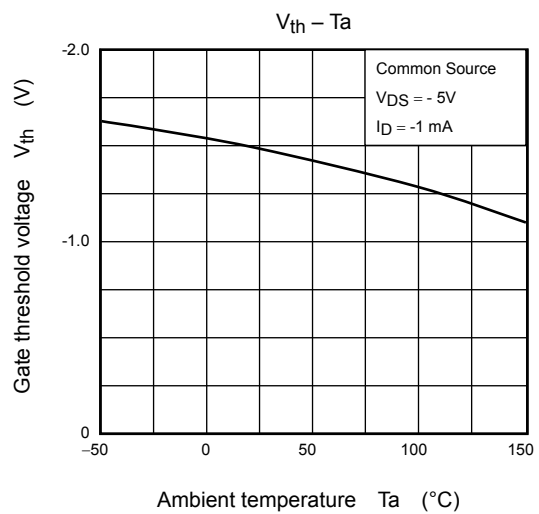
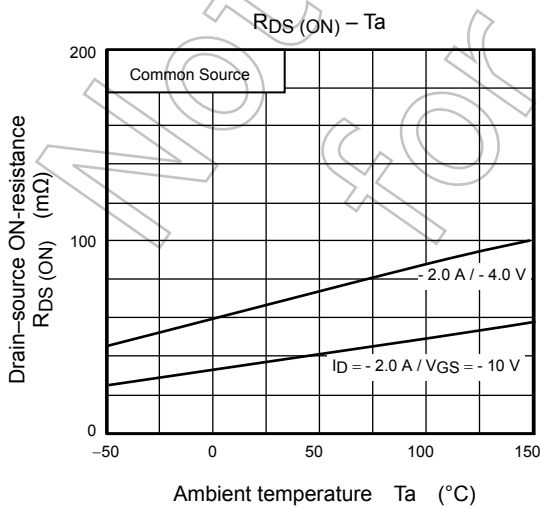
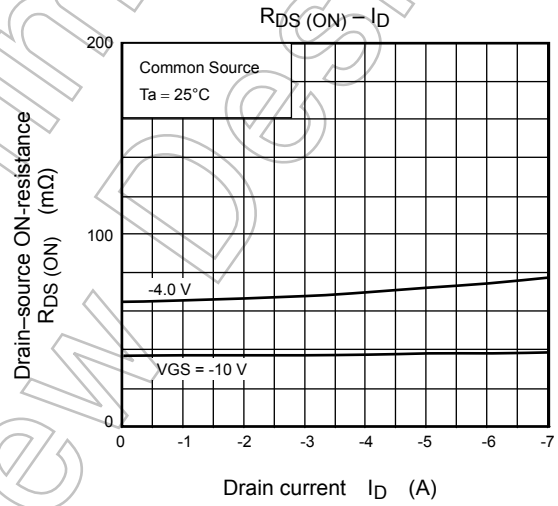
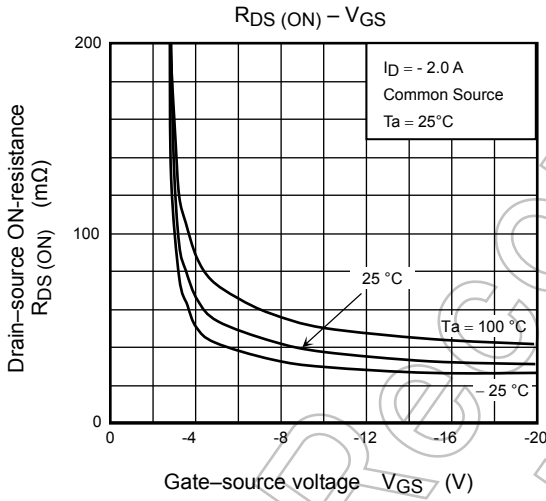
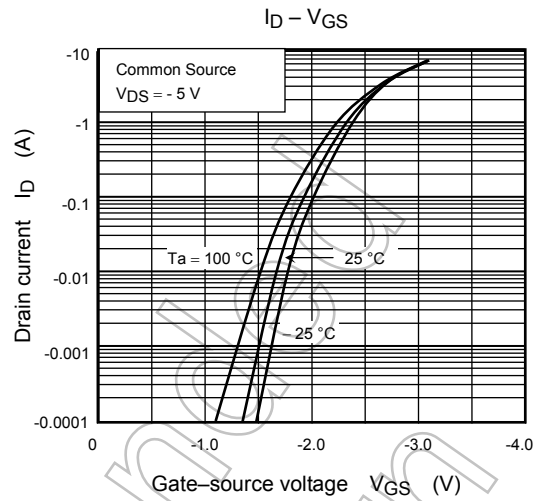
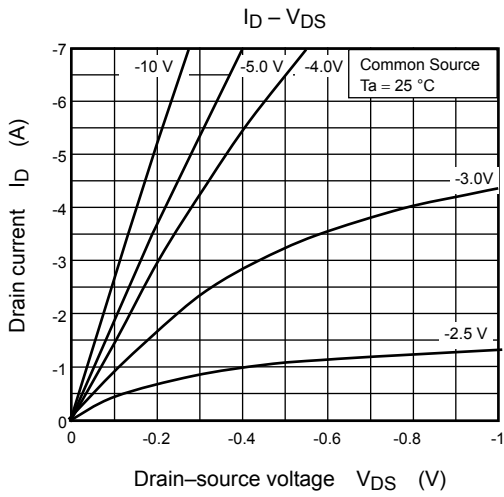
Notice on Usage

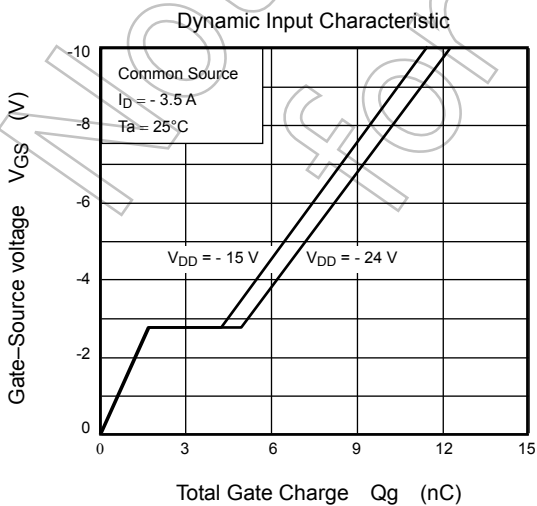
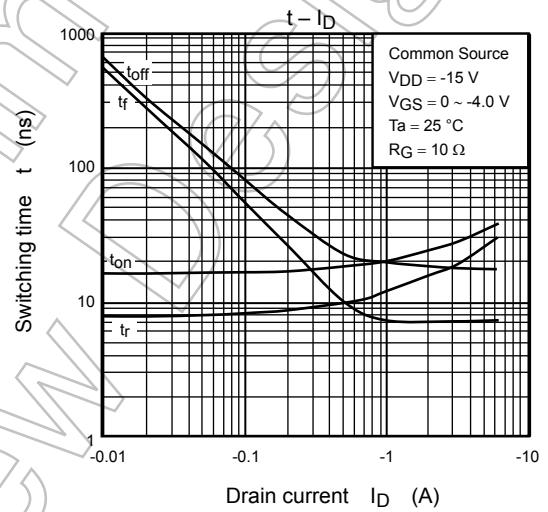
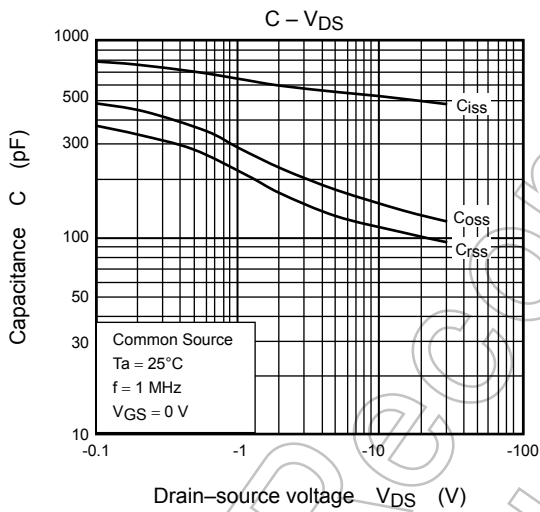
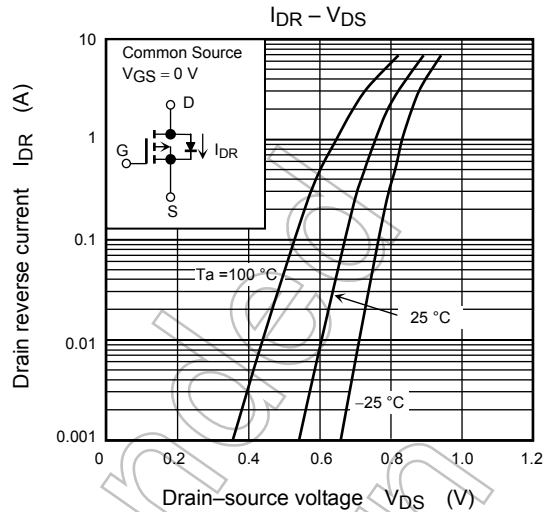
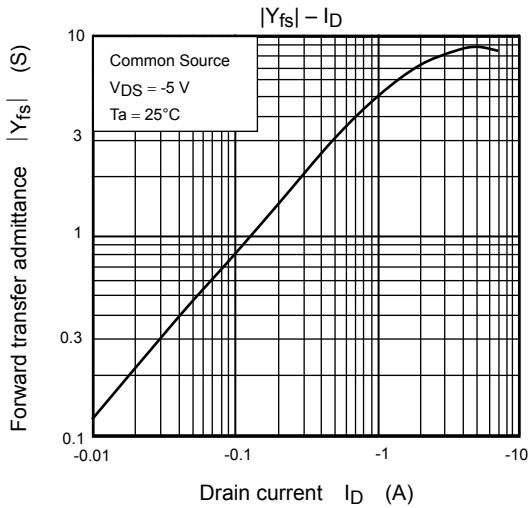
V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = -1\text{ mA}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires a higher voltage than V_{th} and $V_{GS(OFF)}$ requires a lower voltage than V_{th} . (The relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.)

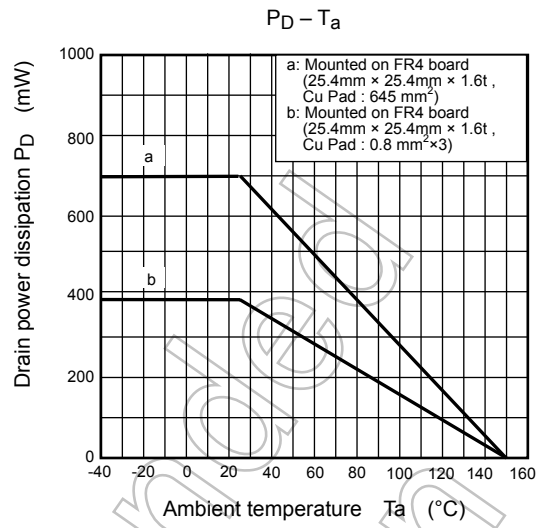
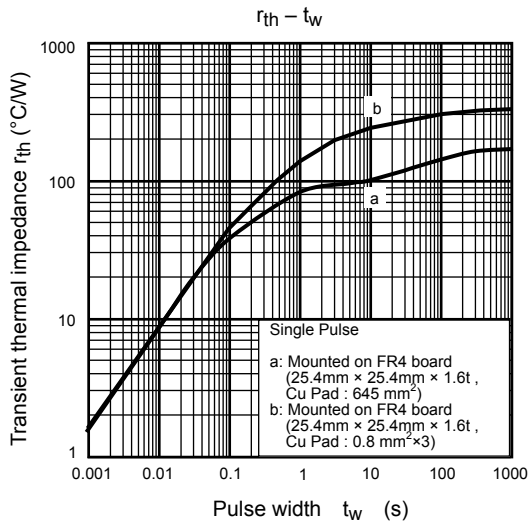
Take this into consideration when using the device.

Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.







Not Recommended for New Design

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