September 2008

Dear Customer

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

Caution in Setting the UART Noise Rejection Time (September 2008)

* If your datasheet is dated 1 July 2008 or earlier, please download the latest datasheet or request it from your local Toshiba office.

Note on Using the Serial Expansion Interface (SEI) (November 2006)

* If your datasheet is dated 19 September 2006 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA Microcontrollers TLCS-870 Family

TLCS-870/X Series

TMP88CH40 TMP88CH40I TMP88PH40 TMP88CH41 TMP88PH41 TMP88FH41 TMP88CS42
TMP88PS42 TMP88CS43 TMP88FW44 TMP88FW45 TMP88FW45A TMP88F846 TMP88CH47
TMP88CK48 TMP88CM48 TMP88CS48A TMP88CK49 TMP88CM49 TMP88C060

TLCS-870/C Series

TMP86P202 TMP86P203 TMP86CH06 TMP86CH06A TMP86PH06 TMP86C906 TMP86C407
TMP86C407I TMP86C407S TMP86C807 TMP86C807I TMP86C807S TMP86F807 TMP86P807
TMP86C408 TMP86C408I TMP86C408S TMP86C808 TMP86C808I TMP86C808S TMP86F808
TMP86P808 TMP86C908 TMP86C809 TMP86CH09 TMP86F409 TMP86F809 TMP86FH09
TMP86FH09A TMP86C909 TMP86C912 TMP86CH12 TMP86FH12 TMP86C420 TMP86C820
TMP86P820 TMP86CH21 TMP86CH21A TMP86C822 TMP86CH22 TMP86PH22 TMP86CP23
TMP86CP23A TMP86CM23 TMP86CM23A TMP86FS23 TMP86PM23 TMP86PS23 TMP86C923
TMP86FP24 TMP86CM25 TMP86CM25A TMP86CS25 TMP86CS25A TMP86FM25 TMP86PS25
TMP86C925 TMP86FM26 TMP86CM27 TMP86CP27A TMP86FS27 TMP86PS27 TMP86C927
TMP86CS28 TMP86FS28 TMP86C829 TMP86C829A TMP86C829B TMP86CH29 TMP86CH29A
TMP86CH29B TMP86CM29 TMP86CM29A TMP86CM29B TMP86CM29L TMP86FM29 TMP86PM29
TMP86PM29A TMP86PM29B TMP86C929A TMP86CS41 TMP86CS43 TMP86CS44 TMP86PS44
TMP86C944 TMP86C845 TMP86C846 TMP86CH46A TMP86CM46A TMP86FH46 TMP86FH46A
TMP86PH46 TMP86PM46 TMP86C847 TMP86C847I TMP86C847S TMP86CH47A TMP86CH47I
TMP86CH47S TMP86CM47A TMP86FH47 TMP86FH47A TMP86PH47 TMP86PM47 TMP86PM47A
TMP86C947 TMP86FM48 TMP86C948 TMP86CH49 TMP86CM49 TMP86CS49 TMP86FS49
TMP86FS49 TMP86FS49AI TMP86FS49B TMP86PM49 TMP86C949 TMP86CS64 TMP86CS64A
TMP86FS64 TMP86PS64 TMP86C964 TMP86CH72 TMP86CM72 TMP86PM72 TMP86C972
TMP86CK74A TMP86CM74A TMP86PM74A TMP86C974 TMP86CH87R TMP86CM87R TMP86PM87R
TMP86C987 TMP86C989 TMP86CH92I TMP86CH92S TMP86FH92 TMP86FH92I TMP86FH93
TMP86C993

TLCS-870 Series

TMP87CH29 TMP87CK29 TMP87CM29 TMP87PM29 TMP87CH48 TMP87CH48I TMP87CM48
TMP87PH48 TMP87PM48 TMP87CM53 TMP87PM53 TMP87CS68 TMP87PS68

*Applicable products include all TLCS-870 Family microcontrollers with the UART function including custom products and products supplied as bare chips that are not listed above. If you have any questions, please contact your local Toshiba sales representative.

September 2008

Caution in Setting the UART Noise Rejection Time

With regard to the TLCS-870, TLCS-870/X and TLCS-870/C Series of Toshiba's 8-bit microcontrollers listed above, please be informed that certain combinations of transfer clock frequency and noise rejection time should not be used in the UART (asynchronous serial interface) as explained below. If you need further information, please contact your local Toshiba sales representative.

[Applicable Usage Conditions]

This caution applies when the timer/counter interrupt is selected as a transfer clock of the UART and the transfer clock frequency (fc) and the RXD input noise rejection time are set to one of the combinations shown in the table below. Under any other conditions, the noise rejection can be used without any problem.

Communication mode setting	Transfer clock select	Transfer clock frequency [Hz] (Note)	RXD input noise rejection time setting	fc frequency [MHz]	Communication speed [bps]
Receive operation (RXE=1)	Timer/counter interrupt (BRG=110)	fc/8	Reject pulses shorter than 31/fc as noise (RXDNC=01)	1.229	9600
				2.458	19200
				4.915	38400
				9.830	76800
		fc/16	Reject pulses shorter than 63/fc as noise (RXDNC=10)	1.229	4800
				2.458	9600
				4.915	19200
				9.830	38400
				19.661	76800
		fc/32	Reject pulses shorter than 127/fc as noise (RXDNC=11)	1.229	2400
				2.458	4800
				4.915	9600
				9.830	19200
				19.661	38400

Note: The transfer clock is calculated by the following equation:
Transfer clock [Hz] = Timer/counter source clock [Hz] ÷ TTREG set value

[Problem] In receive operation (RXE=1), input data on the RXD pin may not be received properly.

[Workaround] If you are using the UART with one of the above noise rejection time settings, disable the noise rejection or change the noise rejection time to a shorter period.

TOSHIBA Microcontrollers TLCS-870 Family
TLCS-870/C Series

TMP86C407/I/S	TMP86C807/I/S	TMP86F807	TMP86P807	TMP86C408/I/S
TMP86C808/I/S	TMP86F808	TMP86P808	JT5BR6	TMP86FH09
TMP86F809	TMP86F409	TMP86CH09	TMP86C809	TMP86CH87R
TMP86CM87R	TMP86PM87R			

November 2006

Dear Customer

Note on Using the Serial Expansion Interface (SEI)

We would like to inform you of the following note on using the Serial Expansion Interface (SEI) incorporated in some of Toshiba's TLCS-870/C Series 8-bit microcontrollers. If you need any further information, please contact your local Toshiba sales representative.

[Note on using the SEI]

The MISO pin of a slave device is set as an output when the SEE bit in the SECR register is set to 1 (enable SEI operation) regardless of the /SS pin state.

The MISO pin is not put in a high-impedance state even if the /SS pin of the slave device is driven high. To place the MISO pin in a high-impedance state, the SEE bit must be cleared to 0 (disable SEI operation).

In a system in which the MISO pins of more than one slave device are interconnected, the SEE bit of each inactive slave device must be cleared to 0 to prevent the MISO bus from being occupied by inactive slave devices. The measures to be taken are explained below.

[Measures to be taken in a system comprising multiple slave devices]

Slave device

- Each slave device should set the SEE bit to 1 only when the /SS pin is low.
- As soon as the /SS pin is driven high, each slave device must clear the SEE bit to 0 to release the MISO pin.

Master device

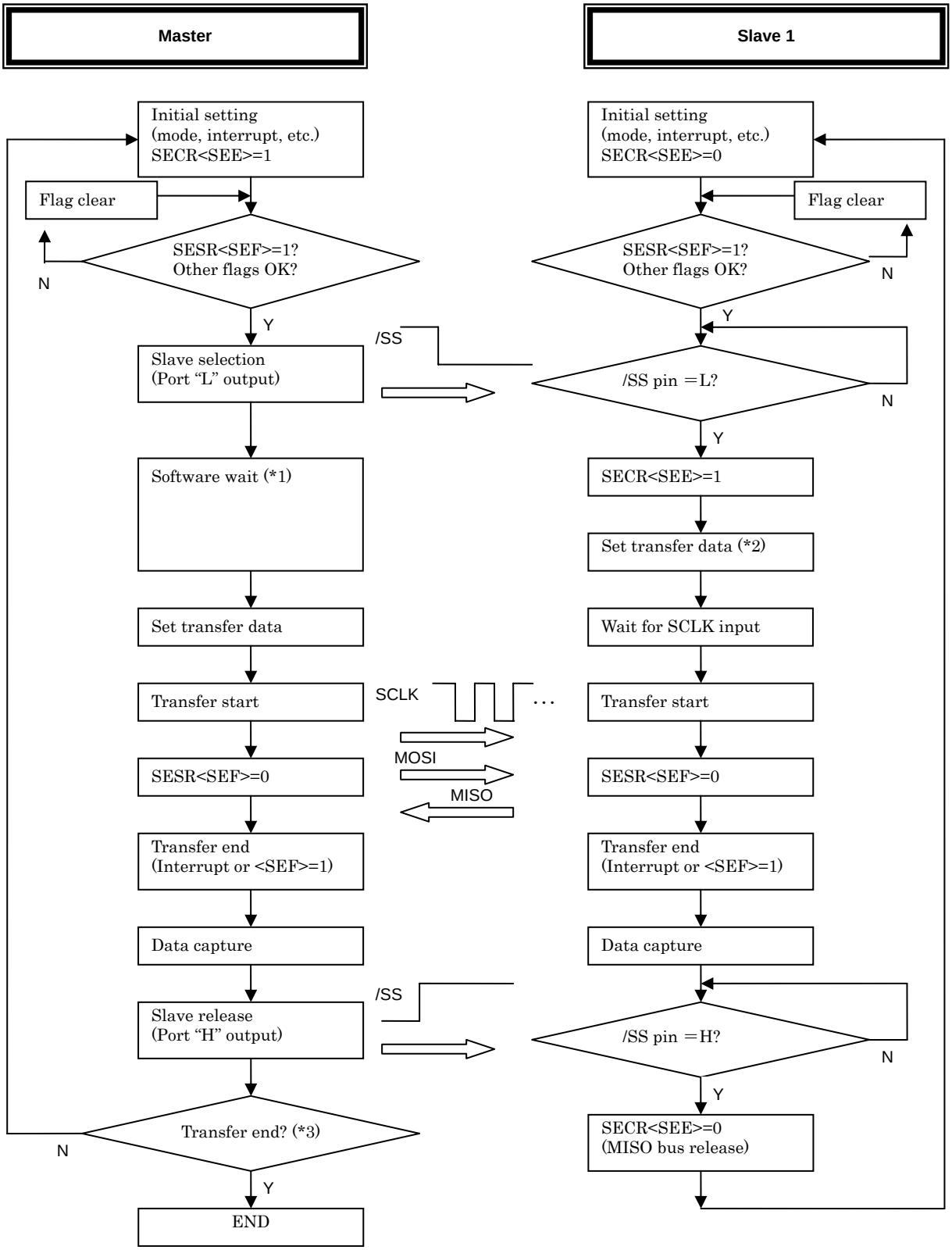
After the master device drives the /SS pin of the selected slave device low, a wait period must be inserted by software to allow the slave device to set up for communications with the master device.

The master device should start transferring data to the slave device by giving careful consideration to the setup time of the slave device.

If the master device wants to communicate with another slave device after completing an SEI transfer, a wait period must be inserted by software to allow the current active slave device to release the MISO bus. Careful consideration should be given to transfer intervals.

[Processing example for a system comprising one master and multiple slaves]

(SECR<CPHA>=1, <CPOL>=1, active slave = slave 1)



*1, The master device should insert a wait period by software. The master device should start transferring data by giving careful consideration to the setup time of the slave device.

*2, When the device is configured as a slave with SECR<CPHA>=0, transfer data must be set in the SEDR register while the /SS pin is high. We recommend setting SECR<CPHA>=1, in which case transfer data can be written regardless of the /SS pin state.

*3, If the master wants to communicate with another slave device, a wait period is required to allow the current active slave device to release the bus. Careful consideration should be given to transfer intervals.