

TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

SSM3K127TU

- Power Management Switch Applications
- High-Speed Switching Applications

- 1.8V drive
- Low ON-resistance: $R_{on} = 286 \text{ m}\Omega$ (max) (@ $V_{GS} = 1.8\text{V}$)
 : $R_{on} = 167 \text{ m}\Omega$ (max) (@ $V_{GS} = 2.5\text{V}$)
 : $R_{on} = 123 \text{ m}\Omega$ (max) (@ $V_{GS} = 4.0\text{V}$)

Absolute Maximum Ratings (Ta = 25°C)

| Characteristic | Symbol | Rating | Unit |
|---------------------------|----------------|------------|------|
| Drain-Source voltage | V_{DSS} | 30 | V |
| Gate-Source voltage | V_{GSS} | ± 12 | V |
| Drain current | DC | I_D | 2.0 |
| | Pulse | I_{DP} | 4.0 |
| Drain power dissipation | P_D (Note 1) | 800 | mW |
| | P_D (Note 2) | 500 | |
| Channel temperature | T_{ch} | 150 | °C |
| Storage temperature range | T_{stg} | -55 to 150 | °C |

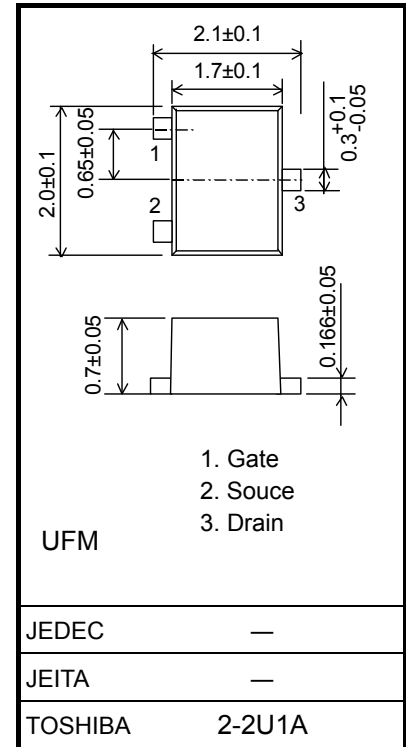
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on a ceramic board.
 (25.4 mm × 25.4 mm × 0.8 t, Cu Pad: 645 mm²)

Note 2: Mounted on an FR4 board.
 (25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm²)

Unit: mm



Weight: 6.6mg (typ.)

Start of commercial production
 2007-04

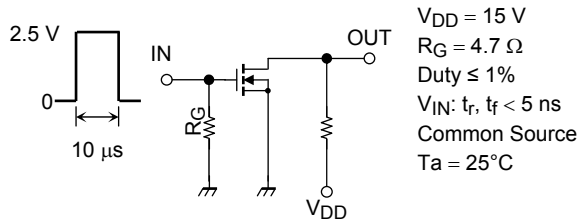
Electrical Characteristics (Ta = 25°C)

| Characteristic | Symbol | Test Conditions | Min | Typ. | Max | Unit | |
|--------------------------------|---------------|--|---|-------|---------|---------------|----|
| Drain-Source breakdown voltage | $V_{(BR)DSS}$ | $I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$ | 30 | — | — | V | |
| | $V_{(BR)DSX}$ | $I_D = 1 \text{ mA}, V_{GS} = -12 \text{ V}$ | 18 | — | — | | |
| Drain cut-off current | I_{DSS} | $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$ | — | — | 1 | μA | |
| Gate leakage current | I_{GSS} | $V_{GS} = \pm 12 \text{ V}, V_{DS} = 0 \text{ V}$ | — | — | ± 1 | μA | |
| Gate threshold voltage | V_{th} | $V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$ | 0.4 | — | 1.0 | V | |
| Forward transfer admittance | $ Y_{fs} $ | $V_{DS} = 3 \text{ V}, I_D = 1.0 \text{ A}$ (Note3) | 2.1 | 4.2 | — | S | |
| Drain-source ON-resistance | $R_{DS(ON)}$ | $I_D = 1.0 \text{ A}, V_{GS} = 4.0 \text{ V}$ (Note3) | — | 93 | 123 | m Ω | |
| | | $I_D = 0.8 \text{ A}, V_{GS} = 2.5 \text{ V}$ (Note3) | — | 115 | 167 | | |
| | | $I_D = 0.5 \text{ A}, V_{GS} = 1.8 \text{ V}$ (Note3) | — | 155 | 286 | | |
| Input capacitance | C_{iss} | $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ | — | 123 | — | pF | |
| Output capacitance | C_{oss} | | — | 43 | — | | |
| Reverse transfer capacitance | C_{rss} | | — | 18 | — | | |
| Total Gate Charge | Q_g | $V_{DS} = 15 \text{ V}, I_D = 2.0 \text{ A}, V_{GS} = 4 \text{ V}$ | — | 1.5 | — | nC | |
| Gate-Source Charge | Q_{gs} | | — | 0.9 | — | | |
| Gate-Drain Charge | Q_{gd} | | — | 0.6 | — | | |
| Switching time | Turn-on time | t_{on} | $V_{DD} = 15 \text{ V}, I_D = 1.0 \text{ A},$ $V_{GS} = 0 \text{ to } 2.5 \text{ V}, R_G = 4.7 \Omega$ | — | 9.2 | — | ns |
| | Turn-off time | t_{off} | | — | 6.4 | — | |
| Drain-Source forward voltage | V_{DSF} | $I_D = -2.0 \text{ A}, V_{GS} = 0 \text{ V}$ (Note3) | — | -0.82 | -1.2 | V | |

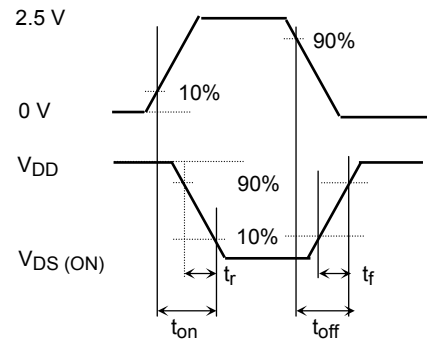
Note 3: Pulse test

Switching Time Test Circuit

(a) Test Circuit

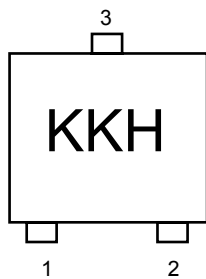


(b) V_{IN}

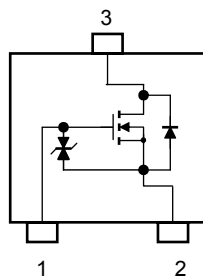


(c) V_{OUT}

Marking



Equivalent Circuit (top view)



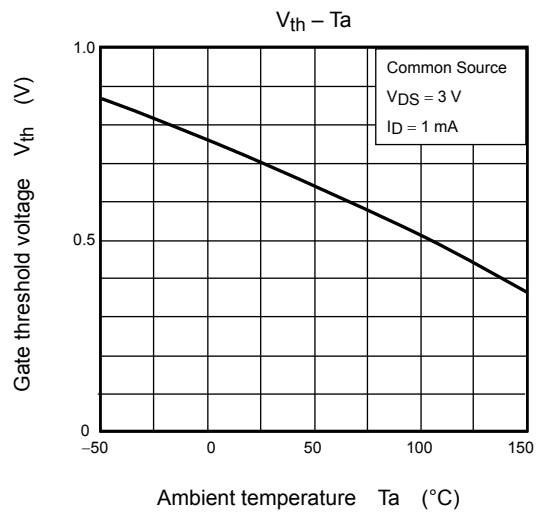
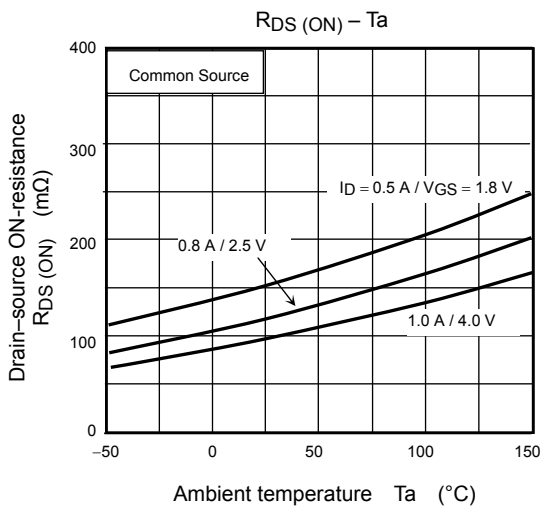
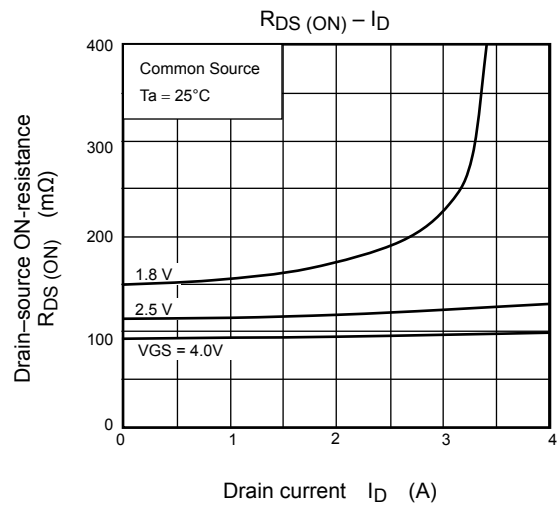
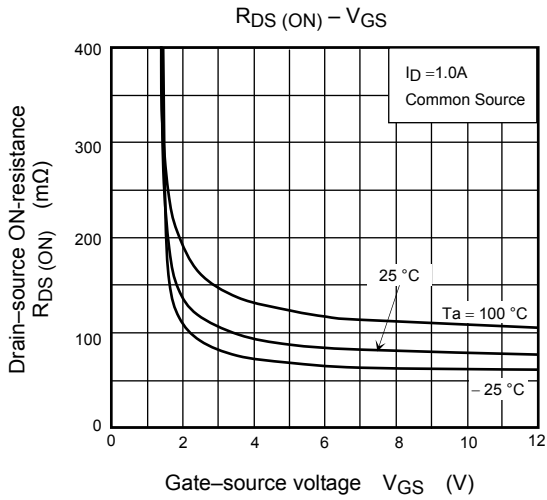
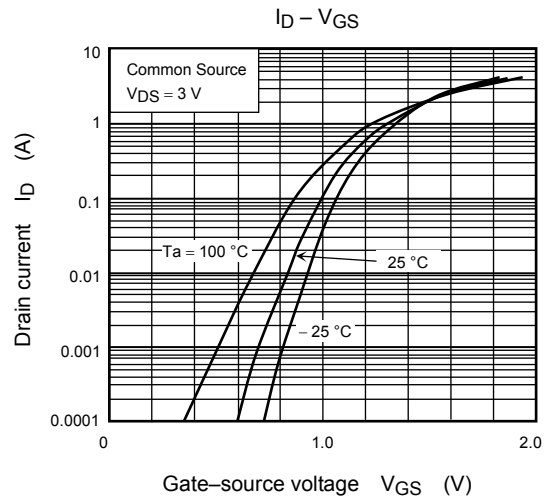
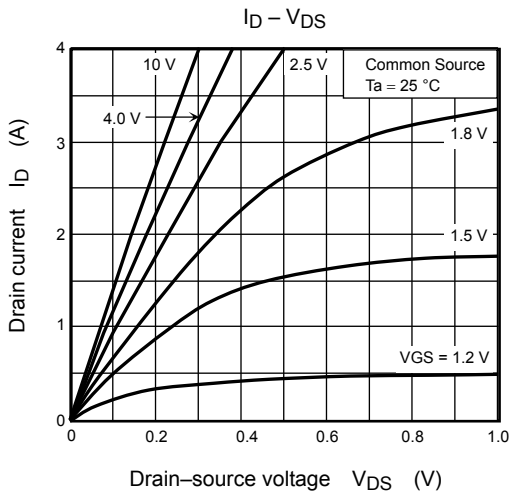
Usage Considerations

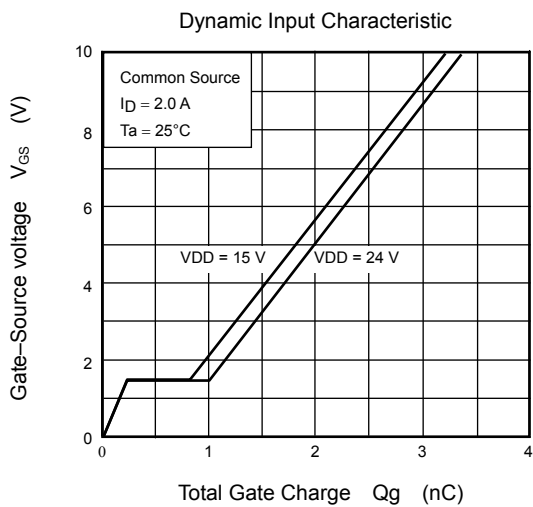
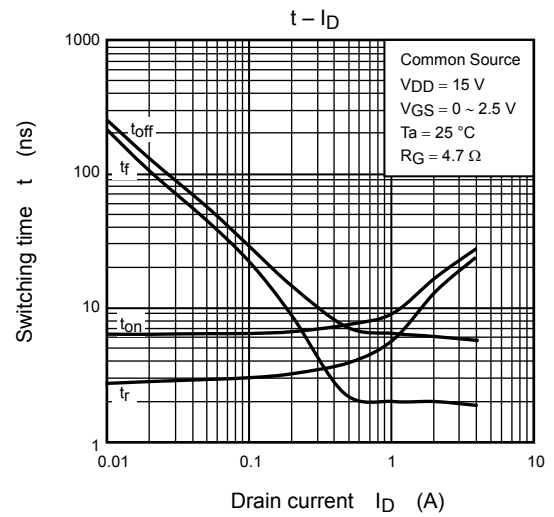
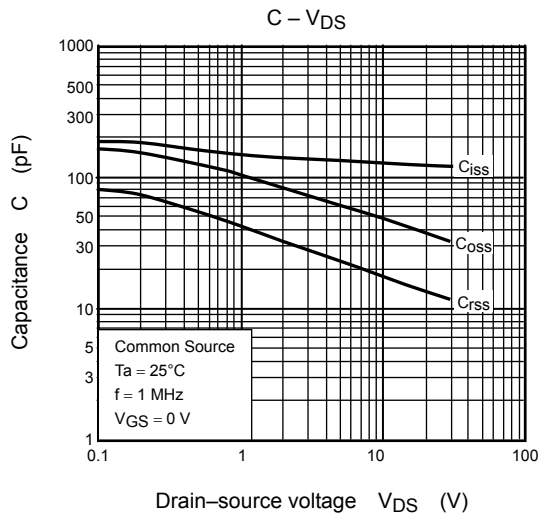
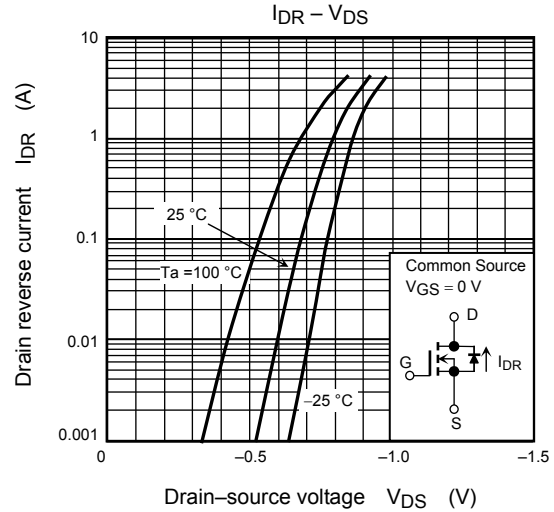
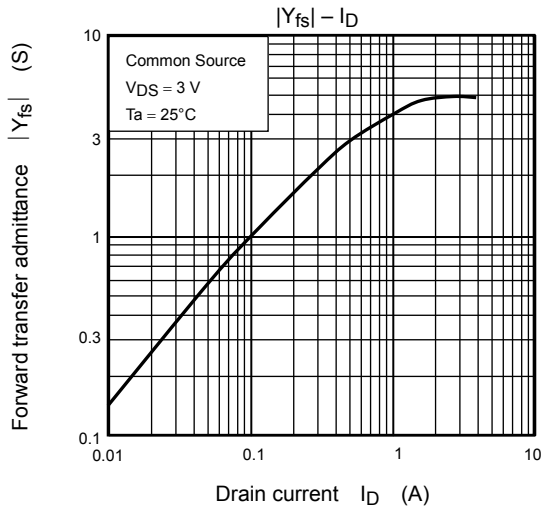
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be below (1 mA for the SSM3K127TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

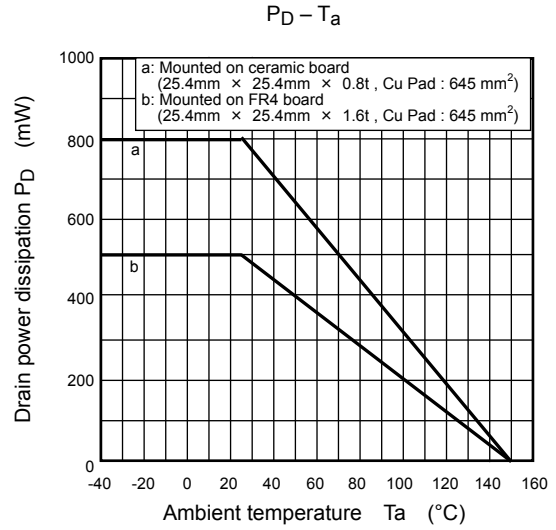
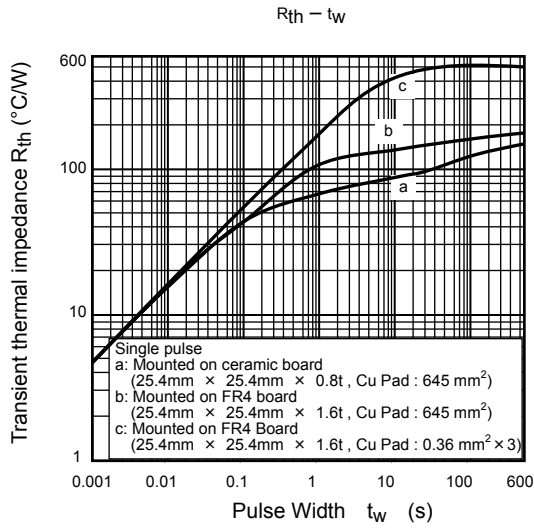
Take this into consideration when using the device.

Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.







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