

TOSHIBA Field-Effect Transistor Silicon N / P Channel MOS Type

# SSM6L40TU

- Power Management Switch Applications
- High-Speed Switching Applications

- N-ch: 4.0-V drive  
P-ch: 4.0 -V drive
- N-ch, P-ch, 2-in-1
- Low ON-resistance
  - Q1 N-ch:  $R_{on} = 182 \text{ m}\Omega$  (max) (@ $V_{GS} = 4 \text{ V}$ )  
 $R_{on} = 122 \text{ m}\Omega$  (max) (@ $V_{GS} = 10 \text{ V}$ )
  - Q2 P-ch:  $R_{on} = 403 \text{ m}\Omega$  (max) (@ $V_{GS} = -4 \text{ V}$ )  
 $R_{on} = 226 \text{ m}\Omega$  (max) (@ $V_{GS} = -10 \text{ V}$ )

### Q1 Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	30	V
Gate-source voltage		$V_{GSS}$	$\pm 20$	V
Drain current	DC	$I_D$	1.6	A
	Pulse	$I_{DP}$	3.2	

### Q2 Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	-30	V
Gate-source voltage		$V_{GSS}$	$\pm 20$	V
Drain current	DC	$I_D$	-1.4	A
	Pulse	$I_{DP}$	-2.8	

### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ ) (Q1, Q2 Common)

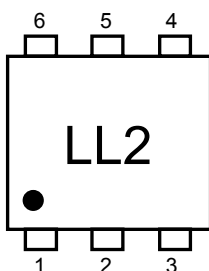
Characteristics	Symbol	Rating	Unit
Drain power dissipation	$P_D$ (Note 1)	500	mW
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

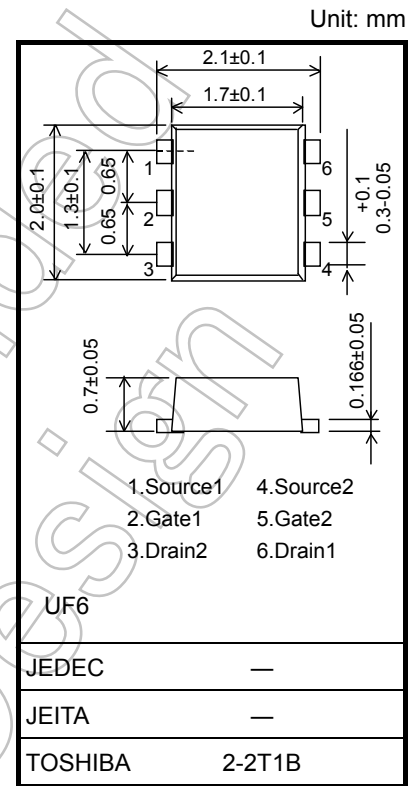
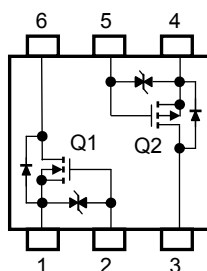
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Mounted on an FR4 board. (total dissipation)  
( $25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}$ , Cu Pad :  $645 \text{ mm}^2$ )

### Marking



### Equivalent Circuit (top view)



Weight: 7.0 mg (typ.)

Start of commercial production  
2008-02

## Q1 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	30	—	—	V
	$V_{(BR)DSX}$	$I_D = 1 \text{ mA}, V_{GS} = -20 \text{ V}$	15	—	—	
Drain cutoff current	$I_{DSS}$	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = 5 \text{ V}, I_D = 1 \text{ mA}$	1.0	—	2.6	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 5 \text{ V}, I_D = 1 \text{ A}$ (Note 2)	1.9	3.7	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = 1 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 2)	—	96	122	$\text{m}\Omega$
		$I_D = 0.5 \text{ A}, V_{GS} = 4 \text{ V}$ (Note 2)	—	130	182	
Input capacitance	$C_{iss}$	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	180	—	pF
Output capacitance	$C_{oss}$		—	34	—	
Reverse transfer capacitance	$C_{rss}$		—	27	—	
Total Gate Charge	$Q_g$	$V_{DS} = 15 \text{ V}, I_D = 1.6 \text{ A}, V_{GS} = 10 \text{ V}$	—	5.1	—	nC
Gate-Source Charge	$Q_{gs}$		—	3.9	—	
Gate-Drain Charge	$Q_{gd}$		—	1.2	—	
Switching time	Turn-on time	$t_{on}$	$V_{DD} = 15 \text{ V}, I_D = 0.5 \text{ A}$	—	9.5	ns
	Turn-off time	$t_{off}$	$V_{GS} = 0 \text{ to } 4 \text{ V}, R_G = 10 \Omega$	—	9.0	
Drain-source forward voltage	$V_{DSF}$	$I_D = -1.6 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 2)	—	-0.8	-1.2	V

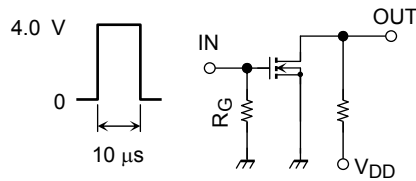
## Q2 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$	-30	—	—	V
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}, V_{GS} = +20 \text{ V}$	-15	—	—	
Drain cutoff current	$I_{DSS}$	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-10	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = -5 \text{ V}, I_D = -1 \text{ mA}$	-0.8	—	-2.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -5 \text{ V}, I_D = -1 \text{ A}$ (Note 2)	1.0	2.0	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -1.0 \text{ A}, V_{GS} = -10 \text{ V}$ (Note 2)	—	175	226	$\text{m}\Omega$
		$I_D = -0.5 \text{ A}, V_{GS} = -4.0 \text{ V}$ (Note 2)	—	290	403	
Input capacitance	$C_{iss}$	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	120	—	pF
Output capacitance	$C_{oss}$		—	32	—	
Reverse transfer capacitance	$C_{rss}$		—	21	—	
Total Gate Charge	$Q_g$	$V_{DS} = -15 \text{ V}, I_D = -1.4 \text{ A}, V_{GS} = -10 \text{ V}$	—	2.9	—	nC
Gate-Source Charge	$Q_{gs}$		—	2.2	—	
Gate-Drain Charge	$Q_{gd}$		—	0.7	—	
Switching time	Turn-on time	$t_{on}$	$V_{DD} = -15 \text{ V}, I_D = -1 \text{ A},$	—	12	ns
	Turn-off time	$t_{off}$	$V_{GS} = 0 \text{ to } -4 \text{ V}, R_G = 10 \Omega$	—	8.5	
Drain-source forward voltage	$V_{DSF}$	$I_D = 1.4 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 2)	—	0.87	1.2	V

Note 2: Pulse test

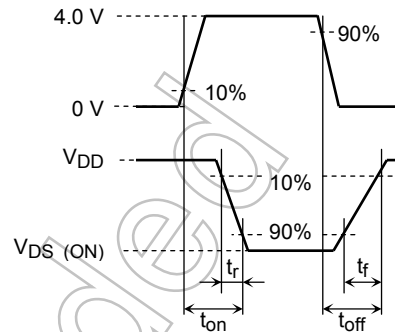
**Q1 Switching Time Test Circuit**

(a) Test Circuit

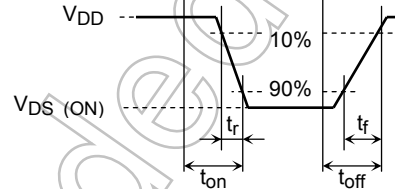


$V_{DD} = 15\text{ V}$   
 $R_G = 10\ \Omega$   
 Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5\text{ ns}$   
 Common Source  
 $T_a = 25^\circ\text{C}$

(b)  $V_{IN}$

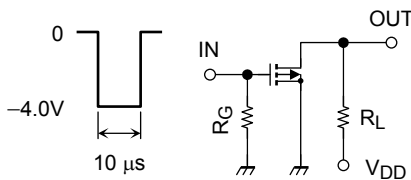


(c)  $V_{OUT}$



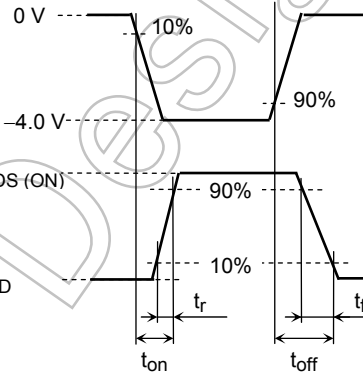
**Q2 Switching Time Test Circuit**

(a) Test Circuit

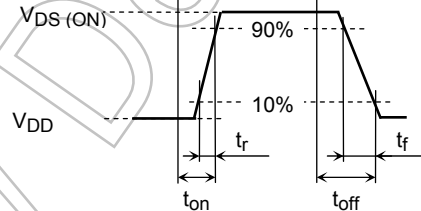


$V_{DD} = -15\text{ V}$   
 $R_G = 10\ \Omega$   
 Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5\text{ ns}$   
 Common Source  
 $T_a = 25^\circ\text{C}$

(b)  $V_{IN}$



(c)  $V_{OUT}$



**Q1 Usage Considerations**

Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be below (1 mA for the Q1 of the SSM6L40TU). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ .

Take this into consideration when using the device.

**Q2 Usage Considerations**

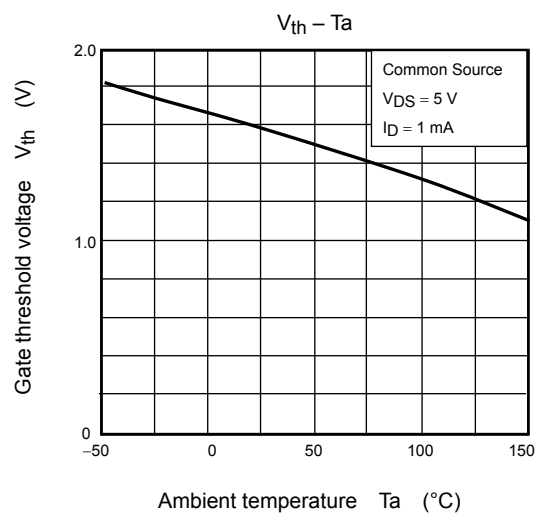
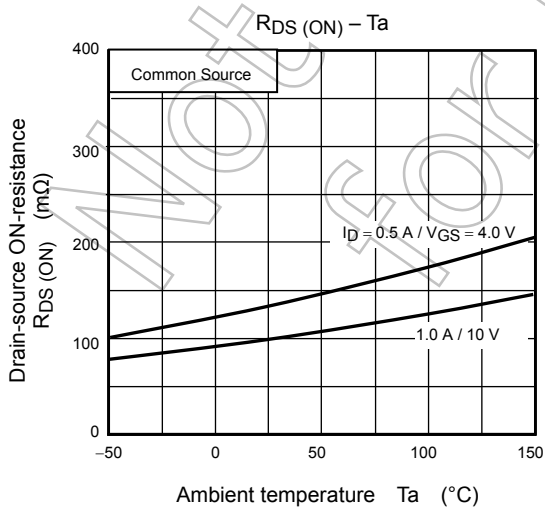
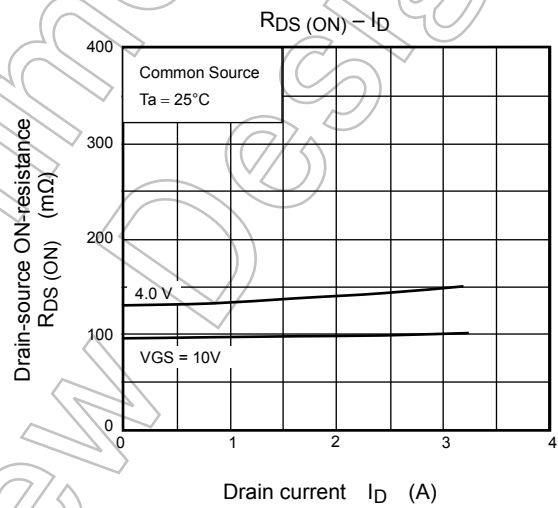
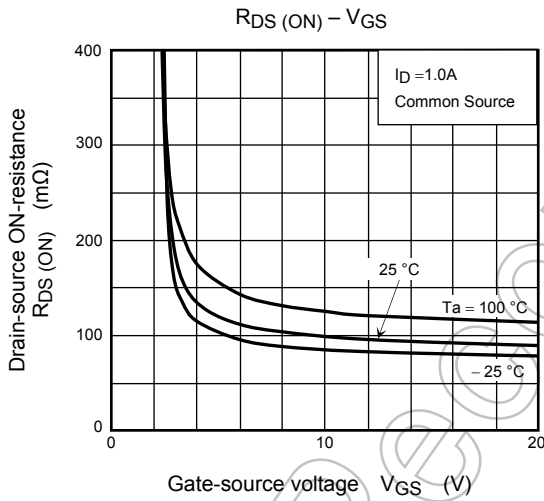
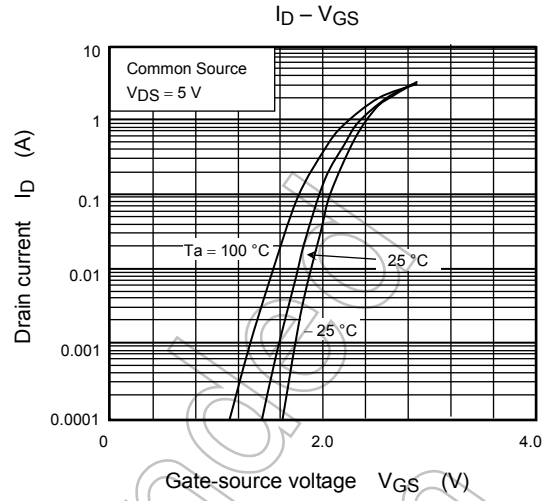
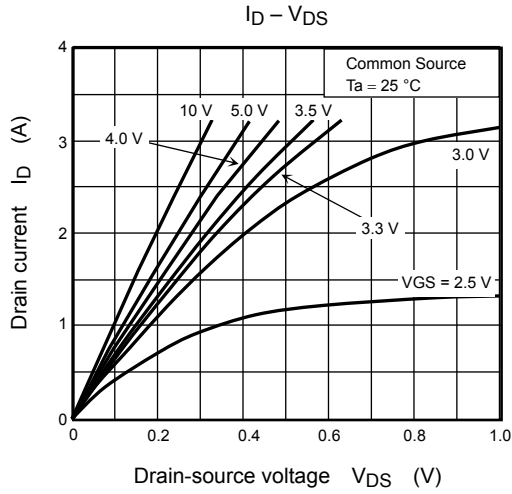
Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be below (-1 mA for the Q2 of the SSM6L40TU). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ .

Take this into consideration when using the device.

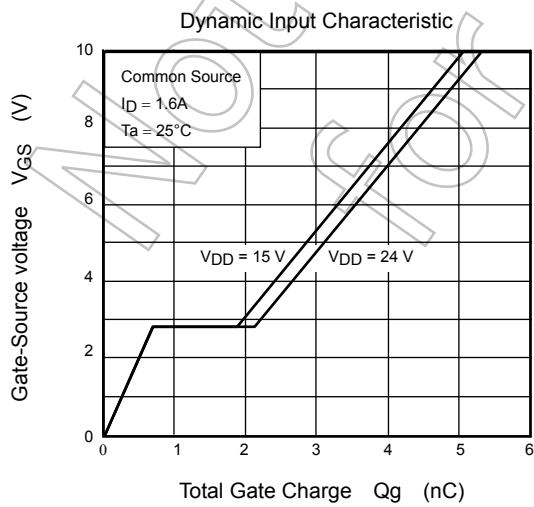
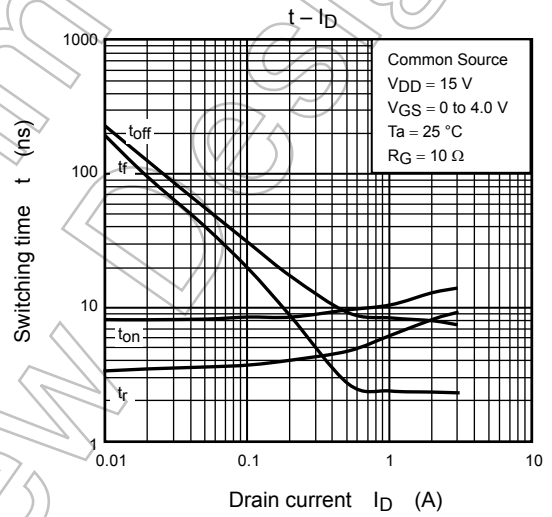
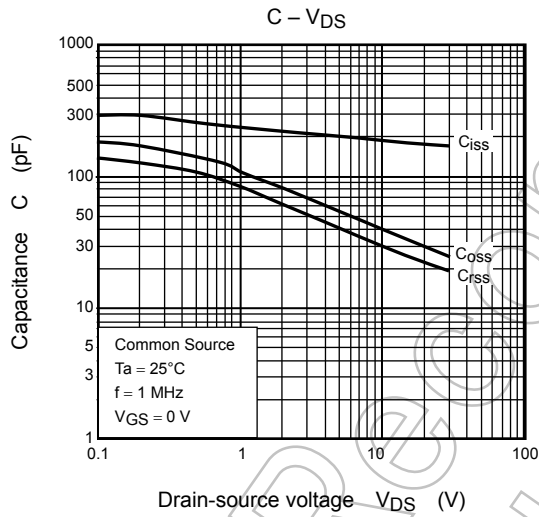
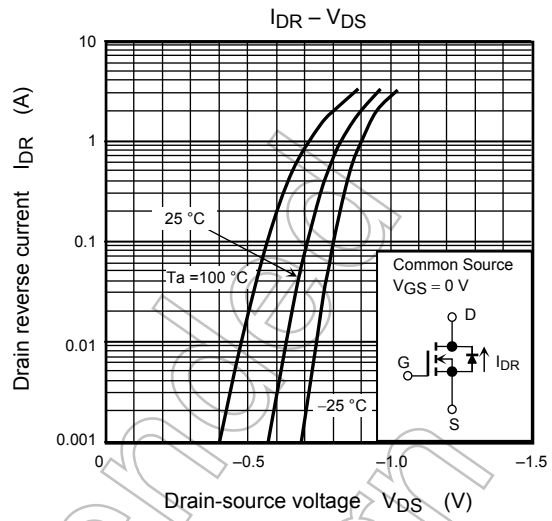
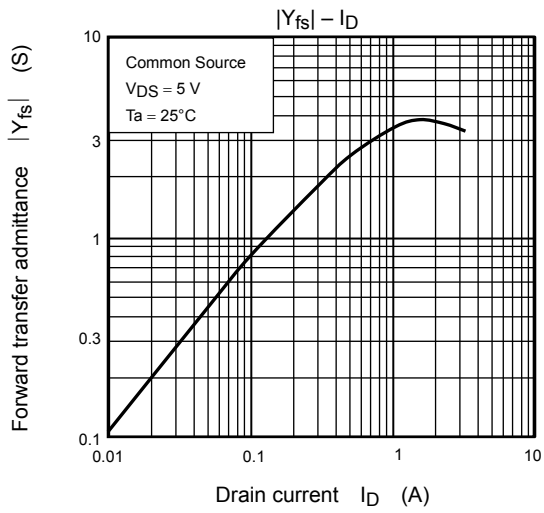
**Handling Precaution**

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

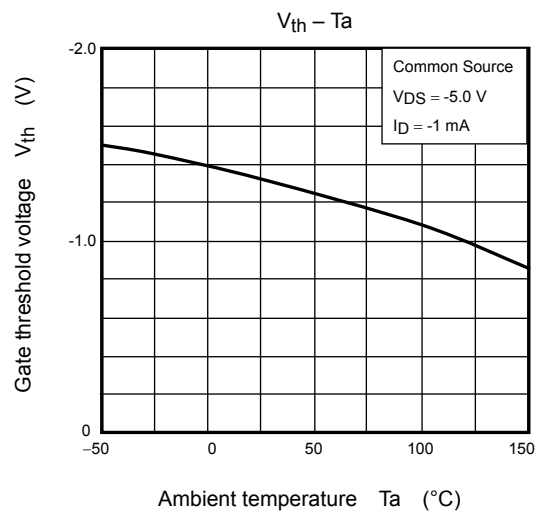
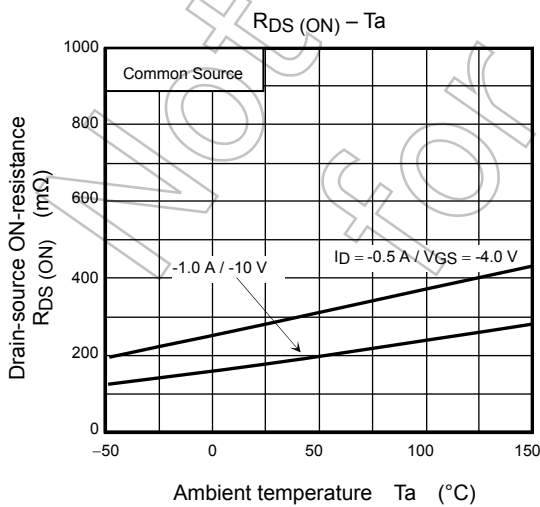
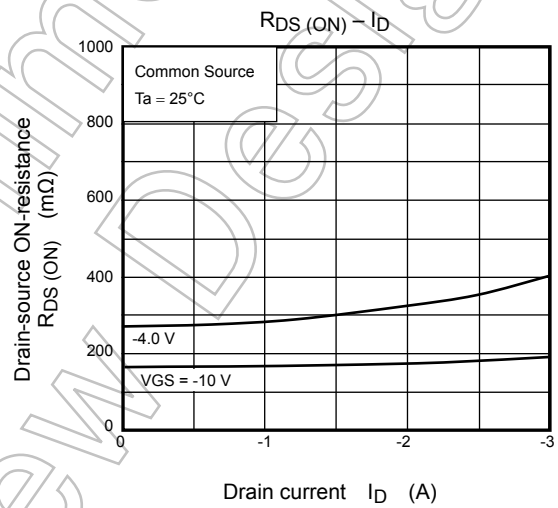
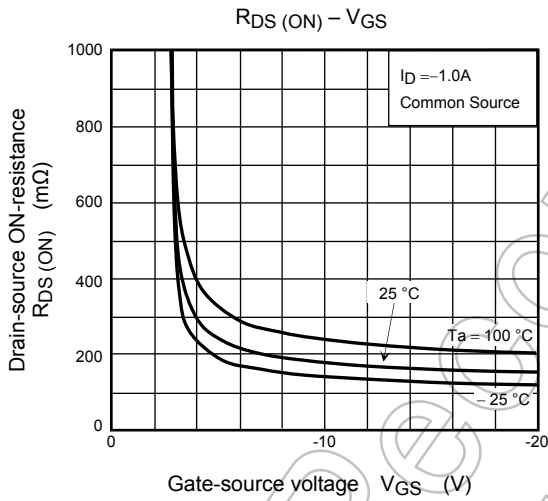
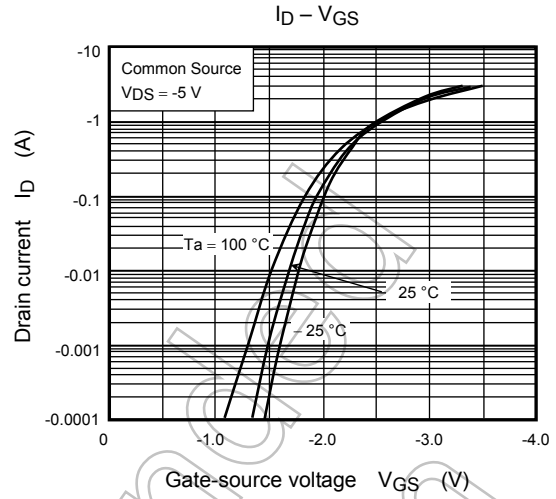
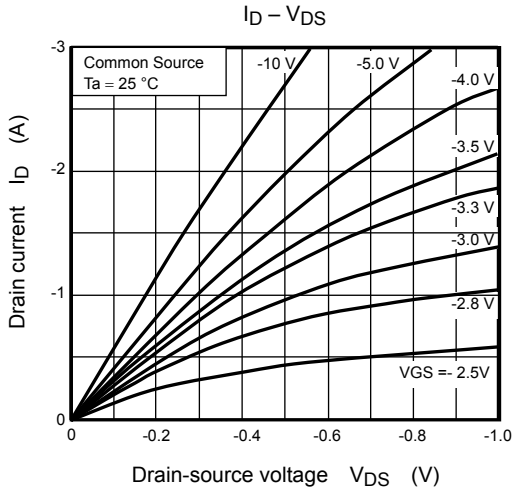
## Q1 (N-ch MOSFET)



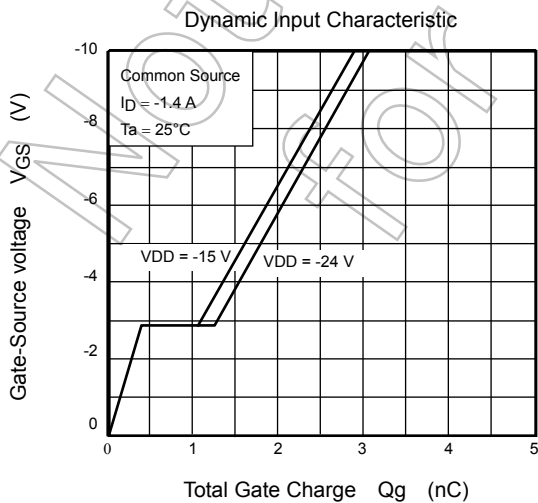
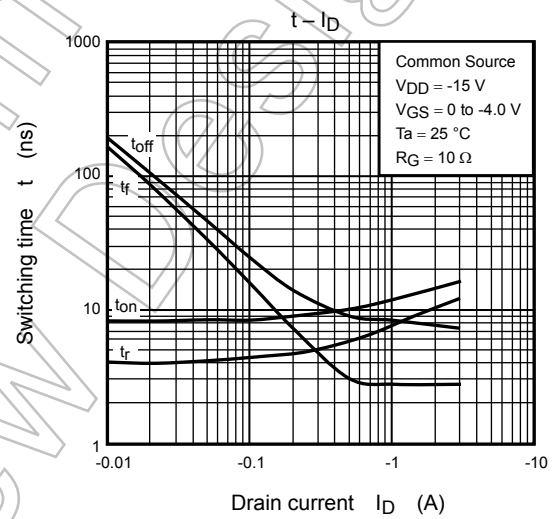
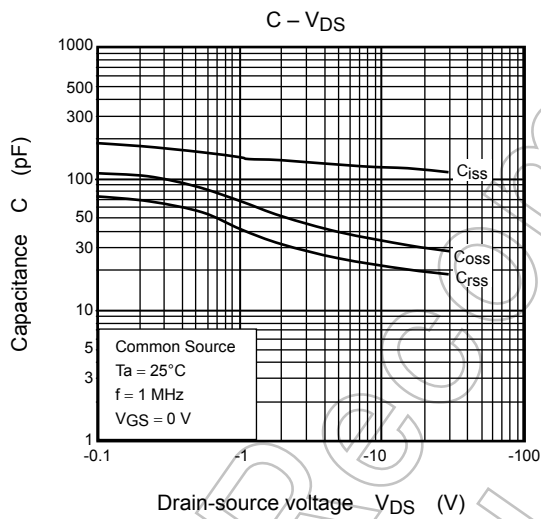
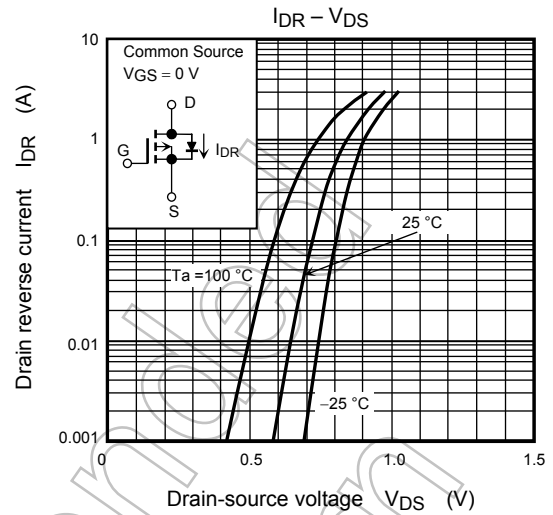
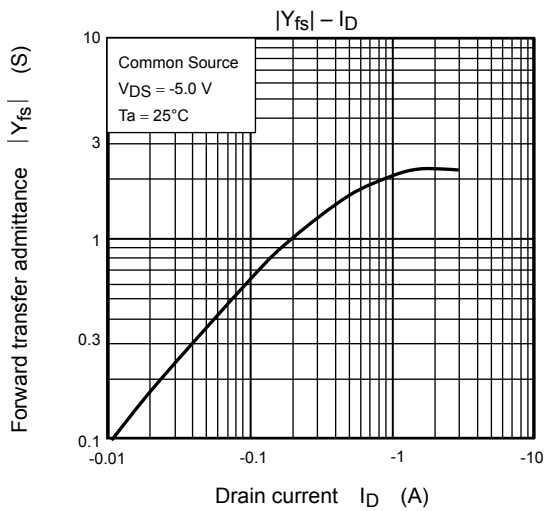
**Q1 (N-ch MOSFET)**



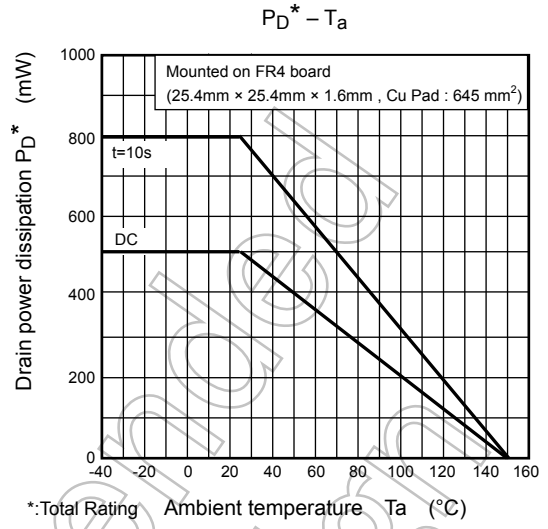
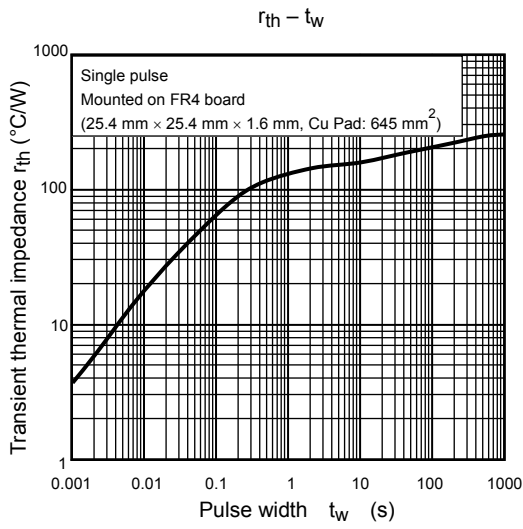
**Q2 (P-ch MOSFET)**



## Q2 (P-ch MOSFET)



Q1, Q2 Common



Not Recommended for New Design

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