TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870/C Series

TMP86PS25FG

TOSHIBA CORPORATION

Semiconductor Company

Revision History

Date	Revision	
2008/3/6	1	First Release
2008/8/29	2	Contents Revised

Caution in Setting the UART Noise Rejection Time

When UART is used, settings of RXDNC are limited depending on the transfer clock specified by BRG. The combination "O" is available but please do not select the combination "–".

The transfer clock generated by timer/counter interrupt is calculated by the following equation :

Transfer clock [Hz] = Timer/counter source clock [Hz] ÷ TTREG set value

BRG setting	Transfer clock [Hz]	RXDNC setting			
		00 (No noise rejection)	01 (Reject pulses shorter than 31/fc[s] as noise)	10 (Reject pulses shorter than 63/fc[s] as noise)	11 (Reject pulses shorter than 127/fc[s] as noise)
000	fc/13	O	O	O	–
110 (When the transfer clock generated by timer/counter interrupt is the same as the right side column)	fc/8	O	–	–	–
	fc/16	O	O	–	–
	fc/32	O	O	O	–
The setting except the above		O	O	O	O

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP86PS25F	P-QFP100-1420-0.65A	TMP86PS25FG	QFP100-P-1420-0.65A	–

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the “RESTRICTIONS ON PRODUCT USE” on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc.
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.).These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in his document shall be made at the customer’s own risk.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

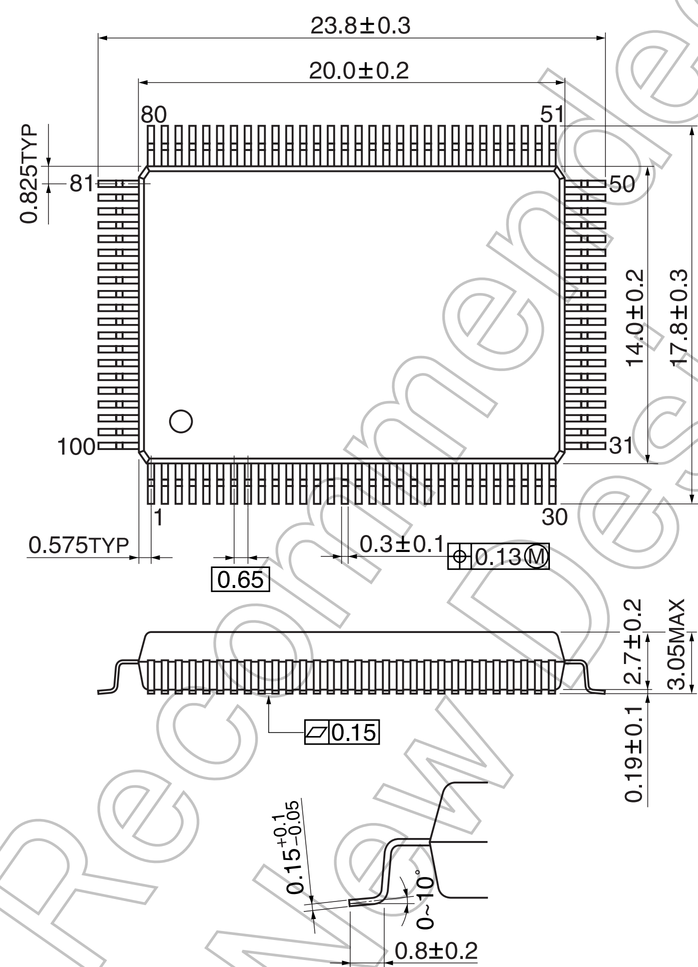
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

QFP100-P-1420-0.65A

Unit: mm



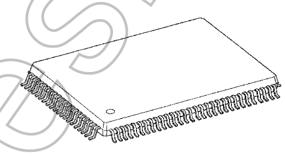
CMOS 8-Bit Microcontroller

TMP86PS25F

The TMP86PS25 is a OTP type MCU which includes 60-Kbyte one-time PROM. It is a pin compatible with a mask ROM product of the TMP86CM25/S25. Writing the program to built-in PROM, the TMP86PS25 operates as the same way as the TMP86CM25/S25. Using the Adapter socket, you can write and verify the data for the TMP86PS25 with a general-purpose PROM programmer same as TC571000D/AD.

Product No.	OTP	RAM	Package	Adapter Socket
TMP86PS25F	60 K × 8 bits	2 K × 8 bits	P-QFP100-1420-0.65A	BM11172

P-QFP100-1420-0.65A

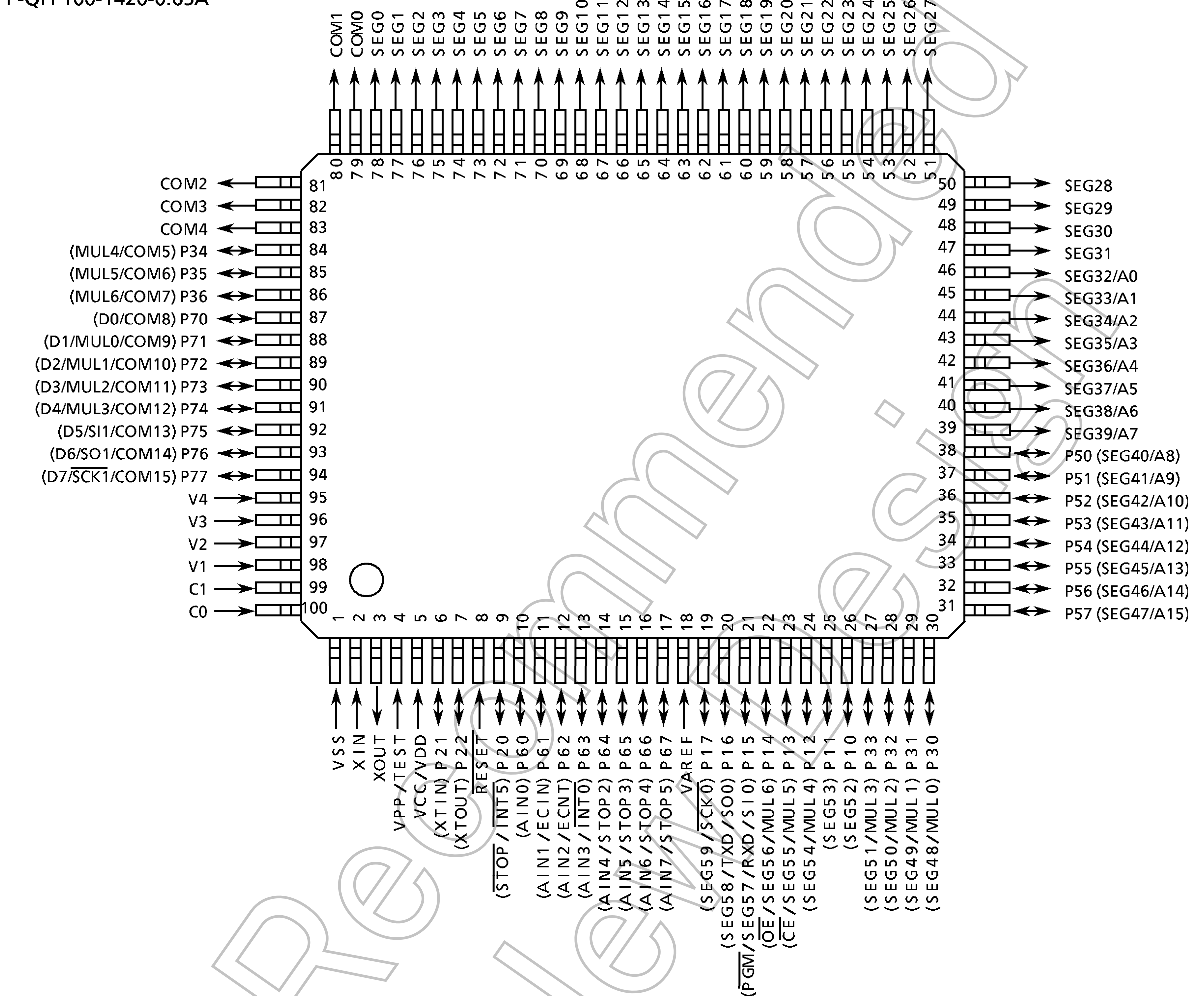


TMP86PS25F

000707EBP1

Pin Assignments (Top View)

P-QFP100-1420-0.65A



Note: Ports assigned as MUL6 to MUL0 can switch pin assignment by the multifunction register (MULSEL). For functions assigned to each pin, see the table below.

Pin name	Function	Pin assignment
MUL0	$\overline{DVO}$	P30 or P71
MUL1	$\overline{PWM3}$, $\overline{PDO3}$, TC3	P31 or P72
MUL2	$\overline{PPG4}$, $\overline{PWM4}$, $\overline{PDO4}$, TC4	P32 or P73
MUL3	$\overline{PPG6}$, $\overline{PWM6}$, $\overline{PDO6}$, TC6	P33 or P74
MUL4	INT1	P12 or P34
MUL5	INT2	P13 or P35
MUL6	INT3	P14 or P36

Pin Function

The TMP86PS25 has MCU mode and PROM mode.

(1) MCU mode

In the MCU mode, the TMP86PS25 is a pin compatible with the TMP86CM25/S25 (Make sure to fix the TEST pin to low level).

(2) PROM mode

Pin Name	Input/Output	Function	Pin Name (MCU mode)
A15 to A8	Input	Input of Memory address for program	P57 to P50
A7 to A0			SEG39 to SEG32
D7 to D0	I/O	Input/Output of Memory data for program	P77 to P70
$\overline{CE}$	Input	Chip enable	P13
$\overline{OE}$		Output enable	P14
$\overline{PGM}$		Program control	P15
VPP	Power supply	+ 12.75 V/5 V (Power supply of program)	TEST
VCC		+ 6.25 V/5 V	VDD
GND, VAREF		0 V	VSS, VAREF
P11, P21	I/O	PROM mode setting pin. Fix to high.	
P10, P22, P20, P61		PROM mode setting pin. Fix to low.	
$\overline{RESET}$			
P64, P65, P67	Output	Output pin for PROM operation test. Open or release.	
P17, P16, P12	I/O	Open	
P66, P63, P62, P60			
P36 to P30			
COM4 to COM0			
SEG31 to SEG0			
V4 to V1			
C1, C0			
XIN	Input	Self oscillation with resonator (8 MHz).	
XOUT	Output		

Note: No pin is applied to A16 input.

Operation

This section describes the functions and basic operational blocks of TMP86PS25.
The TMP86PS25 has PROM in place of the mask ROM which is included in the TMP86CM25/S25. The configuration and function are the same as the TMP86CM25/S25. For the functions of TMP86PS25 in details, see the section of TMP86CM25/S25.
In addition, TMP86PS25 operates as the single clock mode when releasing reset.
When using the dual clock mode, oscillate a low-frequency clock by SET. XTEN command at the beginning of program.

1. Operating Mode

The TMP86PS25 has MCU mode and PROM mode.

1.1 MCU Mode

The MCU mode is set by fixing the TEST/VPP pin to the low level.
In the MCU mode, the operation is the same as the TMP86CM25/S25 (TEST/VPP pin cannot be used open because it has no built-in pull-down resister).

1.1.1 Program Memory

The TMP86PS25 has a 60-Kbyte built-in one time PROM (addresses 1000H to FFFFH in the MCU mode, addresses 0000H to EFFFH in the PROM mode).
When using TMP86PS25 for evaluation of TMP86CM25/S25, the program is written in the program storing area shown in Figure 1-1.

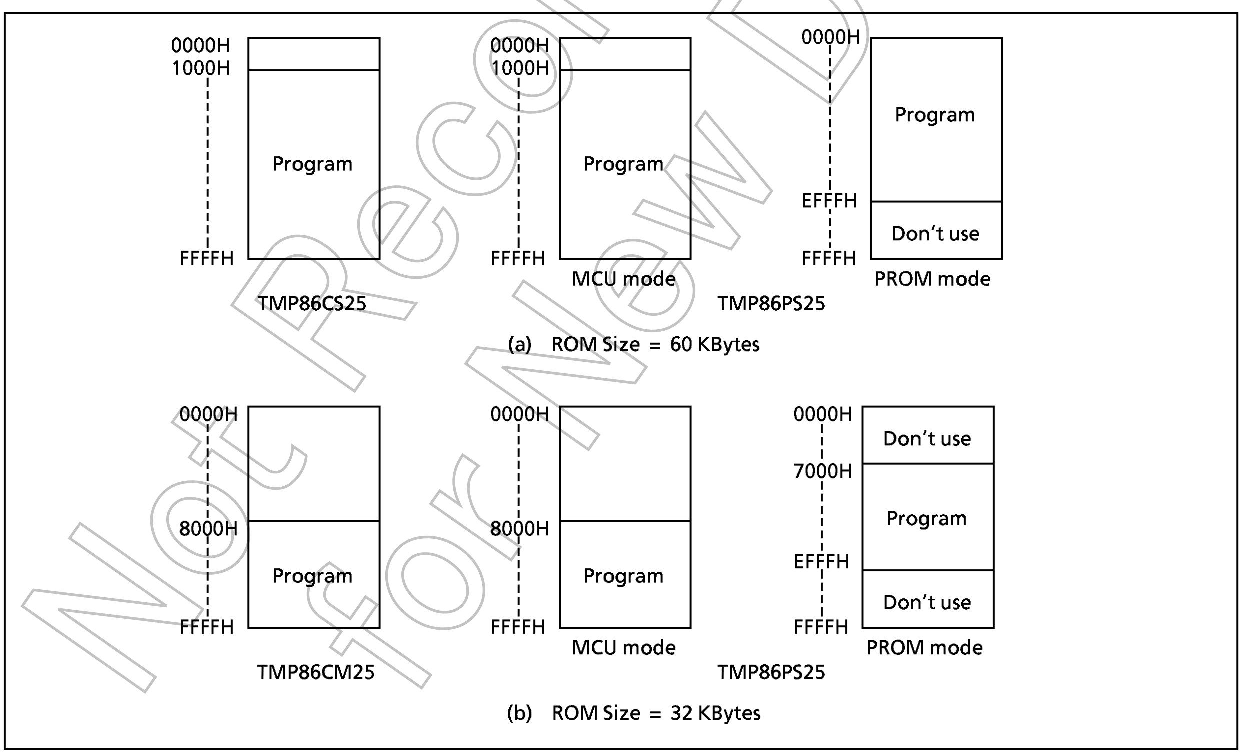


Figure 1-1. Program Memory Area

Note: The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.

1.1.2 Data Memory

TMP86PS25 has a built-in 2 Kbytes Data memory (Static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the TMP86PS25 are the same as those of the TMP86CM25/S25 except that the TEST pin does not have a built-in pull-down resister.

(2) I/O ports

The I/O circuitries of TMP86PS25 I/O ports are the same as the those of TMP86CM25/S25.

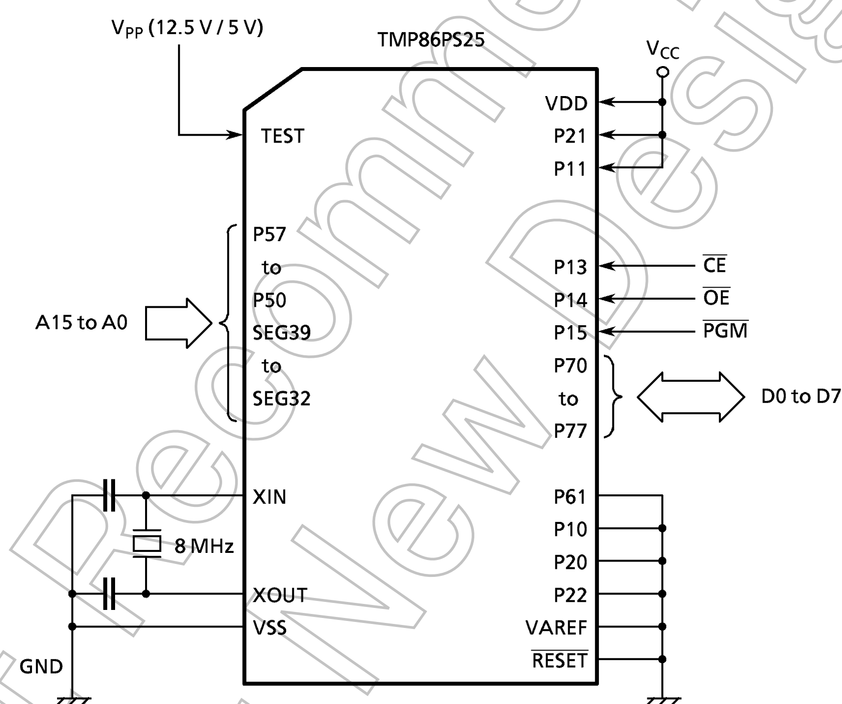
1.2 PROM Mode

The PROM mode is set by setting the $\overline{\text{RESET}}$ pin, the ports P11 to P10, P22 to P20, P61 and $\overline{\text{TEST}}$ as shown in Figure 1-2. The programming and verification for the internal PROM is achieved by using a general-purpose PROM programmer with the adapter socket.

> *Note: The high-speed program mode can be used. The setting is different according to the type of PROM programmer to use, refer to each description of PROM programmer.*
> *The TMP86PS25 does not support the electric signature mode, apply the ROM type of PROM programmer to TC571000D/AD.*

Always set the switch of Adapter socket to the N side when using TOSHIBA's Adapter socket.

EPROM Adapter socket (TC571000 · 1MbitEPROM)



PROM programmer connection adaptor sockets
BM11172 for TMP86PS25F

Inside pin name for TMP86PS25
Outside pin name for EPROM.

No pin is applied to A16 pin of TC571000 (open).

Figure 1-2. PROM Mode Setting

1.2.1 Programming Flowchart (High-speed Program Writing)

The high-speed programming mode is set by applying 12.75 V (programming voltage) to the V_{PP} pin when the V_{CC} is 6.25 V. After the address and data are fixed, the data in the address is written by applying 0.1ms of low level program pulse to $\overline{PGM}$ pin. Then verify if the data is written.
If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{PGM}$ pin.
This programming procedure is repeated until correct data is read from the address (maximum of 25 times).
Subsequently, all data are programmed in all addresses.
When all data were written, verify all address under the condition of $V_{CC} = V_{PP} = 5$ V.

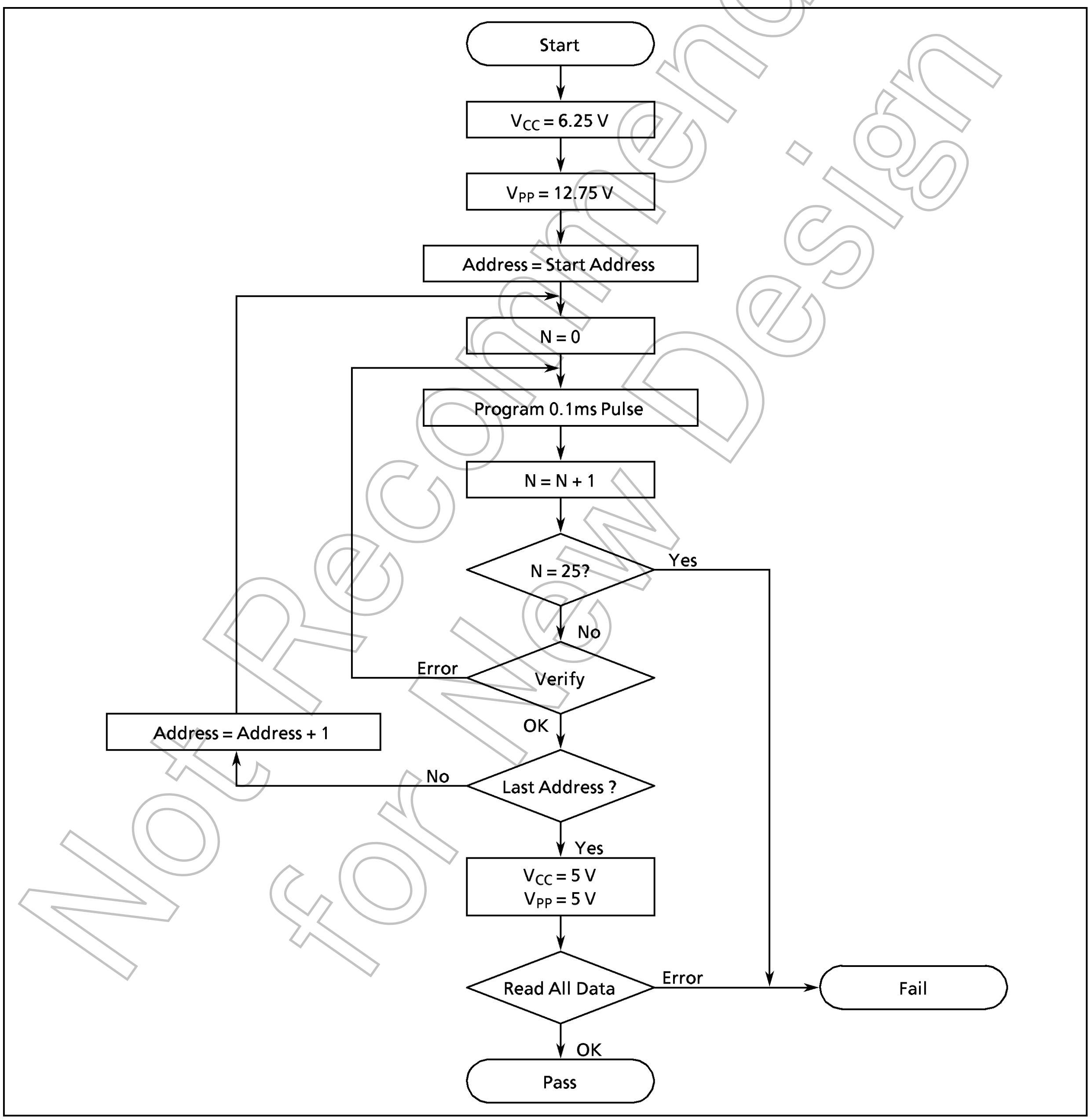


Figure 1-3. Programming Flowchart

1.2.2 Program Writing using a General-purpose PROM Programmer

(1) Recommended OTP adapter

BM11172: for TMP86PS25F

(2) Setting of OTP adapter

Set the switch (SW1) to N side.

(3) Setting of PROM programmer

i) Set PROM type to TC571000D/AD.
VPP: 12.75 V (high-speed program writing)

ii) Data transmission (Note 1)

The PROM of TMP86PS25 is located on different addresses; it depends on operating modes: MCU mode and PROM mode. When you write the data of ROM for TMP86CM25/S25, the data should be transferred from the address for MCU mode to that for PROM mode before writing operation is executed. For the applicable program areas of MCU mode and PROM mode are different, refer to Figure 1-1 Program Memory Area.

Ex. In the block transfer (copy) mode, executed as below.
ROM capacity of 60 KB: Transferred address 1000H to FFFFH to addresses 0000H to EFFFH
ROM capacity of 32 KB: Transferred address 8000H to FFFFH to addresses 7000H to EFFFH

iii) Setting of the program address (Note 1)

Start address: 0000H (When ROM capacity of 32 KB, start address is 7000H.)
End address: EFFFH

(4) Writing program

Write and verify according to the above mentioned "Setting of PROM programmer."

Note 1:	*For the setting method, refer to each description of PROM programmer. Make sure to set the data of address area that is not in used to FF_H.*
Note 2:	*When setting MCU to the adapter or when setting the adapter to the PROM programmer, set the first pin of the adapter and that of PROM programmer socket matched. If the first pin is conversely set, MCU or adapter or programmer would be damaged.*
Note 3:	*The TMP86PS25 does not support the electric signature mode. If PROM programmer uses the signature, the device would be damaged because of applying voltage of 12 ± 0.5 V to pin 9 (A9) of the address. Do not use the signature.*

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Program Voltage	V_{PP}	TEST/V_{PP}	– 0.3 to 13.0	
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT1}		– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P6 Port	– 1.8	mA
	I_{OUT2}	P1, P2, P34 to P36, P5, P6, P7 Port	3.2	
	I_{OUT3}	P30 to P33 Port	30	
Output Current (Total)	ΣI_{OUT2}	P1, P2, P34 to P36, P5, P6, P7 Port	60	
	ΣI_{OUT3}	P30 to P33 Port	80	
Power Dissipation [T_{opr} = 85°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 μ)	°C
Storage Temperature	Tstg		– 55 to 125	
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz	NORMAL1, 2 mode	2.7		
				IDLE0, 1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	1.8		
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW1, 2 mode			
				SLEEP0, 1, 2 mode			
				STOP mode			
Input high Level	V_{IH1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input low Level	V_{IL1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
LCD reference voltage range	$V1_{IN}$	V1	LCDCTL1<REFV> = "1" VDD< V4 (Note 2)		1.0	1.375	
	$V2_{IN}$	V2			2.0	2.750	
	$V3_{IN}$	V3			3.0	4.125	
	$V4_{IN}$	V4			4.0	5.500	
	$V4_{IN}$	V4 (Note 3)	LCDCTL1<REFV> = "0"		–	VDD	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 1.8 to 5.5 V		1.0	4.2	MHz
			V_{DD} = 2.7 to 5.5 V			8.0	
			V_{DD} = 4.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: When LCDCTL1<REFV> is set to "1", always keep the condition of V_{DD} < V4.

Note 3: When LCDCTL1<REFV> is set to "0", always supply the reference voltage from V4 pin.

DC Characteristics (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-state					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN2}	$\overline{RESET}$ Pull-Up		100	220	450	kΩ
Output Leakage Current	I_{LO}	Sink Open Drain, Tri-state	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	μA
Output High Voltage	V_{OH2}	Tri-st Port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT P30 to P33 Port	V_{DD} = 4.5 V, I_{OL} = 1.6mA	–	–	0.4	
Output Low Current	I_{OL}	High Current Port (P30 to P33 Port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply Current in NORMAL 1, 2 mode	V_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3/0.2 V fc = 16 MHz fs = 32.768 kHz	–	6.2	9.0	
Supply Current in IDLE 0, 1, 2 mode				–	3.7	6.5	
Supply Current in SLOW 1 mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz LCD driver is not enable.	–	10	25	μA
Supply Current in SLEEP 1 mode				–	4.5	15	
Supply Current in SLEEP 0 mode				–	3.5	13	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V
Note 2: Input current (I_{IN1}, I_{IN2}); The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.
Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.

AD Conversion Characteristics

(V_{SS} = 0.0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}		3.0	–	–	V
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = V_{AREF} = 5.5 V, V_{SS} = 0.0 V	–	0.6	1.0	mA
Non linearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V, V_{AREF} = 5.0 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

(V_{SS} = 0.0 V, 2.7 V ≦ V_{DD} < 4.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}		2.5	–	–	V
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = V_{AREF} = 4.5 V, V_{SS} = 0.0 V	–	0.5	0.8	mA
Non linearity Error		V_{DD} = 2.7 V, V_{SS} = 0.0 V, V_{AREF} = 2.7 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

(V_{SS} = 0.0 V, 2.0 V ≦ V_{DD} <2.7 V, Topr = – 40 to 85°C) Note 5
(V_{SS} = 0.0 V, 1.8 V ≦ V_{DD} <2.0 V, Topr = – 10 to 85°C) Note 5

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 0.9	–	V_{DD}	V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}	1.8 V ≦ V_{DD} <2.0 V	1.8	–	–	V
		2.0 V ≦ V_{DD} <2.7 V	2.0	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = V_{AREF} = 2.7 V, V_{SS} = 0.0 V	–	0.3	0.5	mA
Non linearity Error		V_{DD} = 1.8 V, V_{SS} = 0.0 V, V_{AREF} = 1.8 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

Note 1: The total error includes all errors except a quantization error, and is defined as maximum deviation from the ideal conversion line.
Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.11.2 Register Configuration".
Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
Note 4: Analog Reference Voltage Range: $\Delta V_{AREF} = V_{AREF} - V_{SS}$
Note 5: When AD is used with V_{DD} < 2.7 V, the guaranteed temperature range varies with the operating voltage.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.25	–	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twcL					

(V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.5	–	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twcL					

(V_{SS} = 0 V, V_{DD} = 1.8 to 2.7 V, Topr = – 40 to 85°C)

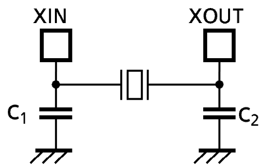
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.95	–	4	μs
		IDLE 0, 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 0, 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 4.2 MHz	–	119.05	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twcL					

Timer Counter 1 input (ECIN) Characteristics

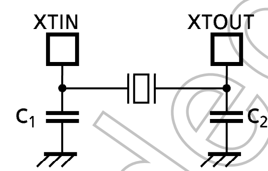
(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition		Min	Typ.	Max	Unit
TC1 input (ECIN input)	t_{TC1}	Frequency measurement mode V_{DD} = 4.5 to 5.5 V	Single edge count	–	–	1.0	MHz
		Frequency measurement mode V_{DD} = 2.7 to 4.5 V	Single edge count	–	–	0.5	
		Frequency measurement mode V_{DD} = 1.8 to 2.7 V	Single edge count	–	–	0.262	

Recommended Oscillating Conditions



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

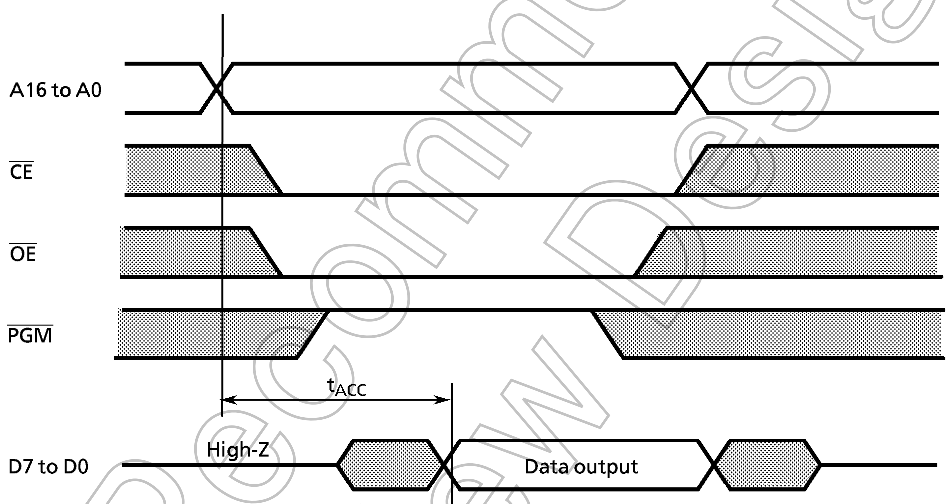
Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL: http://www.murata.co.jp/search/index.html

DC Characteristics, AC Characteristics (PROM Mode) (V_{SS} = 0 V, Topr = – 40 to 85°C)

(1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH4}		2.2	–	V_{CC}	V
Low leve input voltage (TTL)	V_{IL4}		0	–	0.8	
Power supply	V_{CC}		4.75	5.0	5.25	
Power supply of program	V_{PP}					
Address access time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	1.5tcyc + 300	–	ns

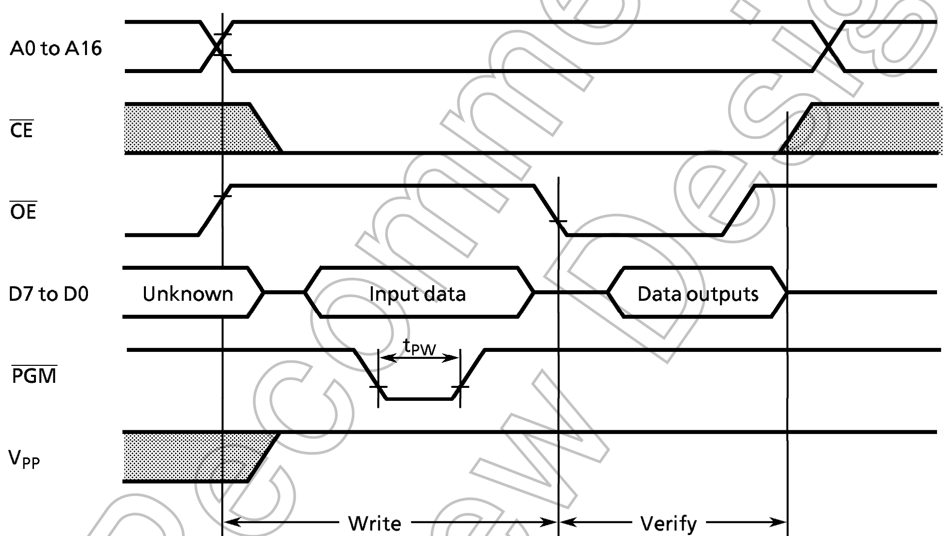
Note: tcyc = 500 ns at 8 MHz



(2) Program operation (High-speed) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH4}		2.2	–	V_{CC}	V
Low leve input voltage (TTL)	V_{IL4}		0	–	0.8	
Power supply	V_{CC}		6.0	6.25	6.5	
Power supply of program	V_{PP}		12.5	12.75	13.0	
Pulse width of initializing program	t_{PW}	V_{CC} = 6.0 V	0.095	0.1	0.105	ms

High-speed program writing



Note 1: The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.

Note2 : The pulling up/down device on the condition of V_{PP} = 12.75 V ± 0.25 V causes a damage for the device. Do not pull up/down at programming.

Note3 : Use the recommended adapter (see 1.2.2 (1)) and mode (see 1.2.2 (3) i). Using other than the above condition may cause the trouble of the writting.