TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870 Series

TMP87C408MG, TMP87C408NG
TMP87C808MG, TMP87C808NG
TMP87C408LMG, TMP87C408LNG
TMP87C808LMG, TMP87C808LNG
TMP87C408DMG

Not Recommended for New Design

TOSHIBA CORPORATION
Semiconductor Company

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

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1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87C408M	SOP28_P_450_1.27	TMP87C408MG	SOP28-P-450-1.27B	TMP87P808MG
TMP87C408N	SDIP28_P_400_1.78	TMP87C408NG	SDIP28-P-400-1.78	TMP87P808NG
TMP87C408DM	SSOP30_P_56_0.65	TMP87C408DMG	SSOP30-P-56-0.65	—
TMP87C808M	SOP28_P_450_1.27	TMP87C808MG	SOP28-P-450-1.27B	TMP87P808MG
TMP87C808N	SDIP28_P_400_1.78	TMP87C808NG	SDIP28-P-400-1.78	TMP87P808NG
TMP87C408LM	SOP28_P_450_1.27	TMP87C408LMG	SOP28-P-450-1.27B	TMP87P808LMG
TMP87C408LN	SDIP28_P_400_1.78	TMP87C408LNG	SDIP28-P-400-1.78	TMP87P808LNG
TMP87C808LM	SOP28_P_450_1.27	TMP87C808LMG	SOP28-P-450-1.27B	TMP87P808LMG
TMP87C808LN	SDIP28_P_400_1.78	TMP87C808LNG	SDIP28-P-400-1.78	TMP87P808LNG

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

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4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE

20070701-EN

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

The publication date of this datasheet is printed at the lower right corner of this notification.

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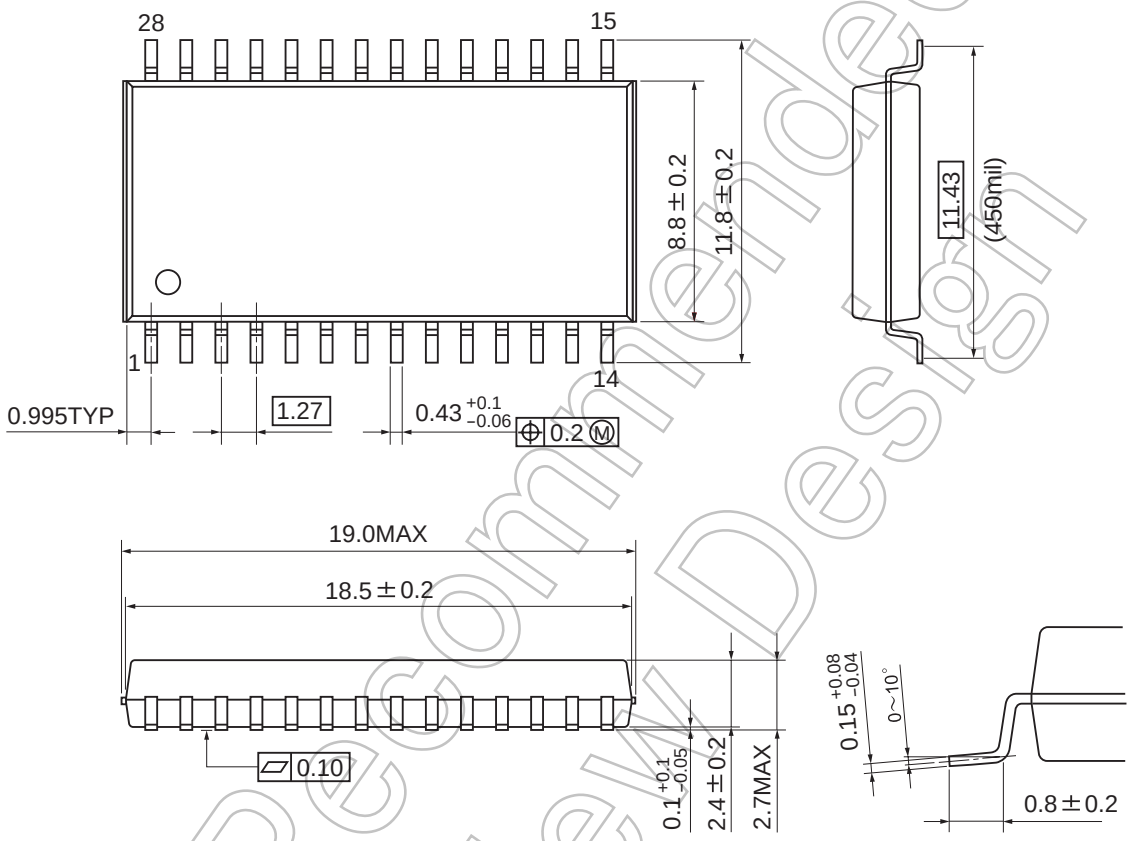
(Annex)

Package Dimensions

SOP28-P-450-1.27B

Unit: mm



Note: Palladium plated

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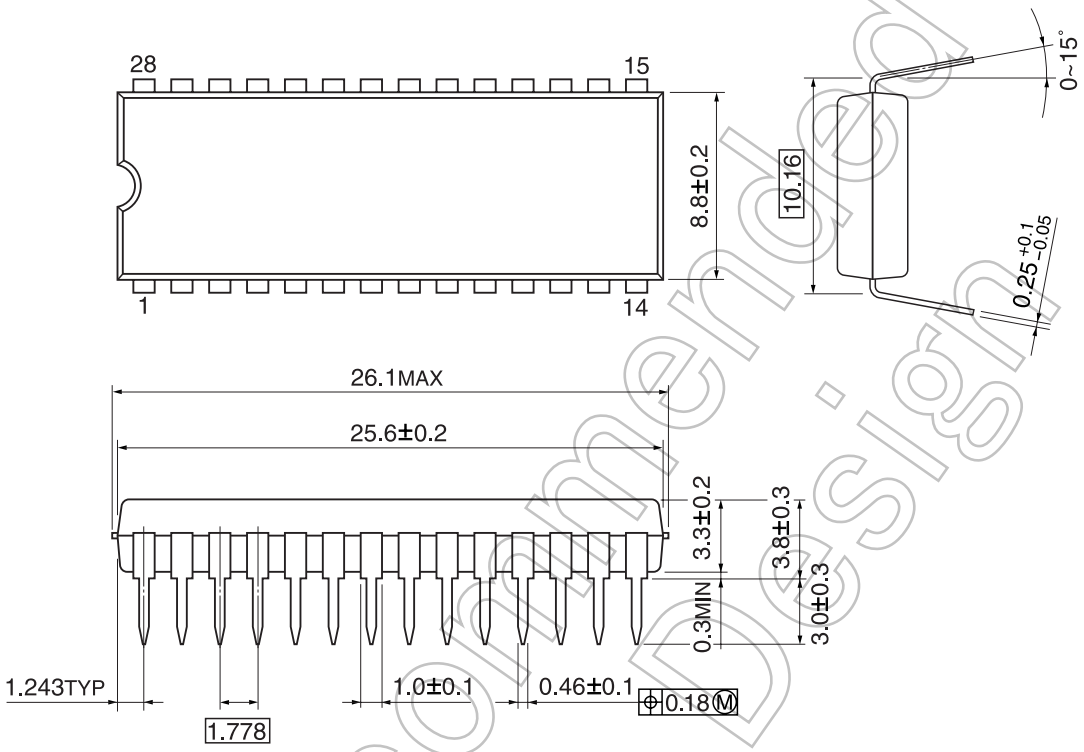
SDIP28-P-400-1.78

Unit: mm



Note: Palladium plated

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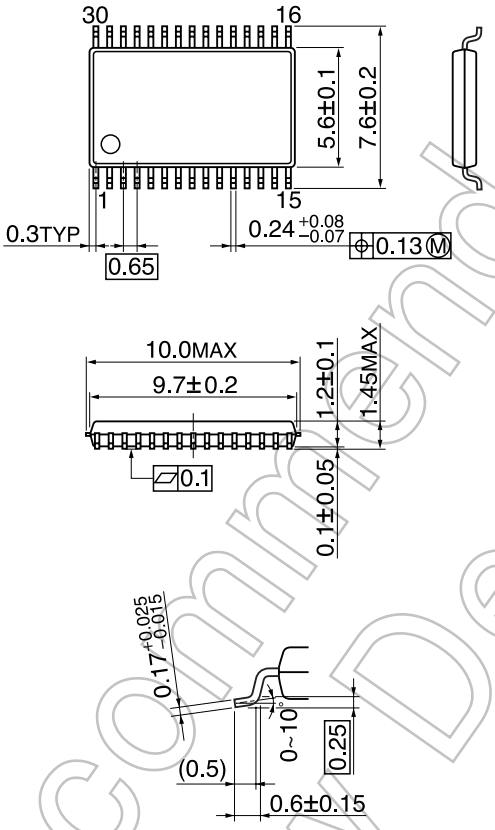
SSOP30-P-56-0.65

Unit: mm



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CMOS 8-Bit Microcontroller

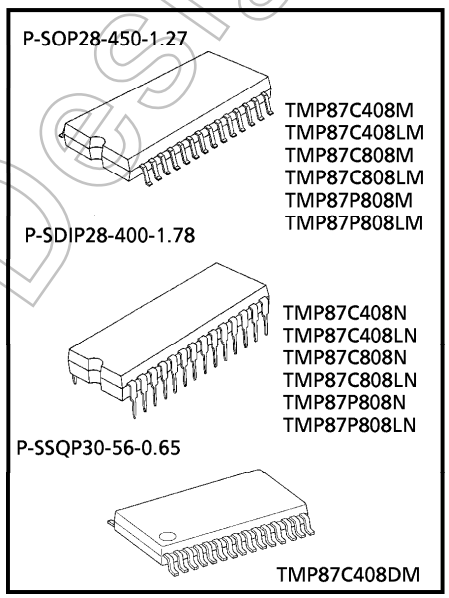
TMP87C408M, TMP87C408N, TMP87C808M, TMP87C808N TMP87C408LM, TMP87C408LN, TMP87C808LM, TMP87C808LN TMP87C408DM

TMP87C408/808/408L/808L is high speed and high performance 8-bit single chip microcomputers to operate on low voltage and low power consumption. This MCU contains ROM, RAM, input/output ports, multi-function timer/counter, a serial interface, and 8-bit A/D converter.

Part No.	ROM	RAM	Package	OTP MCU	Operation Voltage Range
TMP87C408M	4K × 8-bit	256 × 8-bit	P-SOP28-450-1.27	TMP87P808M	2.7 V to 5.5 V at 4.2 MHz 4.5 V to 5.5 V at 8 MHz
TMP87C408N			P-SDIP28-400-1.78	TMP87P808N	
TMP87C408DM			P-SSQP30-56-0.65		
TMP87C808M	8K × 8-bit		P-SOP28-450-1.27	TMP87P808M	
TMP87C808N			P-SDIP28-400-1.78	TMP87P808N	
TMP87C408LM	4K × 8-bit		P-SOP28-450-1.27	TMP87P808LM	1.8 V to 4.0 V at 4.2 MHz
TMP87C408LN			P-SDIP28-400-1.78	TMP87P808LN	
TMP87C808LM	8K × 8-bit		P-SOP28-450-1.27	TMP87P808LM	
TMP87C808LN			P-SDIP28-400-1.78	TMP87P808LN	

Features

- ◆ 8-bit single chip microcomputer TLCS-870 series
- ◆ Minimum instruction execution time: 0.5 μs (at 8 MHz) (TMP87C408/C808/P808)
  0.95 μs (at 4.2 MHz) (TMP87C408L/C808L/P808L)
- ◆ 129 types & 412 basic instructions
  - Multiplication (8 bits × 8 bits, 16 bits ÷ 8 bits)
    : Execution time 3.5 μs (at 8 MHz) (TMP87C408/C808/P808)
    7.0 μs (at 4 MHz) (TMP87C408L/C808L/P808L)
  - Bit manipulations
    (Set / Clear / Complement / Load / Store / Test / Exclusive or)
  - 16-bit data operations
  - 1-byte jump / call (Short relative jump / Vector call)



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- ◆ 10 interrupt sources (External: 4, Internal: 6)
  - All sources have independent latches each, and nested interrupt control is available.
  - Edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ◆ Input / Output ports (22 pins)
  - Middle current output: 6 pins (Typ.7 mA) (TMP87C408/C808/P808) (Typ. 6 mA) (TMP87C408L/C808L/P808L)
- ◆ Two 16-bit Timer/Counters
  - Timer, Eventcounter, Programmable pulse generator output, Pulse width measurement, External trigger timer, Window modes
- ◆ Time Base Timer
  - Interrupt frequency types: 8 types (1 to 16384 Hz)
- ◆ Divider output function (frequency: 4 types)
- ◆ Watchdog Timer
- ◆ One 8-bit Serial Interface
  - With 8 bytes transmit/receive data buffer
  - Internal / external serial clock, and 4/8-bit mode
- ◆ 8-bit Successive approximate type A/D converter with sample and hold
  - 6 analog inputs
  - Conversion time: 23 μs / 92 μs at 8 MHz programmable selectable (TMP87C408/C808/P808)
    46 μs / 184 μs at 4 MHz programmable selectable (TMP87C408L/C808L/P808L)
- ◆ Two Power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up
    Port output hold/high-impedance
  - IDLE mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- ◆ Operating voltage : 2.7 to 5.5 V at 4.2 MHz/4.5 to 5.5 V at 8 MHz (TMP87C408/C808/P808)
  1.8 to 4.0 V at 4.2 MHz (TMP87C408L/C808L/P808L)
- ◆ Emulation pod : BM87C408M0A

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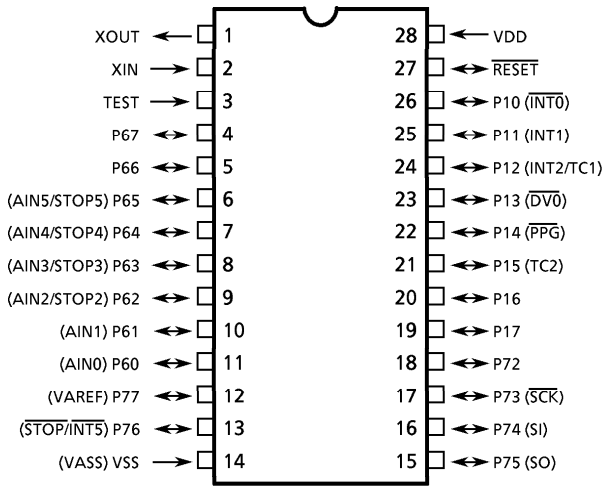
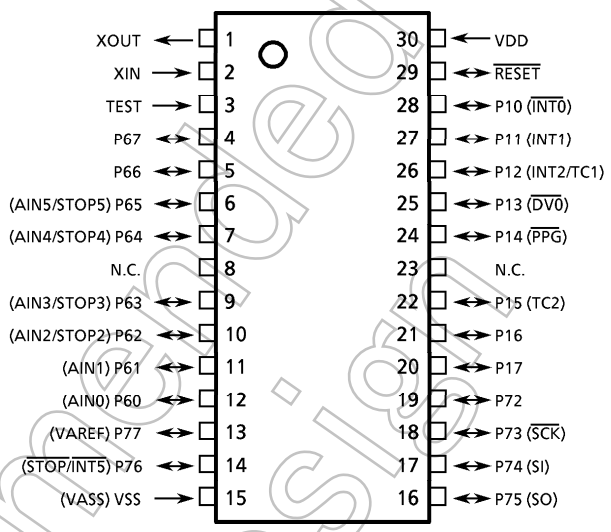
Pin Assignments (Top View)

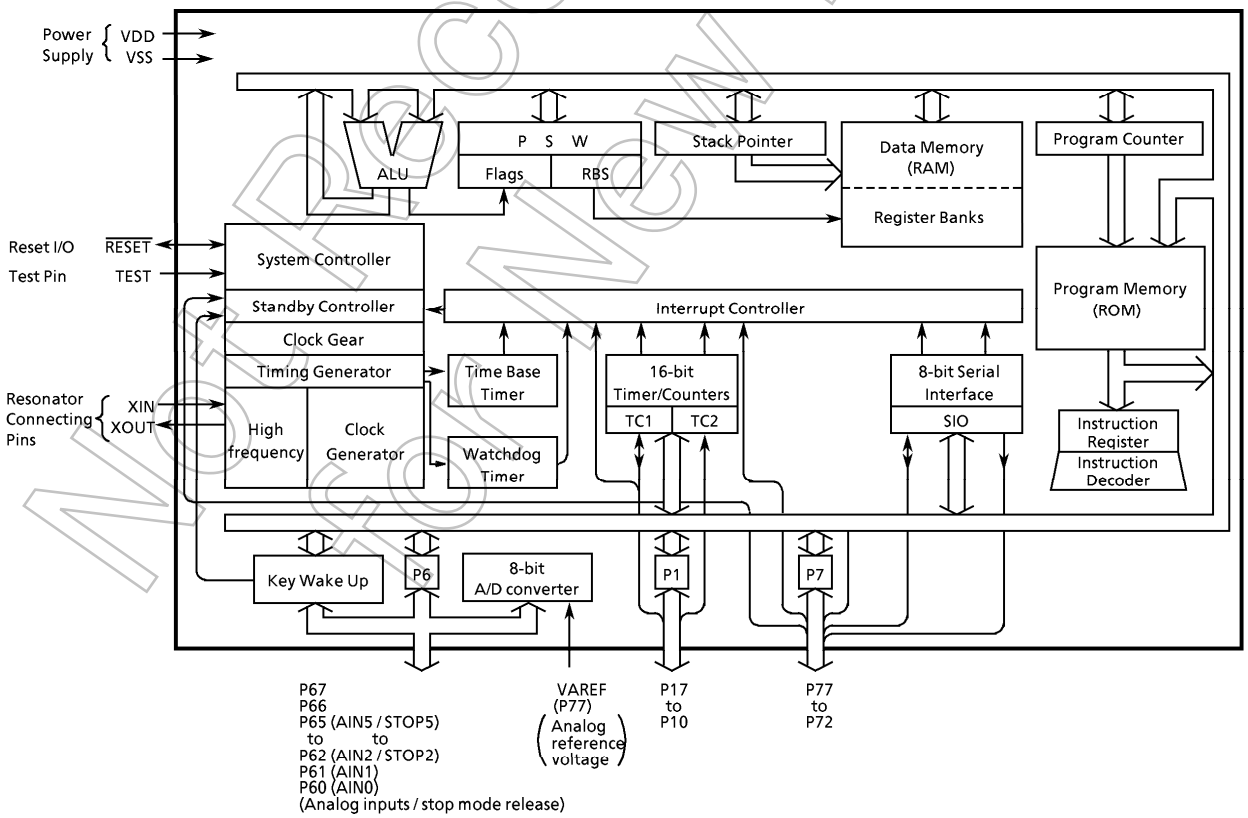
P-SOP28-450-1.27 / P-SDIP28-400-1.78



P-SOP30-56-0.65



Block Diagram



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Pin Function

Pin Name	Input / Output	Function	
P17, P16	I/O	8-bit programmable input/output ports (tri-states) Each bit of these ports can be individually configured as an input or an output under software control. When used as an external interrupt input or a timer counter input, the input mode is configured. When used as a divider output or a PPG output, the latch must be set to "1" and the output mode is configured.	
P15 (TC2)	I/O (Input)		Timer/Counter 2 input
P14 ($\overline{PPG}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{DVO}$)			Divider output
P12 (INT2 / TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P67, P66	I/O (Input)	8-bit programmable input/output port (tri-states). Each bit of the port can be individually configured as an input or an output under software control. When used as an analog input or stop mode release input , the input mode is configured.	
P65 (AIN5 / STOP5)			A/D converter analog inputs / Stop mode release inputs
P64 (AIN4 / STOP4)			
P63 (AIN3 / STOP3)			
P62 (AIN2 / STOP2)			
P61 (AIN1)			A/D converter analog inputs
P60 (AIN0)			
P77 (VAREF)	I/O (Output)	6-bit programmable input/output port (tri-states). Each bit of these ports can be individually configured as an input or an output under software control. When used as an external interrupt input or a serial interface input pin, the input mode is configured. When used as a serial interface output pin, the latch must be set to "1" and the output mode is configured.	Analog reference power supply
P76 ($\overline{STOP}$/$\overline{INT5}$)			STOP mode release input/External interrupt 5 input
P75 (SO)	I/O (Output)		SIO serial data output
P74 (SI)	I/O (Input)		SIO serial data input
P73 ($\overline{SCK}$)	I/O (I/O)		SIO serial clock input/output
P72	I/O		
XIN, XOUT	Input, Output	Resonator connecting pins for clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for outgoing test. Be tied to low.	
VDD	Power Supply	2.7 to 5.5 V (TMP87C408/C808/P808), 1.8 to 4.0 V (TMP87C408L/C808L/P808L)	
VSS (VASS)		0 V (GND)	Analog reference GND

Not Recommended for New Design

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory, the data memory, and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64 Kbytes of memory. Figure 1-1 shows the memory address maps of the 87C408/808/408L/808L. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the RAM address space.

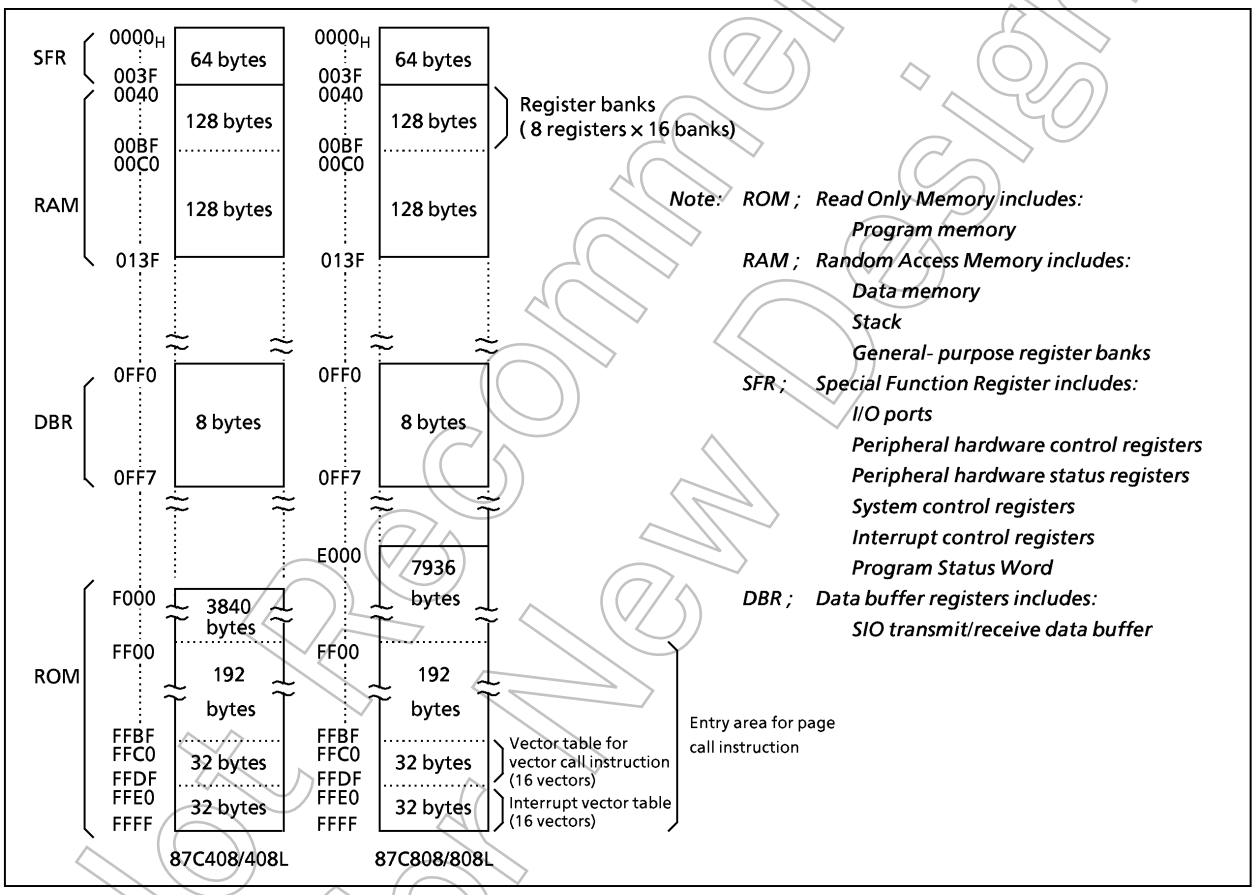

Figure 1-1. Memory Address Map

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1.2 Program Memory (ROM)

The 87C408/408L each have a 4 Kbytes (addresses F000 to $FFFF_H$), the 87C808/808L each have an 8 Kbytes (addresses E000 to $FFFF_H$) of program memory (mask programmed ROM).
Addresses FF00 to $FFFF_H$ of program memory is also used for a special purpose.

(1) Interrupt vector table (addresses FFE0 to $FFFF_H$)
This table consists of a reset vector and 16 interrupt vectors (2 bytes/vector). These vectors store a reset start address and interrupt service routine entry addresses.

(2) Vector table for vector call instructions (addresses FFC0 to $FFDF_H$)
This table stores call vectors (subroutine entry address, 2 bytes/vector) for the vector call instructions [CALLV a]. There are 16 vectors. The CALLV instruction increases memory efficiency when utilized for frequently used subroutine calls (called from 3 or more locations).

(3) Entry area(addresses FF00 to $FFFF_H$) for page call instructions
This is the subroutine entry address area for the page call instructions [CALLP a]. Addresses FF00 to $FFBF_H$ are normally used because addresses FFC0 to $FFFF_H$ are used for the vector tables.

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the current contents of the program counter (PC). There are relative jump and absolute jump instructions. The concepts of page or bank boundaries are not used in the program memory concerning any jump instruction.

Example: The relationship between the jump instructions and the PC.

① 5-bit PC-relative jump [JRS cc, $ + 2 + d]
F8C4H: JRS T, $ + 2 + 08H
When JF = 1, the jump is made to $F8CE_H$, which is 08_H added to the contents of the PC. (The PC contains the address of the instruction being executed + 2; therefore, in this case, the PC contents are $F8C4_H + 2 = F8C6_H$.)

② 8-bit PC-relative jump [JR cc, $ + 2 + d]
F8C4H: JR Z, $ + 2 + 80H
When ZF = 1, the jump is made to $F846_H$, which is $FF80_H$ (-128) added to the current contents of the PC.

③ 16-bit absolute jump [JP a]
F8C4H: JP 0F235H
An unconditional jump is made to address $F235_H$. The absolute jump instruction can jump anywhere within the entire 64K-bytes space.

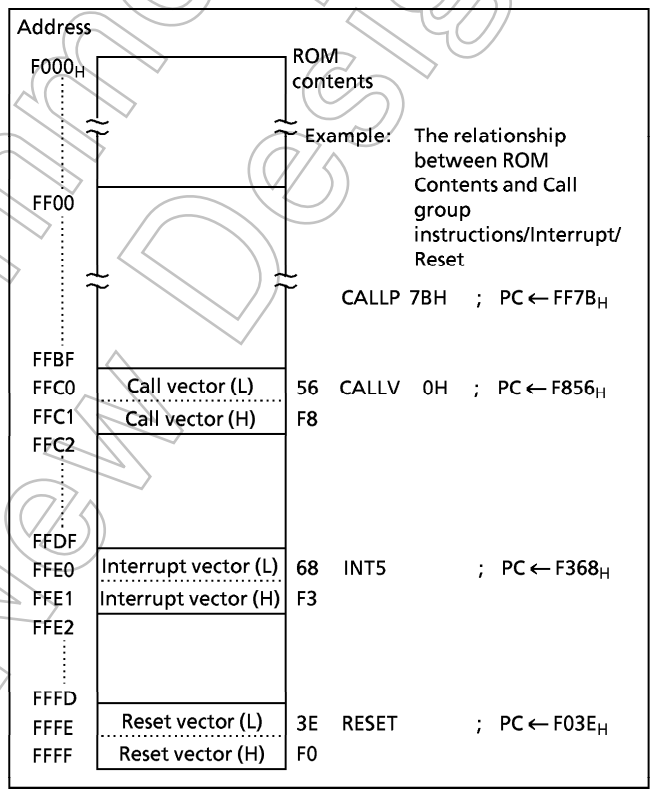

Figure 1-2. Program Memory Map

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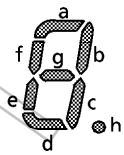
In the TLCS-870 Series, the same instruction used to access the data memory is also used to read out fixed data stored in the program memory. The register offset PC-relative addressing (PC + A) instructions can also be used, and the code conversion, table look-up and n-way multiple jump processing can easily be programmed.

Example 1: Loads the ROM contents at the address specified by the HL register pair contents into the accumulator (87C408: HL ≧ $F000_H$)

```
LD      A, (HL)          ;  A←ROM (HL)
```

Example 2: Converts BCD to 7-segment code (common anode LED). When A = 05_H, 92_H is output to port P1 after executing the following program.

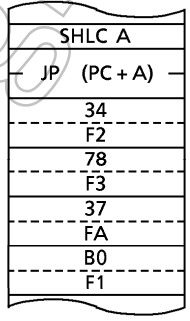
```
        ADD     A, TABLE – $ – 4     ; P1 ←ROM (TABLE + A)
        LD      (P1), (PC + A)
        JRS     T, SNEXT             ; Jump to SNEXT
TABLE:  DB      0C0H, 0F9H, 0A4H, 0B0H, 99H, 92H, 82H, 0D8H, 80H, 98H
SNEXT:
```



Note: "$" is a header address of ADD instruction. DB is a byte data definition instruction.

Example 3: N-way multiple jump in accordance with the contents of accumulator (0 ≦ A ≦ 3).

```
SHLC    A                ;  if A = 00H then PC←F234H
JP      (PC + A)           if A = 01H then PC←F378H
                           if A = 02H then PC←FA37H
                           if A = 03H then PC←F1B0H
DW      0F234H, 0F378H, 0FA37H, 0F1B0H
```



Note: DW is a word data definition instruction. Word = 2 bytes.

1.3 Program Counter (PC)

The program counter (PC) is a 16-bit register which indicates the program memory address where the instruction to be executed next is stored. After reset, the reset vector stored in the vector table (addresses $FFFF_H$ and $FFFE_H$) is loaded into the PC; therefore, program execution is possible from any desired address. For example, when $F0_H$ and $3E_H$ are stored at addresses $FFFF_H$ and $FFFE_H$, respectively, the execution starts from address $F03E_H$ after reset.

The TLCS-870 Series utilizes pipelined processing (instruction pre-fetch); therefore, the PC always indicates 2 addresses in advance. For example, while a 1-byte instruction stored at address $F123_H$ is being executed, the PC contains $F125_H$.

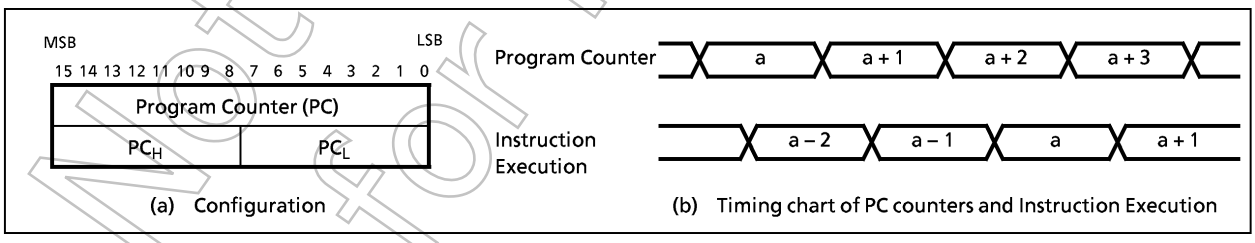


Figure 1-3. Program Counter

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1.4 Data Memory (RAM)

The 87C408/808/408L/808L each have a 256 bytes (addresses 0040 to $013F_H$) of data memory (static RAM). Figure 1.4 shows the data memory map.

Addresses 0000 to $00FF_H$ are used as a direct addressing area to enhance instructions which utilize this addressing mode; therefore, addresses 0040 to $00FF_H$ in the data memory can also be used for user flags or user counters.

Example 1: If bit 2 at data memory address $00C0_H$ is "1", 00_H is written to data memory at address $00E3_H$; otherwise, FF_H is written to the data memory at address $00E3_H$.

```
        TEST    (00C0H).2        ; if (00C0H)2 = 0 then jump
        JRS     T,SZERO
        CLR     (00E3H)          ; (00E3H)←00H
        JRS     T,SNEXT
SZERO:  LD      (00E3H), 0FFH    ; (00E3H)←FFH
SNEXT:
```

Example 2: Increments the contents of data memory at address $00F5_H$, and clears to 00_H when 10_H is exceeded.

```
        INC     (00F5H)
        AND     (00F5H), 0FH
```

General-purpose register banks (8 registers × 16 banks) are also assigned to the 128 bytes of addresses 0040 to $00BF_H$. Access as data memory is still possible even when being used for registers. For example, when the contents of the data memory at address 0040_H is read out, the contents of the accumulator in the bank 0 are also read out.

The stack can be located anywhere within the data memory except the register bank area. For more details on the stack, see section "1.7 Stack and Stack Pointer".

With the TLCS-870 Series, programs in data memory cannot be executed. If the program counter indicates a specific data memory address (addresses 0040 to $013F_H$), an address-trap-reset is generated due to bus error. (Output from the $\overline{RESET}$ pin goes low.)

The data memory contents become unstable when the power supply is turned on; therefore, the data memory should be initialized by an initialization routine.

Example 1: Clears RAM to 0 except the bank 0

```
        LD      HL, 0048H        ; Sets start address to HL register pair
        LD      A, H             ; Sets initial data (A)
        LD      BC, 00F7H        ; Sets number of byte to BC register pair
SRAMCLR: LD     (HL+), A
        DEC     BC
        JRS     F, SRAMCLR
```

Note: "$" is a header address of ADD instruction. The general-purpose registers are mapped in the RAM; therefore, do not clear RAM at the current bank addresses. Clears RAM to 0 except the bank 0.

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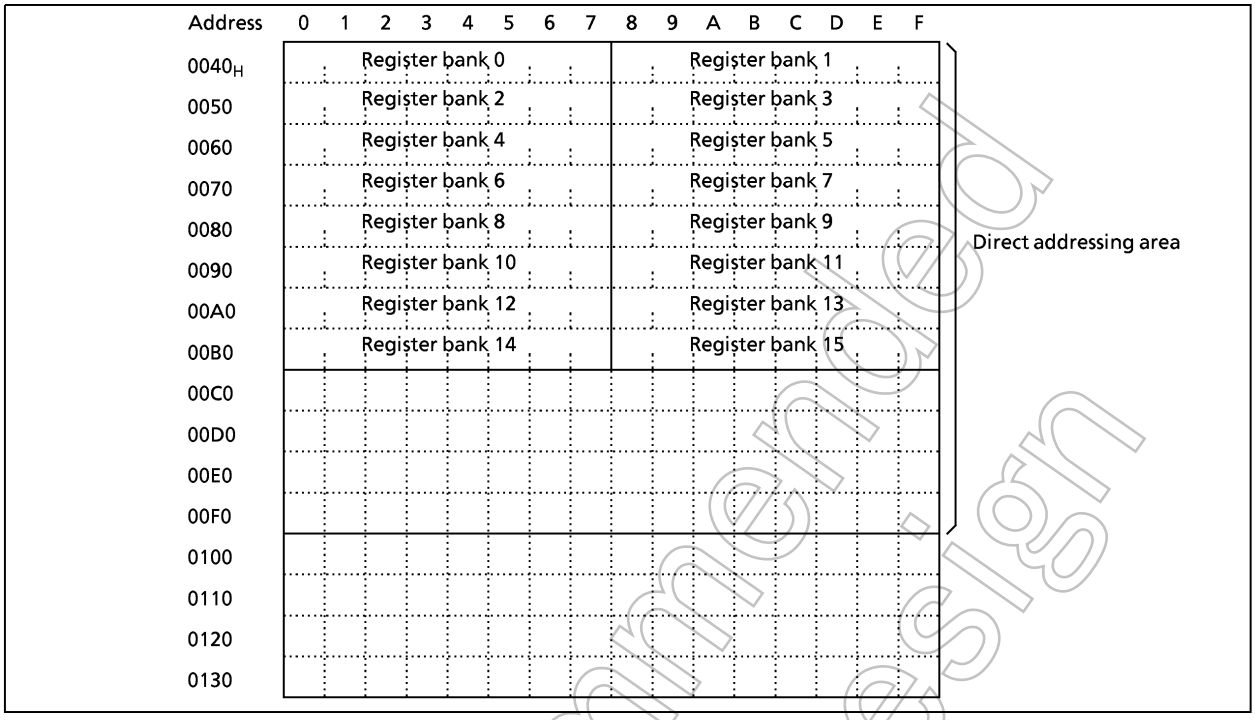

Figure 1-4. Data Memory Map

1.5 General-purpose Register Banks

General-purpose registers are mapped into addresses 0040 to 00BF$_H$ in the data memory. There are 16 register banks, and each bank contains eight 8-bit registers W, A, B, C, D, E, H, and L. Figure 1-5 shows the general-purpose register bank configuration. The unused register banks can be used as a data memory.

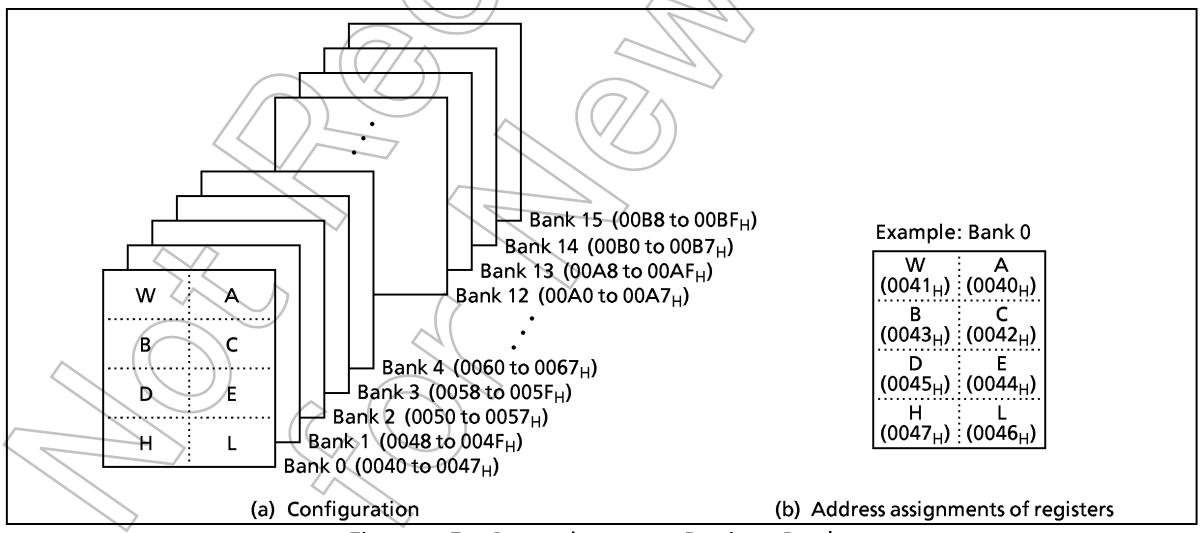

Figure 1-5. General-purpose Register Banks

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In addition to access in 8-bit units, the registers can also be accessed in 16-bit units as the register pairs WA, BC, DE, and HL. Besides its function as a general-purpose register, the register also has the following functions.

(1) A, WA

The A register functions as an 8-bit accumulator and WA the register pair functions as a 16-bit accumulator (W is high byte and A is low byte). Registers other than A can also be used as accumulators for 8-bit operations.

```
Examples: ① ADD  A, B        ; Adds B contents to A contents and stores the result into A.
          ② SUB  WA, 1234H   ; Subtracts 1234H from WA contents and stores the result into WA.
          ③ SUB  E, A        ; Subtracts A contents from B contents, and stores the result into E.
```

(2) HL, DE

The HL register functions as a data pointer/index register/base register, and the DE register pair function as a data pointer to specify the memory address.
HL also has an auto-post-increment and auto-pre-decrement functions. This function simplifies multiple digit data processing, software LIFO (last-in first-out) processing, etc.

```
Example 1: ① LD  A, (HL)        ; Loads the memory contents at the address specified by HL into A.
           ② LD  A, (HL + 52H)  ; Loads the memory contents at the address specified by the value
                                  obtained by adding 52H to HL contents into A.
           ③ LD  A, (HL + C)    ; Loads the memory contents at the address specified by the value
                                  obtained by adding the register C contents to HL contents into A.
           ④ LD  A, (HL + )     ; Loads the memory contents at the address specified by HL into A.
                                  Then increments HL.
           ⑤ LD  A, ( – HL)     ; Decrement HL. Then loads the memory contents at the address
                                  specified by new HL into A.
```

TLCS-870 Series can transfer data directly memory to memory, and operate directly between memory data and memory data. This facilitates the programming of block processing.

```
Example 2:  Block transfer
            LD      B, n          ; Sets number of bytes to transfer – 1
            LD      HL, DSTA      ; Sets destination address
            LD      DE, SRCA      ; Sets source address
SLOOP:      LD      (HL), (DE)    ; (HL) ← (DE)
            INC     HL            ; HL ← HL + 1
            INC     DE            ; DE ← DE + 1
            DEC     B             ; B←B – 1
            JRS     F, SLOOP      ; if B ≧ 0 then loop
```

(3) B, C, BC

Registers B and C can be used as 8-bit buffers or counter, and the BC register pair can be used as a 16-bit buffer or counter. The C register functions as an offset register for register offset index addressing (refer to example 1 ③ above) and as a divisor register for the division instruction.

```
Example 1: Repeat processing
           LD      B, n          ; Sets n as the number of repetitions
SREPEAT:   processing
           DEC     B
           JRS     F, SREPEAT

Example 2: Division (16-bit ÷ 8-bit)
           DIV     WA, C         ; Divides the WA contents by the C contents, places
                                   the quotient in A and the remainder in W.
```

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The general-purpose banks are selected by the 4-bit register bank selector (RBS). During reset, the RBS is initialized to "0". The bank selected by the RBS is called the current bank.
Together with the flag, the RBS is assigned to address $003F_H$ in the SFR as the program status word (PSW). There are 3 instructions [LD RBS, n], [PUSH PSW], [POP PSW] to access the PSW. The PSW can be also operated by the memory access instruction.

```
Example 1: Incrementing the RBS
           INC   (003FH)      ; RBS ← RBS + 1
Example 2: Reading the RBS
           LD    A, (003FH)   ; A ← RBS(The flags are simultaneously read in this instruction.)
```

Highly efficient programming and high speed task switching are possible by using bank changeover to save registers during interrupt and to transfer parameters during subroutine processing. During interrupt, the RBS is automatically saved onto the stack. The bank used before the interrupt is automatically restored by executing an interrupt return instruction [RETI]/[RETN] ; therefore, there is no need for the RBS save/restore software processing.
The TLCS-870 Series supports a maximum of 15 interrupt sources. One bank is assigned to the main program, and one bank can be assigned to each source. Also, to increase the efficiency of data memory usage, assign the same bank to interrupt sources which are not nested.

```
Example:   Saving/restoring registers during interrupt task using bank changeover.
   PINT1:     LD    RBS, n        ; RBS ← n (Bank changeover)
              Interrupt processing
              RETI                ; Maskable interrupt return (Bank automatic restoring)
```

1.6 Program Status Word (PSW)

The program status word (PSW) consists of a register bank selector (RBS) and flags, and the PSW is assigned to address $003F_H$ in the SFR.
The RBS can be read and written using the memory access instruction, however the flags can only be read. When writing to the PSW, the change specified by the instruction is made without writing data to the flags. For example, when the instruction [LD (003FH), 05H] is executed, "5" is written to the RBS and the JF is set to "1", but the other flags are not affected.
During interrupt, PSW is saved to the stack with the program counter. The PSW is restored from the stack by executing return instructions [RETI]/[RETN].
[PUSH PSW] and [POP PSW] are the PSW access instructions.

1.6.1 Register Bank Selector (RBS)

The register bank selector (RBS) is a 4-bit register used to select general-purpose register banks. For example, when RBS = 2, bank 2 is currently selected. During reset, the RBS is initialized to "0".

7	6	5	4	3	2	1	0
JF	ZF	CF	HF	RBS			

Figure 1-6. PSW (Flags, RBS) Configuration

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1.6.2 Flags (FLAG)

The flags are configured with the upper 4 bits: a zero flag, a carry flag, a half carry flag and a jump status flag. The flags are set or cleared under conditions specified by the instruction. These flags except the half carry flag are used as jump condition "cc" for conditional jump instructions [JR cc, $ + 2 + d], [JRS cc, $ + 2 + d]. After reset, the jump status flag is initialized to "1", other flags are not affected.

(1) **Zero flag (ZF)**

The ZF is set to "1" if the operation result or the transfer data is 00_H (for 8-bit operations and data transfers)/0000_H (for 16-bit operations); otherwise the ZF is cleared to "0".
During the bit manipulation instructions, the ZF is cleared to "0" if the contents of the specified bit is "1". This flag is set to "1" when the upper 8 bits of the product are 00_H during the multiplication instruction, and when 00_H for the remainder during the division instruction; otherwise it is cleared to "0".

(2) **Carry flag (CF)**

The CF is set to "1" when a carry occurred during addition or a borrow occurred during subtraction; otherwise the CF is cleared to "0". During division, this flag is set to "1" when the divisor is 00_H (divided by zero error), or when the quotient is 100_H or higher (quotiont-overflow error). The CF is also affected during the shift/rotate instructions. The data shifted out from a register is set to the CF. This flag is also a 1-bit register (a boolean accumulator) for the bit manipulation instructions.
Set/clear/invert are possible with the CF manipulation instructions.

Example: Bit manipulation (The result of exclusive-OR between bit 5 content of address 07_H and bit 0 content of address $9A_H$ is written to bit 2 of address 01_H.)

```
LD    CF, (0007H) . 5     ; (0001H)2 ← (0007H)5 ∀ (009AH)0
XOR   CF, (009AH) . 0
LD    (0001H) . 2, CF
```

(3) **Half carry flag (HF)**

The HF is set to "1" when a carry occurred to bit 4 of the operation result during an 8-bit addition, or when a borrow occurred from bit 4 of the result during an 8-bit subtraction. This flag is useful in the decimal adjustment for BCD operations (adjustments using the [DAA r], or [DAS r] instructions).

Example: BCD operation
(The A becomes 47_H after executing the following program when A = 19_H, B = 28_H.)

```
ADD   A, B        ; A ← 41H, HF ← 1, CF = 0
DAA   A           ; A ← 41H + 06H = 47H (decimal-adjust)
```

(4) **Jump status flag (JF)**

The JF is usually set to "1". Zero or carry information is set to the JF after operation. The JF provides the jump condition for conditional jump instructions [JR T/F, $ + 2 = d], [JRS T/F, $ + 2 + d] (T or F is a condition code).

Example: Jump status flag and conditional jump instruction

```
INC   A
JRS   T, SLABLE1     ; Jump when a carry is caused by the immediately
  ⋮                    preceding operation instruction.
LD    A, (HL)
JRS   T, SLABLE2     ; JF is set to "1" by the immediately preceding
  ⋮                    instruction, making it an unconditional jump
                       instruction.
```

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Example: The accumulator and flags becomes as shown below after executing the following instructions when the WA register pair, the HL register pair, the data memory at address $00C5_H$, the carry flag and the half carry flag contents being "$219A_H$", "$00C5_H$", "$D7_H$", "1", and "0", respectively.

Instruction	Accumulator after execution	Flag after execution			
		JF	ZF	CF	HF
ADDC A, (HL)	72	1	0	1	1
SUBB A, (HL)	C2	1	0	1	0
CMP A, (HL)	9A	0	0	1	0
AND A, (HL)	92	0	0	1	0
LD A, (HL)	D7	1	0	1	0
ADD A, 66H	00	1	1	1	1

Instruction	Accumulator after execution	Flag after execution			
		JF	ZF	CF	HF
INC A	9B	0	0	1	0
ROLC A	35	1	0	1	0
RORC A	CD	0	0	0	0
ADD WA, 0F508H	16A2	1	0	1	0
MUL W, A	13DA	0	0	1	0
SET A.5	BA	1	1	1	0

1.7 Stack, Stack Pointer

1.7.1 Stack

The stack provides the area in which the return address or status, etc. are saved before a jump is performed to the processing routine during the execution of a subroutine call instruction or the acceptance of an interrupt.

On a subroutine call instruction [CALL a] / [CALLP a] / [CALLVn], the return address is saved (the upper byte is pushed first, followed by the lower byte). During software interrupt instruction [SWI] execution or interrupt, the program status word is saved, then the return address is saved.

When returning from the processing routine, executing a subroutine return instruction [RET] restores the contents to the PC from the stack; executing an interrupt return instruction [RETI] / [RETN] restores the contents to the PC and the PSW.

The stack can be located anywhere within the data memory.

1.7.2 Stack Pointer (SP)

The stack pointer (SP) is a 16-bit register to point out the first start address on the stack. The SP is post-decrement when a subroutine call or a push instruction is executed, or when an interrupt is accepted; and the SPC is pre-incremented when a return or a pop instruction is executed. The stack deepens to the direction of the lower address. Figure 1-8 shows the change of the stack access and the SP.

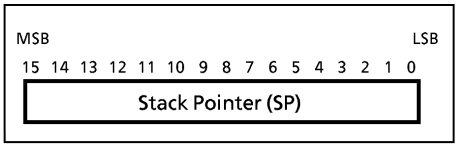

Figure 1-7. Stack Pointer

The SP is not initialized hardware-wise but requires initialization by an initialize routine (sets the highest stack address). [LD SP, mn], [LD SP, gg] and [LD gg, SP] are the SP access instructions (mn; 16-bit immediate data, gg; register pair).

Example 1: To initialize the SP

```
LD      SP, 013FH      ; SP←013F_H
```

Example 2: TO read the SP

```
LD      HL, SP         ; HL←SP
```

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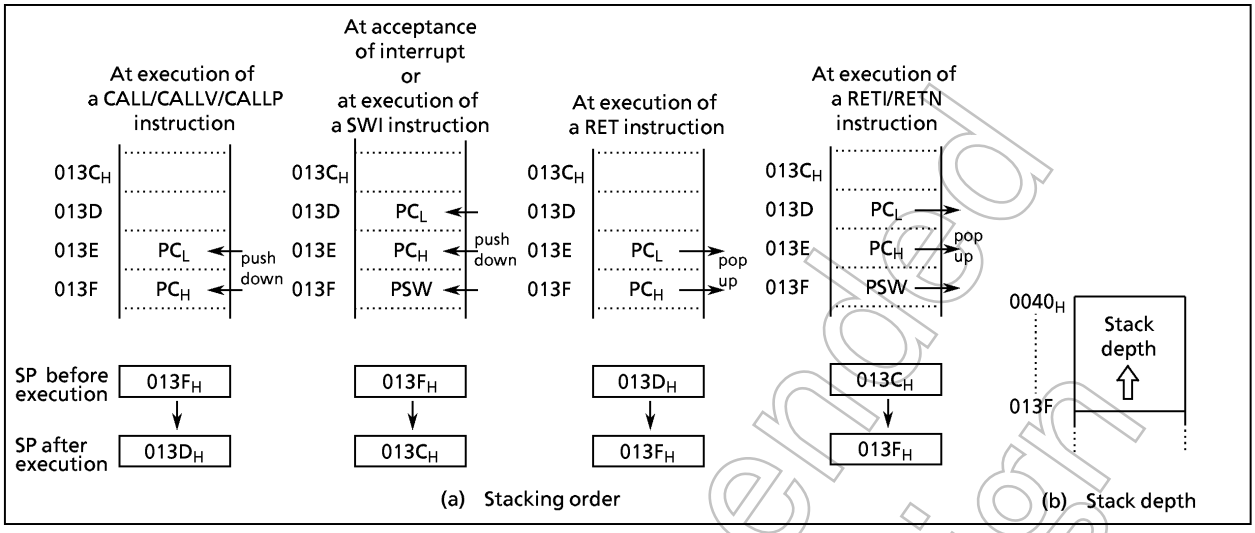

Figure 1-8. Stack

1.8 System Clock Controller

The system clock controller consists of a clock generator, a timing generator, a clock gear, and a stand-by controller.

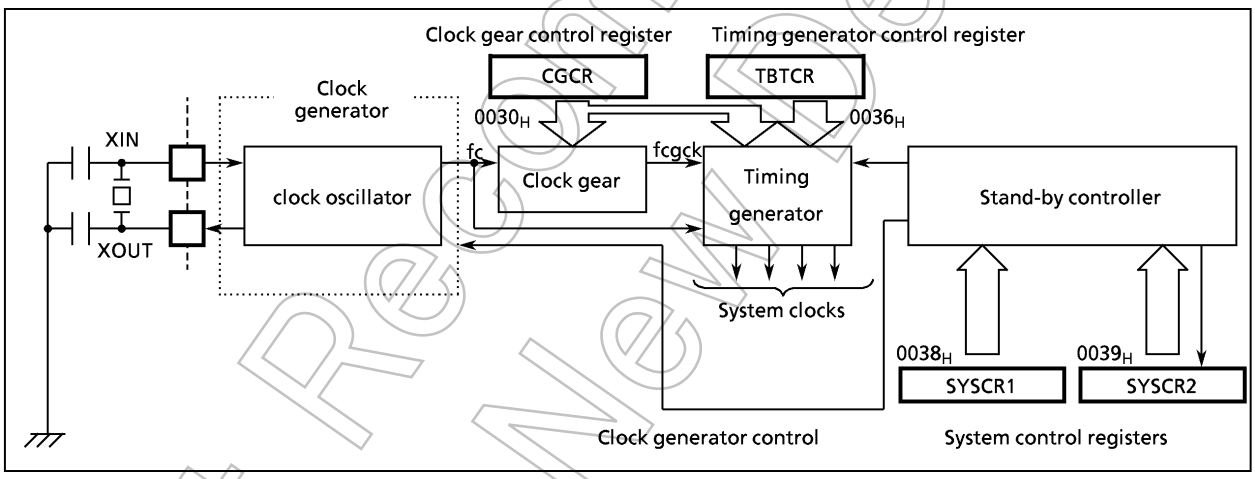

Figure 1-9. System Clock Controller

Not Recommended for New Design

1.8.1 Clock Generator

The clock generator generates the basic clock which provides the system clocks supplied to the CPU core and peripheral hardware.

The clocks (fc) can be easily obtained by connecting a resonator between the XIN/XOUT pins. Clock input from an external oscillator is also possible.

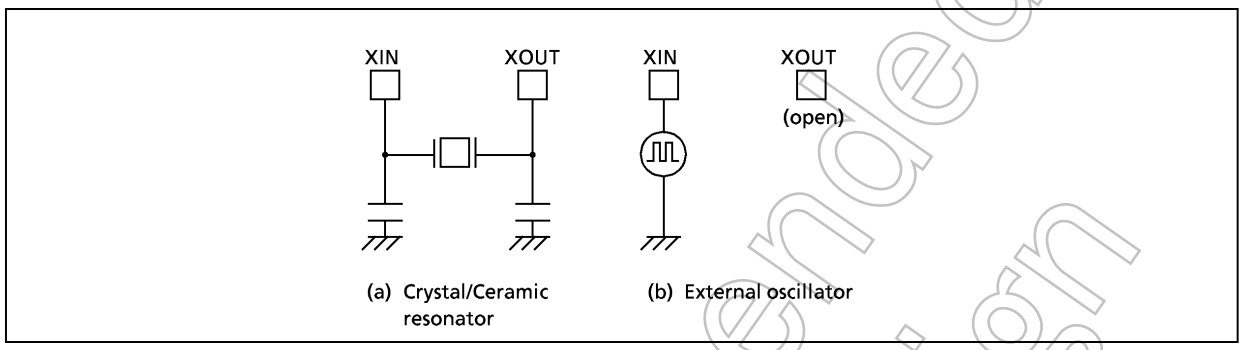

Figure 1-10. Example of Resonator Connection

Note: Accurate Adjustment of the Oscillation Frequency:
Although no hardware to externally and directly monitor the basic clock pulse is provided, the oscillation frequency can be adjusted by making the program to output fixed frequency pulses to the port while disabling all interrupts and monitoring this pulse. With a system requiring adjustment of the oscillation frequency, the adjusting program must be created beforehand.

1.8.2 Clock Gear

The clock gear selects the gear clock (fcgck) which provides the main system clocks supplied to the timing generator from fc, fc/2, fc/4 and fc/8. Power consumption can be reduced by switching of the gear-clock from fc to fc/2, fc/4 and fc/8. The clock gear consists of a divided-by-8 prescaler with a multiplexer.

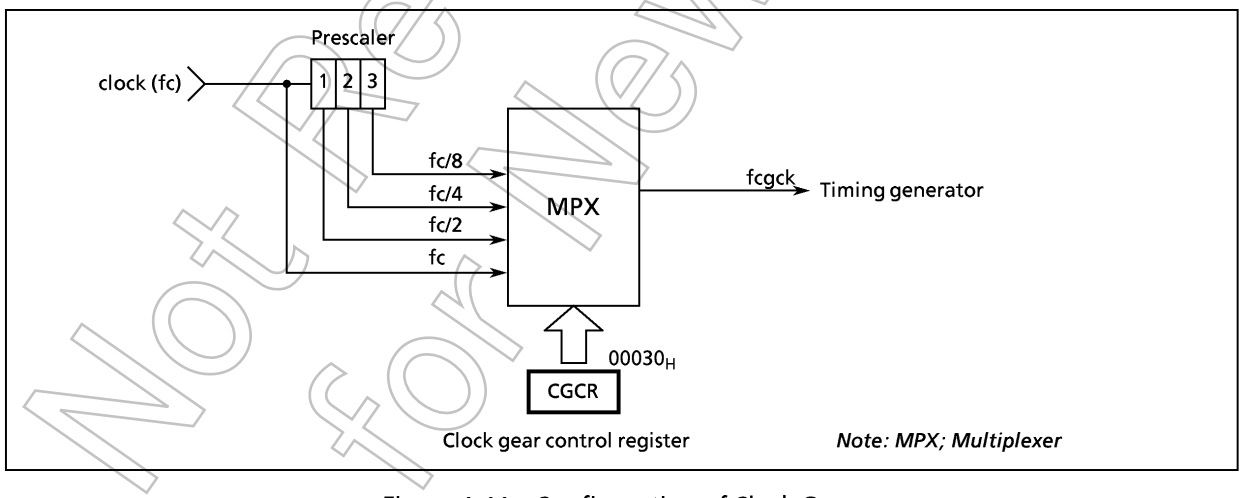

Figure 1-11. Configuration of Clock Gear

Not Recommended for New Design

CGCR (00030_H)

7	6	5	4	3	2	1	0
0	0	0		FCGCK			

(Initial value: 000* 1000)

FCGCK	Gear clock selection (write) / gear clock monitor (read)	0***: reserved 1000: fc 1001: fc/2 1010: fc/4 1011: fc/8 1100: reserved 1101: reserved 111*: reserved	R/W

*Note1: fc ; High-frequency clock * ; Don't care*
Note2: Bit 4 in CGCR is always read in as "1" when a read instruction is executed.
Note3: Always set bit 7 to 5 to "0"

Figure 1-12. Clock gear control register

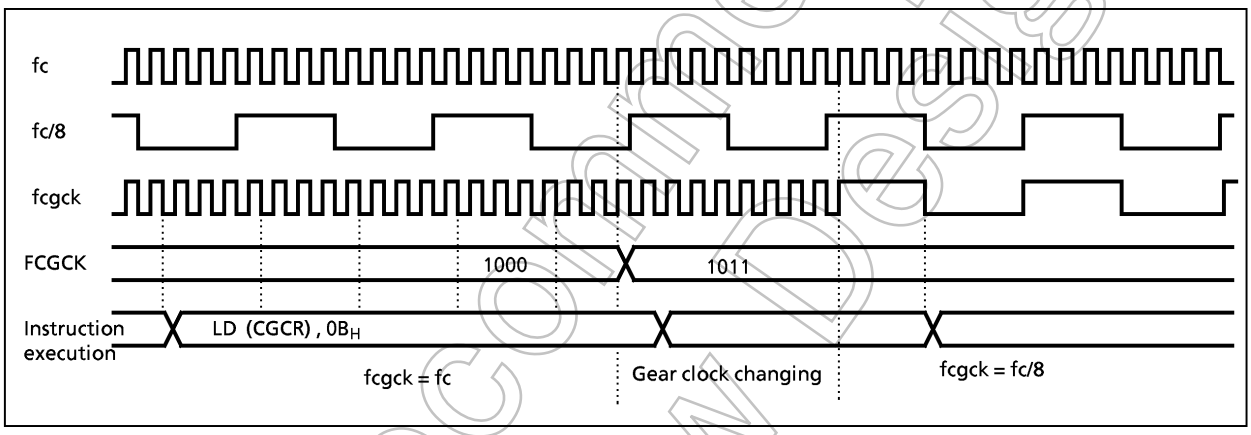

Figure 1-13. Example of clock exchangeable timing by clock gear

1.8.3 Timing Generator

The timing generator generates from the basic clock (fc) or the gear clock (fcgck) the various system clocks supplied to the CPU core and peripheral hardware. The timing generator provides the following functions:

① Generation of main system clock
② Generation of divider output ($\overline{DVO}$) pulses
③ Generation of source clocks for time base timer
④ Generation of source clocks for watchdog timer
⑤ Generation of internal source clocks for timer/counters
⑥ Generation of internal serial clock of serial interface
⑦ Generation of warm-up clocks for releasing STOP mode

(1) Configuration of Timing Generator

The timing generator consists of a 21-stage divider with a divided-by-2 prescaler. During reset and at releasing STOP mode, the divider is cleared to "0", however; the prescaler is not cleared.

Note: Even if the main system clock is changed by the clock gear, the output from the divider is not changed. The peripheral circuit using high-speed divider output (1st output) can not be used when the main system clock slows down.

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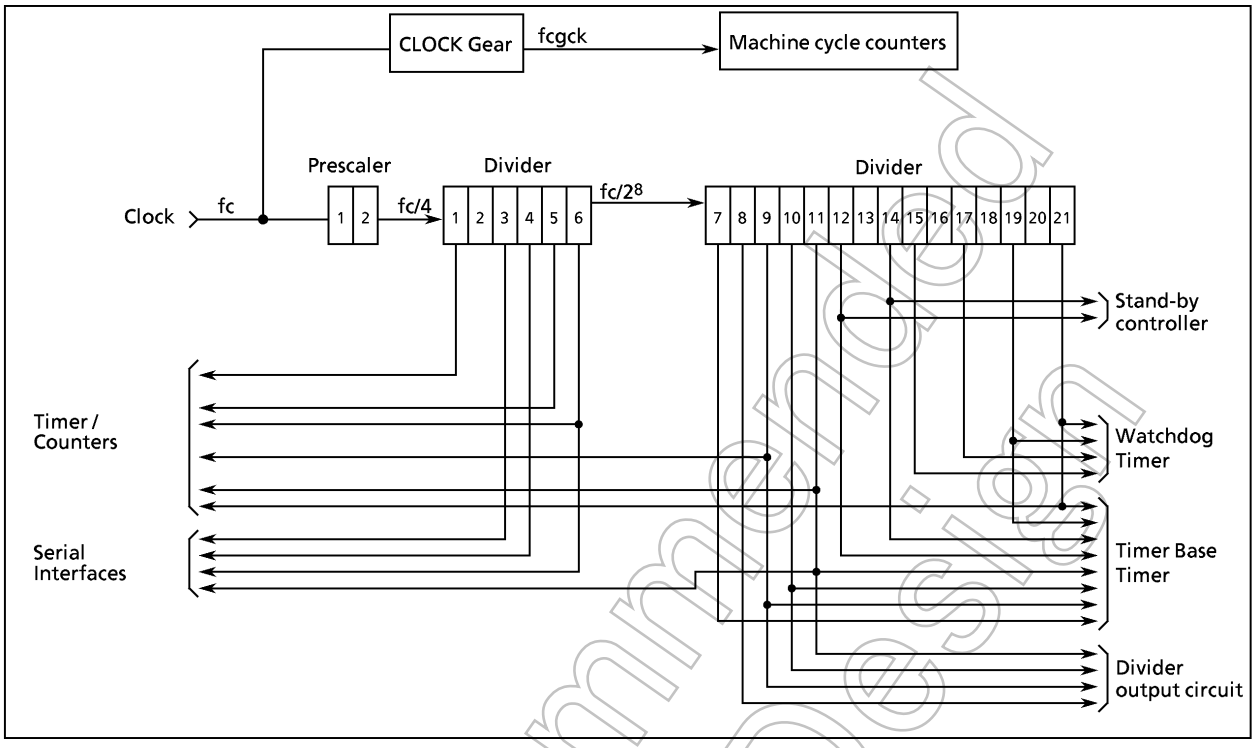


Figure 1-14. Configuration of Timing Generator

(2) Machine Cycle

Instruction execution and built-in hardware operation are synchronized with the system clock.

The minimum instruction execution unit is called an "machine cycle". There are a total of 10 different types of instructions for the TLCS-870 Series: ranging from 1-cycle instructions which require one machine cycle for execution to 10-cycle instructions which require 10 machine cycles for execution.

A machine cycle consists of 4 states (S0 to S3), and each state consists of one main system clock.

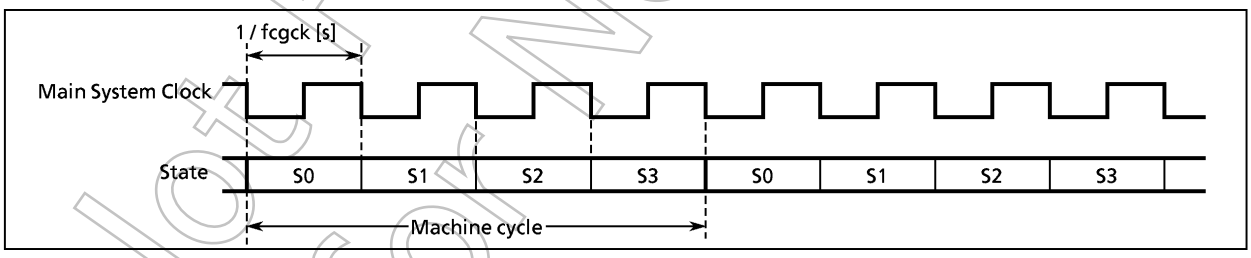


Figure 1-15. Machine Cycle

Table 1-1. Machine Cycle Example

Frequency	Machine cycle			
	fcgck = fc	fcgck = fc/2	fcgck = fc/4	fcgck = fc/8
fc = 8 MHz	0.5 μs	1 μs	2 μs	4 μs

Not Recommended for New Design

1.8.4 Stand-by Controller

The stand-by controller starts and stops the oscillation circuits. These modes are controlled by the system control registers (SYSCR1, SYSCR2). Figure 1.16 shows the operating mode transition diagram and Figure 1.17 shows the system control registers.

(1) **Operation mode**

The machine cycle time is 4/fcgck [s]

① NORMAL mode

In this mode, both the CPU core and on-chip peripherals operate. The TMP87C408/808/408L/808L is placed in this mode after reset.

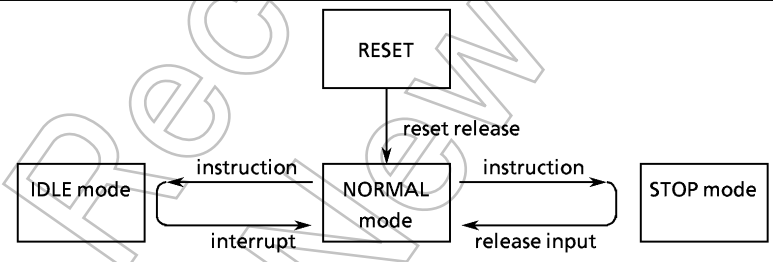
② IDLE mode

In this mode, the CPU and the watchdog timer are halted; however, on-chip peripherals remain active. IDLE mode is started by the system control register 2, and IDLE mode is released to NORMAL mode by an interrupt request from on-chip peripherals or external interrupt inputs. When IMF (interrupt master enable flag) is "1" (interrupt enable), the execution will resume upon acceptance of the interrupt, and the operation will return to normal after the interrupt service is completed. When IMF is "0" (interrupt disable), the execution will resume with the instruction which follows IDLE mode start instruction.

③ STOP mode

In this mode, the internal oscillation circuit is turned off, causing all system operations to be halted. The internal status immediately prior to the halt is held with the lowest power consumption during this mode. The output status of input output ports can be set to either output hold or high-impedance under software control.

STOP mode is started by the system control register 1, and STOP mode is released by $\overline{\text{STOP}}$ input pin (either level-sensitive or edge-sensitive can be selected). After the warming-up period is completed, the execution resumes with the next instruction which follows the STOP mode start instruction.



Mode Transition Diagram

Operating mode	Oscillation circuit	CPU core	Peripheral circuit	Machine cycle time
RESET	turning on oscillation	reset	reset	4 / fcgck [s]
NORMAL		operate	operate	
IDLE		halt		
STOP	Turning off oscillation		halt	—

Figure 1-16. Operating Mode Transition Diagram

Not Recommended for New Design

System Control Register 1

SYSCR1 (0038_H)

7	6	5	4	3	2	1	0
STOP	RELM	0	OUTEN	WUT			

(Initial value: 0000 00**)

STOP	STOP mode start	0: CPU core and peripherals remain active 1: CPU core and peripherals are halted	R/W
RELM	Release method for STOP mode	0: $\overline{STOP}$ pin input rising edge release 1: $\overline{STOP}$ pin input "H" level release	
OUTEN	Port output control during STOP mode	0: High-impedance 1: Remain unchanged	
WUT	Warming-up time at releasing STOP mode	00: 3×2^{16} / fc 01: 2^{16} / fc 10: 3×2^{14} / fc 11: 2^{14} / fc	

Note 1: Always set bit 5 to "0".

Note 2: Bits 1, 0 in SYSCR1 is read in as undefined value when a read instruction is executed.

Note 3: fc ; Clock [Hz]

** ; don't care*

Note 4: When the STOP mode is started by specifying OUTEN = "0", the internal input of port is fixed to "0" and the interrupt of the falling edge may be set.

System Control Register 2

SYSCR2 (0039_H)

7	6	5	4	3	2	1	0
XEN	0	0	IDLE				

(Initial value: 1000 ****)

XEN	High-frequency oscillator control	0: Turn off oscillation 1: Turn on oscillation	R/W
IDLE	IDLE mode start	0: CPU, WDT operate 1: CPU, WDT halt (IDLE mode start)	

Note 1: A reset is applied if XEN is cleared to "0".

Note 2: Always set bit 6, 5 to "0".

*Note 3: WDT ; Watchdog timer, * ; Don't care*

Note 4: Bits 3 to 0 in SYSCR2 are read in as "1" when a read instruction is executed.

Figure 1-17. System Control Registers 1, 2

Not Recommended for New Design

1.8.5 Operating Mode Control

(1) STOP mode (STOP)

STOP mode is controlled by the system control register 1 and the $\overline{STOP}$ pin input. The $\overline{STOP}$ pin is also used both as a port P76 and an $\overline{INT5}$ (external interrupt input 5) pin. The STOP mode is started by setting STOP (bit 7 in SYSCR1) to "1". During STOP mode, the following status is maintained.

① Oscillations are turned off, and all internal operations are halted.
② The data memory, registers (except for DBR), PSW, and port output latches are all held in the status in effect before STOP mode was entered. The port output can select either output hold or high-impedance by setting OUTEN (bit 4 in SYSCR1).
③ The divider of the timing generator is cleared to "0".
④ The program counter holds the address of the instruction after the following instruction which started the STOP mode. [for example, SET (SYSCR1).7]

STOP mode includes a level sensitive release mode and an edge-sensitive release mode, either of which can be selected with RELM (bit 6 in SYSCR1).

a. Level-sensitive release mode (RELM = 1)

In this mode, STOP mode is released by setting the $\overline{STOP}$ pin high. This mode is used for capacitor back-up when the main power supply is cut off and long term battery back-up.
When the $\overline{STOP}$ pin input is high, executing an instruction which starts the STOP mode will not place in STOP mode but instead will immediately start the release sequence (Warm-up). Thus, to confirm that the $\overline{STOP}$ pin input is low. The following method can be used for confirmation:
Using an external interrupt input $\overline{INT5}$ ($\overline{INT5}$ is a falling edge-sensitive input).

Example: Starting STOP mode with an INT5 interrupt.

```
PINT5:  TEST   (P7) . 6                ; To reject noise, the STOP mode does not start if
        JRS    F, SINT5                  port P76 is at high.
        LD     (SYSCR1), 01000000B     ; Sets up the level-sensitive release mode.
        SET    (SYSCR1) . 7            ; Starts STOP mode
        LDW    (IL), 1110011101010111B ; IL12, 11, 7, 5, 3 ← 0 (clears interrupt latches)
SINT5:  RETI
```

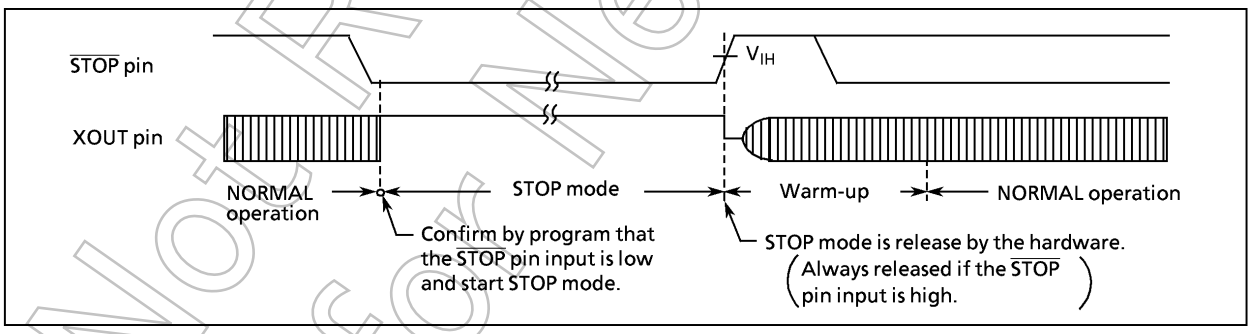


Figure 1-18. Level Mode

Note 1: After warm-up start, even if $\overline{STOP}$ pin input is low again, STOP mode does not restart.
Note 2: When changing to the level-sensitive release mode from the edge-sensitive release mode, the release mode is not switched until a rising edge of the $\overline{STOP}$ pin input is detected.

Not Recommended for New Design

b. Edge mode (RELM = "0")

In this mode, STOP mode is released by a rising edge of the $\overline{STOP}$ pin input. This is used in applications where a relatively short program is repeatedly executed at periodic intervals. This periodic signal (for example, a clock from a low-power consumption oscillator) is input to the $\overline{STOP}$ pin.

In the edge-sensitive release mode, STOP mode is started even when the $\overline{STOP}$ pin input is high.

Example : Starting STOP mode operation in the edge-sensitive release mode

```
LD    (SYSCR1), 00000000B      ; OUTEN ← 0 (specifies high-impedance)
DI                             ; IMF ← 0
SET   (SYSCR1). STOP           ; STOP ← 1 (activates STOP mode)
LDW   (IL), 1110011101010111B  ; IL7, 5, 3 ← 0 (clears interrupt latches)
EI                             ; IMF ← 1
```

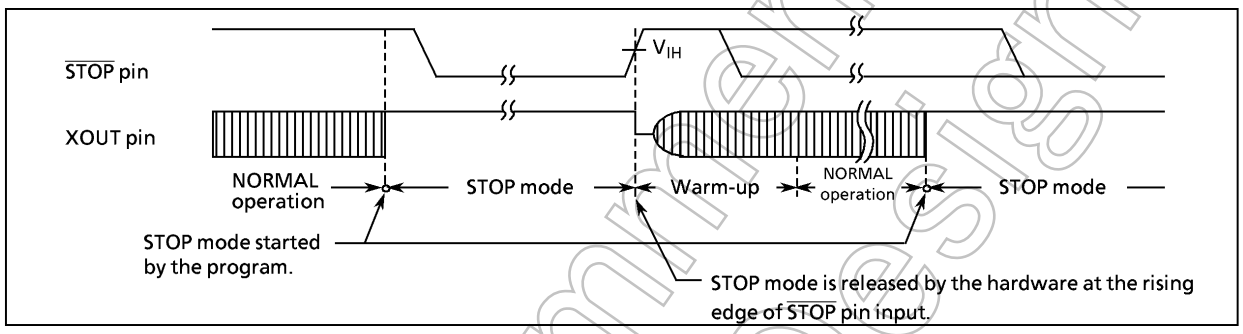


Figure 1-19. Edge-sensitive Mode

STOP mode is released by the following sequence:

① The oscillator is turned on.

② A warming-up period is inserted to allow oscillation time to stabilize. During warm-up, all internal operations remain halted. Four different warming-up times can be selected with WUT (bits 3 and 2 in SYSCR1) as determined by the resonator characteristics.

③ When the warming-up time has elapsed, normal operation resumes with the instruction following the STOP mode start instruction. The start is made after the divider of the timing generator is cleared to "0".

Table 1-2. Warming-up Time example

Warming-up Time [ms]		
WUT	at fc = 4.194304 MHz	at fc = 8 MHz
00	46.87	24.57
01	15.62	8.19
10	11.73	6.15
11	3.91	2.05

Note: The warming-up time is obtained by dividing the basic clock by the divider: therefore, the warming-up time may include a certain amount of error if there is any fluctuation of the oscillation frequency when STOP mode is released. Thus, the warming-up time must be considered an approximate value.

STOP mode can also be released by setting the $\overline{RESET}$ pin low, which immediately performs the normal reset operation.

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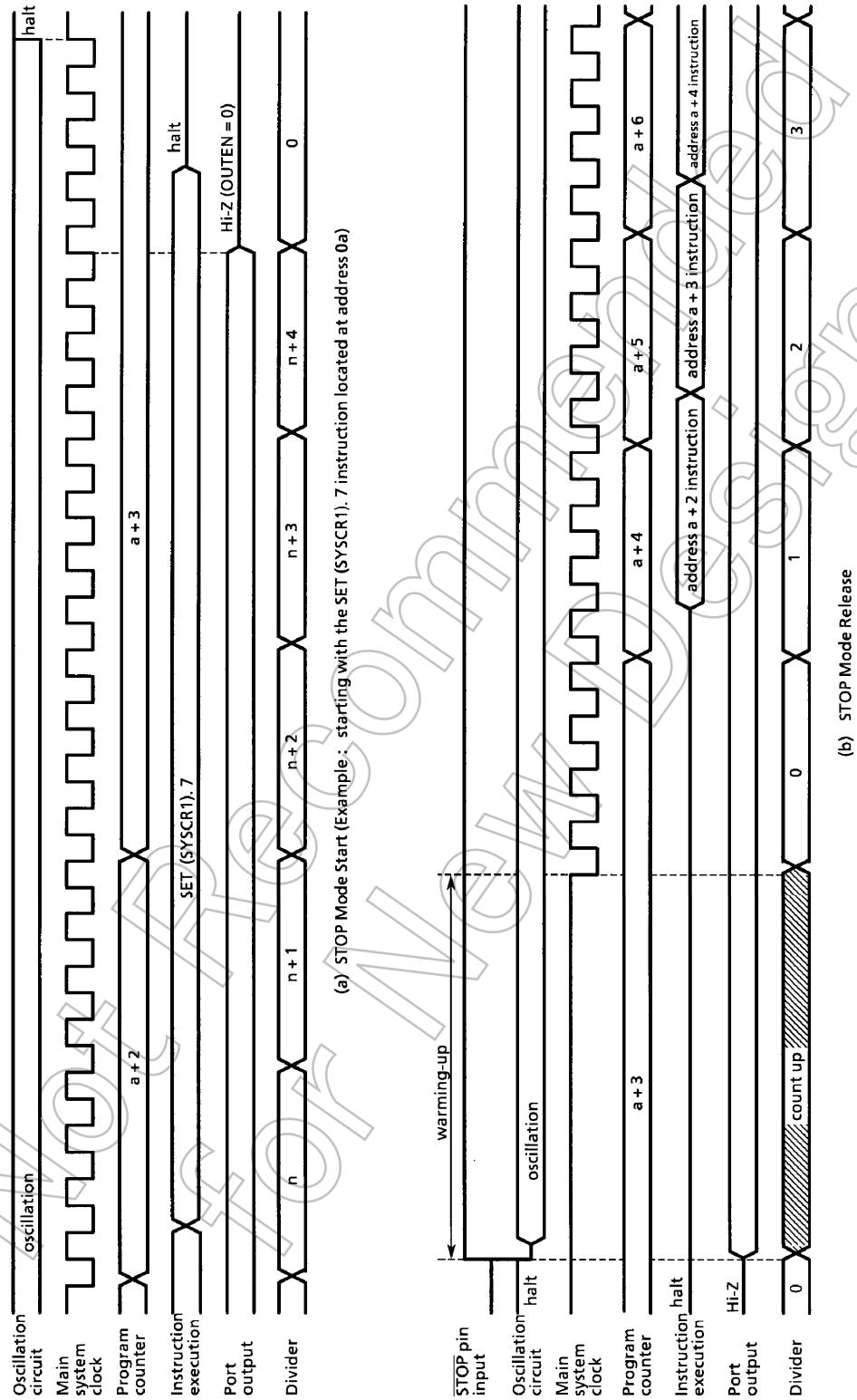

(a) STOP Mode Start (Example : starting with the SET (SYSCR1). 7 instruction located at address 0a)

(b) STOP Mode Release

Figure 1-20. STOP Mode Start/Release

Not Recommended for New Design

Note: When STOP mode is released with a low hold voltage, the following cautions must be observed.
The power supply voltage must be at the operating voltage level before releasing STOP mode. The $\overline{\text{RESET}}$ pin input must also be high, rising together with the power supply voltage. In this case, if an external time constant circuit has been connected, the $\overline{\text{RESET}}$ pin input voltage will increase at a slower rate than the power supply voltage. At this time, there is a danger that a reset may occur if input voltage level of the $\overline{\text{RESET}}$ pin drops below the non-inverting high-level input voltage (hysteresis input).

(2) IDLE mode (IDLE)

IDLE mode is controlled by the system control register 2 (SYSCR2) and maskable interrupts. The following status is maintained during IDLE mode.

① Operation of the CPU and watchdog timer is halted. On-chip peripherals continue to operate.
② The data memory, CPU registers, PSW, and port output latches are all held in the status in effect before IDLE mode was entered.
③ The program counter holds the address of the instruction after the following instruction which started IDLE mode.

Example : Starting IDLE mode.
SET (SYSCR2). 4

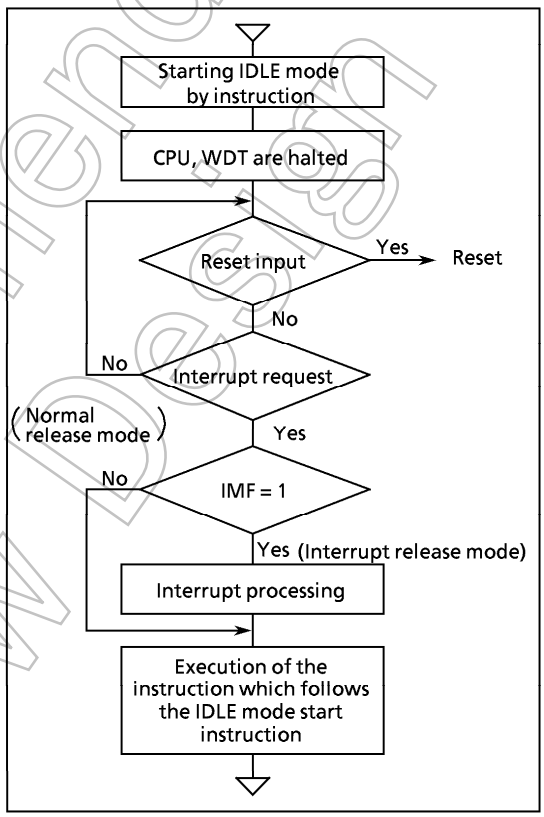

Figure 1-21. IDLE Mode

IDLE mode includes a normal release mode and an interrupt release mode. Selection is made with the interrupt master enable flag (IMF). Releasing the IDLE mode returns to NORMAL.

a. Normal release mode (IMF = "0")

IDLE mode is released by any interrupt source enabled by the individual interrupt enable flag (EF) or an external interrupt 0 ($\overline{\text{INT0}}$) request. Execution resumes with the instruction following the IDLE mode start instruction. The interrupt latch (IL) of the interrupt source for a releasing the IDLE mode cleared to "0" by load instruction.

b. Interrupt release mode (IMF = "1")

IDLE mode is released and interrupt processing is started by any interrupt source enabled with the individual interrupt enable flag (EF) or an external interrupt 0 ($\overline{\text{INT0}}$) request. After the interrupt is processed, the execution resumes from the instruction following the instruction which started IDLE mode.

IDLE mode can also be released by setting the $\overline{\text{RESET}}$ pin low, which immediately performs the reset operation.

Note: When a watchdog timer interrupt is generated immediately before the IDLE mode is started, the watchdog timer interrupt will be processed by IDLE mode will not be started.

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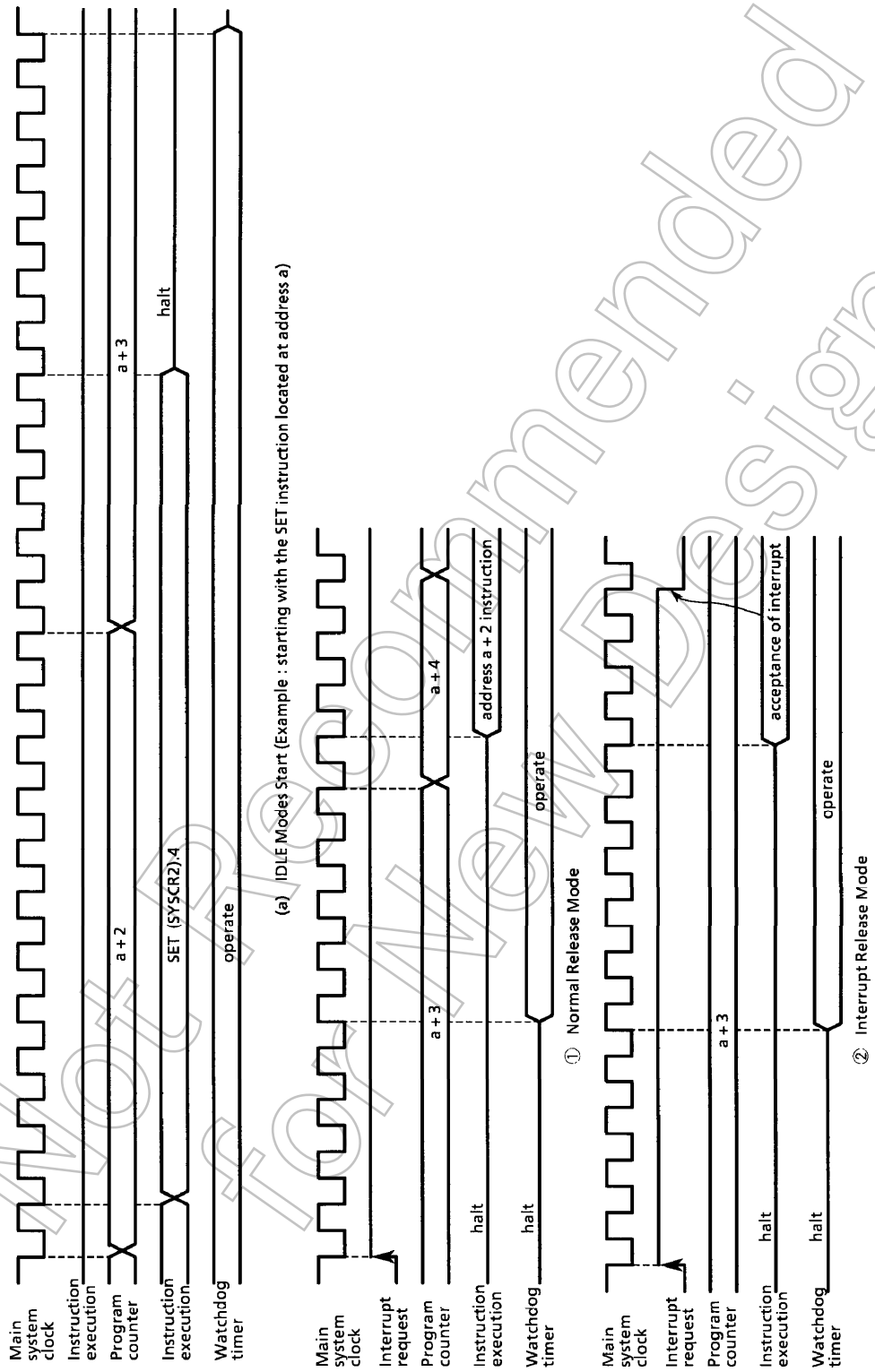


(b) IDLE Mode Release

Figure 1-22. IDLE Mode Start/Release

Not Recommended for New Design

1.9 Interrupt Controller

The 87C408/808/408L/808L each have a total of 10 interrupt sources: 4 externals and 6 internals. Nested interrupt control with priorities is also possible. Two of the internal sources are pseudo non-maskable interrupts; the remainder are all maskable interrupts.

Interrupt latches (IL) that hold the interrupt requests are provided for interrupt sources. Each interrupt vector is independent. The interrupt latch is set to "1" when an interrupt request is generated and requests the CPU to accept the interrupt. The acceptance of maskable interrupts can be selectively enabled and disabled by the program using the interrupt master enable flag (IMF) and the individual interrupt enable flags (EF). When two or more interrupts are generated simultaneously, the interrupt is accepted in the highest priority order as determined by the hardware. Figure 1-23 shows the interrupt controller.

Table 1-3. Interrupt Sources

Interrupt Source			Enable Condition	Interrupt Latch	Vector Table Address	Priority
Internal / External	(Reset)		Non-Maskable	—	$FFFE_H$	High 0
Internal	INTSW	(Software interrupt)	Pseudo non-maskable	—	$FFFC_H$	1
Internal	INTWDT	(Watchdog timer interrupt)		IL_2	$FFFA_H$	2
External	INT0	(External interrupt 0)	IMF = 1, INT0EN = 1	IL_3	$FFF8_H$	3
Internal	INTTC1	(16-bit timer / counter 1 interrupt)	$IMF \cdot EF_4 = 1$	IL_4	$FFF6_H$	4
External	INT1	(External interrupt 1)	$IMF \cdot EF_5 = 1$	IL_5	$FFF4_H$	5
Internal	INTTBT	(Time base timer interrupt)	$IMF \cdot EF_6 = 1$	IL_6	$FFF2_H$	6
External	INT2	(External interrupt 2)	$IMF \cdot EF_7 = 1$	IL_7	$FFF0_H$	7
RESERVED						
Internal	INTSIO	(Serial interface interrupt)	$IMF \cdot EF_9 = 1$	IL_9	$FFEC_H$	8
RESERVED						
RESERVED						
RESERVED						
RESERVED						
Internal	INTTC2	(16-bit timer / counter 2 interrupt)	$IMF \cdot EF_{14} = 1$	IL_{14}	$FFE2_H$	9
External	INT5	(External interrupt 5)	$IMF \cdot EF_{15} = 1$	IL_{15}	$FFE0_H$	Low 10

Not Recommended for New Design

(1) Interrupt Latches (IL_{15} to IL_2)

Interrupt latches are provided for each source, except for a software interrupt. The latch is set to "1" when an interrupt request is generated, and requests the CPU to accept the interrupt. The latch is cleared to "0" just after the interrupt is accepted. All interrupt latches are initialized to "0" during reset.

The interrupt latches are assigned to addresses 003C and $003D_H$ in the SFR. Each latch can be cleared to "0" individually by an instruction; however, the read-modify-write instruction such as bit manipulation or operation instructions cannot be used (Do not clear IL2 for a watchdog timer interrupt to "0"). Thus, interrupt requests can be canceled and initialized by the program. Note that interrupt latches cannot be directly set to "1" by any instruction. The contents of interrupt latches can be read out by an instruction. Therefore, testing interrupt requests by software is possible.

Example 1: Clears interrupt latches

```
        LDW     (IL), 1111110100111111B ; IL9 to IL6←0
```

Example 2: Reads interrupt latches

```
        LD      WA, (IL)                ; W←ILH, A←ILL
```

Example 3: Tests an interrupt latch

```
        TEST    (IL).7                  ; IL7 = 1 then jump
        JR      F, SSET
            .
            .
            .
            .
            .
SSET:
```

Not Recommended for New Design

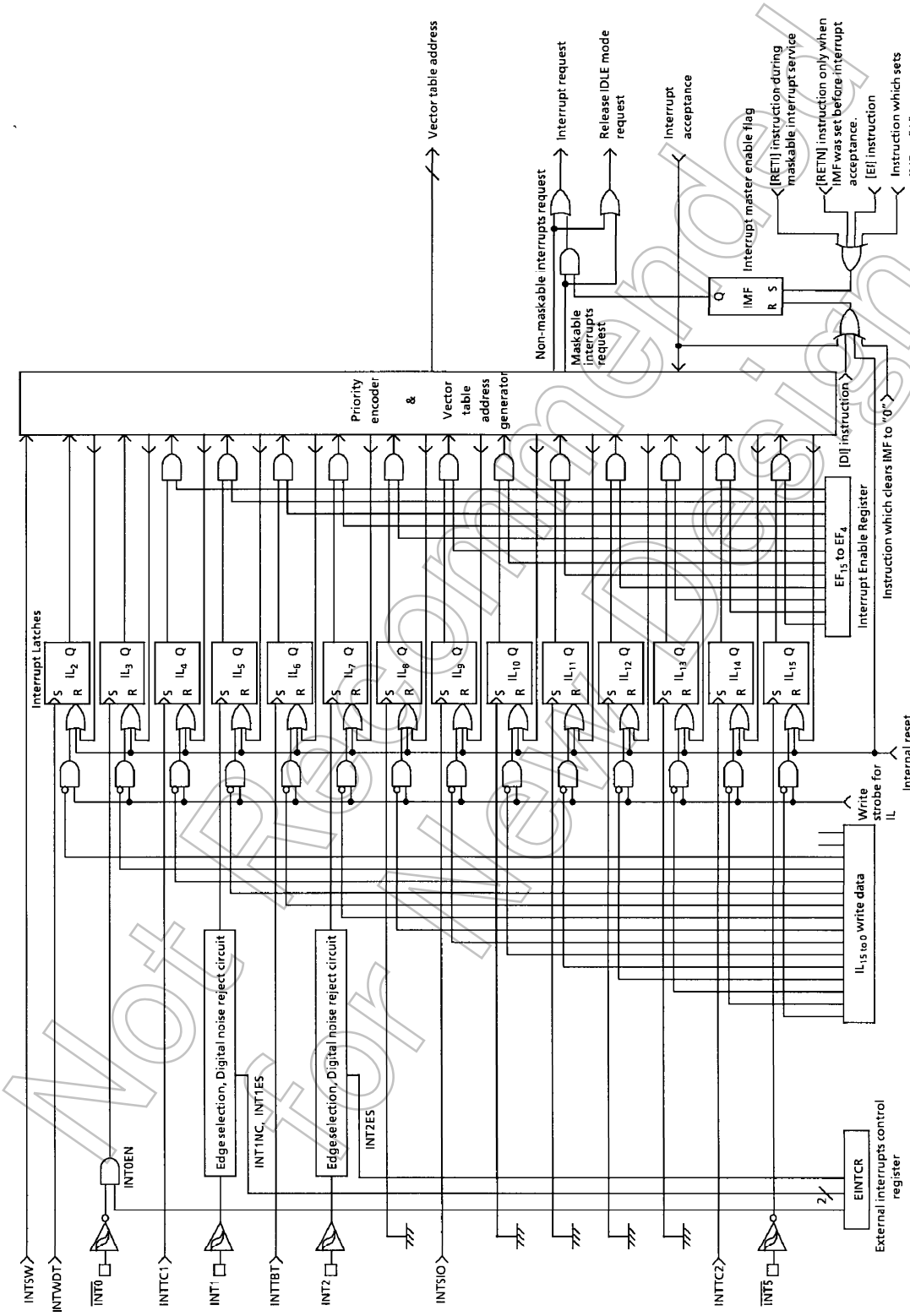


Figure 1-23. Interrupt Controller Block Diagram

Not Recommended for New Design

(2) Interrupt Enable Register (EIR)

The interrupt registers (EIR) enable and disable the acceptance of interrupts except for the pseudo non-maskable interrupts (software and watchdog timer interrupts). Pseudo non-maskable interrupts are accepted regardless of the contents of the EIR; however, the pseudo non-maskable interrupts cannot be nested more than once at the same time.

The EIR consists of an interrupt master enable flag (IMF) and individual interrupt enable flags (EF). These registers are assigned to addresses $003A_H$ and $003B_H$ in the SFR, and can be read and written by an instruction (including read-modify-write instructions such as bit manipulation instructions).

① Interrupt Master Enable Flag (IMF)

The interrupt master enable flag (IMF) enables and disables the acceptance of all interrupts. Clearing this flag to "0" disables the acceptance of all maskable interrupts. Setting to "1" enables the acceptance of interrupts.

When an interrupt is accepted, this flag is cleared to "0" to temporarily disable the acceptance of maskable interrupts. After execution of the interrupt service program, this flag is set to "1" by the maskable interrupt return instruction [RETI] to again enable the acceptance of interrupts. If an interrupt request has already occurred, interrupt service starts immediately after execution of the [RETI] instruction.

Pseudo non-maskable interrupts are returned by the [RETN] instruction. In this case, the IMF is set to "1" only when pseudo non-maskable interrupt service is started with interrupt acceptance enabled (IMF = 1). Note that IMF remains "0" when cleared by the interrupt service program.

The IMF is assigned to bit 0 at address $003A_H$ in the SFR, and can be read and written by an instruction. IMF is normally set and cleared by the [EI] and [DI] instructions, and the IMF is initialized to "0" during reset.

② Individual Interrupt Enable Flags (EF_{15} to EF_4)

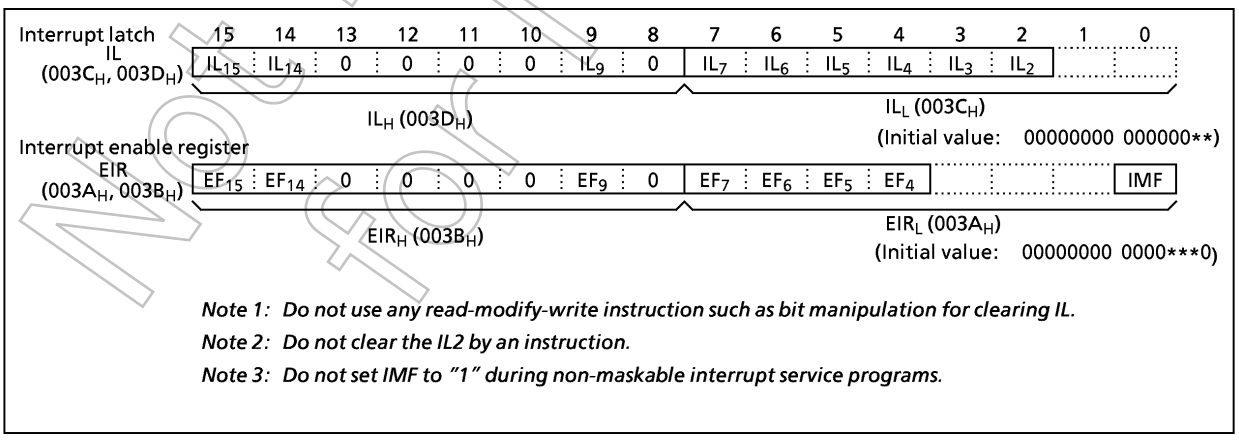
These flags enable and disable the acceptance of individual maskable interrupts, except for an external interrupt 0. Setting the corresponding bit of an individual interrupt enable flag to "1" enables acceptance of an interrupt, setting the bit to "0" disables acceptance.

Example 1: Sets EF for individual interrupt enable, and sets IMF to "1"

```
LDW     (EIR), 1100000010100001B ;  EF15, EF14, EF7, EF5, IMF←1
```

Example 2: Sets an individual interrupt enable flag to "1"

```
SET     (EIRH).1                 ;  EF9←1
```



Note 1: Do not use any read-modify-write instruction such as bit manipulation for clearing IL.

Note 2: Do not clear the IL2 by an instruction.

Note 3: Do not set IMF to "1" during non-maskable interrupt service programs.

Figure 1-24. Interrupt Latch (IL) and Interrupt Enable Register (EIR)

Not Recommended for New Design

1.9.1 Interrupt Sequence

An interrupt request is held until the interrupt is accepted or the interrupt latch is cleared to "0" by a reset or an instruction. Interrupt acceptance sequence requires 8 machine cycles after the completion of the current instruction execution. The interrupt service task terminates upon execution of an interrupt return instruction [RETI] (for maskable interrupts) or [RETN](pseudo non-maskable interrupts). Figure 1-25 shows the timing chart of interrupt acceptance and interrupt return instruction.

(1) Interrupt acceptance

Interrupt acceptance processing is as follows:

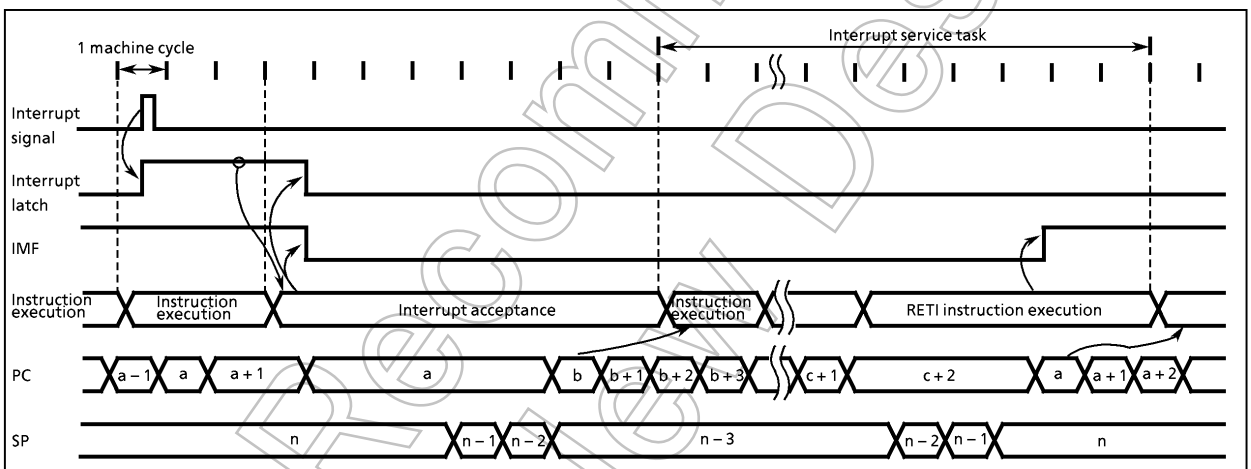
① The interrupt master enable flag (IMF) is cleared to "0" to temporarily disable the acceptance of any following maskable interrupts. When a non-maskable interrupt is accepted, the acceptance of any following interrupts is temporarily disabled.

② The interrupt latch (IL) for the interrupt source accepted is cleared o "0".

③ The contents of the program counter and the program status word are saved (pushed) onto the stack. (pushed down in order of PSW, PC_H, PC_L). The stack pointer (SP) is three decrements.

④ The entry address of the interrupt service program is read from the vector table address corresponding to the interrupt source, and the entry address is loaded to the program counter.

⑤ The instruction stored at the entry address of the interrupt service program is executed.

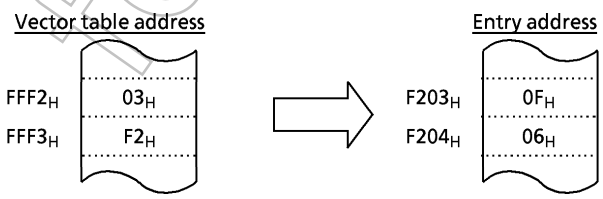


Note 1: a ; return address b ; entry address c ; address when the RETI instruction is stored

Note 2: The maximum response time from when an IL is set until an interrupt acceptance processing starts is 38/fcgck[s]. It equals to setting the IL on the first machine cycle in 10 cycles instruction execution.

Figure 1-25. Timing chart of Interrupt acceptance and Interrupt return Instruction

Example: Correspondence between vector table address for INTTBT and the entry address of the interrupt service program.



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A maskable interrupt is not accepted until the IMF is set to "1" even if a maskable interrupt of higher priority than that of the current interrupt being serviced. In case of nested interrupt service is necessary, the IMF is set to "1" in the interrupt service program. In this case, acceptable interrupt sources are selectively enabled by the individual interrupt enable flags. However, an acceptance of external interrupt 0 cannot be disabled by the EF, therefore, if disablement is necessary, either the external interrupt function must be disabled with the external interrupt control register (INT0EN) or interrupt processing must be avoided by the program. (When INT0EN = 0, the interrupt latch IL_3 is not set, therefore, the falling edge of the $\overline{INT0}$ pin input cannot be detected.)

Example 1: Disables an external interrupt 0 using INT0EN:

```
        CLR     (EINTCR). INT0EN    ; INT0EN←0
```

Example 2: Disables the processing of external interrupt 0 under the software control (using bit 0 at address $00F0_H$ as the interrupt processing disable switch):

```
PINT0:  TEST    (00F0H) . 0    ;  Returns without interrupt processing if (00F0H)0 = 1.
        JRS     T, SINT0
        RETI
SINT0:  Interrupt processing
        RETI
          ⋮
VINT0:  DW      PINT0
```

(2) General-purpose register save / restore

During interrupt acceptance processing, the program counter and the program status word are automatically saved on the stack, but not the accumulator and other registers. These registers are saved by the program if necessary. Also, when nesting multiple interrupt services, it is necessary to avoid using the same data memory area for saving registers.

The following method is used to save / restore the general-purpose registers:

① General-purpose register save / restore by register bank changeover:

General-purpose registers can be saved at high-speed by switching to a register bank that is not in use. Normally, bank 0 is used for the main task and banks 1 to 15 are assigned to interrupt service tasks. To increase the efficiency of data memory utilization, the same bank is assigned for interrupt sources which are not nested.

The switched bank is automatically restored by executing an interrupt return instruction [RETI] or [RETN]. Therefore, it is not necessary for a program to save the RBS.

Example: Register Bank Changeover

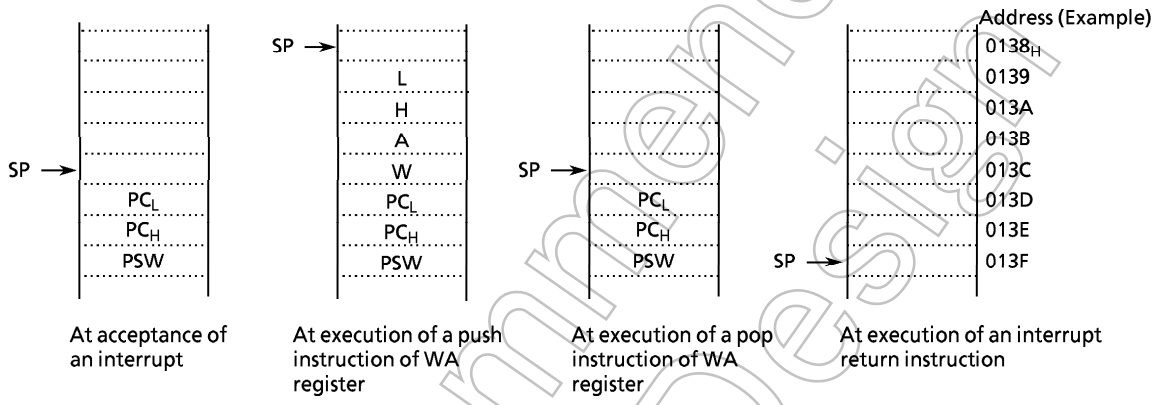
```
PINTxx :  LD      RBS, n        ;  Switches to bank n (1 μs at 8 MHz)
          Interrupt processing
          RETI                  ;  Restores bank and Returns
```

Not Recommended for New Design

② General-purpose register save / restore using push and pop instructions:
To save only a specific register, and when the same interrupt source occurs more than once, the general-purpose registers can be saved/restored using push/pop instructions.

Example: Register save using push and pop instructions

```
PINTxx :  PUSH   WA          ; Save WA register pair
          PUSH   HL          ; Save HL register pair
          Interrupt processing
          POP    HL          ; Restore HL register pair
          POP    WA          ; Restore WA register pair
          RETI               ; Return
```



③ General-purpose registers save/restore using data transfer instruction:
Data transfer instructions can be used to save only a specific general-purpose register during processing of a single interrupt.

Example: Saving / Restoring registers by data memory transfer instructions

```
PINTxx :  LD     (GSAVA), A  ; Save A register
          Interrupt processing
          LD     A, (GSAVA)  ; Restore A register
          RETI               ; Return
```

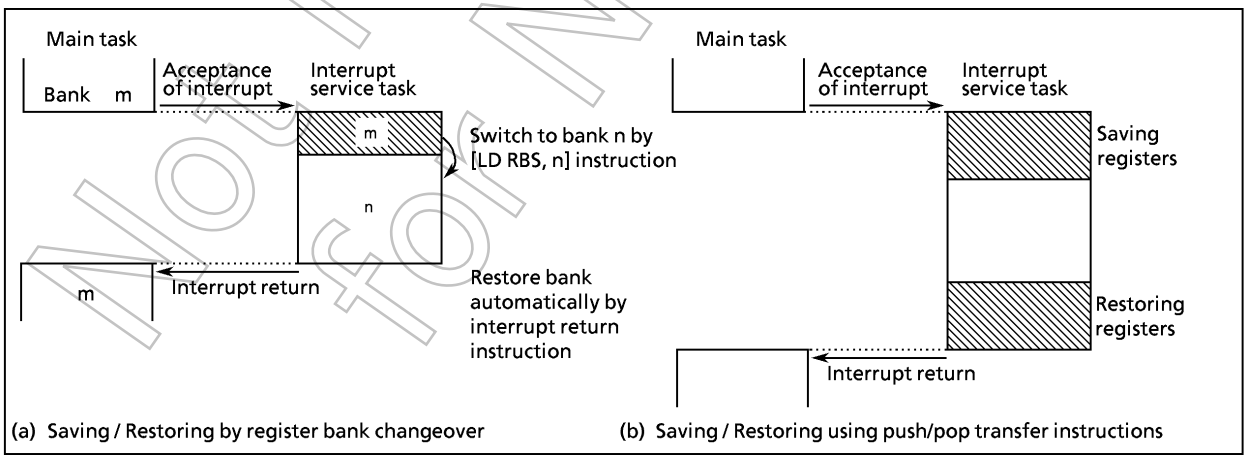


Figure 1-26. Saving / Restoring General-purpose Registers

Not Recommended for New Design

(3) Interrupt return

The interrupt return instructions perform the following operations.

[RETI] Maskable interrupt return	[RETN] Non-maskable interrupt return
① The contents of the program counter and the program status word are restored from the stack.	① The contents of the program counter and program status word are restored from the stack.
② The stack pointer is incremented 3 times.	② The stack pointer is incremented 3 times.
③ The interrupt master enable flag is set to "1".	③ The interrupt master enable flag is set to "1" only when a non-maskable interrupt is accepted in interrupt enable status. However, the interrupt master enable flag remains at "0" when so clear by an interrupt service program.

Interrupt requests are sampled during the final cycle of the instruction being executed. Thus, the next interrupt can be accepted immediately after the interrupt return instruction is executed.

Note: When the interrupt processing time is longer than the interrupt request generation time, the interrupt service is performed but not the main task.

1.9.2 Software Interrupt (INTSW)

Executing the [SWI] instruction generates a software interrupt and immediately starts interrupt processing (INTSW is highest prioritized interrupt). However, if processing of a non-maskable interrupt is already underway, executing the SWI instruction will not generate a software interrupt but will result in the same operation as the [NOP] instruction.

Note: Software interrupt generates during non-maskable interrupt processing to use SWI instruction for software break in a development tool.

Use the [SWI] instruction only for detection of the address error or for debugging.

① Address Error Detection

FF_H is read if for some cause such as noise the CPU attempts to fetch an instruction from a non-existent memory address. Code FF_H is the SWI instruction, so a software interrupt is generated and an address error is detected. The address error detection range can be further expanded by writing FF_H to unused areas of the program memory. Address-trap-reset is generated for instruction fetch from a part of RAM area (addresses 0040 to $013F_H$) or SFR area (0000 to $003F_H$).

Note: The fetch data from addresses, BF80 to $BFFF_H$ for 87C408/808/408L/808L and 87P808/808L is not "FF_H", because the outgoing test ROM is contained.

② Debugging

Debugging efficiency can be increased by placing the SWI instruction at the software break point setting address.

Not Recommended for New Design

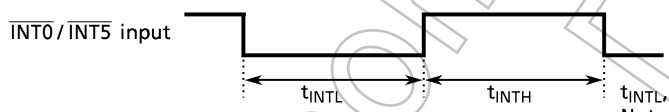
1.9.3 External Interrupts

The 87C408/808/408L/808L each have four external interrupt inputs. Two of these are equipped with digital noise rejection circuits(pulse inputs of less than a certain time are eliminated as noise).
Edge selection is also possible with INT1, INT2 pin. The $\overline{INT0}$ / P10 pin can be configured as either an external interrupt input pin or an input/output port, and is configured as an input port during reset.
Edge selection, noise rejection control and $\overline{INT0}$ / P10 pin function selection are performed by the external interrupt control register.

Table 1-4. External Interrupts

Source	Pin	Secondary function pin	Enable conditions	Edge	Digital noise rejection circuit
INT0	$\overline{INT0}$	P10	IMF = 1, INT0EN = 1	Falling edge	– (Hysteresis input)
INT1	INT1	P11	IMF · EF_5 = 1	Falling edge or Rising edge	Pulses of less than 15/fc or 63/fc[s] are eliminated as noise. Pulses equal to or more than 48/fc [s] or 192/fc [s] are regarded as signals.
INT2	INT2	P12 / TC1	IMF · EF_7 = 1		Pulses of less than 7/fc[s] are eliminated as noise. Pulses equal to or more than 24/fc [s] are regarded as signals.
INT5	$\overline{INT5}$	P76 / $\overline{STOP}$	IMF · EF_{15} = 1	Falling edge	– (Hysteresis input)

Note 1: The noise rejection function is also affected to detect the edge of Timer / Counter input (TC1 pin).
Note 2: The pulse width (both "H" and "L" level) for input to the $\overline{INT0}$ and $\overline{INT5}$ pins must be over 1 machine cycle.



t_{INTL}, t_{INTH} > tcyc
Note: tcyc = 4/fcgck [s] at NORMAL, IDLE mode

Note 3: If a noiseless signal is input to the external interrupt pin in the NORMAL or IDLE mode, the maximum time from the edge of input signal until the IL is set is as follows:
① INT1 pin 49/fc [s] (at INT1NC = 1), 193/fc [s] (at INT1NC = 0)
② INT2 pin 25/fc [s]
Note 4: When INT0EN = 0, the interrupt latch IL_3 is not set even if the falling edge of $\overline{INT0}$ pin input is detected.
Note 5: When high-impedance is specified for port output in STOP mode, port input is forcibly fixed to low level internally. Thus, interrupt latches of external interrupt inputs except P76 ($\overline{STOP}$ / $\overline{INT5}$) which are also used as ports may be set to "1". To specify high-impedance for port output in STOP mode, first disable inteerupt service(IMF = 0), activate stop mode. After releasing stop mode, clear interrupt latches using load instruction, then, enable interrupt service.

Example: Activating stop mode

```
LD    (SYSCR1) , 01000000B        ; OUTEN←0 (Specifies High-impedance)
DI                                ; IMF←0
SET   (SYSCR1) , STOP             ; STOP←1 (Activates STOP mode)
LDW   (IL) , 111111101010111B     ; IL7, 5, 3←0 (Clears interrupt latches)
EI                                ; IMF←1
```

Not Recommended for New Design

EINTCR (0037_H)

7	6	5	4	3	2	1	0
INT1 NC	INT0 EN				INT2 ES	INT1 ES	

(Initial value: 00** *00*)

INT1NC	INT1 noise reject time select	0: Pulses of less than 63/fc [s] are eliminated as noise 1: Pulses of less than 15/fc [s] are eliminated as noise	R/W
INT0EN	P10 / $\overline{INT0}$ pin configuration	0: P10 input / output port 1: $\overline{INT0}$ pin (Port P10 should be set to an input mode.)	
INT2 ES INT1 ES	INT2, INT1 edge select	0: Rising edge 1: Falling edge	

*Note: fc ; clock [Hz] * ; Don't care*

Figure 1-27. External Interrupt Control Register

1.10 Watchdog Timer (WDT)

The Watchdog Timer rapidly detects the CPU malfunction such as endless looping caused by noise or the like, and resumes the CPU to the normal state.

The Watchdog Timer signal for detecting malfunction can be selected either a reset output or a non-maskable interrupt request. However, selection is possible only once after reset.

After reset, the signal is initialised to the reset output.

When the Watchdog Timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals.

Not Recommended for New Design

1.10.1 Watchdog Timer Configuration

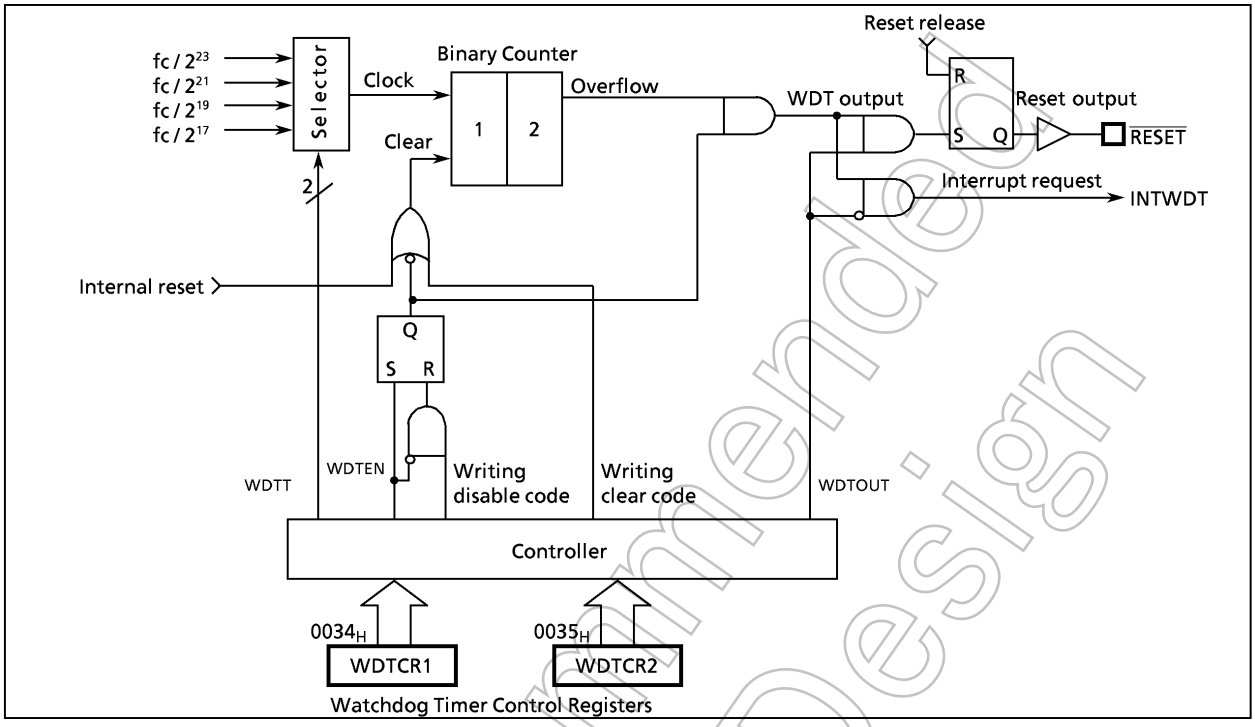


Figure 1-28. Watchdog Timer Configuration

1.10.2 Watchdog Timer Control

Figure 1-29 shows the Watchdog Timer control registers. The Watchdog Timer is automatically enabled after reset.

(1) Malfunction detection methods using the Watchdog Timer

The CPU malfunction is detected as follows.

① Setting the detection time, selecting output, and clearing the binary counter.

② Repeatedly clearing the binary counter within the setting detection time.

If the CPU malfunction occurs for any cause, the Watchdog Timer output will become active at the rising of an overflow from the binary counters unless the binary counters are cleared. At this time, when WDTOUT = 1 a reset is generated, which drives the $\overline{\text{RESET}}$ pin to reset the internal hardware. When WDTOUT = 0, a Watchdog Timer interrupt (INTWDT) is generated.

The Watchdog Timer temporarily stops counting in the STOP mode including warm-up or IDLE mode, and automatically restarts (continues counting) when the STOP / IDLE mode is released.

Example: Sets the Watchdog Timer detection time to 2^{21}/fc[s] and resets the CPU malfunction.

```
                LD    (WDTCR2), 4EH          ; Clears the binary counters
                LD    (WDTCR1), 00001101B    ; WDTT←10, WDTOUT←1
Within WDT      LD    (WDTCR2), 4EH          ; Clears the binary counters
detection                                      (Always clear immediately after changing WDTT)
time            :
                LD    (WDTCR2), 4EH          ; Clears the binary counters
Within WDT      :
detection
time            :
                LD    (WDTCR2), 4EH          ; Clears the binary counters
                :
```

Not Recommended for New Design

Watchdog Timer Control Register 1

WDTCR1 (0034_H)

7	6	5	4	3	2	1	0
				WDT EN	WDTT		WDT OUT

(Initial value **** 1001)

WDTEN	Watchdog timer enable / disable	0: Disable (It is necessary to write the disable code to WDTCR2.) 1: Enable	write only
WDTT	Watchdog timer detection time	00: 2^{25} / fc [s] 01: 2^{23} / fc 10: 2^{21} / fc 11: 2^{19} / fc	
WDTOUT	Watchdog timer output select	0: Interrupt request 1: Reset output	

Note 1: WDTOUT cannot be set to "1" by program after clearing WDTOUT to "0".
*Note 2: fc ; clock[Hz] * ; Don't care*
Note 3: WDTCR1 is a write-only register and must not be used with any of read-modify-write instructions.
Note 4: Disable the Watchdog Timer or clear the counter just before switching to STOP mode. When the counter is cleared just before switching to STOP mode, clear the counter again subsequently to releasing STOP mode.

Watchdog Timer Control Register 2

WDTCR2 (0035_H)

7	6	5	4	3	2	1	0

(Initial value **** ****)

WDTCR2	Watchdog Timer control code write register	$4E_H$: Watchdog Timer binary counter clear (clear code) $B1_H$: Watchdog Timer disable (disable code) Others: Invalid	write only

Note 1: The disable code is invalid unless written when WDTEN = 0.
*Note 2: * ; Don't care*
Note 3: Since WDTCR2 is a write-only register, read-modify-write instructions (e.g., bit manipulating instructions such as SET of CLR and arithmetic instructions such as AND or OR) cannot be used for read/write to this register.
Note 4: To clear the binary counter doesn't initialize the source clock, therefore, it is recommended to clear the binary counter within 3/4 of the detection period.

Figure 1-29. Watchdog Timer Control Registers

(2) Watchdog Timer Enable

The Watchdog Timer is enabled by setting WDTEN (bit 3 in WDTCR1). WDTEN is initialized to "1" during reset, so the Watchdog Timer operates immediately after reset is released.

(3) Watchdog Timer Disable

The Watchdog Timer is disabled by writing the disable code ($B1_H$) to WDTCR2 after clearing WDTEN (bit 3 in WDTCR1) to "0". The Watchdog Timer is not disabled if this procedure is reversed and the disable code is written to WDTCR2 before WDTEN is cleared to "0". During disabling the Watchdog Timer , the binary counters are cleared to "0".

Example: Disables Watchdog Timer

```
LDW (WDTCR1) , 0B101H      ;  WDTEN←0, WDTCR2←disable code
```

Table 1-5. Watchdog Timer Detection Time

Detection time	
WDTT	fc = 8 MHz
00	4.194 s
01	1.048 s
10	262.1 ms
11	65.5 ms

Not Recommended for New Design

1.10.3 Watchdog Timer Interrupt (INTWDT)

This is a pseudo non-maskable interrupt which can be accepted regardless of the contents of the EIR. If a Watchdog Timer interrupt or a software interrupt is already accepted, however, the new Watchdog Timer interrupt waits until the previous interrupt processing is completed (the end of the [RETN] instruction execution).

The stack pointer (SP) should be initialized before using the Watchdog Timer output as an interrupt source with WDTOUT.

```
Example:  Watchdog Timer interrupt setting up.
          LD   SP, 013FH              ;  Sets the stack pointer
          LD   (WDTCR1) , 00001000B   ;  WDTOUT←0
```

1.10.4 Watchdog Timer Reset

If the Watchdog Timer output becomes active, a reset is generated, which drives the $\overline{RESET}$ pin low to reset the internal hardware. The reset output time is 12/fcgck to 16/fcgck [s] (1.5 to 2.0 μs at 8 MHz, 3.0 to 4.0 μs at 4 MHz). The $\overline{RESET}$ pin is sink open drain input / output with pull-up resistor.

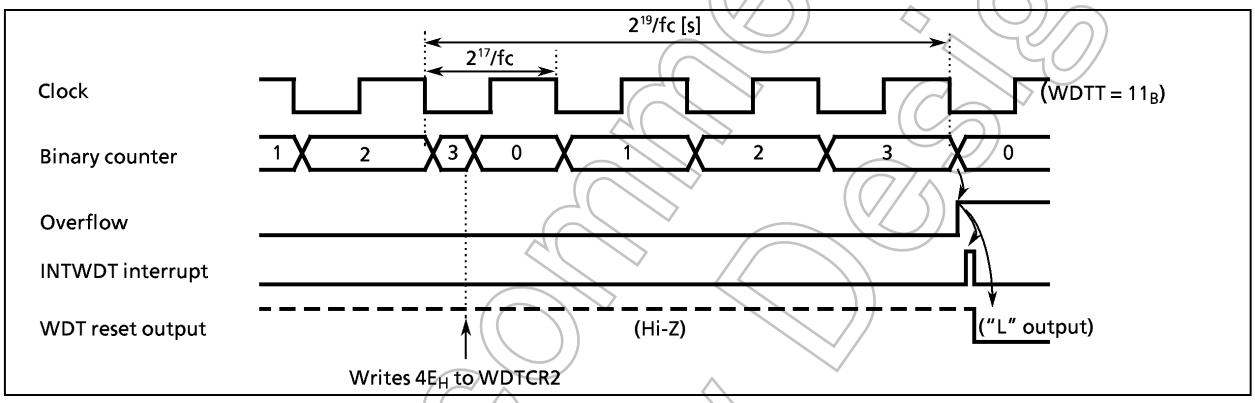


Figure 1-30. Watchdog Timer Interrupt / Reset

1.11 Reset Circuit

TMP87C408/808/408L/808L each have four types of reset generation procedures: an External reset input, an Address trap reset, a Watchdog Timer reset and a System clock reset.

Table 1.8 shows on-chip hardware initialization by reset action.

The internal source reset circuit (Watchdog Timer reset, Address trap reset, and System clock reset) is not initialized when power is turned on. Thus, output from the $\overline{RESET}$ pin may go low (maximum 16/fc[s] (2 μs at 8 MHz, 4 μs at 4 MHz)).

Table 1-8. On-chip Hardware Initialization by Reset Action

On-chip Hardware	Initial Value	On-chip Hardware	Initial Value
Program counter (PC)	$(FFFF_H)$ · $(FFFE_H)$	Prescaler and Divider of Timing generator	0
Register bank selector (RBS)	0	Watchdog Timer	Enable
Jump status flag (JF)	1		
Interrupt master enable flag (IMF)	0	Output latches of input/output port	Refer to I/O port circuitry
Interrupt individual enable flags (EF)	0		
Interrupt latches (IL)	0	Control register	Refer to control registers

Not Recommended for New Design

1.11.1 External Reset Input

The $\overline{RESET}$ pin contains a hysteresis input with an internal pull-up resistor. When the $\overline{RESET}$ pin is held at low for at least 3 machine cycles (12/fcgck [s]) with the power supply voltage within the operating voltage range and oscillation stable, a reset is applied and the internal state is initialized.
When the $\overline{RESET}$ pin input goes high, the reset operation is released and the program execution starts at the vector address stored at addresses FFFE to $FFFF_H$.

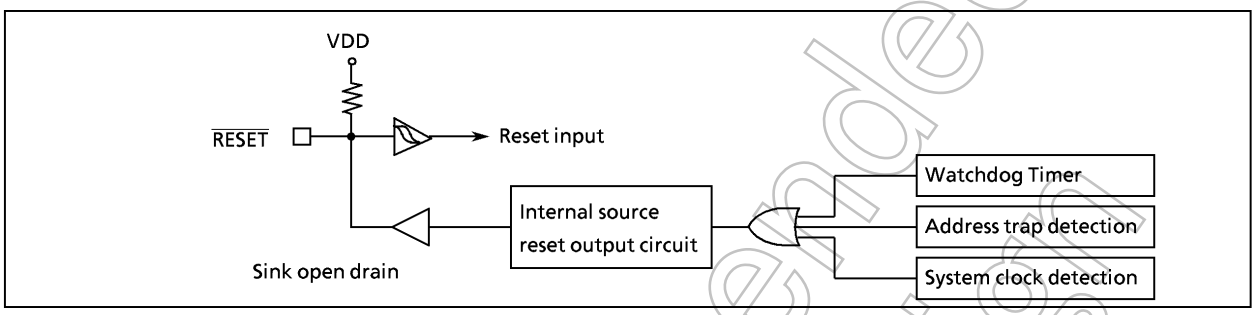


Figure 1-31. Reset Circuit

1.11.2 Address Trap Reset

An Address trap reset is one of fail-safe function that detects CPU malfunction caused by noise or the like. If the CPU attempts to fetch an instruction from a part of RAM or SFR, an internal reset will be generated. Then, the $\overline{RESET}$ pin output will go low. The reset time is 12/fcgck to 16/fcgck [s] (1.5 to 2.0 μs at 8MHz, 3.0 to 4.0 μs at 4 MHz).

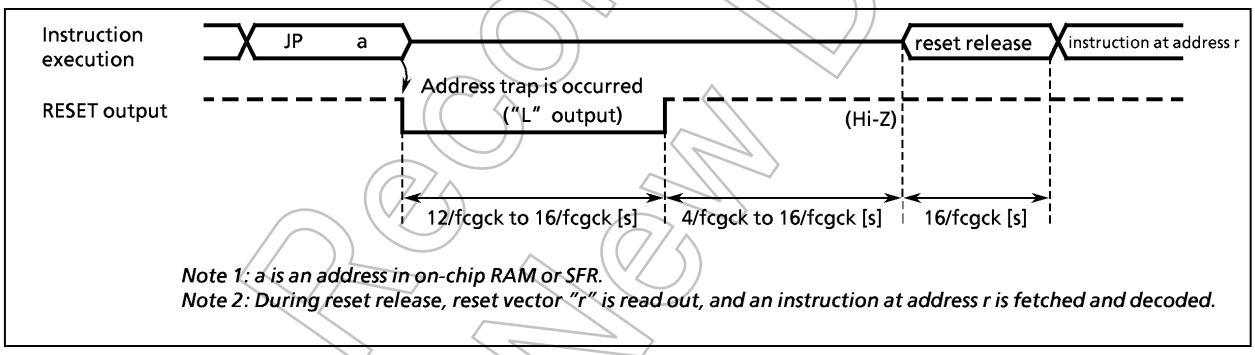


Figure 1-32. Address Trap Reset

1.11.3 Watchdog Timer Reset

Refer to Section "1.10 Watchdog Timer".

1.11.4 System Clock Reset

Clearing XEN to "0" stops a system clock, and causes CPU to deadlock. This can be prevented by automatically generating a reset signal whenever XEN = 0 is detected to continue the oscillation. Then the $\overline{RESET}$ pin output goes low . The reset time is 12/fcgck to 16/fcgck [s] (1.5 to 2.0 μs at 8MHz, 3.0 to 4.0 μs at 4 MHz).

Not Recommended for New Design

2. On-Chip Peripherals Functions

2.1 Special function register (SFR) and Data Buffer Register (DBR)

The TLCS-870 Series uses the memory mapped I/O system, and all peripheral control and data transfers are performed through the special function registers (SFR) and data buffer registers (DBR).

The SFR are mapped to addresses 0000 to $003F_H$, and the DBR to addresses 0FF0 to $0FF7_H$. Figure 2-1 shows the 87C408/808/408L/808L SFR, DBR.

Address	Read	Write
0000_H	reserved	
01	P1 port	
02	reserved	
03	〃	
04	〃	
05	〃	
06	P6 port	
07	P7 port	
08	reserved	
09	〃	
0A	–	–
0B	–	P1CR (P1 port I/O control)
0C	–	P6CR (P6 port I/O control)
0D	–	P7CR1 (P7 port I/O control 1)
0E	ADCCR (A/D converter control)	
0F	ADCDR (A/D conv. result)	–
10	–	$TREG1A_L$ (Timer register 1A)
11	–	$TREG1A_H$
12	$TREG1B_L$ (Timer register 1B)	
13	$TREG1B_H$	
14	–	TC1CR (TC1 control)
15	–	TC2CR (TC2 control)
16	–	$TREG2_L$ (Timer register 2)
17	–	$TREG2_H$
18	reserved	
19	〃	
1A	〃	
1B	〃	
1C	〃	
1D	〃	
1E	〃	
1F	〃	

Address	Read	Write
0020_H	SIOSR (SIO status)	SIOCR1 (SIO1 control)
21	–	SIOCR2
22	reserved	
23	〃	
24	〃	
25	〃	
26	〃	
27	P7CR2 (P7 port I/O control 2)	
28	reserved	
29	〃	
2A	〃	
2B	〃	
2C	〃	
2D	〃	
2E	〃	
2F	STOPCR (Key Wake-up control)	
30	CGCR (Clock Gear control)	
31	reserved	
32	〃	
33	〃	
34	–	WDTCR1 (Watchdog Timer control)
35	–	WDTCR2
36	TBTCR (TBT / TG / DVO control)	
37	EINTCR (External interrupt control)	
38	SYSCR1 (System control)	
39	SYSCR2	
3A	EIR_L (Interrupt enable register)	
3B	EIR_H	
3C	IL_L (Interrupt latch)	
3D	IL_H	
3E	reserved	
3F	PSW	RBS (Register bank selector)

(a) Special Function Register

Address	Read	Write
$0F80_H$	reserved	
〃	〃	
0FEF	〃	
0FF0	SIO transmit and receive data buffer (8 byte)	
F1		
F2		
F3		
F4		
F5		
F6		
F7		
0FF8	reserved	
to	〃	
0FFF		

(b) Data Buffer Registers

Note 1: Do not access reserved areas by the program.

Note 2: – ; cannot be accessed.

Note 3: When defining address $003F_H$ with assembler symbols, use GPSW and GRBS.

Note 4: Write-only registers and interrupt latches cannot use the read-modify-write instructions (bit manipulation instructions such as SET, CLR, etc. and logical operation instructions such as AND, OR, etc.)

Note 5: PSW ; Program Status Word

Figure 2-1. SFR & DBR

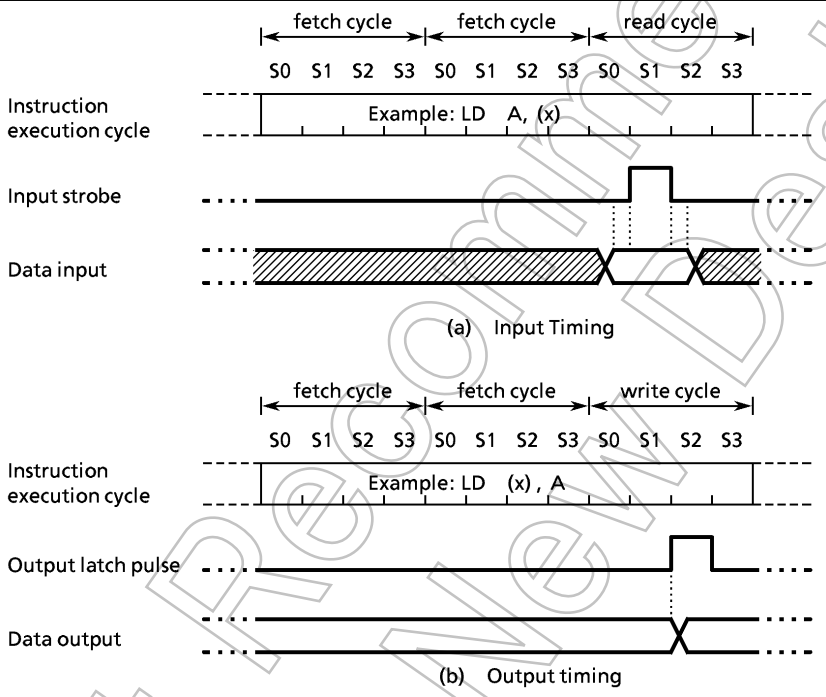
Not Recommended for New Design

2.2 I/O Ports

The 87C408/808/408L/808L each have 3 ports, 22 pin input / output ports.

① P1 port ; 8-bit I/O port (External interrupt input, Timer/Counter input/output, and Divider output)
② P6 port ; 8-bit I/O port (Analog input, STOP mode release input)
③ P7 port ; 6-bit I/O port (Serial interface, External interrupt, Timer/Counter input / output, and Analog reference power supply)

Each output port contains a latch, which holds the output data. All input ports do not have latches, so the external input data should either be held externally until read or reading should be performed several times before processing. Figure 2-2 shows input / output timing examples.
External data is read from an I/O port in the S1 state of the read cycle during execution of the read instruction. This timing can not be recognized from outside, so that transient input such as chattering must be processed by the program. Output data output changes in the S2 state of the write cycle during execution of the instruction which writes to an I/O port.



Note: The positions of the read an write cycles may vary, depending on the instruction.

Figure 2-2. Input / Output Timing (Example)

When reading an I/O port except programmable I/O ports, whether the pin input data or the output latch contents are read depends on the instructions, as shown below:

(1) Instructions that read the output latch contents

① XCH r, (src)
② SET / CLR / CPL (src).b
③ SET / CLR / CPL (pp).g
④ LD (src).b, CF
⑤ LD (pp).b,CF
⑥ ADD / ADDC / SUB / SUBB / AND / OR / XOR (src), n
⑦ (src) side of ADD/ADDC/SUB/SUBB/AND/OR/XOR (src), (HL)

(2) Instructions that read the pin input data

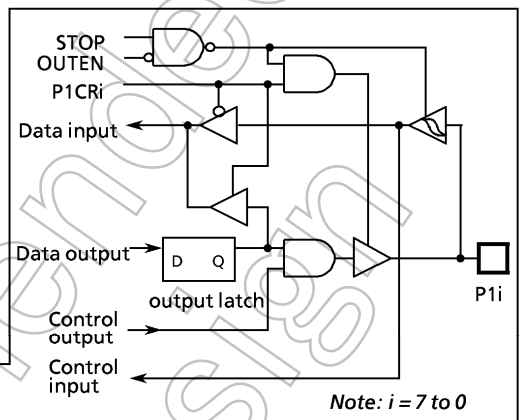
Instructions other than the above (1) and (HL) side of ADD/ADDC/SUB/SUBB/AND/OR/XOR (scr), (HL)

Not Recommended for New Design

2.2.1 Port P1(P17 to P10)

Port P1 is an 8-bit input / output port which can be configured as an input or an output for each bit individually. Input / output mode is specified by the port P1 input/output control register (P1CR). During reset, the P1CR is initialized to "0", which configures port P1 as an input. The P1 output latches are also initialized to "0".

Port P1 is also used as an External interrupt input, a Timer / Counter input, and a Divider output. When used as secondary function pin, the input pins should be set to the input mode, and the output pins should be set to the output mode and beforehand the output latch should be set to "1". It is recommended that pins P11 and P12 should be used as External interrupt inputs, Timer / Counter input, or input ports. The interrupt latch is set at the rising or falling edge of the output when used as output ports. Pin P10 can be configured as either an input / output ports with INT0EN or an External interrupt input. During reset, pin P10 is configured as an input port.



	7	6	5	4	3	2	1	0	
P1 (0001_H)	P17	P16	P15 TC2	P14 $\overline{PPG}$	P13 $\overline{DVO}$	P12 INT2 TC1	P11 INT1	P10 $\overline{INT0}$	(Initial value: 0000 0000)
P1CR ($000B_H$)									(Initial value: 0000 0000)

P1CR	I/O control for port P1 (set for each bit individually)	0: Input mode 1: Output mode	Write only

Note: P1CR is a write-only register and must not be used with any of the read-modify-write instructions.

Figure 2-3. Port 1 and P1CR

Example: Sets P17, P16 and P14 as output ports, P13 and P11 as input ports, and the others as function pins. Internal output data is "1" for the P17 and P14 pins, and "0" for the P16 pin.

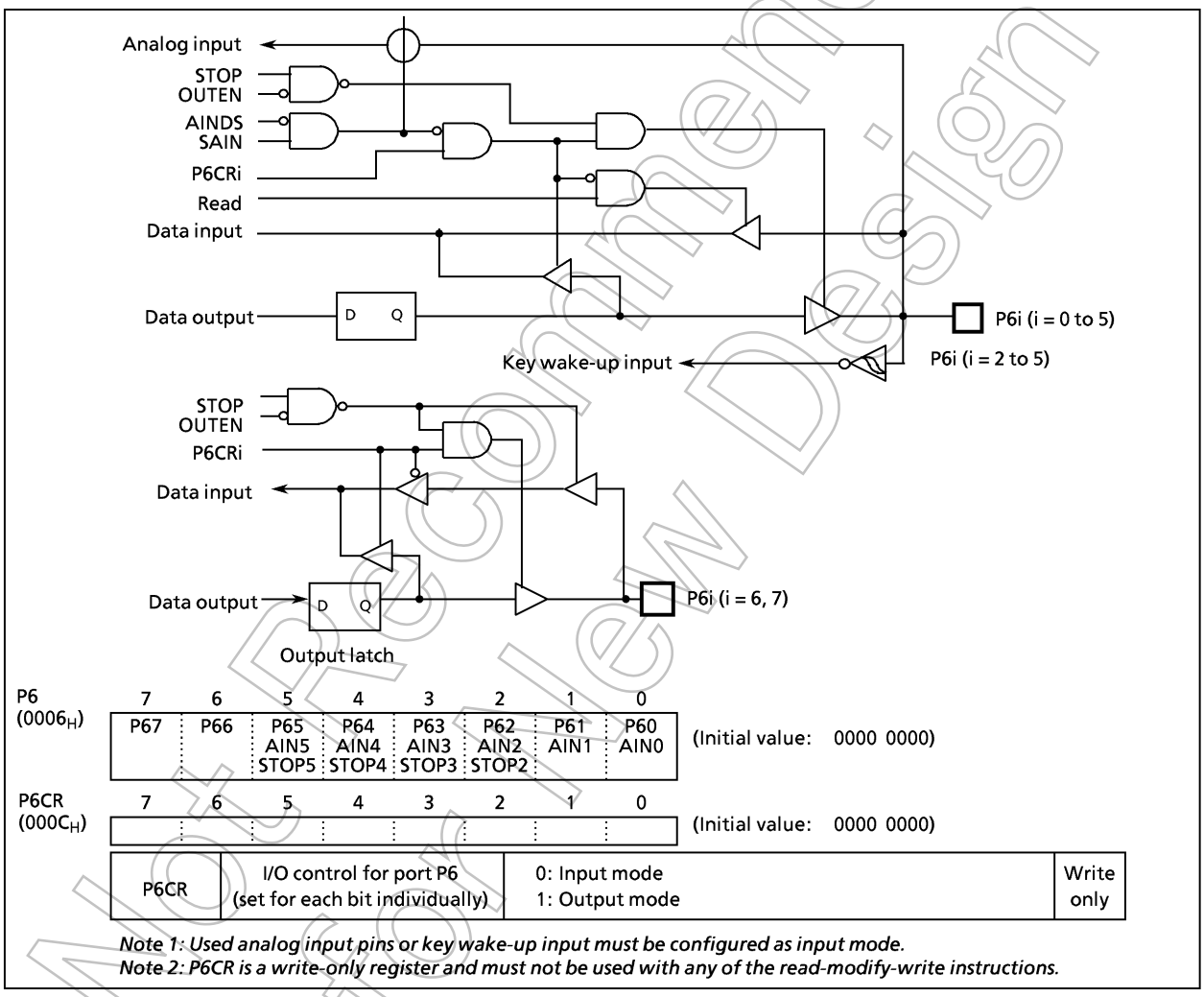
```
LD    (EINTCR), 01000000B      ;  INT0EN←1
LD    (P1), 10111111B          ;  P17←1, P14←1, P16←0
LD    (P1CR), 11010000B
```

Note: The port set to an input mode reads pin input state. When used with input/output modes, output latch contents of the port set to an input mode may be placed by execution of bit operate instruction.

Not Recommended for New Design

2.2.2 Port P6 (P67 to P60)

Port P6 is an 8-bit general-purpose input/output port which can be configured as an input or an output for each bit individually. P60 to P65 are also used as Analog inputs and P62 to P65 are also used as key wake-up inputs. Input / output mode is specified by port P6 input/output control register (P6CR) and AINDS (bit 4 in ADCCR). During reset, P6CR is set to "0", AINDS is set to "1", and port P6 is in input mode. During reset, the output latches of port P6 is initialized to "0". P6CR is write-only register. When port P6 is not used as analog input, it can be used input / output port. However output instructions must not be performed to maintain the precision at using A/D converter. When the input instruction is executed to port P6 during using A/D converter, "0" is read into the pin that selects Analog input, and "1" or "0" is read into the pin that does not select Analog input, depending on the input level of pins. In the case of using port P6 as key wake-up inputs, please refer to Section "2.9 Key wake up".



Note 1: Used analog input pins or key wake-up input must be configured as input mode.
Note 2: P6CR is a write-only register and must not be used with any of the read-modify-write instructions.

Figure 2-4. Port P6 and P6CR

Note: The port set to an input mode reads pin input state. When used with input/output modes, output latch contents of the port set to an input mode may be placed by execution of bit operate instruction.

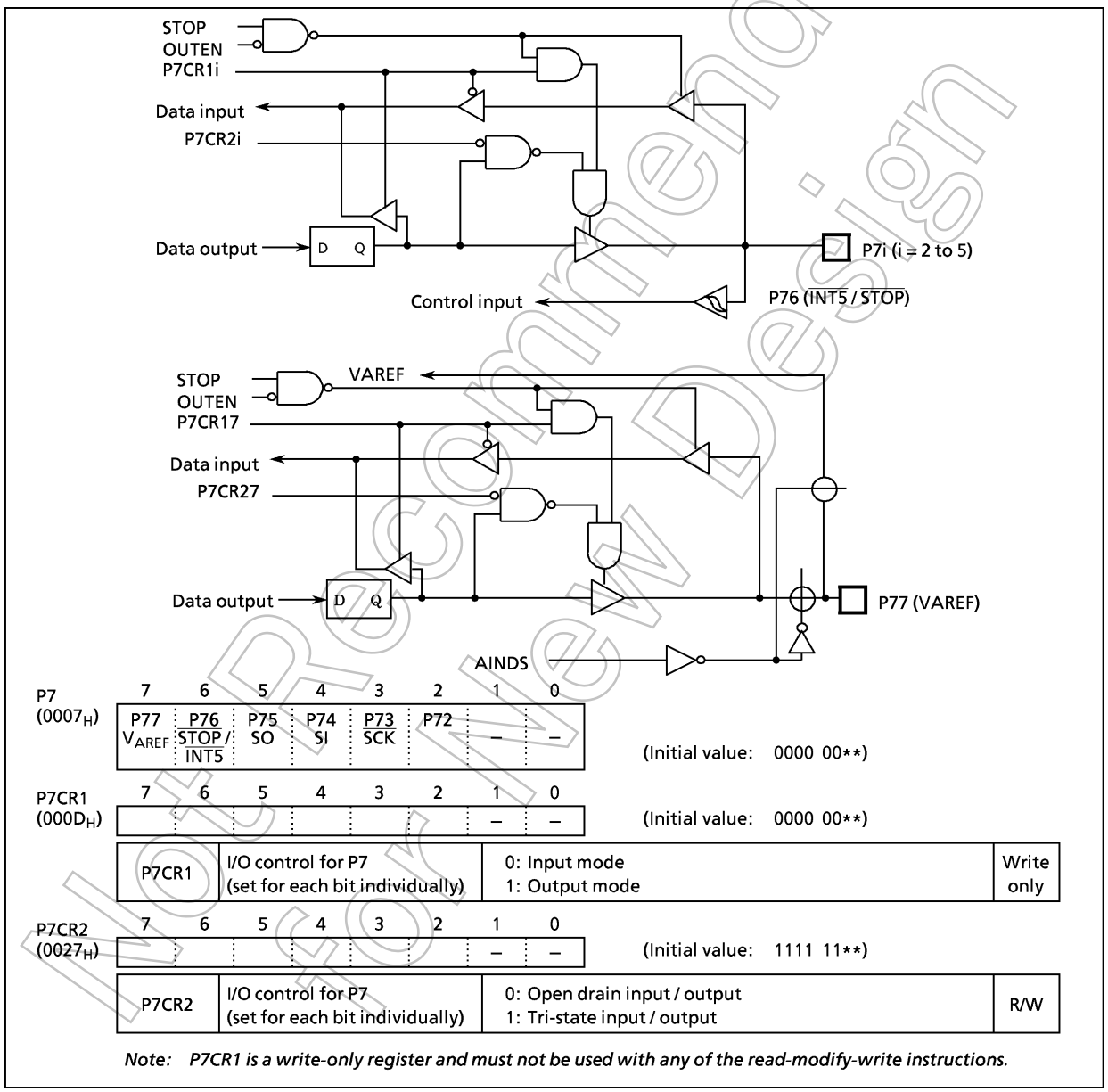
Not Recommended for New Design

2.2.3 Port P7 (P77 to P72)

Port P7 is a 6-bit general-purpose input / output port which can be configured as either input or output for each bit individually. Input / output mode is specified by port 7 input / output control register 1 (P7CR1). Input/output circuit is specified by port 7 input / output control register 2 (P7CR2). During reset, P7CR1 is cleared to "0", and port P7 is configured as an input mode. The output latches are initialized to "0". P7CR1 is write-only register. It is recommended that pin P76 should be used as an external interrupt input, a STOP mode release signal input, or an input port.

If used as an output port, the interrupt latch is set on the falling edge of the output pulse.

P77 is used as an analog reference power suppy pin (VAREF) if an analog input is enabled (AINDS = 0).



Note: P7CR1 is a write-only register and must not be used with any of the read-modify-write instructions.

Figure 2-5. Port P7 and P7CR

Not Recommended for New Design

Note 1: The port set to an input mode reads pin input state. When used with input/output modes, output latch contents of the port set to an input mode may be placed by execution of bit operate instruction.
Note 2: In case of using port P65 to P62 as key wake-up input, P76 pin must be used as input only (in cluding $\overline{\text{INT5}}$/$\overline{\text{STOP}}$), must not be used as output port.
*Note 3: * ; Don't Care*

Example: The lower 2-bit of Port P7 is set to an output port and the others are set to an input port.

```
LD    (P7CR1), 0FH      ;   P7CR1←00001111
```

Not Recommended for New Design

2.3 Time Base Timer (TBT)

The time-base timer is used to generate the base time for key scan and dynamic display processing. For this purpose, it generates a time-base timer interrupt (INTTBT) at predetermined intervals.
This interrupt is generated beginning with the first rising edge of the source clock (the timing generator's divider output selected by TBTCK) after the time-base timer is enabled. Note that since the divider cannot be cleared by a program, the first interrupt only may occur earlier than the set interrupt period. (See Figure 2-6, (b).)
When selecting the interrupt frequency, make sure the time-base timer is disabled. (Do not change the selected interrupt frequency when disabling the active timer either.) However, you can select the interrupt frequency simultaneously when enabling the timer.

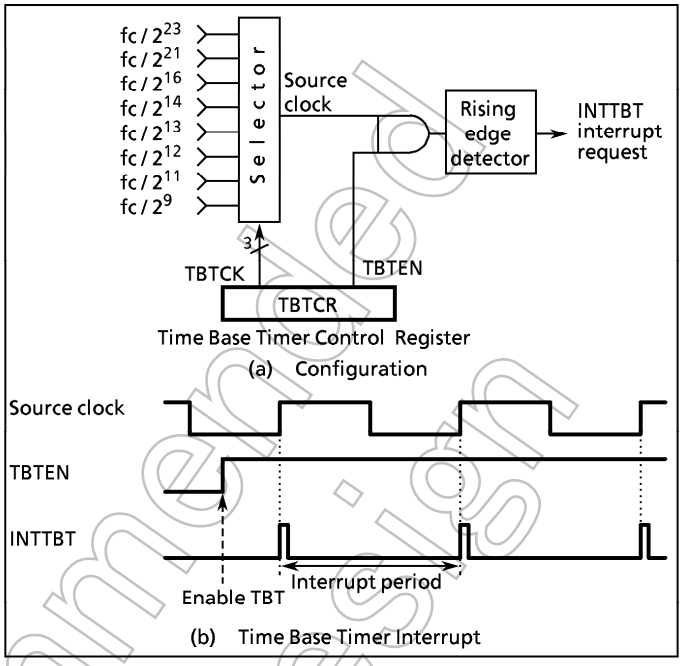


Figure 2-6. Time Base Timer

TBTCR (0036_H)

7	6	5	4	3	2	1	0
(DVOEN)	(DVOCK)		0	TBTEN	TBTCK		

(Initial value: 0**0 0***)

TBTEN	Time Base Timer enable/disable	0: Disable 1: Enable	R/W
TBTCK	Time base timer interrupt frequency select	000: fc / 2^{23} [Hz] 001: fc / 2^{21} 010: fc / 2^{16} 011: fc / 2^{14} 100: fc / 2^{13} 101: fc / 2^{12} 110: fc / 2^{11} 111: fc / 2^{9}	

*Note 1: fc ; clock [Hz], * ; Don't care*
Note 2: The fourth bit in TBTCR must be to "0".

Figure 2-7. Time Base Timer Control Register

Table 2-1. Time Base Timer Interrupt Frequency [Hz]

TBTCK	NORMAL, IDLE mode (at fc = 8 MHz)
000	0.95
001	3.81
010	122.07
011	488.28
100	976.56
101	1953.12
110	3906.25
111	15625

Not Recommended for New Design

2.4 Divider Output ($\overline{DVO}$)

A 50% duty pulse can be output using the Divider output circuit, which is useful for piezo-electric buzzer drive. Divider output is from pin P13 ($\overline{DVO}$). The P13 output latch should be set to "1" and then the P13 should be configured as an output mode.

TBTCR (0036_H)

7	6	5	4	3	2	1	0
DVOEN	DVOCK		0	(TBTEN)	(TBTCK)		

(Initial value: 0**0 0***)

DVOEN	Divider output enable/disable	0: Disable 1: Enable	R/W
DVOCK	Divider output ($\overline{DVO}$ pin) frequency selection	00: fc / 2^{13} [Hz] 01: fc / 2^{12} 10: fc / 2^{11} 11: fc / 2^{10}	

*Note: fc ; High-frequency clock [Hz], * ; Don't care*

Figure 2-8. Divider Output Control Register

Example: 1 kHz pulse output (at fc = 8 MHz)

```
SET     (P1).3              ; P13 output latch ←1
LD      (P1CR), 00001000B   ; Configures P13 as an output mode
LD      (TBTCR), 10000000B  ; DVOEN←1, DVOCK←00
```

Table 2-2. Frequency of Divider Output [kHz]

DVOCK	At fc = 4 MHz	At fc = 8 MHz
00	0.512	0.976
01	1.024	1.953
10	2.048	3.906
11	4.096	7.812

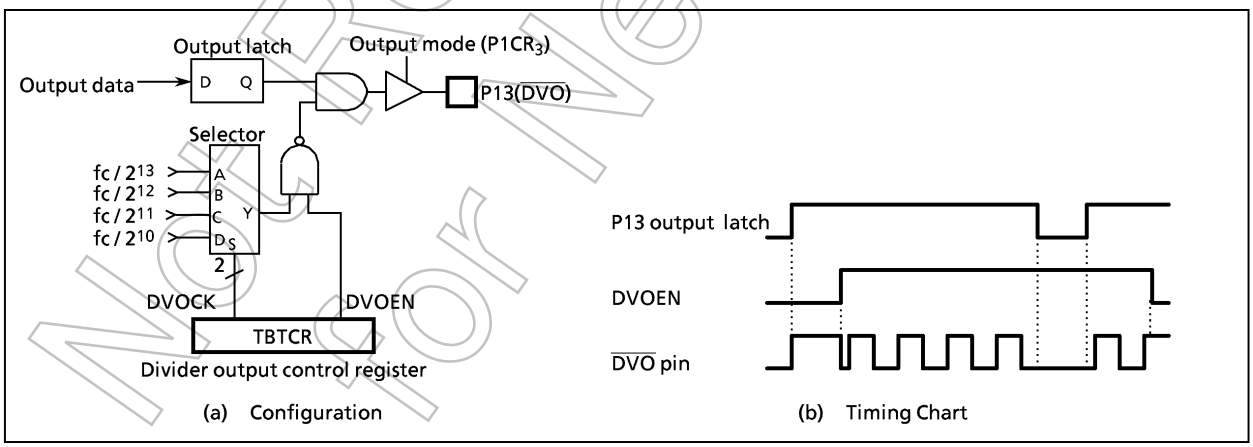


Figure 2-9. Divider Output

Not Recommended for New Design

2.5 16-bit Timer/Counter 1 (TC1)

2.5.1 Configuration

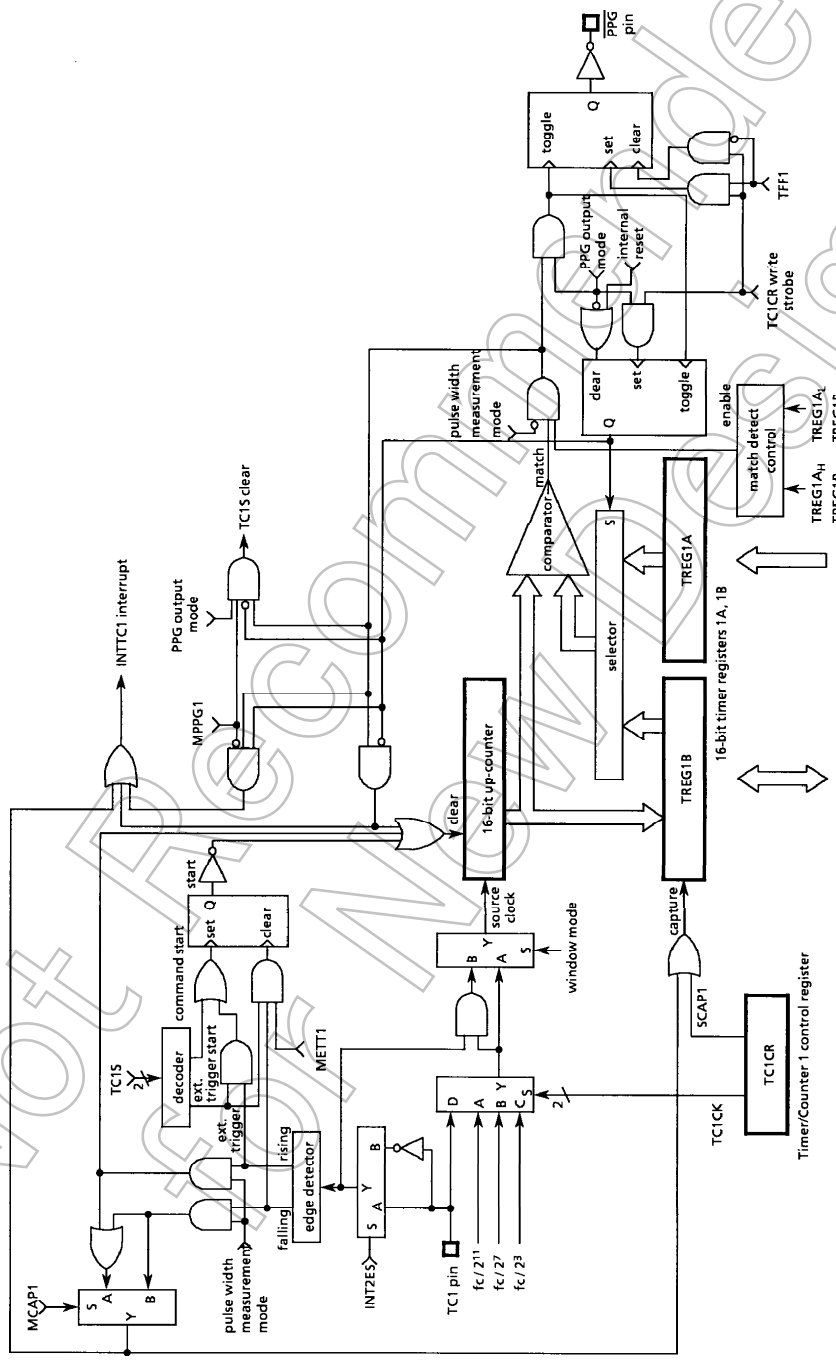


Figure 2-10. Timer/Counter 1

Not Recommended for New Design

2.5.2 Control

The Timer/Counter 1 is controlled by a Timer/Counter 1 control register (TC1CR) and two 16-bit timer registers (TREG1A and TREG1B).

Timer register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TREG1A (0010_H, 0011_H)	$TREG1A_H$ (0011_H)								$TREG1A_L$ (0010_H)							
									Write only							
TREG1B (0012_H, 0013_H)	$TREG1B_H$ (0013_H)								$TREG1B_L$ (0012_H)							
Timer/Counter									Read / Write (Write available in only PPG output mode)							

	7	6	5	4	3	2	1	0
TC1CR (0014_H)	TFF1	SCAP1 MCAP1 METT1 MPPG1	TC1S		TC1CK		TC1M	

(Initial value: 0000 0000)

TC1M	TC1 mode select	00: Timer / External trigger timer / Event counter mode 01: Window mode 10: Pulse width measurement mode 11: PPG (Programmable pulse generate) output mode	Write only
TC1CK	TC1 source clock select	00: Internal clock $fc / 2^{11}$ [Hz] 01: Internal clock $fc / 2^{7}$ 10: Internal clock $fc / 2^{3}$ 11: External clock (TC1 pin input)	
TC1S	TC1 start control	00: Stop & counter clear 01: Command start 10: reserved 11: External trigger start	
SCAP1	Software capture control	0: – 1: Software capture trigger	
MCAP1	Pulse width measurement control	0: Double edge capture 1: Single edge capture	
METT1	External trigger timer control	0: Trigger start 1: Trigger start & stop	
MPPG1	PPG output control	0: Continuous pulse 1: Single pulse	
TFF1	Timer F/F1 control	0: Clear 1: Set	

Note 1: fc ; clock [Hz]

Note 2: Writing to the low-byte of the timer registers ($TREG1A_L$, $TREG1B_L$), the comparison is inhibited until the high-byte ($TREG1A_H$, $TREG1B_H$) is written. (Only the low-byte of the timer registers cannot be changed.) After writing to the high-byte, the comparison within 1 machine cycle(during instruction execution) is ignored.

Note 3: Set the mode, source clock, edge (INT2ES), PPG output control and timer F/F1 control when TC1 stops (TC1S = 00).

Note 4: Software capture can be used in only timer and event counter modes. SCAP1 is automatically cleared to "0" after software capture.

Note 5: Values to be loaded to timer registers must satisfy the following condition.
TREG1A > TREG1B > 0 (PPG output mode) ; TREG1A > 0 (except for PPG output mode)

Note 6: Always write "0" to TFF1 except the PPG output mode.

Note 7: TC1CR is a write-only register, which cannot be accessed by any read-modify-write instructions such as bit operate, etc.

Note 8: TREG1B cannot be written after setting to PPG output mode.

Figure 2-11. Timer Registers and Control Register TC1

Not Recommended for New Design

2.5.3 Function

Timer/Counter 1 has six operating modes: Timer, External trigger timer, Event counter, Window, Pulse width measurement, and Programmable pulse generator output mode.

(1) **Timer** Mode

In this mode, counting up is performed using the internal clock. The contents of the Timer register 1A (TREG1A) are compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared to "0". Counting up resumes after the counter is cleared. The current contents of up-counter can be transferred to the Timer register 1B (TREG1B) by setting SCAP1(bit 6 in TC1CR) to "1"(software capture function). SCAP1 is automatically cleared to "0" after capturing.

Table 2-3. Timer/Counter 1 Source Clock (Internal Clock) (at fc = 8 MHz)

TC1CK	Resolution [μs]	Maximum time setting [s]
00	256	16.8
01	16	1.0
10	1	65.5 m

Example 1: Sets the Timer mode with source clock fc/2^{11}[Hz] and generates an interrupt 1 s. later (at fc = 8 MHz).

```
LDW     (TREG1A), 1000H        ; Sets the timer register (1s ÷ 2^11 / fc = 1000H)
SET     (EIRL). EF4            ; Enables INTTC1 interrupt
EI
LD      (TC1CR), 00010000B     ; Starts TC1
```

Note: TC1CR is a write-only register, which cannot start by [SET(TC1CR).4] instruction.

Example 2: Software capture

```
LD      (TC1CR) , 01010000B    ; SCAP1←1
LD      WA, (TREG1B)           ; Reads captured value
```

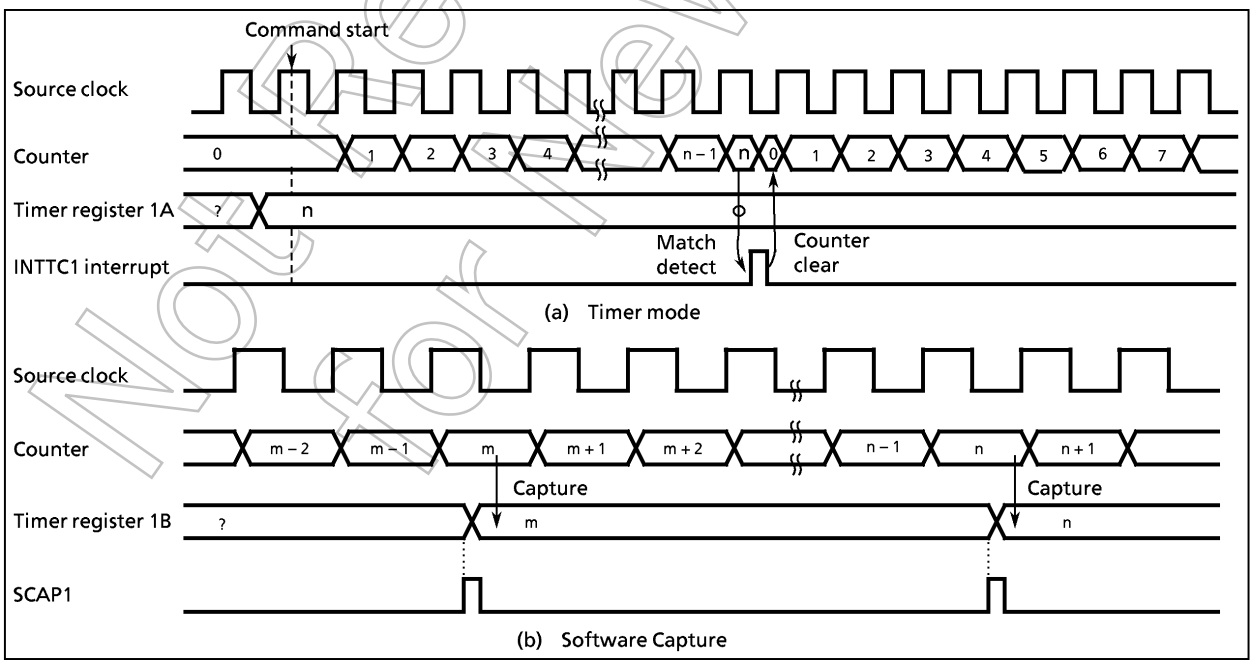


Figure 2-12. Timer Mode Timing Chart

Not Recommended for New Design

(2) **External Trigger Timer** mode

In this mode, counting up is started by an external trigger. This trigger is the edge of the TC1 pin input. Either the riging or the falling edge can be selected. Edge selection is the same as for INT2 pin. Source clock is used an internal clock selected. The contents of TREG1A is compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared to "0" and halted. The counter is restarted by the selected edge of the TC1 pin input.

When the edge input is opposite to the edge input way of the count start trigger at METTI (bit 6 in TC1CR) = 1, the counter is cleared, and count stops. In this mode, pulse input with a constant pulse width generates interrupt. When METT1 is "0", the opposite edge input is ignored. The edge of TC1 pin input before match detection is also ignored.

The TC1 pin input has the same noise rejection as the INT2 pin, therefore, pulses of 7/fc [s] or less are rejected as noise in NORMAL or IDLE mode. A pulse width of 24/fc [s] or more is required for edge detection.

Example 1: Generates interrupt after 100 μs from TC1 pin input rising edge (at fc = 8 MHz).

```
LD      (EINTCR), 00000000B     ; INT2ES←0 (rising edge)
LDW     (TREG1A), 0064H         ; 100 μs ÷ 2^3 / fc = 64H
SET     (EIRL).EF4              ; Enables INTTC1 interrupt
EI
LD      (TC1CR), 00111000B      ; Starts TC1 external trigger, METT = 0
```

Example 2: When "L" level pulses of 4ms or more is input to TC1 pin, generates interrupt. (at fc = 8 MHz)

```
LD      (EINTCR), 00000100B     ; INT2ES←1 ("L" level)
LDW     (TREG1A), 00FAH         ; 4 ms ÷ 2^7 / fc = FAH
SET     (EIRL).EF4              ; Enables INTTC1 interrupt
EI
LD      (TC1CR), 01110100B      ; Starts TC1 external trigger , METT = 1
```

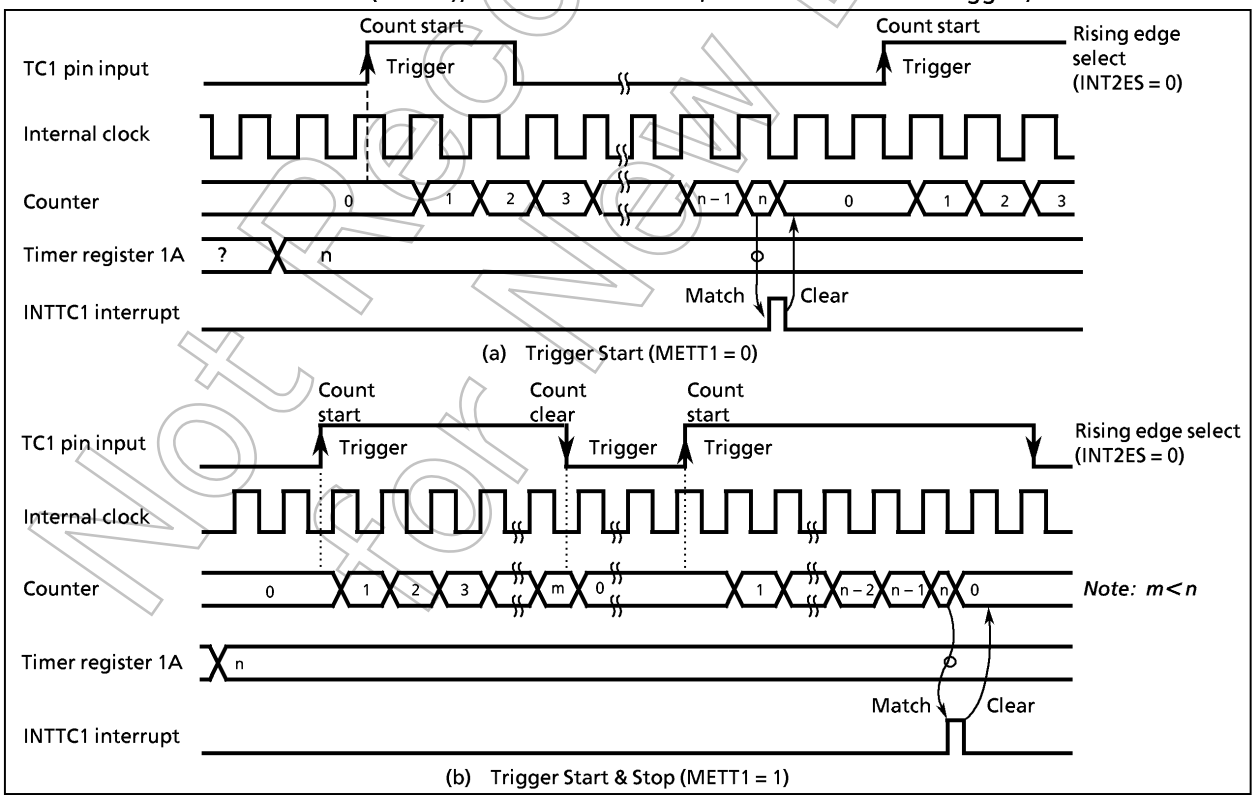


Figure 2-13. External Trigger Timer Mode Timing Chart

Not Recommended for New Design

(3) **Event Counter** Mode

In this mode, events are counted on the edge of the TC1 pin input. Either the rising and the falling edge can be selected with INT2 pin. The contents of TREG1A are compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared. Counting up resumes every edge of the TC1 pin input after the counter cleared. The maximum applied frequency is fc/2^4 [Hz] in NORMAL or IDLE mode.

Setting SCAP1 to "1" transfers the current contents of up-counter to TREG1B (software capture).

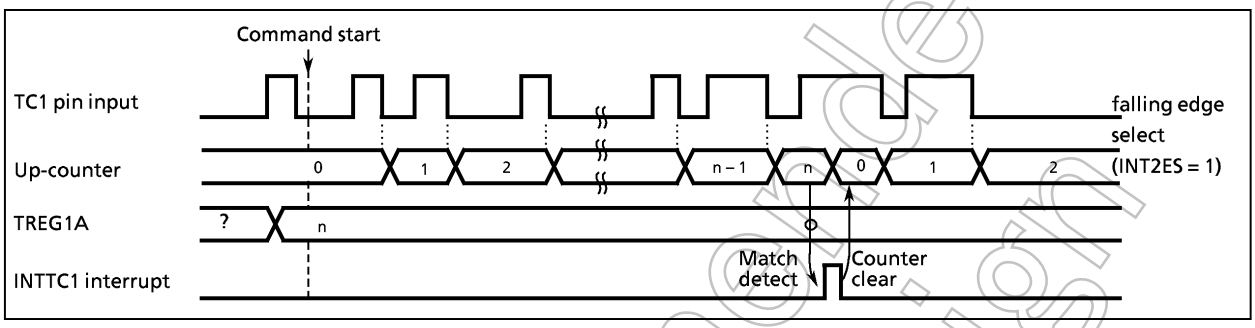


Figure 2-14. Event Counter Mode Timing Chart

(4) **Window** mode

Counting up is performed on the rising edge of the pulse that is the logical AND-ed product of the TC1 pin input (Window pulse) and an internal clock. The contents of TREG1A are compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared. Positive or negative logic for the TC1 pin input can be selected with INT2 pin.

It is necessary that the maximum applied frequency be such that the counter value can be analyzed by the program. That is, the frequency must be considerably slower than the selected internal clock.

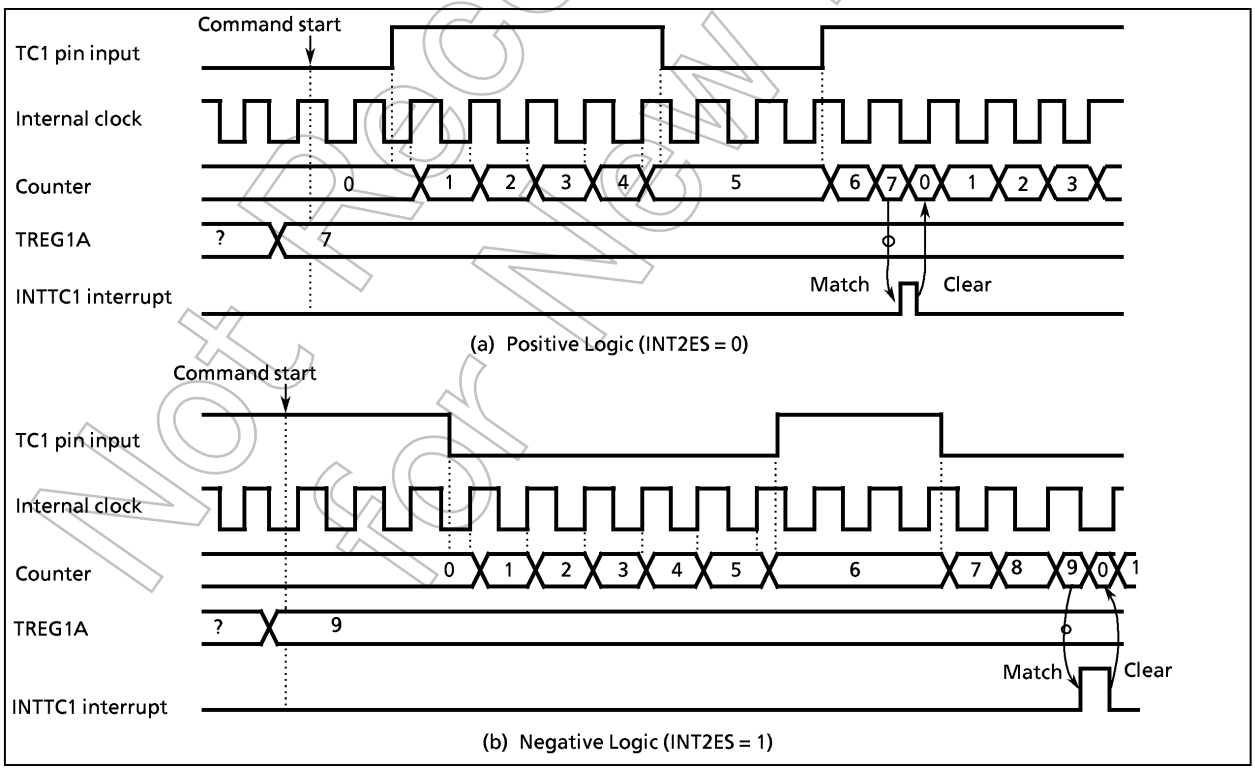


Figure 2-15. Window Mode Timing Chart

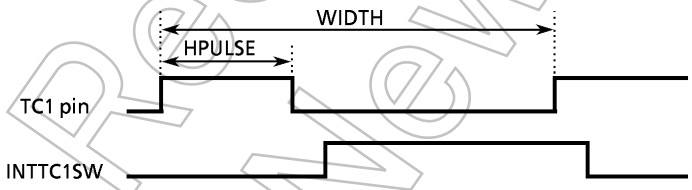
Not Recommended for New Design

(5) **Pulse width measurement** mode

Counting is started by a trigger of the rising (falling) edge of the TC1 pin input (set to external trigger start by TC1CR). The source clock is used an internal clock. On the next falling (rising) edge, the counter contents are transferred to TREG1B and an interrupt is generated. The counter is cleared when the single edge capture mode is set. When double edge capture is set, the counter continues and, at the next rising (falling) edge, the counter contents are again transferred to TREG1B. If a falling (rising) edge capture value is required, it is necessary to read out TREG1B contents until a rising (falling) edge is detected. Falling or rising edge is selected with INT2ES, and single edge or double edge is selected with MCAP1 (bit 6 in TC1CR).

Example: Duty measurement (Resolution fc/2^7[Hz])

```
            CLR   (INTTC1SW). 0          ; INTTC1 service switch initial setting
            LD    (EINTCR), 00000000B    ; Sets the rising edge at the INT2ES edge
            LD    (TC1CR), 00000110B     ; Sets the TC1 mode and source clock
            SET   (EIRL). EF4            ; Enables INTTC1
            EI
            LD    (TC1CR), 00110110B     ; Starts TC1 with an external trigger in MCAP1 = 0
             ⋮
PINTTC1:    CPL   (INTTC1SW). 0          ; Complements INTTC1 service switch
            JRS   F, SINTTC1
            LD    (HPULSE), (TREG1BL)    ; Reads TREG1B ("H" level pulse width)
            LD    (HPULSE + 1), (TREG1BH)
            RETI
SINTTC1:    LD    (WIDTH), (TREG1BL)     ; Reads TREG1B (Period)
            LD    (WIDTH + 1), (TREG1BH)
             ⋮                           ; Duty calculation
            RETI
             ⋮
VINTTC1:    DW    PINTTC1
```



Not Recommended for New Design

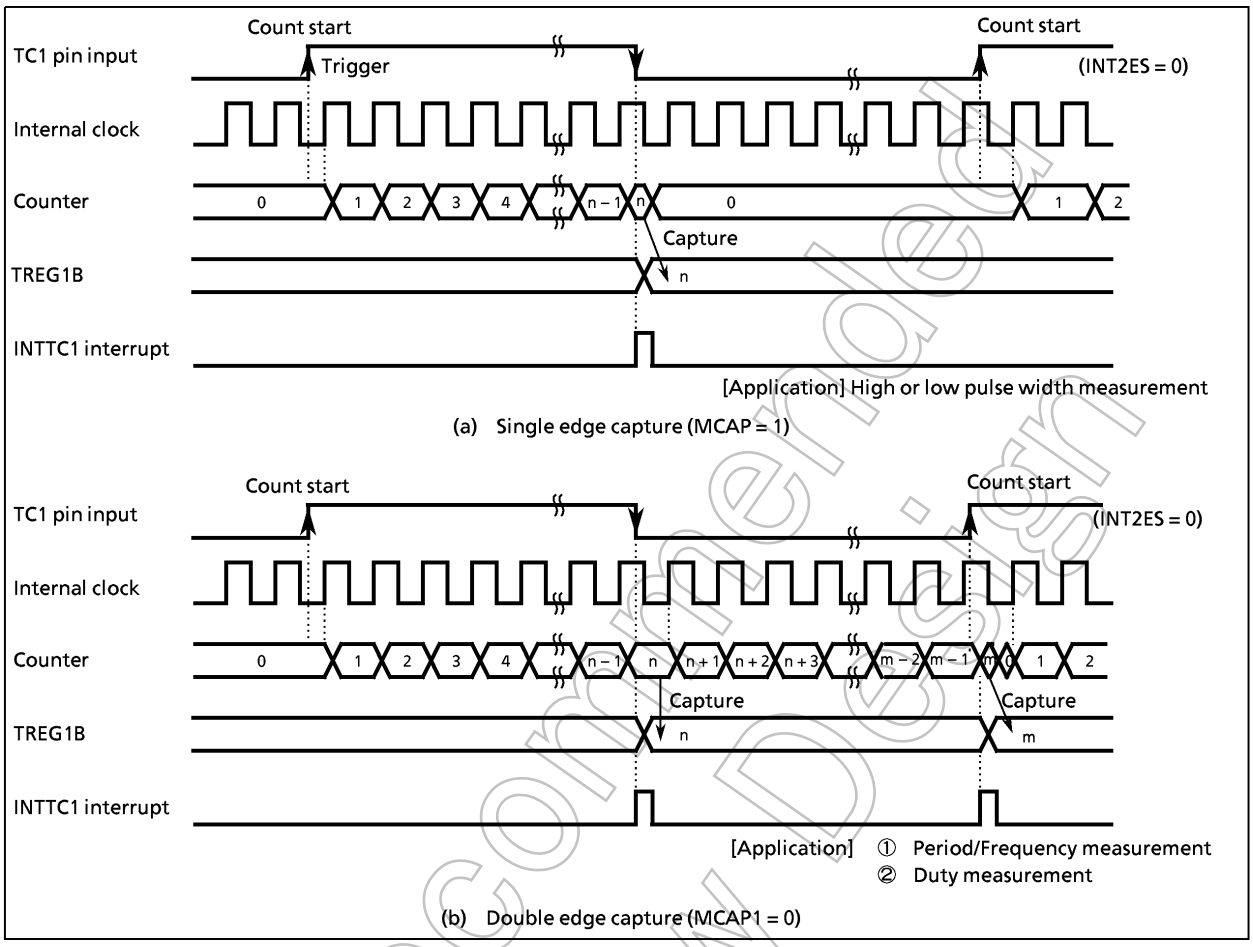


Figure 2-16. Pulse Width Measurement Mode

(6) **Programmable Pulse Generate** (PPG) **output** mode

Counting is started by an edge of the TC1 pin input (either the rising or falling edge can be selected) or by a command. Either the rising or falling edge can be selected by INT2ES of EINTCR. The source clock is used an internal clock. First, the contents of TREG1B are compared with the contents of the up-counter. If a match is found, Timer F/F1 output is toggled. INTTC1 interrupt is generated at continuous output (MPPG1 = 0). Next, Timer F/F1 is again toggled and the counter is cleared by matching with TREG1A. An INTTC1 interrupt is generated at this time. Timer F/F1 output is inverted and connected to the P14 ($\overline{PPG}$) pin. In the case of PPG output, set the P14 output latch to "1" and configure as an output mode. Timer F/F1 is cleared to "0" during reset. The Timer F/F1 value can also be set by TFF1 (bit 7 in TC1CR) and either a positive or negative logic pulse output is available. Also, writing to the TREG1B is not possible unless the Timer/Counter 1 is set to the PPG output mode.

Example: "H" level 800 μs, "L"" level 200 μs pulse output at fc = 8 MHz

```
SET     (P1).4                  ; P14 output latch←1
LD      (P1CR), 00010000B       ; Sets P14 to an output mode
LD      (TC1CR), 10001011B      ; Sets PPG output mode
LDW     (TREG1A), 03E8H         ; Sets a period (1 ms ÷ 1 μs = 03E8H)
LDW     (TREG1B), 00C8H         ; Sets "L" level pulse width (200 μs ÷ 1 μs = 00C8H)
LD      (TC1CR), 10010011B      ; Start
```

Not Recommended for New Design

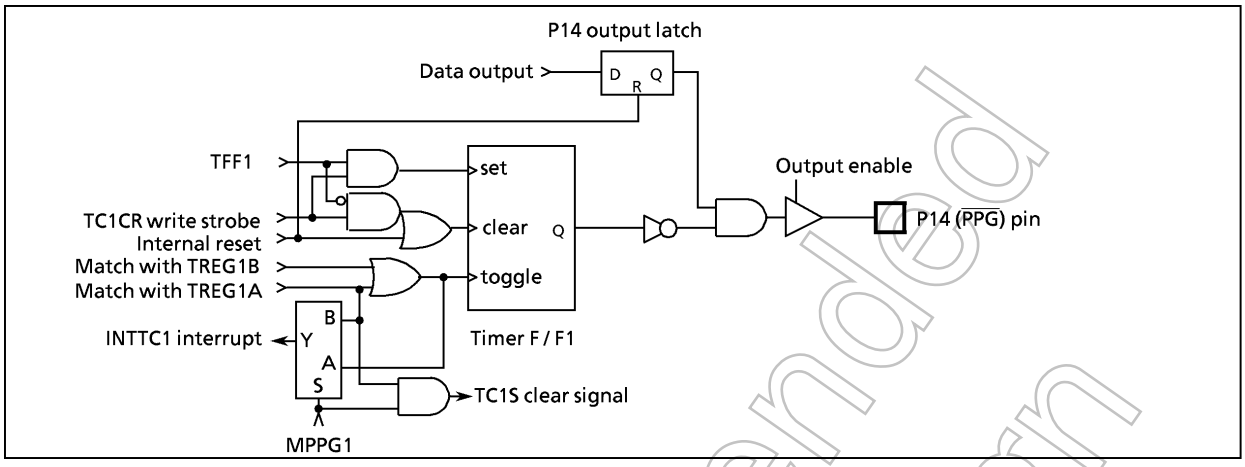


Figure 2-17. $\overline{\text{PPG}}$ Output

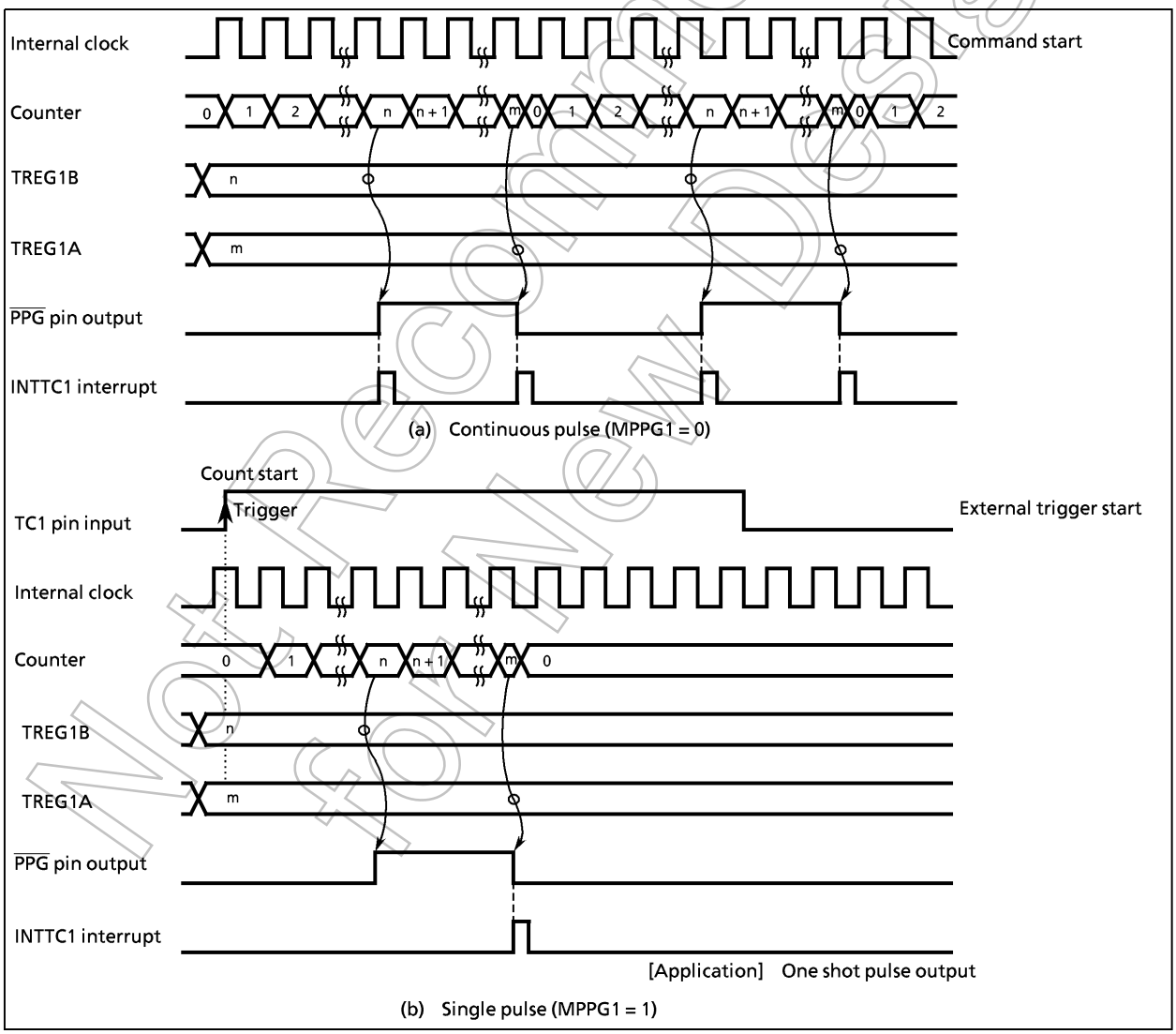


Figure 2-18. PPG Output Mode Timing Chart

Not Recommended for New Design

2.6 16-bit Timer/Counter 2 (TC2)

2.6.1 Configuration

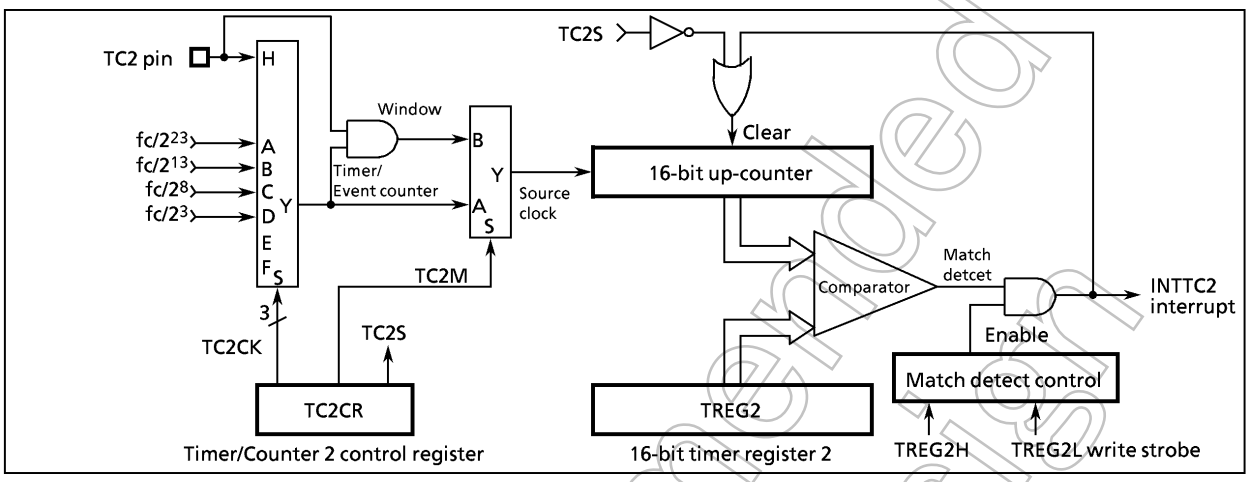


Figure 2-19. Timer/Counter 2 (TC2)

2.6.2 Control

The Timer/Counter 2 is controlled by a Timer/Counter 2 control register (TC2CR) and a 16-bit timer register 2 (TREG2).

TREG2 (0016_H, 0017_H)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$TREG2_H$ (0017_H)								$TREG2_L$ (0016_H)							

Write only

TC2CR (0015_H)

7	6	5	4	3	2	1	0
		TC2S	TC2CK				TC2M

(Initial value: **00 00*0)

TC2M	Timer/Counter 2 operating mode select	0: Timer/Event counter mode 1: Window mode	Write only
TC2CK	Timer/Counter 2 source clock select	000 : Internal clock fc / 2^{23} [Hz] 001 : Internal clock fc / 2^{13} 010 : Internal clock fc / 2^8 011 : Internal clock fc / 2^3 100 : reserved 101 : reserved 110 : reserved 111 : External clock (TC2 pin input)	
TC2S	Timer/Counter 2 start control	0: Stop and counter clear 1: Start	

*Note 1: fc; clock [Hz], *; Don't care*

Note 2: When writing to the low byte of timer register 2 ($TREG2_L$), the comparison is inhibited until the high-byte ($TREG2_H$) is written.
After writing to the high-byte, any match during 1 machine cycle (instruction execution cycle) is ignored.

Note 3: Set the mode and source clock when Timer/Counter stops (TC2S = 0).

Note 4: Values to be loaded to the timer register must satisfy the following condition.
TREG2 > 0

Note 5: TC2CR and TREG2 is a write-only register and cannot be used with any of the read-modify-write instructions.

Figure 2-20. Timer Register 2 and TC2 Control Register

Not Recommended for New Design

2.6.3 Function

The Timer/Counter 2 has three operating modes: Timer, Event counter and Window modes.

(1) **Timer** Mode

In this mode, the internal clock is used for counting up. The contents of TREG2 are compared with the contents of up-counter. If a match is found, an INTTC2 interrupt is generated, and the counter is cleared. Counting up is resumed after the counter is cleared.

Table 2-4. Source Clock (Internal Clock) for Timer/Counter 2 (at fc = 8 MHz)

TC2CK	Resolution	Maximum time setting
000	1.05 s	19.1 h
001	1.02 ms	1.1 min
010	32 μs	2.1 s
011	1 μs	65.5 ms

Example: Sets the Timer mode with source clock $fc/2^3$ [Hz] and generates an interrupt every 25 ms (at fc = 8 MHz).

```
LDW     (TREG2), 61A8H          ; Sets the TREG2 (25 ms ÷ 2^3 / fc = 61A8H)
SET     (EIRH).EF14             ; Enables INTTC2 interrupt
EI
LD      (TC2CR), 00101100B      ; Starts TC2
```

(2) **Event Counter** Mode

In this mode, events are counted on the rising edge of the TC2 pin input. The contents of TREG2 are compared with the contents of the up-counter. If a match is found, an INTTC2 interrupt is generated, and the counter is cleared. The maximum frequency applied to the TC2 pin is $fc/2^4$ [Hz] in NORMAL or IDLE mode. But, a pulse width of 2 machine cycles or more is required for both "H" and "L" level.

Example: Sets the Event counter mode and generates an INTTC2 interrupt 640 counts later

```
LDW     (TREG2), 640            ; Sets the TREG2
SET     (EIRH).EF14             ; Enables INTTC2 interrupt
EI
LD      (TC2CR), 00111100B      ; Starts TC2
```

(3) **Window** Mode

In this mode, counting up is performed by an internal clock during "H" level of TC2 external pin input (Window pulse). The contents of TREG2 are compared with the contents of up-counter. If a match is found, an INTTC2 interrupt is generated, and the up-counter is cleared to "0".

It is necessary that the maximum applied frequency must be considerably slower than the selected internal clock.

Example: Inputs "H" level pulse of 120 ms or more and generates interrupt. (at fc = 8 MHz).

```
LDW     (TREG2), 0078H          ; Sets TREG2 (120 ms ÷ 2^13/fc = 0078H)
SET     (EIRH).EF14             ; Enables INTTC2 interrupt
EI
LD      (TC2CR), 00100101B      ; Starts TC2
```

Not Recommended for New Design

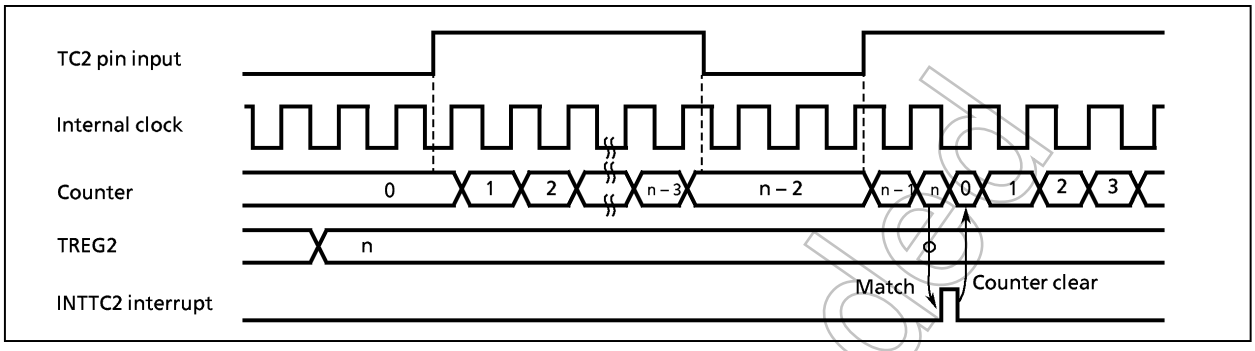


Figure 2-21. Window Mode Timing Chart

Not Recommended for New Design

2.7 Serial Interface (SIO)

The 87C408/808/408L/808L each have one clocked-synchronous 8-bit Serial interfaces (SIO). The Serial interface has an 8-byte transmit and receive data buffer that can automatically and continuously transfer up to 64 bits of data.

The Serial interface is connected to external devices via pins P75 (SO), P74 (SI), and P73 ($\overline{SCK}$). The Serial interface pins are also used as port P7. When used as Serial interface pins, the output latches of these pins should be set to "1". In the Transmit mode, pins P74 can be used as normal I/O ports, and in the Receive mode, the pins P75 can be used as normal I/O ports.

2.7.1 Configuration

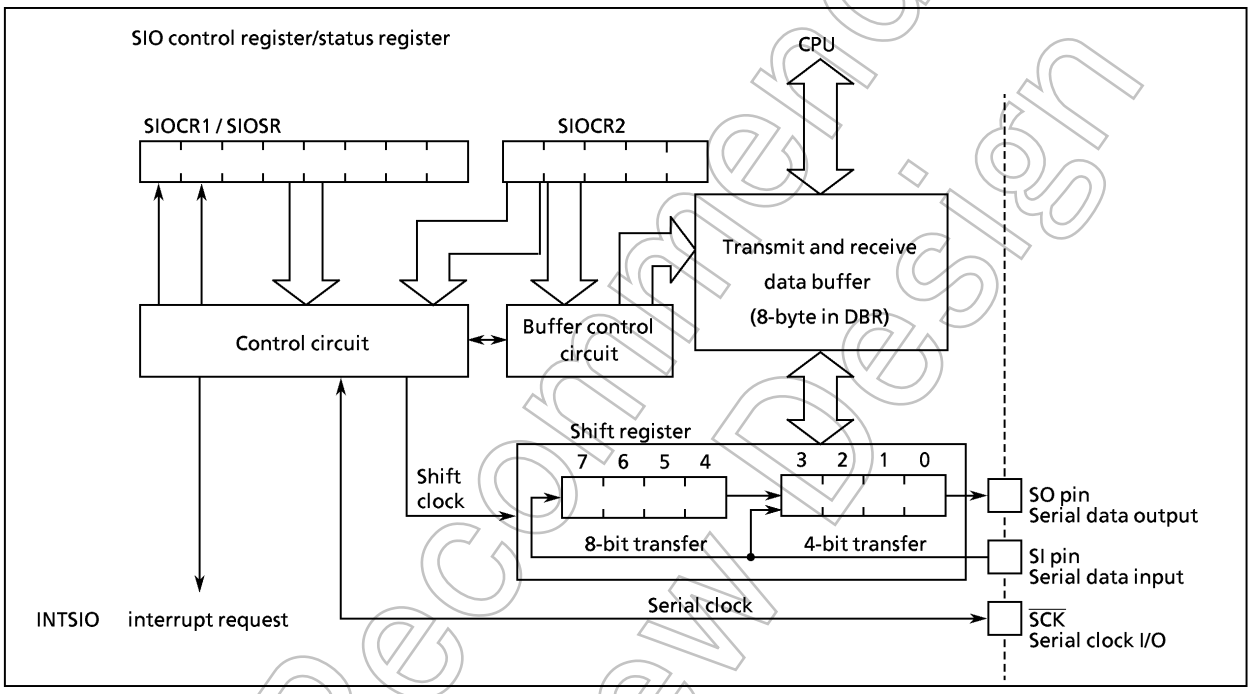


Figure 2-22. Serial Interface

2.7.2 Control

The Serial interface is controlled by SIO control registers (SIOCR1/SIOCR2). The Serial interface status can be determined by reading SIO status registers (SIOSR).

The transmit and receive data buffer is controlled by the BUF (bits 2 to 0 in SIOCR2). The data buffer is assigned to addresses 0FF0 to $0FF7_H$ for SIO in the DBR area, and can continuously transfer up to 8 words at one time. When the specified number of words has been transferred, a buffer empty (in the Transmit mode) or a buffer full (in the Receive mode or Transmit/Receive mode) interrupt (INTSIO) is generated.

Not Recommended for New Design

Serial interface control register 1

SIOCR1 (0020_H)

7	6	5	4	3	2	1	0
SIOS	SIO INH	SIOM			SCK		

(Initial value: 0000 0000)

SIOS	Indicate transfer start/stop	0: Stop 1: Start	Write only
SIOINH	Continue/abort transfer	0: Continue transfer 1: Abort transfer (automatically cleared after abort)	
SIOM	Transfer mode select	000: 8-bit Transmit mode 010: 4-bit Transmit mode 100: 8-bit Transmit/Receive mode 101: 8-bit Receive mode 110: 4-bit Receive mode	
SCK	Serial clock select	000: Internal clock fc / 2^{13} [Hz] 001: Internal clock fc / 2^8 010: Internal clock fc / 2^6 011: Internal clock fc / 2^5 } (output on $\overline{SCK}$ pin) 111: External clock (input form $\overline{SCK}$ pin)	

Note 1: Set SIOS to "0" and SIOINH to "1" when setting the Transmit mode or serial clock.
Note 2: SIOCR1 is a write-only register and must not be used with any of read-modify-write instructions such as bit manipulation.

Serial interface control register 2

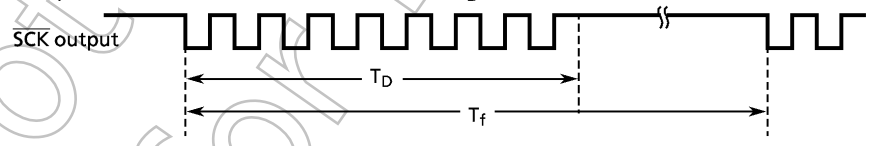
SIOCR2 (0021_H)

7	6	5	4	3	2	1	0
			WAIT		BUF		

(Initial value: ***0 0000)

WAIT	Wait control	Always sets "00" except 8-bit Transmit/Receive mode. 00: $T_f = T_D$ (non-wait) 01: $T_f = 2T_D$ 10: $T_f = 4T_D$ (wait) 11: $T_f = 8T_D$	Write only
BUF	Number of transfer words	Buffer address used 000: 1 word transfer $0FF0_H$ 001: 2 word transfer 0FF0 to $0FF1_H$ 010: 3 word transfer 0FF0 to $0FF2_H$ 011: 4 word transfer 0FF0 to $0FF3_H$ 100: 5 word transfer 0FF0 to $0FF4_H$ 101: 6 word transfer 0FF0 to $0FF5_H$ 110: 7 word transfer 0FF0 to $0FF6_H$ 111: 8 word transfer 0FF0 to $0FF7_H$	

Note 1: T_f ; frame time (1 word data transfer time), T_D ; data transfer time



Note 2: The lower 4 bits of each buffer are used during 4-bit transfers. Zeros (0) are stored to the upper 4 bits when receiving.
Note 3: Transmitting starts at the lowest address. Received data are also stored starting from the lowest address to the highest address. First, address $0FF0_H$ is transferred.
Note 4: The value to be loaded to BUF is held after transfer is completed.
Note 5: SIOCR2 must be set when the serial interface is stopped (SIOF = 0).
Note 6: SIOCR2 is a write-only register and must not be used with any of read-modify-write instructions such as bit manipulation.
*Note 7: * ; Don't care*

Figure 2-23. Serial Interface Control Register

Not Recommended for New Design

SIOSR (0020_H)

7	6	5	4	3	2	1	0
SIOF	SEF	"1"	"1"	"1"	"1"	"1"	"1"

SIOF	Serial transfer operating status monitor	0:Transfer terminated 1:Transfer in process	(After SIOS is cleared to "0", SIOF is cleared to "0" at the termination of transfer or setting of SIOINH.)	read only
SEF	Shift operating status monitor	0:Shift operation terminated 1:Shift operation in process		

Figure 2-24. Serial Interface Status Register

(1) **Serial Clock**

a. Clock Source

SCK (bits 2 to 0 in SIOCR1) is able to select the following.

① Internal Clock

Any of four frequencies can be selected. The serial clock is output to the outside on the $\overline{SCK}$ pin. The $\overline{SCK}$ pin goes high when transfer starts.

When data writing (in the Transmit mode) or reading (in the Receive mode or the Transmit/Receive mode) cannot keep up with the serial clock rate, there is a wait function that automatically stops the serial clock and holds the next shift operation must the read/write processing is completed.

Table 2-5. Serial Clock Rate (at fc = 8MHz)

SCK	Maximum transfer rate [Kbit / s]
000	0.95
001	30.5
010	122
011	244

Note: 1 Kbit = 1024 bit

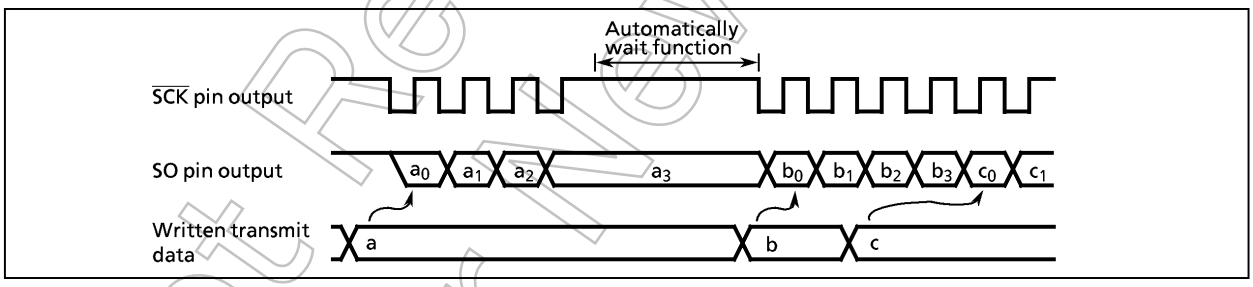
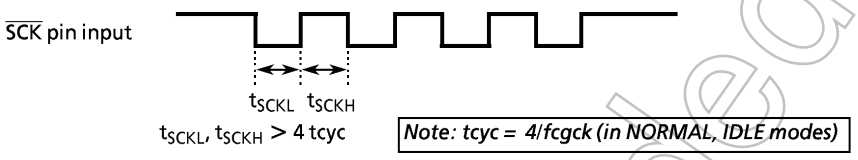


Figure 2-25. Clock Source (Internal Clock)

Not Recommended for New Design

② External Clock

An external clock connected to the $\overline{SCK}$ pin is used as the serial clock. In this case, the P73 ($\overline{SCK}$)) output latch must be set to "1". To ensure shifting, a pulse width of at least 4 machine cycles is required. Thus, the maximum transfer speed is 244 Kbit/s (at fc = 8 MHz).



b. Shift edge

The leading edge is used to transmit, and the trailing edge is used to receive.

① Leading Edge

Transmitted data are shifted on the leading edge of the serial clock (falling edge of the $\overline{SCK}$ pin input/output).

② Trailing Edge

Received data are shifted on the trailing edge of the serial clock (rising edge of the $\overline{SCK}$ pin input/output).

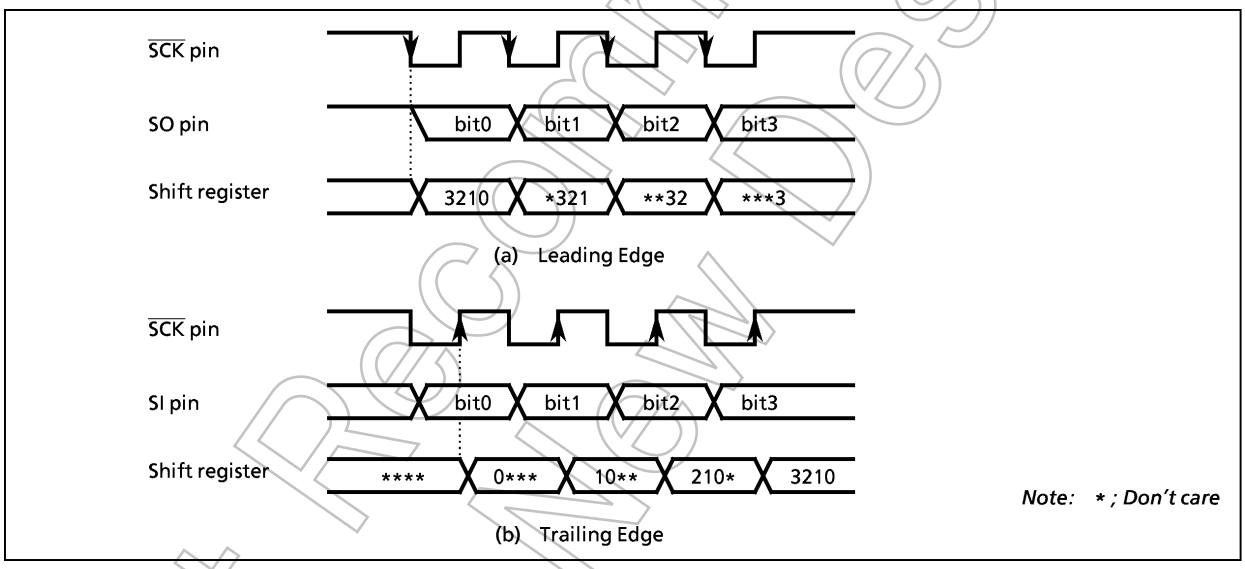


Figure 2-26. Shift Edge

(2) **Number of Bits of Transfer**

Either 4-bit or 8-bit serial transfer can be selected. When 4-bit serial transfer is selected, only the lower 4-bits of the transmit/receive data buffer register are used. The upper 4-bits are cleared to "0" when receiving.

The data is transferred in sequence starting at the least significant bit (LSB).

(3) **Number of Words to Transfer**

Up to 8 words consisting of 4 bits of data (4-bit serial transfer) to 8 bits (8-bit serial transfer) of data can be transferred continuously. The number of words to be transferred is loaded to BUF.

An INTSIO interrupt is generated when the specified number of words has been transferred. If the number of words is to be changed during transfer, the serial interface must be stopped before making the change. The number of words can be changed during automatic-wait operation of an internal clock. In this case, the serial interface is not required to be stopped.

Not Recommended for New Design

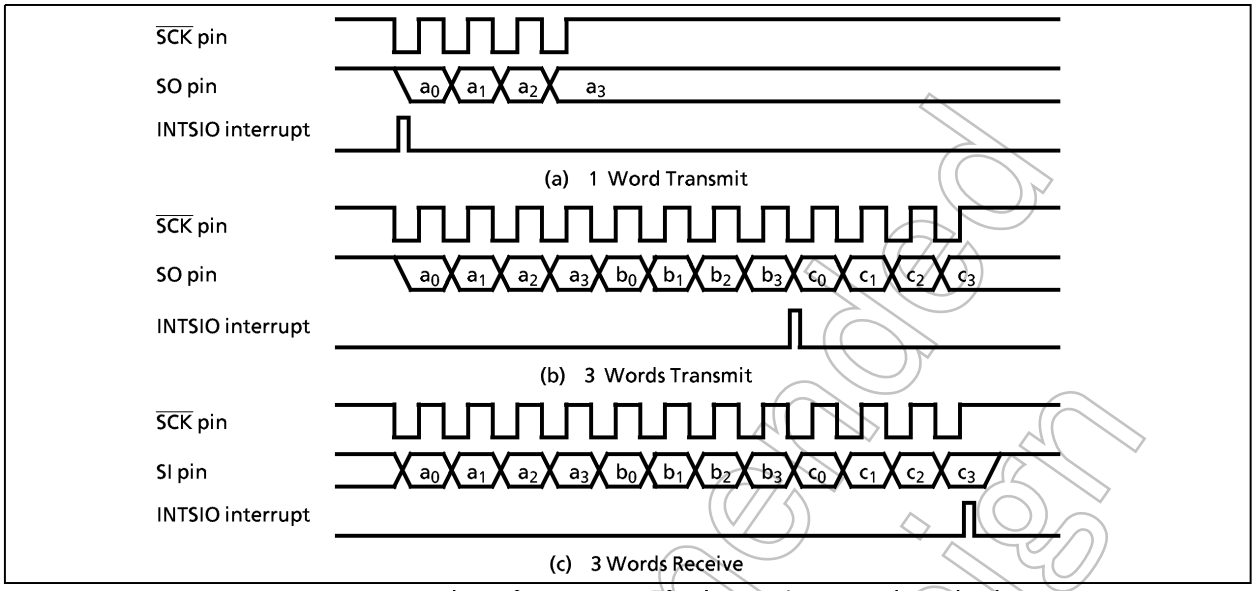


Figure 2-27. Number of Bits to Transfer (Example: 1 word = 4 bits)

(4) **Transfer Mode**

SIOM (bits 3 to 5 in SIOCR1) is used to select the Transmit, Receive, or Transmit/Receive mode.

a. 4-bit and 8-bit Transmit Modes

In these modes, the Transmit mode is set to the control register and then the data to be transmitted first are written to the data buffer registers (DBR).

After the data area written, the transmission is started by setting SIOS to "1". The data are then output sequentially to the SO pin in synchronous with the serial clock, starting with the least significant bit (LSB). As soon as the LSB has been output, the data are transferred from the data buffer register to the shift register per 1 word. When the final data bit has been transferred and the data buffer register is empty, an INTSIO (buffer empty) interrupt is generated to request the next transmitted data.

When the internal clock is used, the serial clock will stop and perform an automatic wait if the next transmitted data are not loaded to the data buffer register by the time the number of data words specified with the BUF has been transmitted. Writing even one word of data cancels the automatic-wait; therefore, when transmitting two or more words, always write the next word before transmission of the previous word is completed.

Note: Automatic-waits are also canceled by writing to a DBR not being used as a transmit data buffer register; therefore, during SIO do not use such DBR for other applications. For example, when 3 words are transmitted, do not use the DBR of the remained 5 words.

When an external clock is used, the data must be written to the data buffer register before shifting next data. Thus, the transfer speed is determined by the maximum delay time from the generation of the interrupt request to writing of the data to the data buffer register by the interrupt service program.

When the transmit is started, after the SIOF goes "high" output from the SO pin holds final bit of the last data until falling edge of the $\overline{SCK}$.

The transmission is ended by clearing SIOS to "0" or set SIOINH to "1" in the buffer empty interrupt service program to end transmitting. After SIOS is cleared, the transmission is ended at the time that the final bit of the data being shifted has been output. That the transmission has ended can be determined from the status of SIOF (bit 7 in SIOSR). SIOF is cleared to "0" when the transmission is completed. When SIOINH is set, the transmission is immediately ended and SIOF is cleared to "0".

Not Recommended for New Design

When an external clock is used, it is also necessary to clear SIOS to "0" before shifting the next data; otherwise, dummy data will be transmitted and the operation will end. If it is necessary to change the number of words, SIOS should be cleared to "0", then BUF must be rewritten after confirming that SIOF has been cleared to "0".

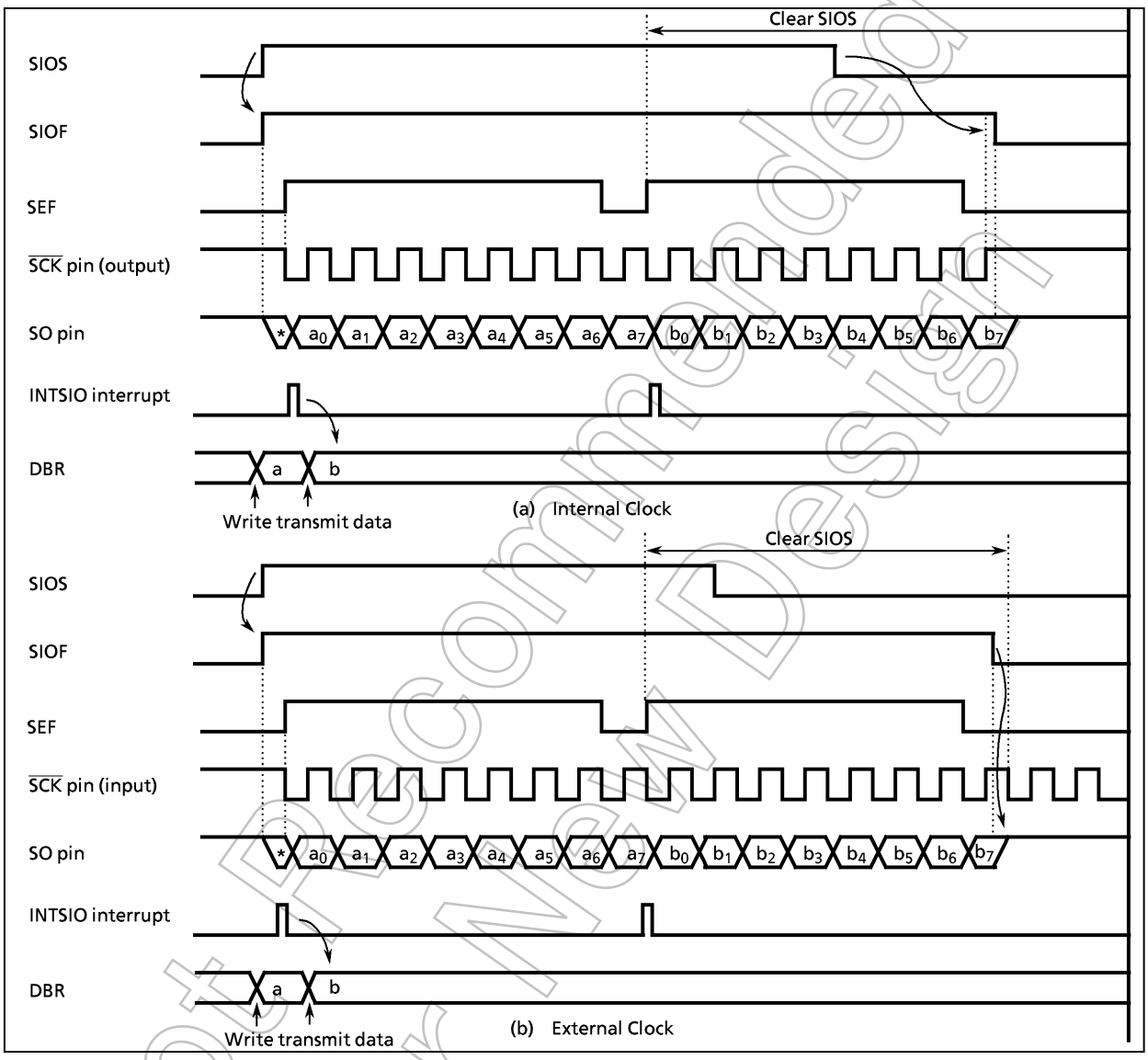


Figure 2-28. Transmitted Data (Example: 8-bit, 1 word)

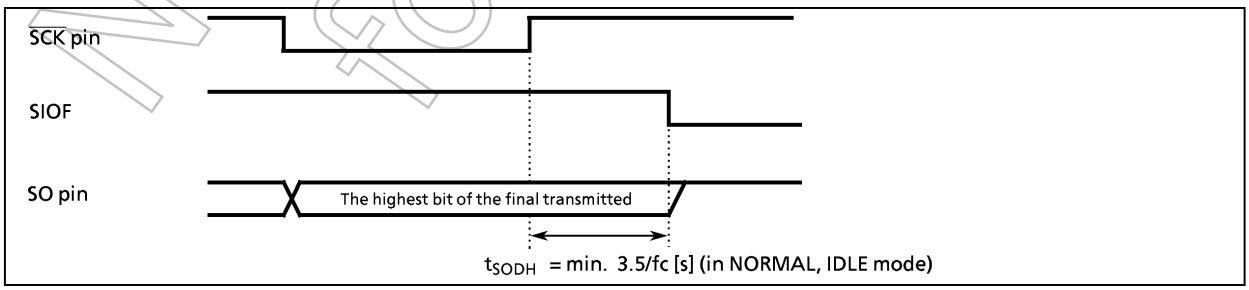


Figure 2-29. Transmitted Data Hold Time at end of transmit

Not Recommended for New Design

b. 4-bit and 8-bit Receive Modes

After setting the control registers to the Receive mode, set SIOS to "1" to enable receiving. The data are then transferred to the shift register via the SI pin in synchronous with the serial clock, starting with the least significant bit (LSB). When one word of data has been received, it is transferred from the shift register to the data buffer register (DBR). When the number of words specified with the BUF has been received, an INTSIO (buffer full) interrupt is generated to request that these data be read out. The data are then read from the data buffer registers by the interrupt service program.

When the internal clock is used, and the previous data are not read from the data buffer register before the next data are received, the serial clock will stop and an automatic-wait will be initiated until the data are read. A wait will not be initiated if even one data word has been read.

Note: Automatic-waits are also canceled by reading a DBR not being used as a received data buffer register; therefore, during SIO do not use such DBR for other applications.

When an external clock is used, the shift operation is synchronized with the external clock; therefore, the previous data are read before the next data are transferred to the data buffer register. If the previous data have not been read, the next data will not be transferred to the data buffer register and the receiving of any more data will be canceled. When an external clock is used, the maximum transfer speed is determined by the delay between the time when the interrupt request is generated and when the data received have been read.

The receiving is ended by clearing SIOS to "0" or setting SIOINH to "1" in buffer full interrupt service program. When SIOS is cleared, the current data are transferred to the buffer. After SIOS cleaned, the transmissions is ended at the time that the final bit of the data being shifted has been output. That the transmission has ended can be determined from the status of SIOF (bit 7 in SIOSR). SIOF is cleared to "0" when the transmission is ended. After confirmed the receiving termination, the final receiving data is read. When SIOINH is set, the receiving is immediately ended and SIOF is cleared to "0". (The received data is ignored, and it is not required to be read out.) If it is necessary to change the number of words in external clock operation, SIOS should be cleared to "0" then BUF must be rewritten after confirming that SIOF has been cleared to "0".

If it is necessary to change the number of words in internal clock operation, during automatic-wait which occurs after completion of data receiving. (BUF must be rewritten before the received data is read out.)

Note: The buffer contents are lost when the transfer mode is switched. If it should become necessary to switch the Transfer mode, end receiving by clearing SIOS to "0", read the last data and then switch the Transfer mode.

Not Recommended for New Design

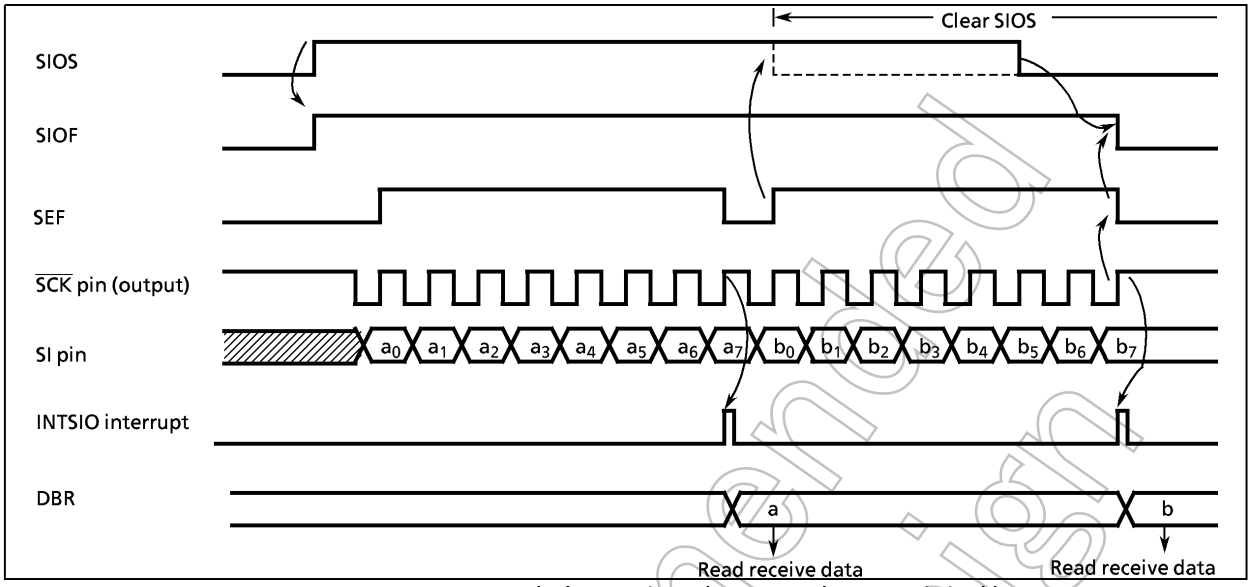


Figure 2-30. Receive Mode (Example: 8-bit, 1 word, internal clock)

c. 8-bit Transmit/Receive Mode

After setting the control registers to the Transmit/Receive mode, write the data to be transmitted first to the data buffer registers (DBR). After that, enable transmitting and receiving by setting SIOS to "1". When transmitting, the data are output from the SO pin at leading edges of the serial cock, starting with the least significant bit (LSB). When receiving, the data are input through the SI pin at the trailing edges of the serial clock. 8-bit data are transferred from the shift register to the data buffer register. An INTSIO interrupt is generated when the number of data words specified with the BUF has been transferred. The interrupt service program reads the received data from the data buffer register, the transmitted data is written. The data buffer register is used for both transmitting and receiving; therefore, always write the data to the transmitted after reading all the received data.

When the internal clock is used, a wait is initiated until the received data are read and the next data are written. A wait will not be initiated if even one data word has been written.

Note: Waits are also canceled by writing to a DBR not being used as the transmit/received data buffer register; therefore, do not use such DBR for other applications.

When an external clock is used, the shift operation is synchronized with the external clock; therefore, it is necessary to read the received data and write the data to be transmitted next before starting the next shift operation. When an external clock is used, the maximum transfer speed is determined by the maximum delay between generation of an interrupt request and the received data are read and the data to be transmitted next are written.

When the transmit is started, after the SIOF goes "high" output from the SO pin holds final bit of the last data until falling edge of the $\overline{SCK}$.

The transmit/receive operation is ended by clearing SIOS to "0" or set SIOINH to "1" in INTSIO interrupt service program. When SIOS is cleared, the current data are transferred to the data buffer register. The transmit/receive is ended at the time that the final bit of the data being shifted has been output. The end of transmit/receive can be determined from the status of SIOF (bit 7 in SIOSR). SIOF is cleared to "0" when the transmit/receive is ended. When SIOINH is set, the transmission is immediately ended and SIOF is cleared to "0".

If the number of words is to be changed during transfer, SIOS must be cleared to "0" and BUF is rewritten after SIOF is determined to be cleared to "0" during automatic-wait operation of an external clock operation. The number of words can be changed in an internal clock. In this case BUF must be rewritten before the received data is read out.

Not Recommended for New Design

Note: The buffer contents are lost when the Transfer mode is switched. If it should become necessary to switch the Transfer mode, end receiving by clearing SIOS to "0", read the last data and then switch the Transfer mode.

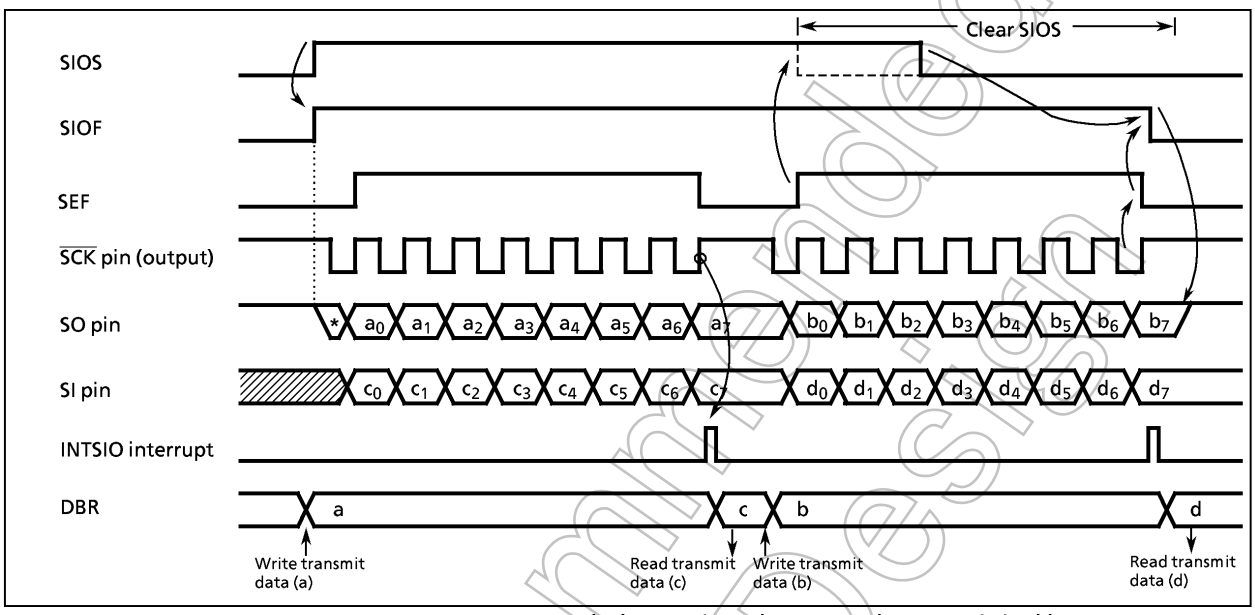


Figure 2-31. Transmit/Receive Mode (Example: 8-bit, 1 word, internal clock)

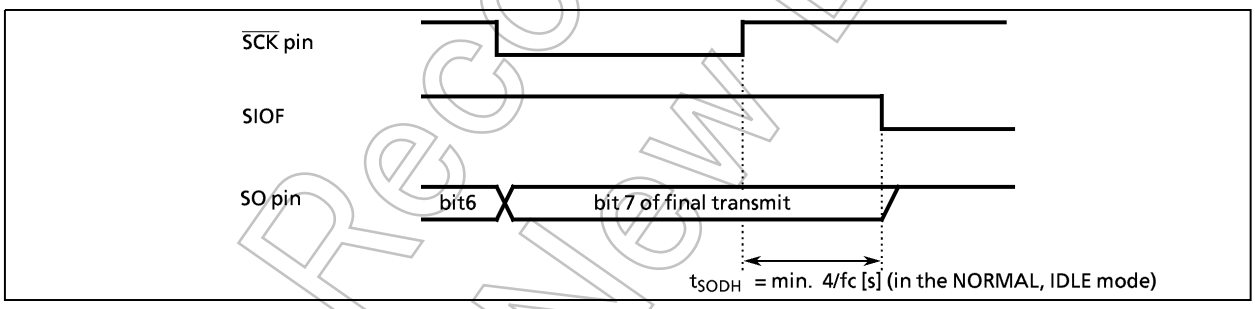


Figure 2-32. Transmitted Data Hold Time at end of transmit/receive

Not Recommended for New Design

2.7.3 NOTES FOR USAGE OF SIO

If same ringing noise occurs at rising or falling of $\overline{SCK}$ pin, note that the $\overline{SCK}$ pin does not function as Schmitt circuit.

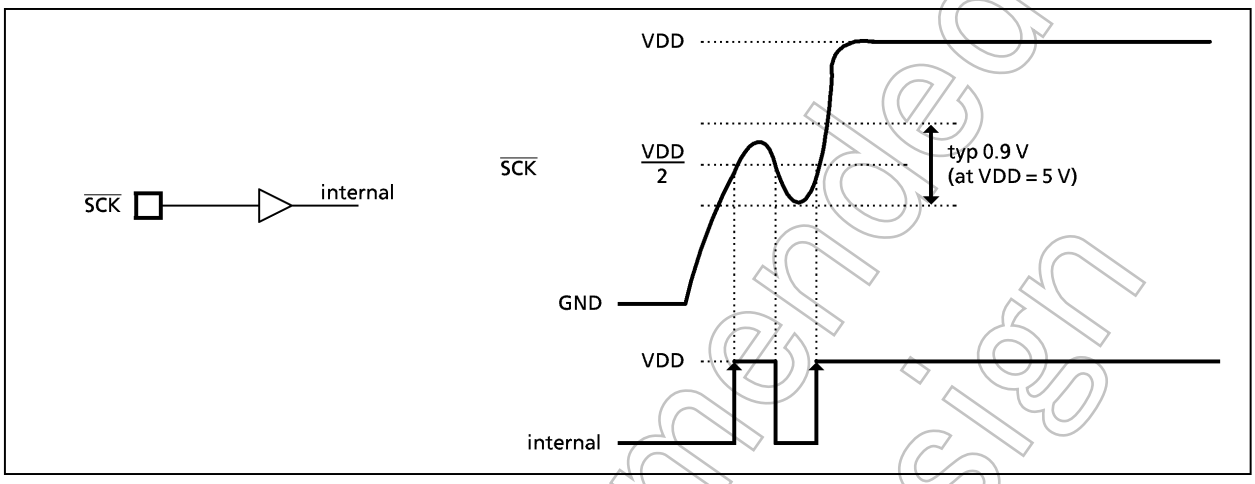


Figure 2-33. Example of ringing noise

The $\overline{SCK}$ pin is used as a count clock for detecting the ending point of the serial data. If some rising noise occurs on the $\overline{SCK}$ input line, as Figure 1, some miscounting will be performed, thus the function for shifting the receive data will finish earlier than anticipated, it shown as Figure 2-34.

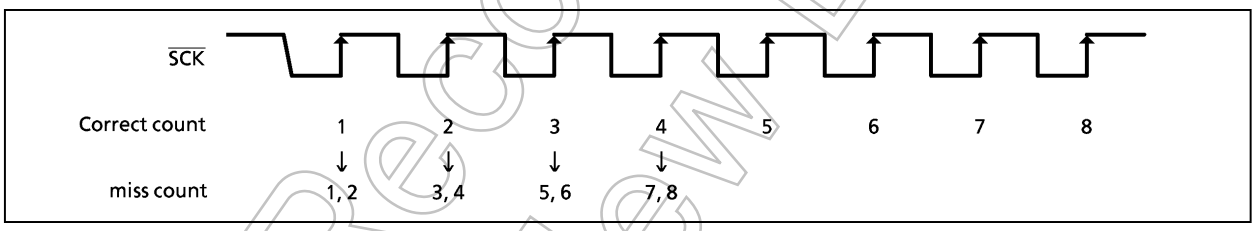


Figure 2-34. Example of miss count (at 8-bit receive mode)

Note 1: In case of $\overline{SCK}$ pin is used as input, it is recommended that Schmitt circuit is inserted externally.
Note 2: Additionally, SI pin does not function as Schmitt circuit, so we suggest that Schmitt circuit is inserted externally.

Not Recommended for New Design

2.8 8-bit A/D Converter (ADC)

The 87C408/808/408L/808L each have an 8-bit successive approximate type A/D converter with sample and hold.

Analog reference power supply (VAREF) is automatically cut off in STOP mode or analog input disable.

2.8.1 Configuration

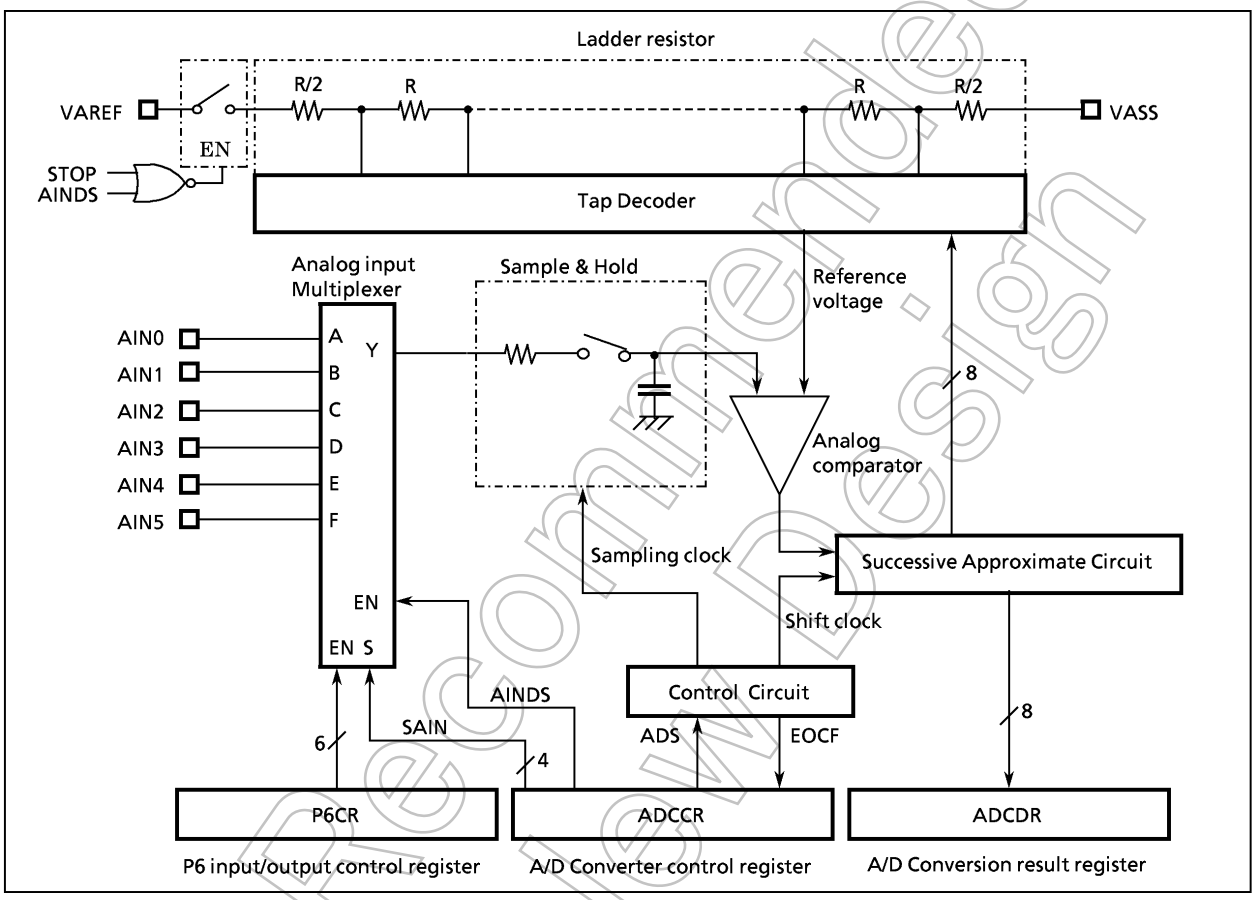


Figure 2-35. A/D Converter (ADC)

2.8.2 Control

The A/D converter is controlled by an A/D converter control register (ADCCR). Reading EOCF of ADCCR recognizes A/D converter operation state, and reading A/D conversion result register (ADCDR) recognizes A/D conversion result.

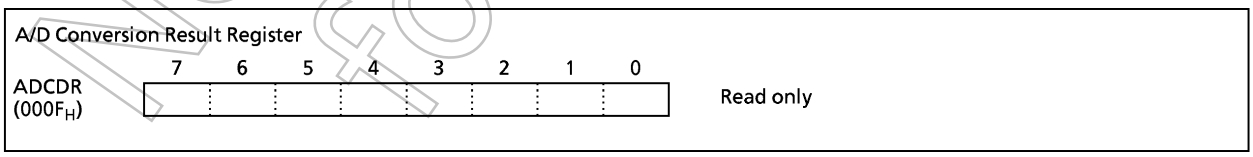


Figure 2-36. A/D Conversion Result Register

Not Recommended for New Design

A/D Converter Control Register

ADCCR ($000E_H$)

7	6	5	4	3	2	1	0
EOCF	ADS	ACK	AINDS	SAIN			

(Initial value: 0001 0000)

SAIN	Analog input selection	0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: reserved 0111: reserved 1 ***: reserved	R/W
AINDS	Analog input control	0: Enable 1: Disable	
ACK	Conversion time	0: Conversion time = 184/fcgck 1: Conversion time = 736/fcgck	
ADS	A/D conversion start	0: – 1: A/D conversion start	
EOCF	A/D conversion end flag	0: Under conversion or Before conversion 1: End of conversion	R

*Note 1: * ; Don't care*
Note 2: Select analog input when A/D converter stops.
Note 3: The ADS is automatically cleared to "0" after starting conversion.
Note 4: The EOCF is cleared to "0" when reading the ADCDR.
Note 5: The EOCF is read-only. The written data is ignored.

Figure 2-37. A/D Converter Control Register

2.8.3 Operation

The high side of an analog reference voltage is applied to VAREF pin, and the low side is applied to VASS pin. The reference voltage between VAREF and VASS is divided into the voltage corresponding with bits by radar resistance. The reference voltage is compared with an analog input voltage and A/D conversion is performed.

Note: VASS is the same as VSS.

(1) Start of A/D conversion

First, selects one of analog input channels (AIN5 to AIN0) by SAIN(bit 3 to 0 in ADCCR). Clear the AINDS (bit 4 in ADCCR) to "0". The channel used as an analog input is cleared to "0" by P6 input control (P6CR).

Note: The pin that is not used as an analog input can be used as regular input/output pins. During conversion, do not perform output instruction to maintain a precision for all of the pins.

A/D conversion time is set with the ACK (bit 5 in ADCCR).
A/D conversion is started by setting the ADS (bit 6 in ADCCR) to "1".
A/D conversion time is from A/D conversion until setting the conversion result to ADCDR. When ACK = 0, conversion is accomplished in 184/fcgck [s] (46 machine cycles). For example, 23 μs in fcgck = 8 MHz. The EOCF (bit 7 in ADCCR) is set to "1" at end of conversion.When ADS is set to "1" during A/D conversion, conversion is initialized and restarted.Sampling of an analog input voltage is performed in 4 machine cycles after A/D conversion start is indicated.

Note 1: To keep the same level of an analog input during 4 Machine Cycle Time is necessary for charging the electron to the sample hold circuit of the 87C408/808/P808 which has a resistor (typ. 5 kΩ) and a capacitor (typ. 12pF).
Note 2: To keep the same level of an analog input during 4 Machine Cycle Time is necessary for charging the electron to the sample hold circuit of the 87C408L/808L/P808L which has a resistor (typ. 7 kΩ) and a capacitor (typ. 11pF).

Not Recommended for New Design

(2) Reading of A/D conversion result

After the end of conversion (EOCF = 1), read the conversion result from the ADCDR. The EOCF is automatically cleared to "0" when reading the ADCDR. When the conversion result is read out during A/D conversion, the invalid value is read out.

(3) A/D conversion in STOP mode

When the MCU places in the STOP mode during the A/D conversion, the conversion is terminated and the A/D conversion value become indefinite. Thus EOCF is maintained to "0" after returned from the STOP mode. However, if the STOP mode is started after the end of A/D conversion (EOCF = "1"), the A/D conversion value and EOCF state are held.

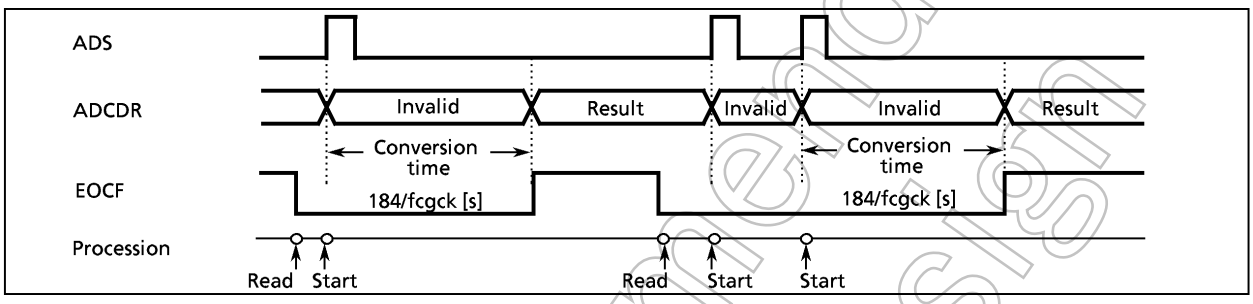


Figure 2-38. A/D Conversion Timing Chart (ACK = 0)

Example: After AIN4 pin is selected as an analog input channel, A/D conversion is started. EOCF is confirmed and the converted result is read out. It is saved to address $009E_H$ in RAM.

```
        ; AIN SELECT
        LD      (ADCCR) , 00000100B     ; selects AIN4
        ; A/D CONVERT START
        SET     (ADCCR) . 6             ; ADS = 1
SLOOP:  TEST    (ADCCR) . 7             ; EOCF = 1 ?
        JRS     T, SLOOP
        ; RESULT DATA READ
        LD      (9EH), (ADCDR)
```

Figure 2-39 shows the relationship between An analog input voltage and A/D converted 8-bit digital value.

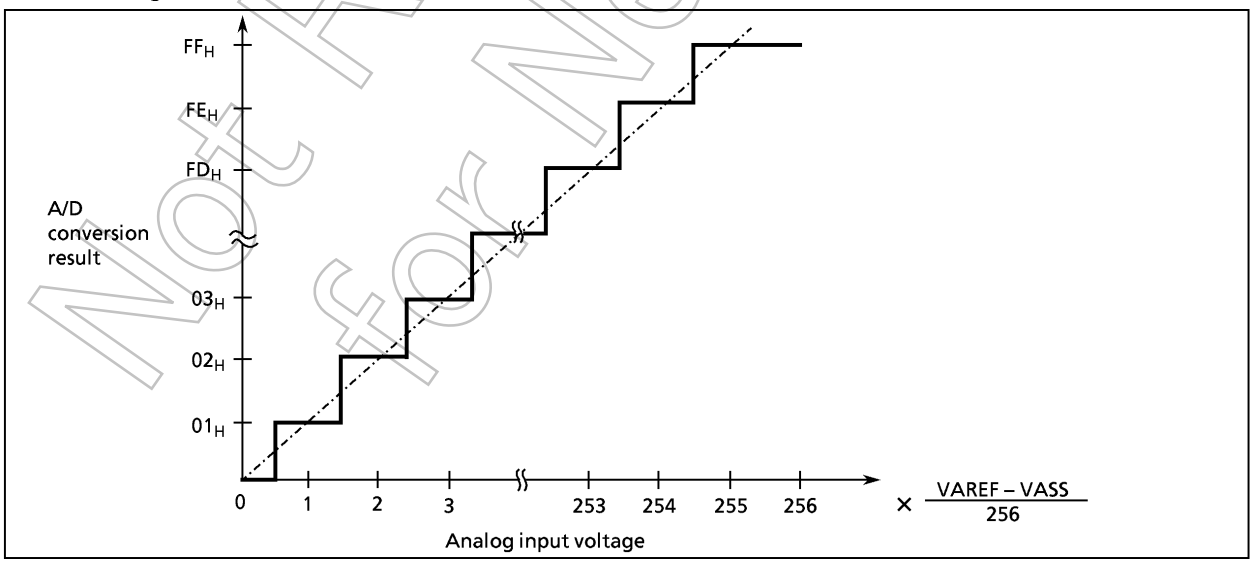


Figure 2-39. Analog Input Voltage vs. A/D Conversion Result (typ.)

Not Recommended for New Design

2.9 Key Wake Up

The87C408/808/408L/808L can control STOP mode with four pins such as P62, P63, P64 and P65 other than P76 ($\overline{INT5}/\overline{STOP}$).
When the STOP mode is controlled in port inputs of P62, P63, P64 and P65, system register 1 (SYSCR1) must start the STOP mode (Level release mode). Edge mode cannot use at key wake-up.

STOP mode control register

STOPCR ($002F_H$)	7	6	5	4	3	2	1	0
	–	–	STOP5	STOP4	STOP3	STOP2	–	–

(Initial value: **0000**)

STOP2	P62 port releases from STOP mode	0: Disable 1: Enable	Read / Write
STOP3	P63 port releases from STOP mode	0: Disable 1: Enable	
STOP4	P64 port releases from STOP mode	0: Disable 1: Enable	
STOP5	P65 port releases from STOP mode	0: Disable 1: Enable	

Figure 2-40. Stop Mode Control Register

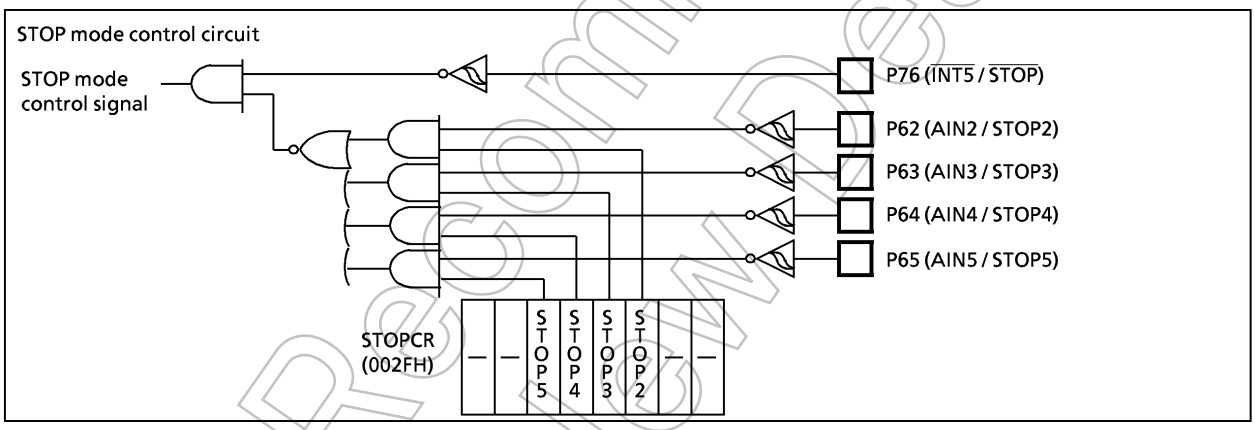


Figure 2-41. Stop Mode Control Circuit

Each bit of P62 to P65 can be individually connected with internal pull-up resistor under the STOP mode control register (STOPCR).

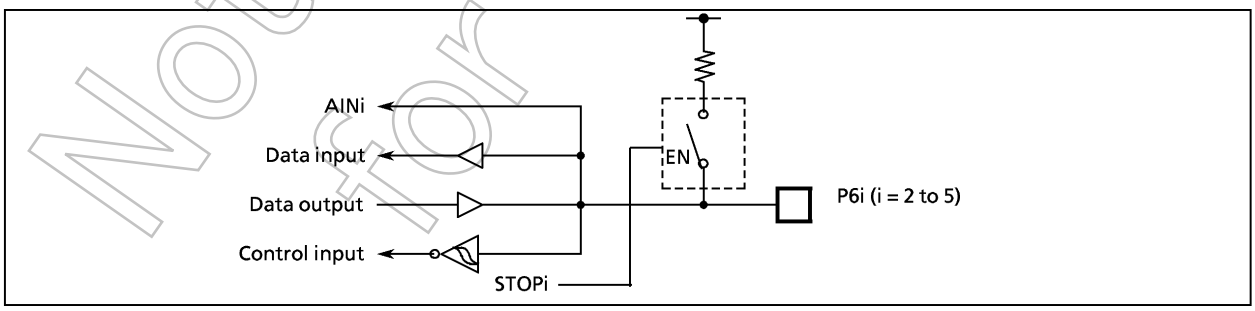


Figure 2-42. Port P6i (i = 2 to 5)

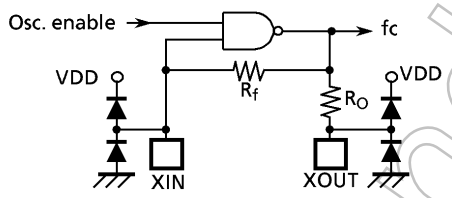
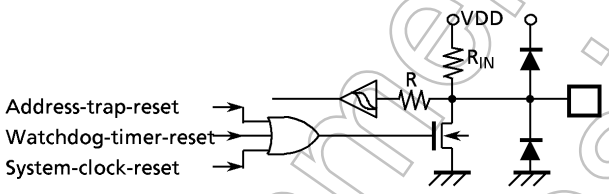
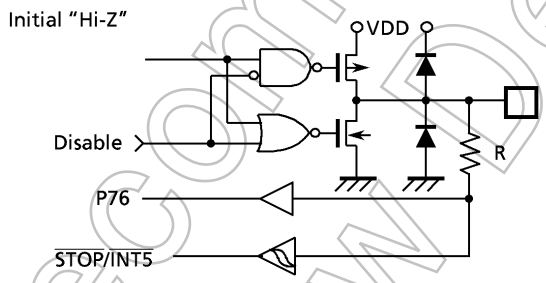
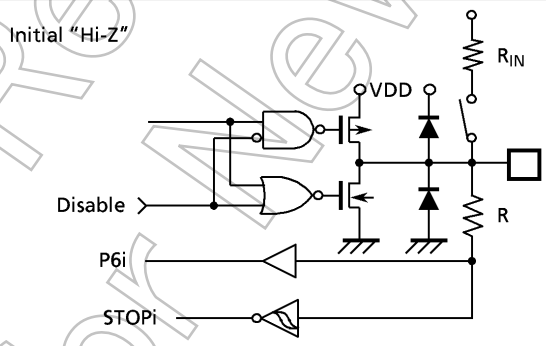
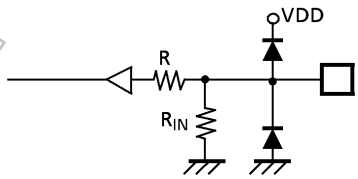
Note: In case of using port P65 to P62 as key wake-up input, P76 pin must be used as input only (in cluding $\overline{INT5}/\overline{STOP}$), must not be used as output port.

Not Recommended for New Design

Input / Output Circuit

(1) Control pins

The input/output circuits of the 87C408/808/408L/808L control pins are shown below.

Control Pin	I/O	Input / Output Circuitry and Code	Remarks
XIN XOUT	Input Output		High-frequency resonator connecting pin R_f = 1.2 MΩ (typ.) R_O = 1.5 kΩ (typ.)
RESET	I/O		Sink open drain output Hysteresis input Pull-up resistor R_{IN} = 220 kΩ (typ.) R = 1 kΩ (typ.)
$\overline{\text{STOP}}$/INT5 (P76)	Input		Hysteresis input R = 1 kΩ (typ.)
STOPi (P6i)	Input		Hysteresis input i = 2 to 5 Pull-up resistor R_{IN} = 70 kΩ (typ.) (87C408/808) R_{IN} = 130 kΩ (typ.) (87C408L/808L) R = 1 kΩ (typ.)
TEST	Input		Pull-down resister R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)

Note: The 87P808/808L does not have a pull-down resistor for TEST pin. Be sure to fix the TEST Pin to low.

Not Recommended for New Design

(2) Input / Output Ports

The input / output circuits of the 87C408/808/408L/808L input / output ports are shown below.

Port	I/O	Input / Output Circuitry and Code	Remarks
P1	I/O	Initial "Hi-Z" VDD Disable R	Tri-state I/O Hysteresis input R = 1 kΩ (typ.)
P6	I/O	Initial "Hi-Z" VDD Disable R	Tri-state I/O R = 1 kΩ (typ.)
P7	I/O	Initial "Hi-Z" P-ch Control VDD Disable R	Tri-state I/O R = 1 kΩ (typ.)

Not Recommended for New Design

Electrical Characteristics

(1) 87C408/808

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter		Symbol	Conditions		Ratings	Unit
Supply Voltage		V_{DD}			– 0.3 to 6.5	V
Input Voltage		V_{IN}			– 0.3 to V_{DD} + 0.3	V
Output Voltage		V_{OUT}			– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	IOL	I_{OUT1}	P1, P6		3.2	mA
		I_{OUT2}	P7 (Middle current port)		15	mA
	IOH	I_{OUT3}	P1, P6, P7		– 1.8	mA
Output Current (Total)	IOL	Σ I_{OUT1}	P1, P6		50	mA
		Σ I_{OUT2}	P7 (Middle current port)		60	mA
	IOH	Σ I_{OUT3}	P1, P6, P7		30	mA
Power Dissipation [Topr = 70°C]		PD		SDIP	300	mW
				SOP	180	
Input Current		I_{IN1}	P1, P6, P7		1.0	mA
		I_{IN2}			– 1.0	
Soldering Temperature (time)		Tsld			260 (10 s)	°C
Storage Temperature		Tstg			– 55 to 125	°C
Operating Temperature		Topr			– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL mode	4.5	5.5	V
				IDLE mode			
			fc = 4.2 MHz	NORMAL mode	2.7		
				IDLE mode			
			STOP mode		2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$2.7\ V \leqq V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$2.7\ V \leqq V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		1.0	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL mode and IDLE mode.

Note 3: Minimum of clock frequency: 1 MHz ≦ fcgck

Not Recommended for New Design

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions			Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs				–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V			–2	–	2	μA
	I_{IN2}	Tri-state ports							
	I_{IN3}	$\overline{RESET}$, STOPi							
Input Resistance	R_{IN1}	TEST				30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$				100	220	450	
	R_{IN3}	STOPi	i = 2 to 5			30	70	150	
Output Leakl Current	I_{LO}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0V			–2	–	2	μA
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA			4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P7	V_{DD} = 4.5V, I_{OL} = 1.6 mA			–	–	0.4	V
Output Low Current	I_{OL3}	P7	V_{DD} = 4.5 V, V_{OL} = 1.0 V			–	7	–	mA
Supply Current in NORMAL mode	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz V_{IN} = 5.3 V / 0.2V	fcgck	fc	–	6.5	10	mA
					fc/2	–	4.0	6.4	
					fc/4	–	2.6	4.7	
					fc/8	–	1.9	3.9	
Supply Current in IDLE mode				fcgck	fc	–	3.3	5.0	
					fc/2	–	2.4	3.9	
					fc/4	–	1.9	3.5	
					fc/8	–	1.6	3.3	
Supply Current in NORMAL mode			V_{DD} = 3.0 V fc = 4.19 MHz V_{IN} = 2.8 V / 0.2V	fcgck	fc	–	1.5	2.5	
					fc/2	–	0.85	1.6	
					fc/4	–	0.6	1.2	
Supply Current in IDLE mode				fcgck	fc	–	0.8	1.4	
					fc/2	–	0.55	1.1	
					fc/4	–	0.45	0.9	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V			–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C, VDD = 5 V.
Note 2: Input Current I_{IN1}, I_{IN3}: The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.
Note 3: I_{DD} ; Except for I_{REF}

Not Recommended for New Design

A/D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		2.7	–	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage Range	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Reference Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} (V_{SS}) = 0.0 V	–	0.8	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V V_{AREF} = 5.000 V V_{ASS} (V_{SS}) = 0.000 V or V_{DD} = 2.7 V V_{AREF} = 2.700 V V_{ASS} (V_{SS}) = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note: Quantizing error is not contained in those errors.

TMP87C408DM

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Nonlinearity Error		V_{DD} = 2.7 V V_{AREF} = 2.700 V V_{ASS} (V_{SS}) = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 3	
Full Scale Error			–	–	± 3	
Total Error			–	–	± 4	

Note: For the TMP87C408, the guaranteed value for A/D conversion accuracy is different when V_{DD} = 2.7 V.

Not Recommended for New Design

A.C. Characteristics (Ⅰ)

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

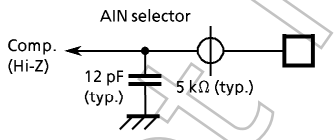
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL mode	0.5	–	4	μs
		In IDLE mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}	fc = 8 MHz (XIN input)				
A/D Conversion Time	t_{ADC}	ACK = 0	–	46	–	tcy
		ACK = 1		184		
A/D Sampling Time	t_{AIN}		–	4		

A.C. Characteristics (Ⅱ)

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

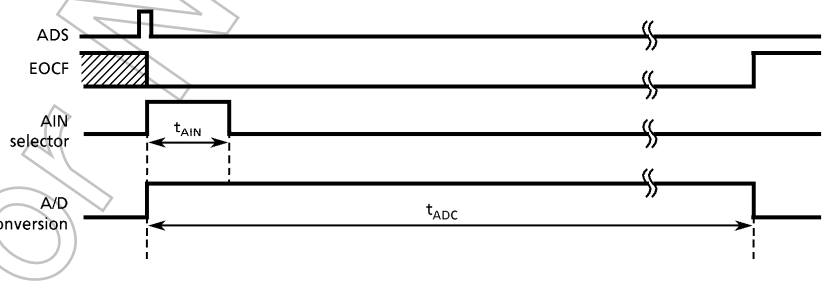
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL mode	0.95	–	4	μs
		In IDLE mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation	110	–	–	ns
Low Level Clock Pulse Width	t_{WCL}	fc = 4.2 MHz				
A/D Conversion Time	t_{ADC}	ACK = 0	–	46	–	tcy
		ACK = 1		184		
A/D Sampling Time	t_{AIN}		–	4		

Note: A/D conversion timing:
Internal circuit for AIN0 to 5



※ To keep the same level of an analog input during t_{AIN} is necessary for charging the electron to the sample hold circuit.

A/D conversion timing



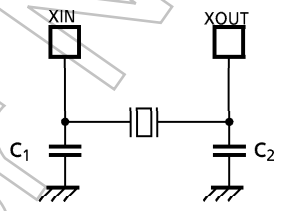
Not Recommended for New Design

Recommended Oscillating Conditions (Ⅰ) (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Conditions C_1	Recommended Conditions C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz (VDD = 4.5 to 5.5 V)	KYOCERA	KBR8.0M	30 pF	30 pF
			MURATA	CSAC8.00MT	30 pF	30 pF
			MURATA	CSA8.00MTZ CST8.00MTW CSTS8.00MT	—	—
		4.19 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.19MG	30 pF	30 pF
			MURATA	CST4.19MGW	—	—
		4 MHz (VDD = 2.7 to 5.5 V)	KYOCERA	KBR4.0MS	30 pF	30 pF
	Crystal Oscillator	8 MHz (VDD = 4.5 to 5.5 V)	TOYOCOM	210B 8.0000	20 pF	20 pF
		4 MHz (VDD = 2.7 to 5.5 V)	TOYOCOM	204B 4.000		

Recommended Oscillating Conditions (Ⅱ) (V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Conditions C_1	Recommended Conditions C_2
High-frequency Oscillation	Ceramic Resonator	4.19 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.19MG	30 pF	30 pF
			MURATA	CST4.19MGW	—	—
		4 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.00MG	30 pF	30 pF
				CSA4.00MGC	—	—
			MURATA	CST4.00MGW CSTC4.00MG	—	—
			MURATA	CSTCS4.00MG	—	—



(1) High-frequency Oscillation

Note: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

Not Recommended for New Design

Electrical Characteristics

(1) 87C408L/808L

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter		Symbol	Conditions		Ratings	Unit
Supply Voltage		V_{DD}			– 0.3 to 5.5	V
Input Voltage		V_{IN}			– 0.3 to V_{DD} + 0.3	V
Output Voltage		V_{OUT}			– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	IOL	I_{OUT1}	P1, P6		3.2	mA
		I_{OUT2}	P7 (Middle current port)		15	mA
	IOH	I_{OUT3}	P1, P6, P7		– 1.8	mA
Output Current (Total)	IOL	Σ I_{OUT1}	P1, P6		50	mA
		Σ I_{OUT2}	P7 (Middle current port)		60	mA
	IOH	Σ I_{OUT3}	P1, P6, P7		30	mA
Power Dissipation [Topr = 70°C]		PD		SDIP	300	mW
				SOP	180	
Input Current		I_{IN1}	P1, P6, P7		1.0	mA
		I_{IN2}			– 1.0	
Soldering Temperature (time)		Tsld			260 (10 s)	°C
Storage Temperature		Tstg			– 55 to 125	°C
Operating Temperature		Topr			– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 4.2 MHz	NORMAL mode	1.8	4.0	V
				IDLE mode			
			STOP mode				
Input High Voltage	V_{IH}				V_{DD} × 0.90	V_{DD}	V
Input Low Voltage	V_{IL}				0	V_{DD} × 0.10	V
Clock Frequency	fc	XIN, XOUT	V_{DD} = 1.8 to 4.0 V		1.0	4.2	MHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL mode and IDLE mode.

Note 3: Minimum of clock frequency: 1 MHz ≦ fcgck

Not Recommended for New Design

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions			Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs				–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 4.0 V V_{IN} = 4.0 V / 0 V			–2	–	2	μA
	I_{IN2}	Tri-state ports							
	I_{IN3}	RESET, STOP							
Input Resistance	R_{IN1}	TEST				30	70	150	kΩ
	R_{IN2}	RESET				100	220	450	
	R_{IN3}	STOPi	i = 2 to 5			30	130	150	
Output Leakl Current	I_{LO}	Tri-state ports	V_{DD} = 4.0 V, V_{OUT} = 4.0 V / 0V			–2	–	2	μA
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.0 V, I_{OH} = – 0.5 mA			3.6	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P7	V_{DD} = 4.0V, I_{OL} = 1.3 mA			–	–	0.4	V
Output Low Current	I_{OL3}	P7	V_{DD} = 4.0 V, V_{OL} = 1.0 V			–	6	–	mA
Supply Current in NORMAL mode	I_{DD}			fcgck	fc	–	2.25	3.6	mA
					fc/2	–	1.35	2.5	
					fc/4	–	0.9	1.9	
Supply Current in IDLE mode				fcgck	fc	–	1.2	1.9	
					fc/2	–	0.9	1.7	
					fc/4	–	0.7	1.5	
Supply Current in NORMAL mode				fcgck	fc	–	1.5	2.5	
					fc/2	–	0.85	1.6	
					fc/4	–	0.6	1.2	
Supply Current in IDLE mode				fcgck	fc	–	0.8	1.4	
					fc/2	–	0.55	1.1	
					fc/4	–	0.45	0.9	
Supply Current in NORMAL mode				fcgck	fc	–	0.9	1.3	
					fc/2	–	0.5	0.8	
					fc/4	–	0.3	0.45	
Supply Current in IDLE mode				fcgck	fc	–	0.35	0.5	
					fc/2	–	0.23	0.35	
					fc/4	–	0.17	0.26	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V			–	0.5		μA

Note 1: Typical values show those at Topr = 25°C, VDD = 4 V.
Note 2: Input Current I_{IN1}, I_{IN3}: The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.
Note3: I_{DD} ; Except for I_{REF}

Not Recommended for New Design

A/D Conversion Characteristics (I)

(V_{SS} = 0V, V_{DD} = 1.8 to 4.0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		1.8	–	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage Range	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Nonlinearity Error		1.8 V ≦ V_{AREF} < 2.7 V V_{AREF} ≦ V_{DD} ≦ 4.0 V_{ASS} (V_{SS}) = 0.000 V ACK = 1 (Note2)	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

Note1: Quantizing error is not contained in those errors.
Note2: ACK ; bit5 of ADCCR (#000E_H) . conversion time = 184 tcy (175.6 μs / at fcgck = 4.19 MHz)

A/D Conversion Characteristics (II)

(V_{SS} = 0V, V_{DD} = 2.7 to 4.0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		2.7	–	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage Range	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Reference Current	I_{REF}	V_{AREF} = 4.0V, V_{ASS} (V_{SS}) = 0.0V	–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 4.0 V V_{AREF} = 4.000 V V_{ASS} (V_{SS}) = 0.000 V or V_{DD} = 2.7 V V_{AREF} = 2.700 V V_{ASS} (V_{SS}) = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note: Quantizing error is not contained in those errors.

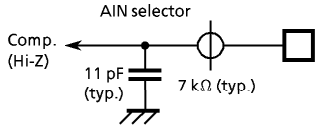
Not Recommended for New Design

A.C. Characteristics

(V_{SS} = 0 V, V_{DD} = 1.8 to 4.0 V, Topr = – 30 to 70°C)

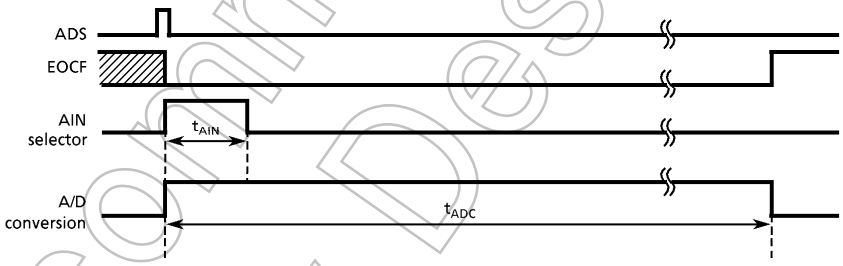
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL mode	0.95	–	4	μs
		In IDLE mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation fc = 4.2 MHz	110	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
A/D Conversion Time	t_{ADC}	ACK = 0	–	46	–	tcy
		ACK = 1		184		
A/D Sampling Time	t_{AIN}		–	4		

Note: A/D conversion timing:
Internal circuit for AIN0 to 5



※ To keep the same level of an analog input during t_{AIN} is necessary for charging the electron to the sample hold circuit.

A/D conversion timing

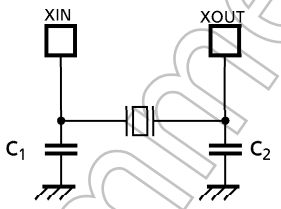


Not Recommended for New Design

Recommended Oscillating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Conditions C_1	Recommended Conditions C_2
High-frequency Oscillation	Ceramic Resonator	4.19 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.19MG	30 pF	30 pF
			MURATA	CST4.19MGW	—	—
		4 MHz (VDD = 2.7 to 5.5 V)	MURATA	CSA4.00MG	30 pF	30 pF
				CSA4.00MGC	—	—
			MURATA	CST4.00MGW CSTC4.00MG	—	—
			MURATA	CSTCS4.00MG	—	—



(1) High-frequency Oscillation

Note: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

Not Recommended for New Design

Not Recommended for New Design