TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91PW18AFG

Not Recommended for New Design

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

CAUTION
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0 to INT4), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Not Recommended for New Design

Low Voltage/Low Power

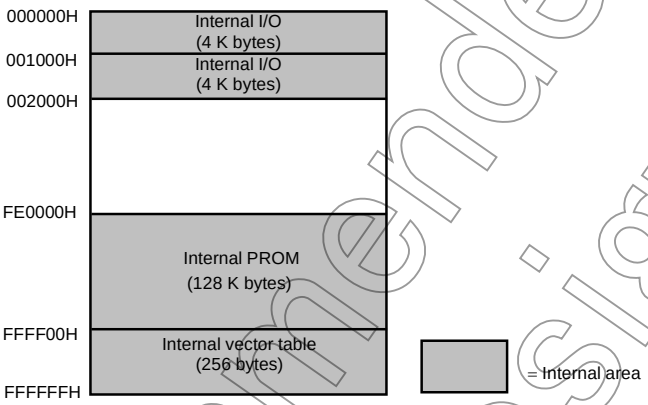
CMOS 16-Bit Microcontroller

TMP91PW18AFG

1. Outline and Device Characteristics

TMP91PW18A is OTP type MCU which 128-Kbyte one-time PROM. Using the adapter-socket, you can write and verify the data for TMP91PW18A. TMP91PW18A has the same pin-assignment with TMP91CW18A (Mask ROM type).

Writing the program to built-in PROM, TMP91PW18A operates as the same way with TMP91CW18A.



Memory map of TMP91PW18A

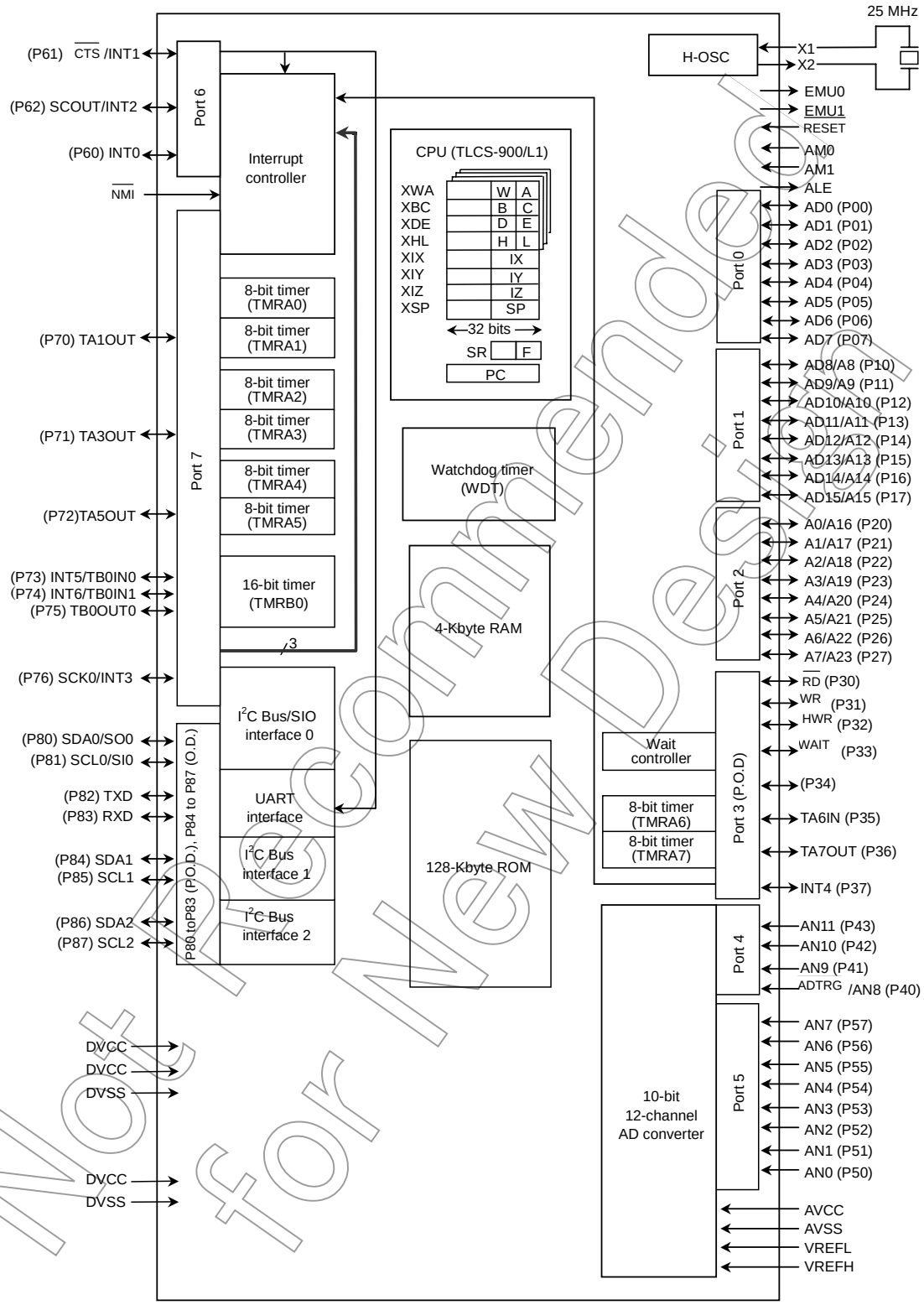
Product Number	ROM	RAM	Package	Adaptor Socket
TMP91PW18AFG	OTP 128 Kbytes	4 Kbytes	QFP80-P-1420-0.80B	BM11179

Not Recommended for New Design

RESTRICTIONS ON PRODUCT USE

20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.).These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in his document shall be made at the customer's own risk.
- The products described in this document shall not be used or embedded to any downstream products of which manufacture, use and/or sale are prohibited under any applicable laws and regulations.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patents or other rights of TOSHIBA or the third parties.
- Please contact your sales representative for product-by-product details in this document regarding RoHS compatibility. Please use these products in this document in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances. Toshiba assumes no liability for damage or losses occurring as a result of noncompliance with applicable laws and regulations.
- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.



( ): Initial function after reset

Not Recommended for New Design

Figure 1.1 Block Diagram of TMP91PW18A

2. Pin Assignment and Functions

This section shows TMP91PW18A pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1.1 is a pin assignment diagram for TMP91PW18A.

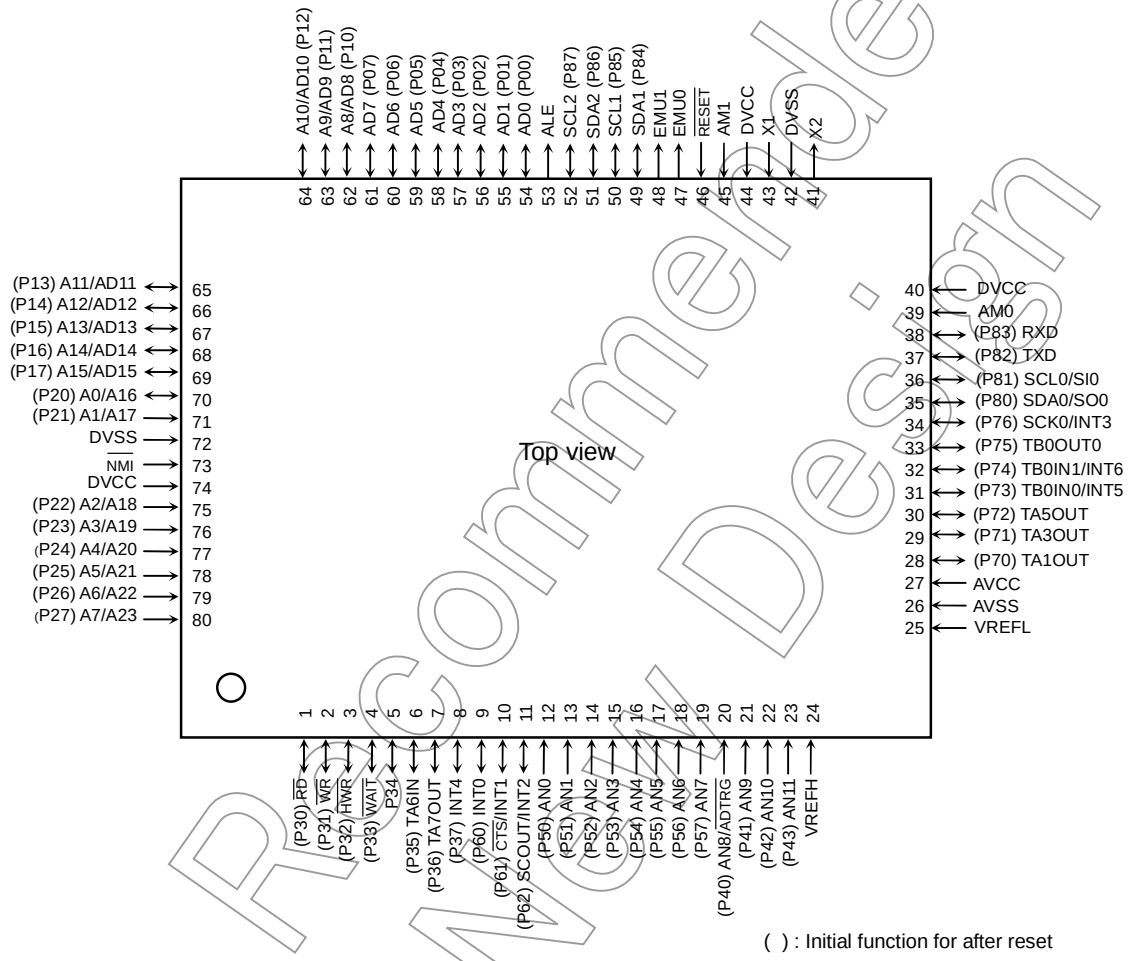


Figure 2.1.1 Pin Assignment Diagram (80-pin QFP)

Not Recommended for New Design

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Table 2.2.1 Pin Names and Functions (1/3)

Pin Name	Number of Pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (Lower): Bits 0 to 7 of address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (Upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	1	I/O Output	Port 30: I/O port By setting (P3<P30> = 0, P3FC<P30FC> = 1), $\overline{RD}$ signal is generated during reading internal areas. Read: Strobe signal for reading external memory Open-drain output pin by programmable
P31 $\overline{WR}$	1	I/O Output	Port 31: I/O port Write: Strobe signal for writing data to pins AD0 to AD7 Open-drain output pin by programmable
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High Write: Strobe signal for writing data to pins AD8 to AD15 Open-drain output pin by programmable
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait Open-drain output pin by programmable
P34	1	I/O	Port 34: I/O port Open-drain output pin by programmable
P35 TA6IN	1	I/O Input	Port 35: I/O port Timer A6 input Open-drain output pin by programmable
P36 TA7OUT	1	I/O Output	Port 36: I/O port Timer A7 output Open-drain output pin by programmable
P37 INT4	1	I/O Input	Port 37: I/O port Interrupt request pin 4: Interrupt request pin with programmable rising edge/falling edge levels Open-drain output pin by programmable
P40 to P43 AN8 to AN11 $\overline{ADTRG}$	4	Input Input Input	Port 40: Pin used to input port Analog input: Pin used to input to AD converter AD Trigger: Signal used to request start of AD conversion
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Pin used to input port Analog input: Pin used to input to AD converter
P60 INT0	1	I/O Input	Port 60: I/O port Interrupt request pin 0: Interrupt request pin with programmable rising edge/falling edge levels
P61 $\overline{CTS}$ INT1	1	I/O Input Input	Port 61: I/O port Serial data send enable (Clear to send) Interrupt request pin 1: Interrupt request pin with programmable rising edge/falling edge levels
P62 SCOUT INT2	1	I/O Output Input	Port 62: I/O port System clock output: outputs f_{FPH} or fs clock Interrupt request pin 2: Interrupt request pin with programmable rising edge/falling edge levels

Not Recommended for New Design

Table 2.2.2 Pin Names and Functions (2/3)

Pin Name	Number of Pins	I/O	Functions
P70 TA1OUT	1	I/O Output	Port 70: I/O port Timer A1 output
P71 TA3OUT	1	I/O Output	Port 71: I/O port Timer A3 output
P72 TA5OUT	1	I/O Output	Port 72: I/O port Timer A5 output
P73 TB0IN0 INT5	1	I/O Input Input	Port 73: I/O port Timer B0 input 0 Interrupt request pin 5: Interrupt request pin with programmable rising edge/falling edge levels
P74 TB0IN1 INT6	1	I/O Input Input	Port 74: I/O port Timer B0 input 1 Interrupt request pin 6: Interrupt request pin with rising edge levels.
P75 TB0OUT0	1	I/O Output	Port 75: I/O port Timer B0 output 0
P76 SCK0 INT3	1	I/O I/O Input	Port 76: I/O port Serial clock I/O 0 Interrupt request pin 3: Interrupt request pin with programmable rising edge/falling edge levels
P80 SO0 SDA0	1	I/O Output I/O	Port 80: I/O port Serial bus interface send data at SIO mode 0 Serial bus interface send/receve data at I^2C mode 0 Open-drain output pin by programmable
P81 SI0 SCL0	1	I/O Input I/O	Port 81: I/O port Serial bus interface receve data at SIO mode 0 Serial bus interface clock I/O data at I^2C mode 0 Open-drain output pin by programmable
P82 TXD	1	I/O Output	Port 82: I/O port Serial send data (UART) Open-drain output pin by programmable
P83 RXD	1	I/O Input	Port 83: I/O port Serial receive data (UART) Open-drain output pin by programmable
P84 SDA1	1	I/O I/O	Port 84: I/O port Serial bus interface send/receive data at I^2C mode 1 N-ch FET open-drain output
P85 SCL1	1	I/O I/O	Port 85: I/O port Serial bus interface clock I/O data at I^2C mode 1 N-ch FET open-drain output
P86 SDA2	1	I/O I/O	Port 86: I/O port Serial bus interface send/receive data at I^2C mode 2 N-ch FET open-drain output
P87 SCL2	1	I/O I/O	Port 87: I/O port Serial bus interface clock I/O data at I^2C mode 2 N-ch FET open-drain output

Not Recommended for New Design

Table 2.2.3 Pin Names and Functions (3/3)

Pin Name	Number of Pins	I/O	Functions
ALE	1	Output	Address latch enable can be disabled to reduce noise
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable
AM0 to AM1	2	Input	Address mode: The VCC pin should be connected
EMU0/EMU1	1	Output	Test pins: Open pins
$\overline{RESET}$	1	Input	Reset: Initializes TMP91CW18A (with pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
X1/X2	2	I/O	High-frequency oscillator connection pins
DVCC	3		Power supply pins (All Vcc pins should be connected with the power supply pin.)
DVSS	2		GND pins (All pins should be connected with GND (0V).)

Not Recommended for New Design

2.3 PROM Mode

Table 2.3.1 Names and Functions of PROM Mode

Pin Function	Pin Number	I/O	Function	Pin Name (MCU mode)
A7 to A0	8	Input	Program memory address input	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Program memory data I/O	P07 to P00
$\overline{CE}$	1	Input	Chip enable input	P32
$\overline{OE}$	1	Input	Output control input	P30
$\overline{PGM}$	1	Input	Program control input	P31
VPP	1	Power supply	12.75 V/5 V (Power supply of program)	AM1
VCC	4	Power supply	6.25 V/5 V	DVCC, AVCC
VSS	4	Power supply	0V	DVSS, AVSS
P34	1	Input	Fix to low level (Security pin)	
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)	
AM0	1	Input		
ALE	1	Output	Open	
X1	1	Input	Crystal	
X2	1	Output		
P43 to P41, P37 to P35, P75 to P70	12	Input	Fix to high level	
P40 P57 to P50 P62 to P60 P87 to P80 VREFH VREFL $\overline{NMI}$, EMU1, EMU0	26	I/O	Open	

Not Recommended for New Design

3. Operation

This section describes in blocks the functions and basic operations of TMP91PW18A.

TMP91PW18A has PROM in place of the mask ROM which is included in the TMP91CW18A.

The other configuration and functions are the same as the TMP91CW18A.

Regarding the function of the TMP91PW18A which is not described herein, see the TMP91CW18A.

The TMP91PW18A has two operational modes: MCU mode and PROM mode.

3.1 MCU Mode

(1) Mode setting and function

The MCU mode is set by driving AM1 pin and AM0 pin. In the MCU mode, the operation is same as TMP91CW18A.

3.2 Memory Map

Figure 3.2.1, 2 are memory map of TMP91PW18A.

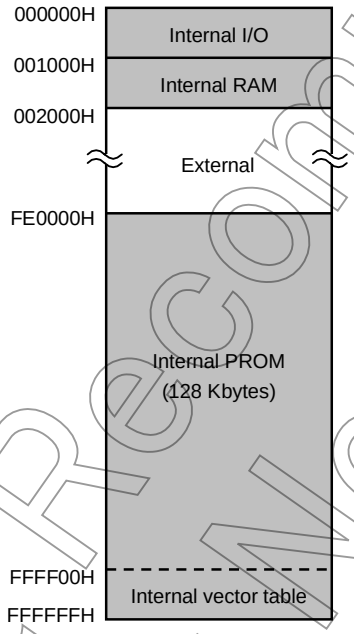


Figure 3.2.1 Memory Map in MCU Mode

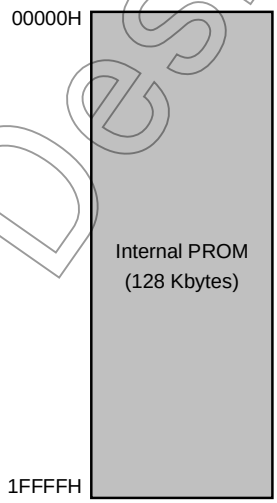


Figure 3.2.2 Memory Map in PROM Mode

Not Recommended for New Design

3.3 PROM Mode

(1) Mode setting and function

PROM mode is set by setting the RESET and AM0 pins to the "L" level, and AM1 pin to "VPP" level. The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adaptor socket.

1. OTP adaptor

   BM11179: TMP91PW18A

2. Setting OTP adaptor

   Set the switch (SW1) to N side.

3. Setting PROM programmer

   i) Set PROM type to TC571000D

      size: 1 Mbit (128 K × 8 bits)

      VPP: 12.75 V

      t_{PW}: 100 μs

   The electric signature mode (Hereinafter referred to as "signature") is not supported. Therefore, if signature is used, the device is damaged because 12.75 V is applied to A9 of address. Do not use signature.

   ii) Transfering the data (Copy)

   In TMP91PW18A, PROM is placed on addresses 00000H to 1FFFFH in PROM mode, and addresses FE0000H to FFFFFFH in MCU mode.

   Therefore data should be transferred to addresses 00000H to 1FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode (See instruction manual of PROM programmer) or making the object data.

   iii) Setting the programming address

      Start address: 00000H

      End address: 1FFFFH

4. Programming

   Program/verify according to the procedures of PROM programmer.

Not Recommended for New Design

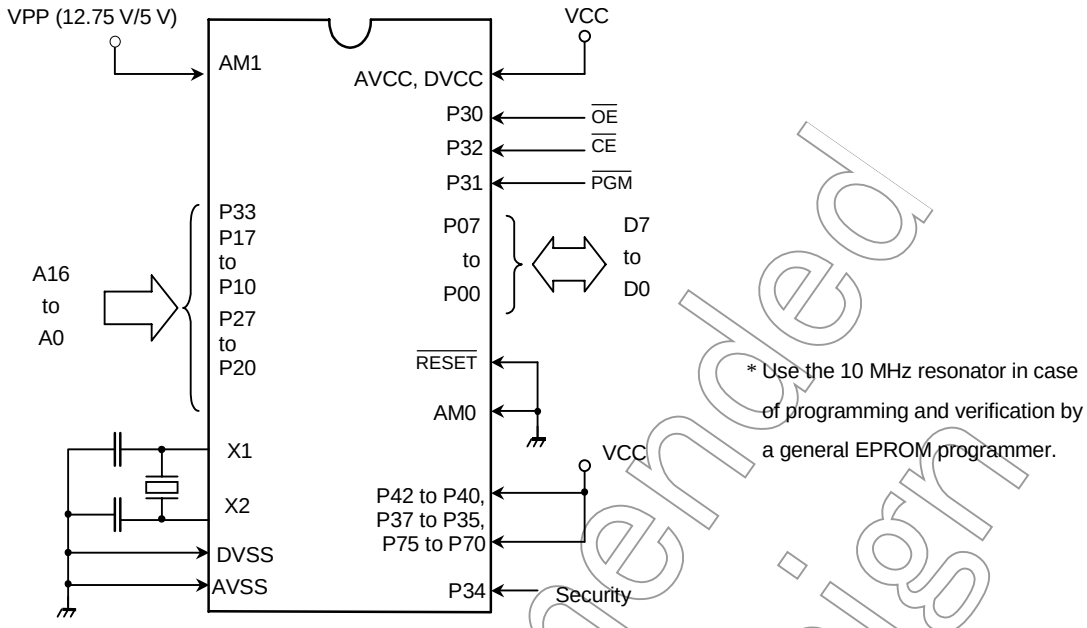


Figure 3.3.1 Setting Pin of PROM Mode

(2) Programming flowchart

The programming mode is set by applying 12.75 V (Programming voltage) to the AM1 pin when the following pins are set as follows (VCC: 6.25 V, $\overline{\text{RESET}}$: "L" level, AM0: "L" level).

While address and data are fixed and CE pin is set to "L" level, 0.1 ms of "L" level pulse is applied to PGM pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to PGM pin.

The programming procedure is repeated until correct data is read from the address (25 times maximum).

Subsequently, all data are programmed in all address.

The verification for all data is done under the condition of AM1 = VCC = 5 V after all data were programmed. Figure 3.3.2 shows the programming flowchart.

Not Recommended for New Design

High speed programming.

Flowchart

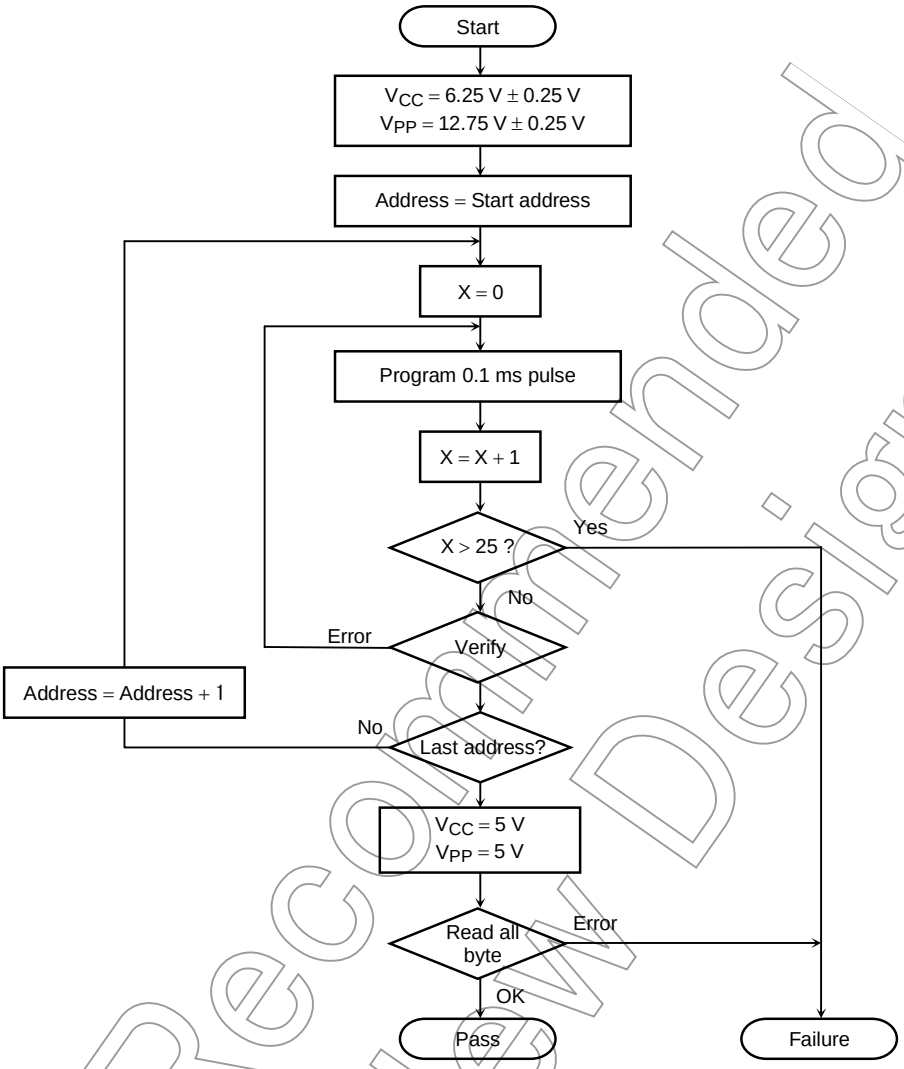


Figure 3.3.2 Flow Chart

Not Recommended for New Design

(3) Security bit

The TMP91PW18A has a security bit.

If the security bit is programmed to 0, the content of the PROM can not be read in PROM mode.

(How to program the security bit)

The difference from the programming producedures described in section 3.3 1 are follows.

1. Setting OTP adapter

   Set the switch (SW1) to S side.

2. Setting PROM programmer

   i) Transferring the data

   ii) Setting programming address

   The security bit is in bit 0 of address 00000H.

   Set the start address 00000H and the end address 00000H.

   Set the data FEH at the address 00000H.

Not Recommended for New Design

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 6.5	V
Input voltage	VIN	−0.5 to V_{CC} + 0.5	
Output current	IOL	2	mA
Output current	IOH	−2	
Output current (Total)	ΣIOL	80	
Output current (Total)	ΣIOH	−80	
Power dissipation (Ta = 70°C)	PD	600	mW
Soldering temperature (10 s)	TSOLDER	260	°C
Storage temperature	TSTG	−65 to 150	
Operating temperature	TOPR	−30 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Solderability of lead free products

Test parameter	Test condition	Note
Solderability	Use of Sn-37Pb solder Bath Solder bath temperature = 230°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux	Pass: solderability rate until forming ≥ 95%
	Use of Sn-3.0Ag-0.5Cu solder bath Solder bath temperature = 245°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux (use of lead free)	

Not Recommended for New Design

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note)	Max	Unit
Power supply voltage ($AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V)		V_{CC}	fc = 8 to 25 MHz	4.5		5.5	V
Input low voltage	P00 to P17 (AD0 to AD15)	VIL	$V_{CC} \geq 4.5$ V	−0.3		0.8	V
	P20 to P87	VIL1	V_{CC} = 4.5 to 5.5 V			0.3 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$	VIL2				0.25 V_{CC}	
	AM0, AM1	VIL3				0.3	
	X1	VIL4				0.2 V_{CC}	
Input high voltage	P00 to P17 (AD0 to AD15)	VIH	V_{CC} = 4.5 to 5.5 V	0.7 V_{CC}		V_{CC} + 0.3	
	P20 to P87	VIH1	V_{CC} = 4.5 to 5.5 V	0.7 V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$	VIH2		0.75 V_{CC}			
	AM0, AM1	VIH3		V_{CC} − 0.3			
	X1	VIH4		0.8 V_{CC}			
Output low voltage		VOL	IOL = 1.6 mA (V_{CC} = 4.5 to 5.5 V)			0.45	V
Output high voltage		VOH	IOH = − 400 μA (V_{CC} = 5.0 V ± 10 %)	0.8V_{CC}			

Note: Typical values are for when Ta = 25°C and V_{CC} = 5.0 V uncles otherwise noted.

DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ. (Note 1)	Max	Unit
Input leakage current	ILI	0.0 ≤ V_{IN} ≤ V_{CC}			0.02	±5	μA
Output leakage current	ILO	0.2 ≤ V_{IN} ≤ V_{CC} − 0.2			0.05	±10	
Power down voltage (at STOP, RAM backup)	VSTOP	V IL2 = 0.2 V_{CC}, V IH2 = 0.8 V_{CC}		2.0		5.5	V
$\overline{RESET}$ pull-up resistor	RRST	V_{CC} = 5 V ± 10%		40		200	kΩ
Pin capacitance	CIO	fc = 1 MHz				10	pF
Schmitt width $\overline{RESET}$, $\overline{NMI}$	VTH			0.4	1.0		V
Programmable pull-up resistor	RKH	V_{CC} = 5 V ± 10%		40		200	kΩ
NORMAL (Note 2)	I_{CC}	V_{CC} = 5 V ± 10 % fc = 25 MHz (Typ. V_{CC} = 5.0 V)			23.5	35.0	mA
IDLE2					9.5	15.0	
IDLE1					4.4	9.0	
STOP		Ta ≤ 70°C	V_{CC} = 4.5 to 5.5 V		0.2	20	μA

Note 1: Typical values are for when Ta = 25°C and V_{CC} = 5.0 V unless otherwise noted.

Note 2: I_{CC} measurement conditions (NORMAL):
All functions are operational; output pins are open and input pins are fixed.

Not Recommended for New Design

4.3 AC Characteristics

(1) Vcc = 5.0 V ± 10 %

No.	Parameter	Symbol	Variable		f_{FPH} = 25 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} period (= x)	t_{FPH}	40	31250	40		ns
2	A0 to A15 vaild → ALE fall	t_{AL}	0.5x – 15		5		ns
3	ALE fall → A0 to A15 hold	t_{LA}	0.5x – 15		5		ns
4	ALE high width	t_{LL}	x – 20		20		ns
5	ALE fall → $\overline{RD}$ / $\overline{WR}$ fall	t_{LC}	0.5x – 20		0		ns
6	$\overline{RD}$ rise → ALE rise	t_{CLR}	0.5x – 15		5		ns
7	$\overline{WR}$ rise → ALE rise	t_{CLW}	x – 15		25		ns
8	A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACL}	x – 25		15		ns
9	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACH}	1.5x – 50		10		ns
10	$\overline{RD}$ rise → A0 to A23 hold	t_{CAR}	0.5x – 20		0		ns
11	$\overline{WR}$ rise → A0 to A23 hold	t_{CAW}	x – 20		20		ns
12	A0 to A15 valid → D0 to D15 input	t_{ADL}		3.0x – 45		75	ns
13	A0 to A23 valid → D0 to D15 input	t_{ADH}		3.5x – 35		105	ns
14	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.0x – 40		40	ns
15	$\overline{RD}$ low width	t_{RR}	2.0x – 20		60		ns
16	$\overline{RD}$ rise → D0 to D15 hold	t_{HR}	0		0		ns
17	$\overline{RD}$ rise → A0 to A15 output	t_{RAE}	x – 15		25		ns
18	$\overline{WR}$ low width	t_{WW}	1.5x – 20		40		ns
19	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	1.5x – 50		10		ns
20	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	x – 15		25		ns
21	A0 to A23 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode]	t_{AWH}		3.5x – 90		50	ns
22	A0 to A15 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode]	t_{AWL}		3.0x – 80		40	ns
23	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold [(1 + N) WAIT mode]	t_{CW}	2.0x + 0		80		ns
24	A0 to A23 valid → Port input	t_{APH}		3.5x – 120		20	ns
25	A0 to A23 valid → Port hold	t_{APH2}	3.5x		140		ns
26	A0 to A23 valid → Port valid	t_{AP}		3.5x + 100		319	ns

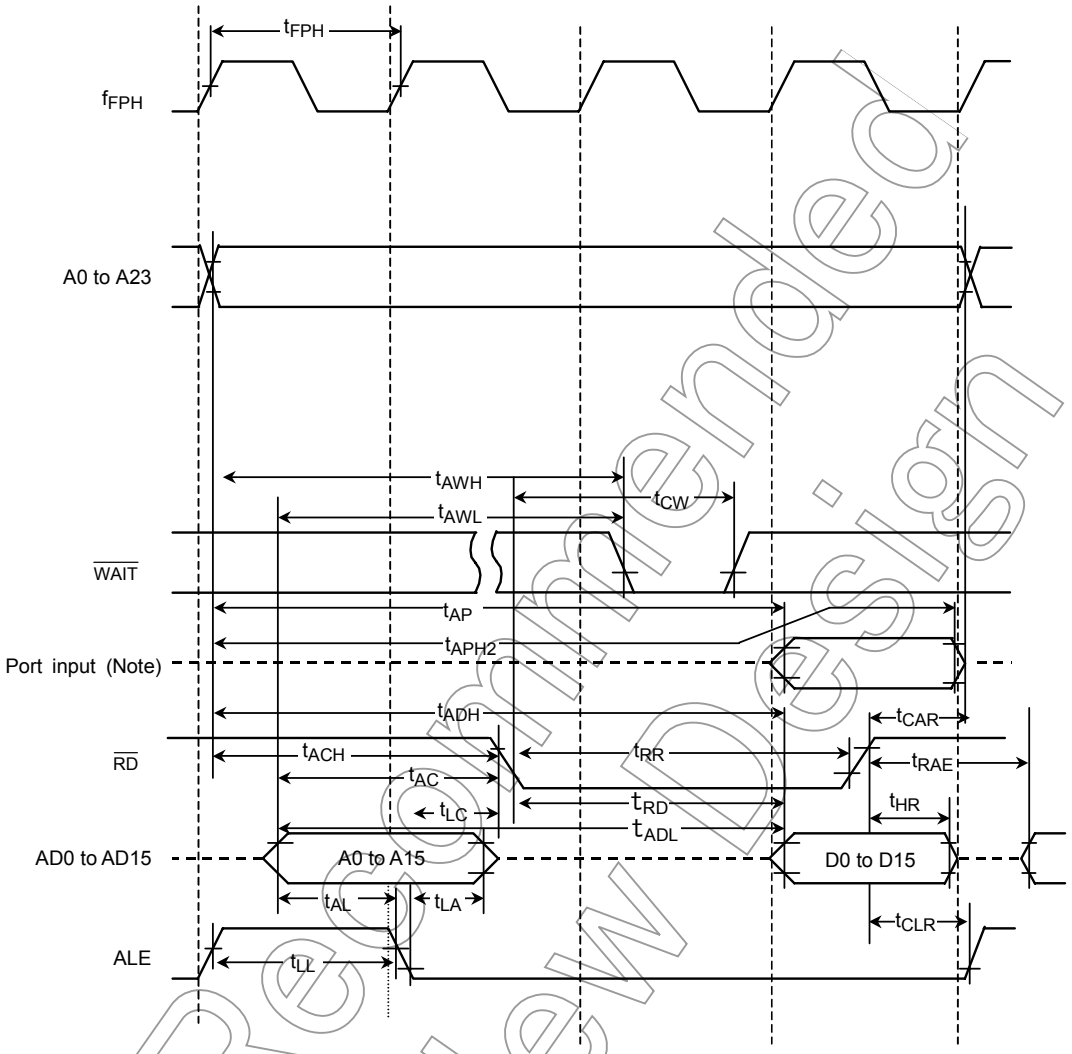
AC measuring conditions

- Output level: High 2.2 V_{CC}/Low 0.8 V_{CC}, CL = 50 pF
- Input level: High 2.4 V_{CC}/Low 0.45 V_{CC} (AD0 to AD15)
  High 0.8 V_{CC}/Low 0.2 V_{CC} (except AD0 to AD15)

Not Recommended for New Design

(2) V_{CC} = 5.0 V ± 10 %

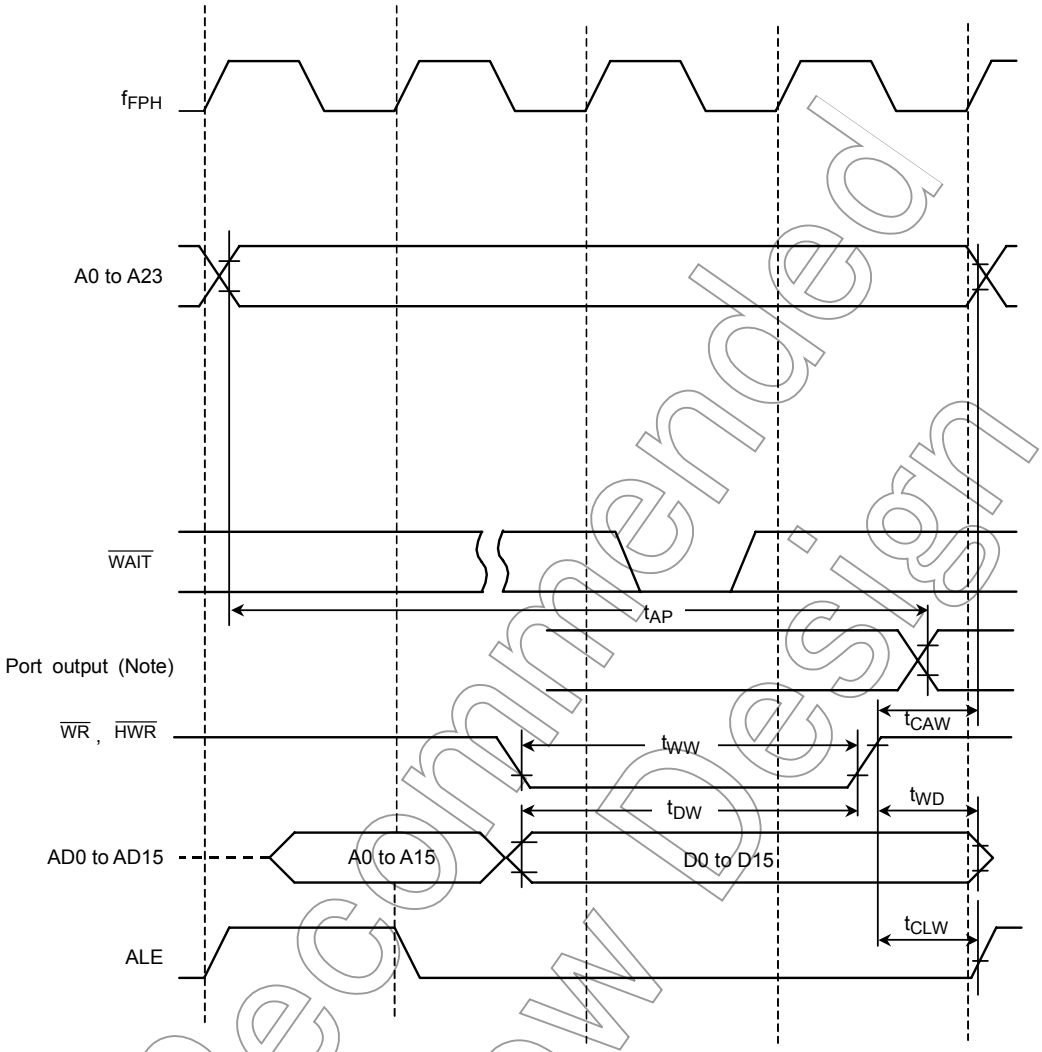
1. Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

Not Recommended for New Design

2. Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

Not Recommended for New Design

4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog input voltage range (+)	VREFH	V_{CC} = 5 V ± 10%	V_{CC} – 1.5 V	V_{CC}	V_{CC}	V
Analog input voltage range (–)	VREFL	V_{CC} = 5 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage range	VAIN		V_{REFL}		V_{REFH}	
Analog input voltage range <VREFON> = 1	IREF (VREFL = 0 V)	V_{CC} = 5 V ± 10%		1.44	2.00	mA
<VREFON> = 0		V_{CC} = 5 V ± 10%		0.02	5.0	μA
Error (Not including quantizing errors)	–	V_{CC} = 5 V ± 10%		±1.0	±4.0	LSB

Note 1: 1 LSB = (VREFH – VREFL)/1024 [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value for I_{CC} includes the current which flows through the AV_{CC} pin.

4.5 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Parameter	Symbol	Variable		25 MHz		Unit
		Min	Max	Min	Max	
Clock period	t_{VCK}	8X + 100		420		ns
Clock low level width	t_{VCKL}	4X + 40		200		ns
Clock high level width	t_{VCKH}	4X + 40		200		ns

4.6 Interrupt, Capture

(1) $\overline{NMI}$, INT0 to INT4 interrupts

Parameter	Symbol	Variable		25 MHz		Unit
		Min	Max	Min	Max	
$\overline{NMI}$, INT0 to INT4 low level width	t_{INTAL}	4X + 40		200		ns
$\overline{NMI}$, INT0 to INT4 high level width	t_{INTAH}	4X + 40		200		ns

(2) INT5 to INT6 interrupts, capture

The INT5 to INT6 input width depends on the system clock and prescaler clock settings.

System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1:0>	t_{INTBL} (INT5 to INT6 low-level width)		t_{INTBH} (INT5 to INT6 high-level width)		Unit
		Variable	f_{FPH} = 25 MHz	Variable	f_{FPH} = 25 MHz	
		Min	Max	Min	Max	
0 (fc)	00 (f_{FPH})	8X + 100	420	8X + 100	420	ns
	10 (fc/16)	128Xc + 0.1	5.22	128Xc + 0.1	5.22	μs

Xc: Period of clock fc

Not Recommended for New Design

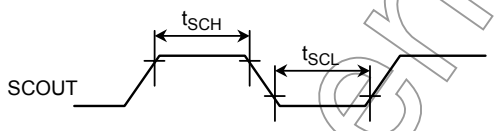
4.7 SCOUT Pin AC Characteristics

Parameter	Symbol	Variable		25 MHz		Condition	Unit
		Min	Max	Min	Max		
Low-level width	t_{SCH}	0.5T – 15		5		V_{CC} = 5 V ± 10%	ns
High-level width	t_{SCL}	0.5T – 15		5		V_{CC} = 5 V ± 10%	ns

T = Period of SCOUT

Measurement condition

Output level: High 0.7 V_{CC}/Low 0.3 V_{CC}, CL = 10 pF



4.8 Read Operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5°C V_{CC} = 5 V ± 10 %

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} read voltage	V_{PP}	–	4.5	5.5	V
Input high voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	–	2.2	V_{CC} + 0.3	
Input low voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	–	–0.3	0.8	
Address to output delay	t_{ACC}	C_L = 50 pF	–	2.25 TCYC + α	ns

TCYC = 400 ns (10 MHz clock)
α = 200 ns

4.9 Program Operation in PROM Mode

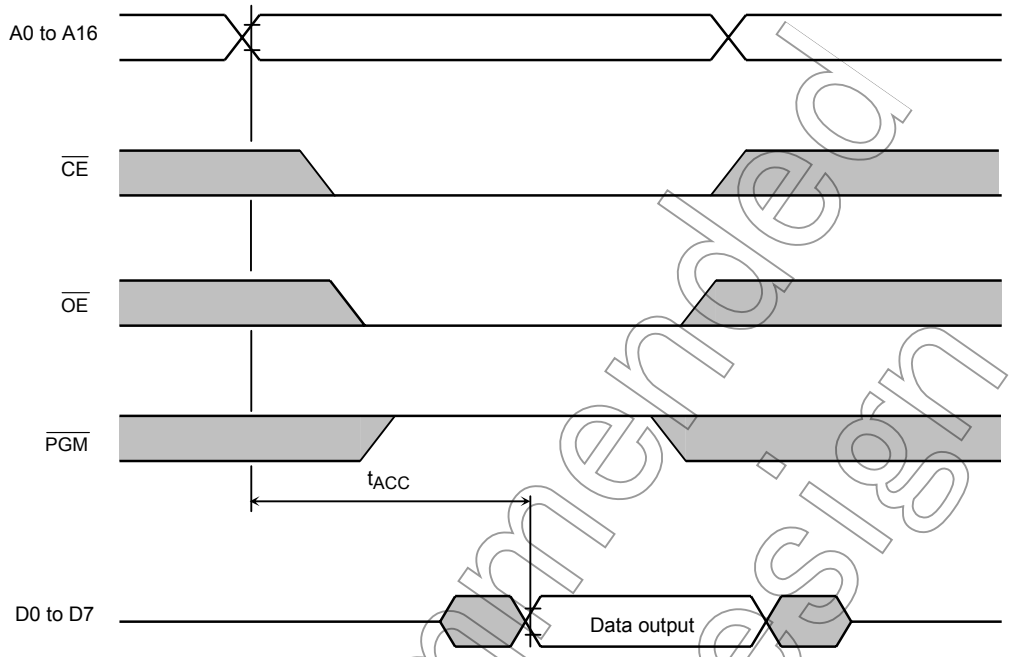
DC/AC characteristics

Ta = 25 ± 5°C V_{CC} = 6.25 V ± 0.25 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Programing supply voltage	V_{PP}	–	12.50	12.75	13.00	V
Input high voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH}	–	2.6		V_{CC} + 0.3	
Input low voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL}	–	–0.3		0.8	
Vcc supply current	I_{CC}	fc = 10 MHz	–		50	mA
V_{PP} supply current	I_{PP}	V_{PP} = 13.00 V	–		50	
$\overline{PGM}$ program pulse width	t_{PW}	C_L = 50 pF	0.095	0.1	0.105	ms

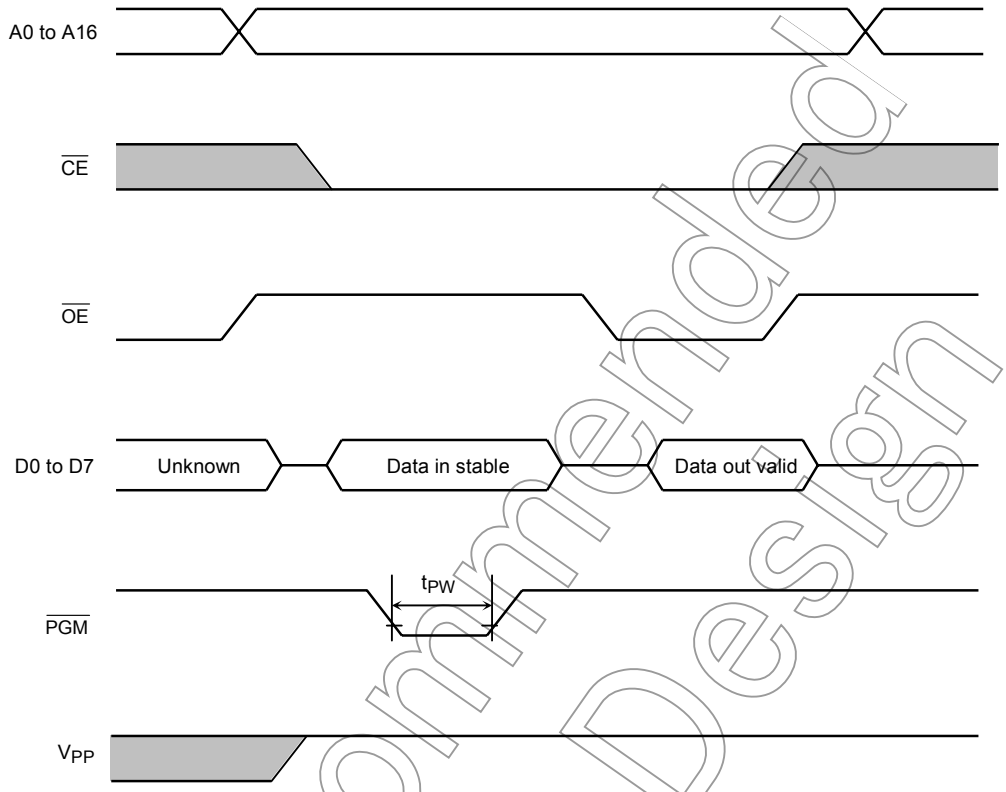
Not Recommended for New Design

4.10 Timing Chart of Read Operation in PROM Mode



Not Recommended for New Design

4.11 Timing Chart of Program Operation in PROM Mode



Note 1: The power supply of V_{PP} (12.75 V) must be turned on at the same time or the later time for a power supply of V_{CC} and must be turned off at the same time or early time for a power supply of V_{CC}.

Note 2: The device suffers a damage taking out and putting in on the condition of V_{PP} = 12.75 V.

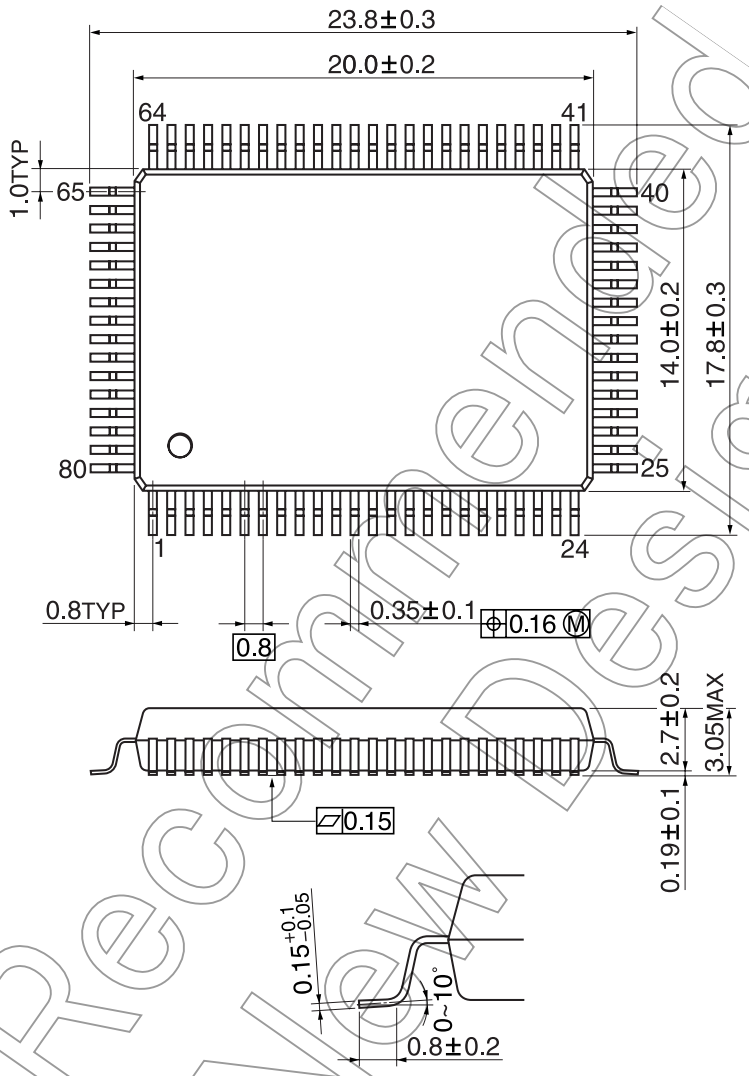
Note 3: The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the programming.

Not Recommended for New Design

5. Package Dimensions

QFP80-P-1420-0.80B

Unit: mm



Not Recommended for New Design