TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91PW11FG

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

CAUTION
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0, INTRTC), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

TOSHIBA Microcontrollers
900 Family
(TMP91CW11) (TMP91PW11)

Datasheet Modifications: I²C Bus Mode Control

The following problem is included in the explanation of the I²C bus function of this data sheet. It will guide the correction as follows. Please read it for the explanation of this data sheet as follows.

▪ **In the explanation of the Serial bus interface Control Register 1 in "I²C bus mode control register"**

1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
2. Add the following note.

Serial clock selection		
000	- (Note)	fc = System clock: fc, Clock gear: fc/1, 20 MHz (Output on SCL PIN)
001	- (Note)	
010	- (Note)	
011	75.8 kHz	
100	38.5 kHz	
101	19.4 kHz	
110	9.73 kHz	
111	(reserved)	

Note: This I²C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I²C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I²C specification is not guaranteed in that case.

▪ **In "I²C bus mode control"**

1. Add the following sentence about the communication baud rate.
2. Modify the equations as shown below.

(3) Serial clock

a. Clock source

SBICR1<SCK2 to 0> are used to select a maximum transfer frequency output on the SCL pin in the master mode. **Set a communication baud rate that meets the I²C bus specification, such as the shortest pulse width of t_{LOW}, based on the equations shown below.** In both master mode and slave mode, a pulse width of at least 4 machine cycles is required for both high and low levels.

$$t_{LOW} = 2^{n-1}/f_{SBI}$$

$$t_{HIGH} = 2^{n-1}/f_{SBI} + 8/f_{SBI}$$

$$fscl = 1/(t_{Low} + t_{HIGH}) = \frac{f_{SBI}}{2^n + 8}$$

Note: f_{SBI} is the clock f_{FPH} which is selected SYSCR0<PRCK1:0>.

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

Previous Part Number (in Body Text)	New Part Number
TMP91PW11F	TMP91PW11FG

2. Package code and dimensions

Previous Package Code (in Body Text)	New Package Code
P-LQFP100-P-1414-0.50C	LQFP100-P-1414-0.50C

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Solderability of lead free products

Test Parameter	Test Condition	Note
Solderability	Use of Sn-37Pb solder Bath Solder bath temperature = 230°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux	Pass: Solderability rate until forming ≥ 95%
	Use of Sn-3.0Ag-0.5Cu solder bath Solder bath temperature = 245°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux (use of lead free)	

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

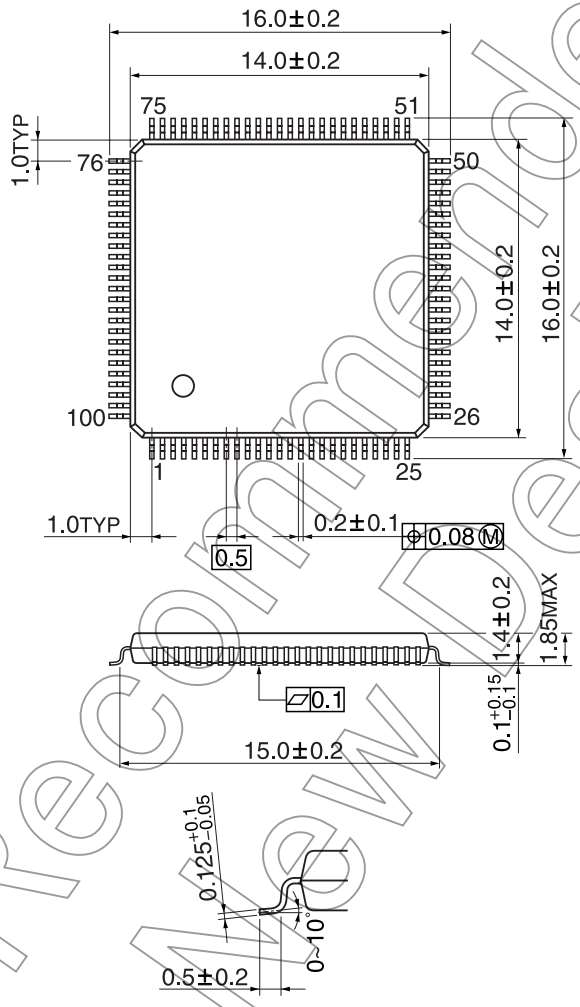
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

LQFP100-P-1414-0.50C

Unit: mm



Low Voltage/Low Power CMOS 16-bit Microcontroller

TMP91PW11F

1. Outline and Device Characteristics

The TMP91PW11 is OTP type MCU which includes 128 Kbyte One-time PROM. Using the adapter-socket, you can write and verify the data for the TMP91CW11 by general EPROM programmer.

The TMP91PW11 has the same pin-assignment as the TMP91CW11 (Mask ROM type).

Writing the program to Built-in PROM, the TMP91PW11 operates as the same way as the TMP91CW11.

MCU	ROM	RAM	Package	Adapter Socket
TMP91PW11F	OTP 128 Kbyte	4 Kbyte	P-LQFP100-1414-0.50C	BM11129

000707EBP1

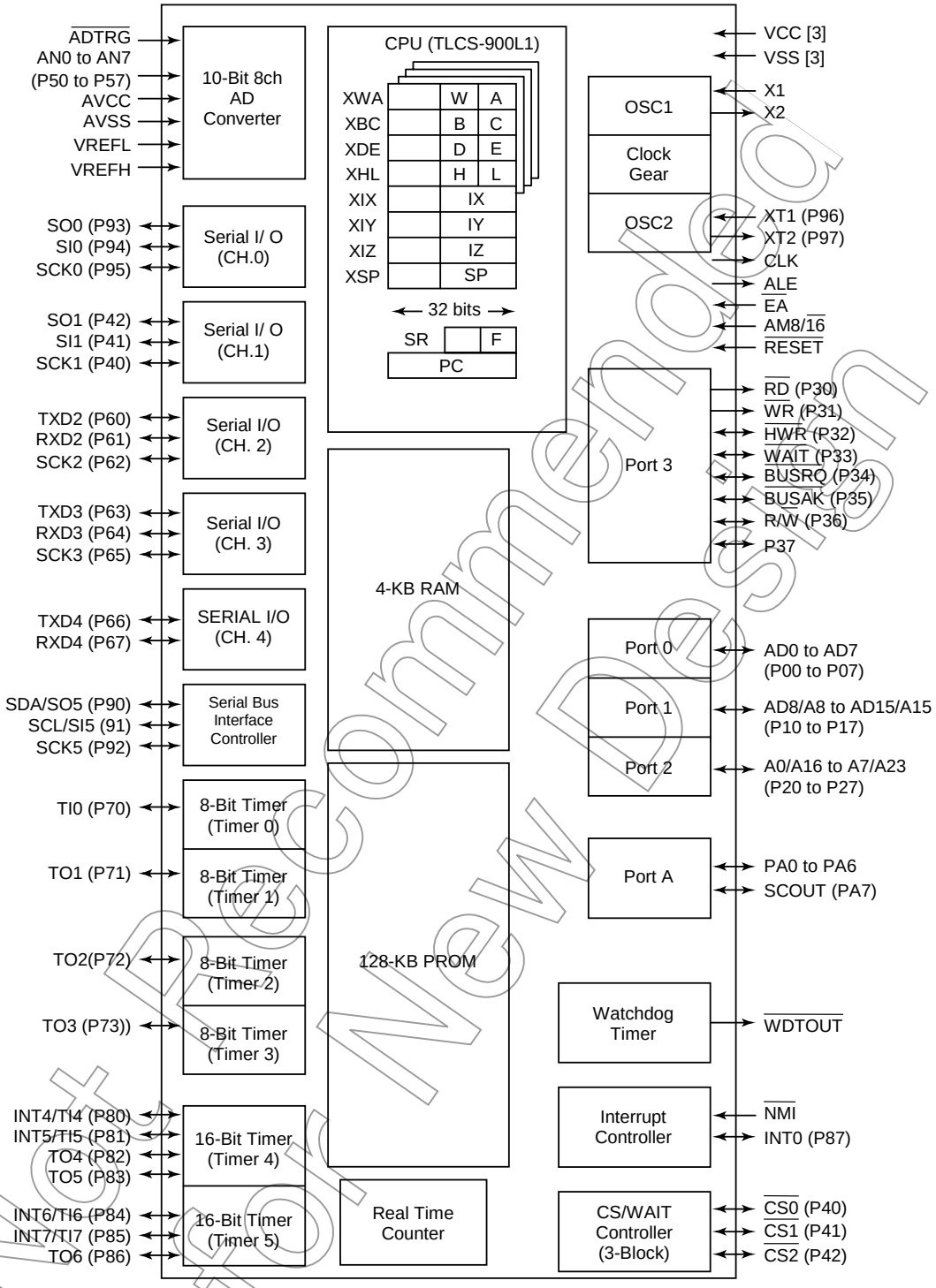


Figure 1.1 TMP91PW11 block diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91PW11F, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of TMP91PW11F.

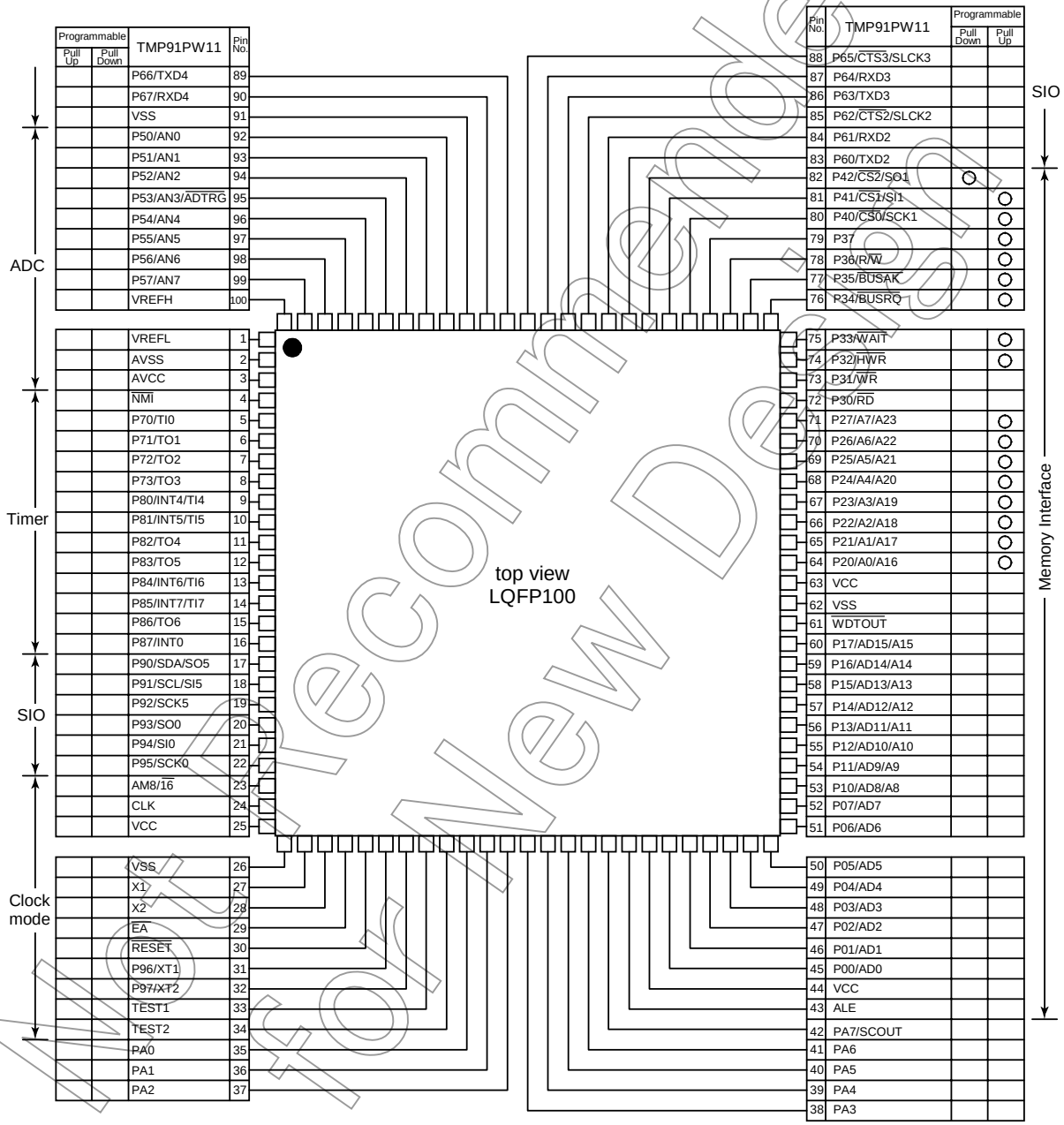


Figure 2.1.1 Pin assignment

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin names and functions (1/4)

Pin name	Number of pins	I/O	Function
P00 to P07	8	I/O	Port 0: I/O port that allows selection of I/O on a bit basis
AD0 to AD7		Tri-state	Address/data (lower): Bits 0 to 7 of address/data bus
P10 to P17	8	I/O	Port 1: I/O port that allows selection of I/O on a bit basis
AD8 to AD15		Tri-state	Address data (upper): Bits 8 to 15 of address/data bus
A8 to A15		Output	Address: 8 to 15 of address bus
P20 to P27	8	I/O	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor)
A0 to A7		Output	Address: Bits 0 to 7 of address bus
A16 to A23		Output	Address: Bits 16 to 23 of address bus
P30	1	Output	Port 30: Output port
$\overline{RD}$		Output	Read: Strobe signal for reading external memory
P31	1	Output	Port 31: Output port
$\overline{WR}$		Output	Write: Strobe signal for writing data on pins AD0 to 7
P32	1	I/O	Port 32: I/O port (with pull-up resistor)
$\overline{HWR}$		Output	High write: Strobe signal for writing data on pins AD8 to 15
P33	1	I/O	Port 33: I/O port (with pull-up resistor)
$\overline{WAIT}$		Input	Wait: Pin used to request CPU bus wait
P34	1	I/O	Port34: I/O port(with pull-up resistor)
$\overline{BUSRQ}$		Input	Bus request: Signal used to request high impedance for AD0 to 15, A0-23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35	1	I/O	Port 35: I/O port (with pull-up resistor)
$\overline{BUSAK}$		Output	Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, R$\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36	1	I/O	Port 36: I/O port (with pull-up resistor)
R/$\overline{W}$		Output	Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor)
P40	1	I/O	Port 40: I/O port (with pull-up resistor)
$\overline{CS0}$		Output	Chip select 0: Outputs 0 when address is within specified address area.
SCK1		I/O	Serial clock I/O 1

Note: This device's built-in memory or built-in I/O cannot be accessed with the external DMA controller, using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.2 Pin names and functions (2/4)

Pin name	Number of pins	I/O	Function
P41	1	I/O	Port 41: I/O port (with pull-up resistor)
$\overline{CS1}$		Output	Chip select 1: Outputs 0 if address is within specified address area.
SI1		Input	Serial receive data 1
P42	1	I/O	Port 42: I/O port (with pull-down resistor)
$\overline{CS2}$		Output	Chip select 2: Outputs 0 if address is within specified address area.
SO1		Output	Serial send data 1
P50 to P52	3	Input	Port5: Input port
AN0 to AN7		Input	Analog input: Analog signal input for AD converter
P53	1	Input	Port 53: Input Port
AN3		Input	Analog input = Analog signal input for AD converter
$\overline{ADTRG}$		Input	AD external trigger
P54 to P57	4	Input	Port 5: Input Port
AN4 to AN7		Input	Analog input: Analog signal input for AD converter
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
P60	1	I/O	Port 60: I/O port (Programmable open drain)
TXD2		Output	Serial send data 2
P61	1	I/O	Port 61: I/O port
RXD2		Input	Serial receive data 2
P62	1	I/O	Port 62: I/O port
$\overline{CTS2}$		Input	serial data send enable 2 (Clear To Send)
SCLK2		I/O	Serial Clock I/O 2
P63	1	I/O	Port 63: I/O port
TXD3		Output	Serial send data 3
P64	1	I/O	Port 64: I/O port
RXD3		Input	Serial receive data 3
P65	1	I/O	Port 65: I/O port
$\overline{CTS3}$		Input	Serial data send enable 3 (Clear To Send)
SCLK3		I/O	Serial Clock I/O 3
P66	1	I/O	Port 66: I/O port
TXD4		Output	Serial send data 4
P67	1	I/O	Port 67: I/O port
RXD4		Input	Serial receive data 4
P70	1	I/O	Port 70: I/O port
TI0		Input	Timer input 0: timer 0 input
P71	1	I/O	Port 71: I/O port
TO1		Output	Timer output 1: Timer 0 or 1 output
P72	1	I/O	Port 72: I/O port
TO2		Output	PWM output 2: 8-bit PWM timer 2 output
P73	1	I/O	Port 73: I/O port
TO3		Output	PWM output 3: 8-bit PWM timer 3 output

Table 2.2.3 Pin names and functions (3/4)

Pin name	Number of pins	I/O	Function
P80	1	I/O	Port 80: I/O port
TI4		Input	Timer input 4: Timer 4 count/capture trigger signal input
INT4		Input	Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81	1	I/O	Port 81: I/O port
TI5		Input	Timer input 5: Timer 4 count/capture trigger signal input
INT5		Input	Interrupt request pin 5: Interrupt request pin with rising edge
P82	1	I/O	Port 82: I/O port
TO4		Output	Timer output 4: Timer 4 output pin
P83	1	I/O	Port 83: I/O port
TO5		Output	Timer output 5: Timer 4 output pin
P84	1	I/O	Port 84: I/O port
TI6		Input	Timer input 6: Timer 5 count/capture trigger signal input
INT6		Input	Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85	1	I/O	Port 85: I/O port
TI7		Input	Timer input 7: Timer 5 count/capture trigger signal input
INT7		Input	Interrupt request pin 7: Interrupt request pin with rising edge
P86	1	I/O	Port 86: I/O port
TO6		Output	Timer output 6: Timer 5 output pin
P87	1	I/O	Port 87: I/O port
INT0		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90	1	I/O	Port 90: I/O port (Programmable open-drain)
SDA		I/O	SBI I^2C bus mode channel data
SO5		Output	Serial send data 5
P91	1	I/O	Port 91: I/O port (Programmable open drain)
SCL		I/O	SBI I^2C bus mode clock
SI5		Input	Serial receive data 5
P92	1	I/O	Port 92: I/O port
SCK5		I/O	Serial Clock I/O 5
P93	1	I/O	Port 93: I/O port (Programmable open drain)
SO0		Output	Serial send data 0
P94	1	I/O	Port 94: I/O port
SI0		Input	Serial receive data 0
P95	1	I/O	Port 95: I/O port
SCK0		I/O	Serial clock I/O 0
PA0 to PA5	6	I/O	Port A0 to A5: I/O ports (large current output)
PA6	1	I/O	Port A6: I/O port

Table 2.2.4 Pin names and functions (4/4)

Pin name	Number of pins	I/O	Function
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output: Outputs system clock or 2 times oscillation clock for synchronizing to external circuit.
$\overline{\text{WDTOUT}}$	1	Output	Watchdog timer output pin
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs [System Clock ÷ 2] Clock. Pulled-up during reset. can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	Fixed to 1.
AM8/$\overline{16}$	1	Input	Fixed to 1.
ALE	1	Output	Address Latch Enable (Can be disabled for reducing noise.)
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
XT1 P96	1	Input I/O	Low Frequency Oscillator connecting pin Port 96: I/O port (Open Drain Output)
XT2 P97	1	Output I/O	Low Frequency Oscillator connecting pin Port 97: I/O port (Open Drain Output)
TEST1/TEST2	2	Output /Input	TEST1 Should be connected with TEST2 pin.
VCC	3		Power supply pin (All VCC pins are connected to the power supply source.)
VSS	3		GND pin (All Vss pins are connected to the GND (0 V).)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)

Note: Built-in pull-up/pull-down resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

2.3 PROM mode

Table 2.3.1 Name and function of PROM mode

Pin function	Number of pins	Input / Output	Function	Pin name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of program	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output enable	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V/5 V (Power supply of program)	$\overline{EA}$
VCC	4	Power supply	6.25 V/5 V	VCC, AVCC
VSS	4	Power supply	0 V	VSS, AVSS

Pin function	Number of pins	Input/ Output	Pin state
P34	1	Input	Fix to low level (security pin)
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)
CLK	1	Input	
ALE	1	Output	Open
X1	1	Input	Self oscillation with resonator
X2	1	Output	
P42 to P40 P37 to P35 AM8/ $\overline{16}$	7	Input	Fix to high level
TEST1/TEST2	2	Input / Output	Short
P57 to P50 P67 to P60 P73 to P70 P87 to P80 P97 to P90 PA7 to PA0 VREFH VREFL $\overline{NMI}$ $\overline{WDTOUT}$	48	I/O	Open

3. Operation

This section describes the functions and basic operational blocks of the TMP91PW11.

The TMP91PW11 has PROM in place of the mask ROM which is included in the TMP91CW11. The other configuration and functions are the same as the TMP91CW11. Regarding the function of the TMP91PW11, which is not described herein, see the TMP91CW11.

The TMP91PW11 has two operational modes: MCU mode and PROM mode.

3.1 MCU mode

(1) Mode-setting and function

The MCU mode is set by releasing the CLK pin (Pin open). In the MCU mode, the operation is the same as TMP91CW11.

(2) Memory-map

The memory map of TMP91PW11 is the same as that of TMP91CW11. The memory map in MCU mode and the memory map in PROM mode are shown in Figure 3.2.1.

3.2 Memory Map

Figure 3.2.1 are the memory map of the TMP91PW11.

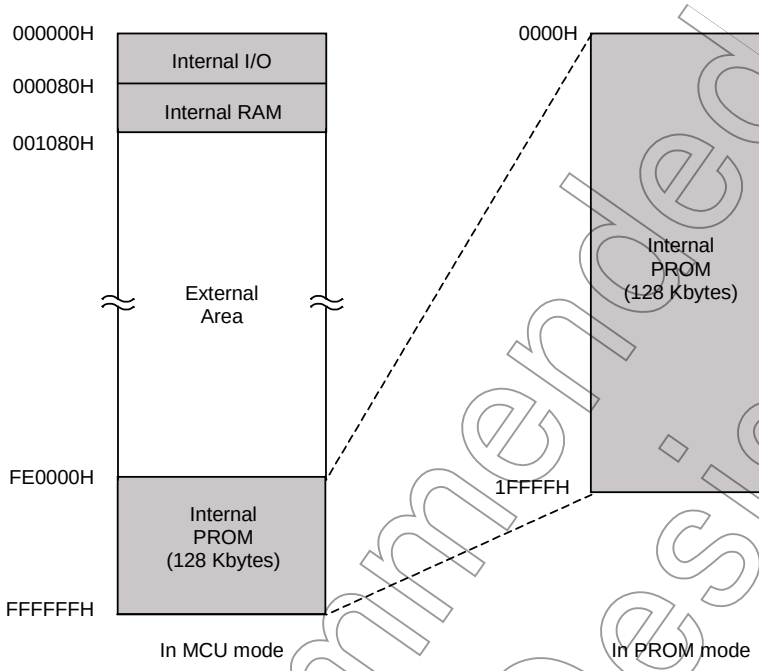


Figure 3.2.1 Memory map

3.3 PROM Mode

(1) Mode setting and programming

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the L level. The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adapter socket.

a. OTP adapter
BM11129: TMP91PW11F adapter

b. Setting OTP adapter
Set the switch (SW1) to N side.

c. Setting PROM programmer

i) Set PROM type to TC571000D.
Size: 1 Mbit (128 K × 8 bit)

VPP: 12.75 V

t_{PW}: 100 μs

The electric signature mode (hereinafter referred to as "signature") is not supported. Therefore using signature with PROM programmer applies Voltage of 12.75 V to Pin 9 (A9) of the address, and the device is damaged. Do not use signature.

ii) Transferring the data (copy)

In TMP91PW11F, PROM is placed on addresses 00000 to 1FFFFH in PROM mode, and addresses FE0000H to FFFFFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 1FFFFH in PROM mode using the object converter (toucan) or the block transfer mode. (see instruction manual of PROM programmer.)

iii) Setting program address

Start address: 00000H

End address: 1FFFFH

d. Programming
Program/verify according to the procedures of PROM programmer.

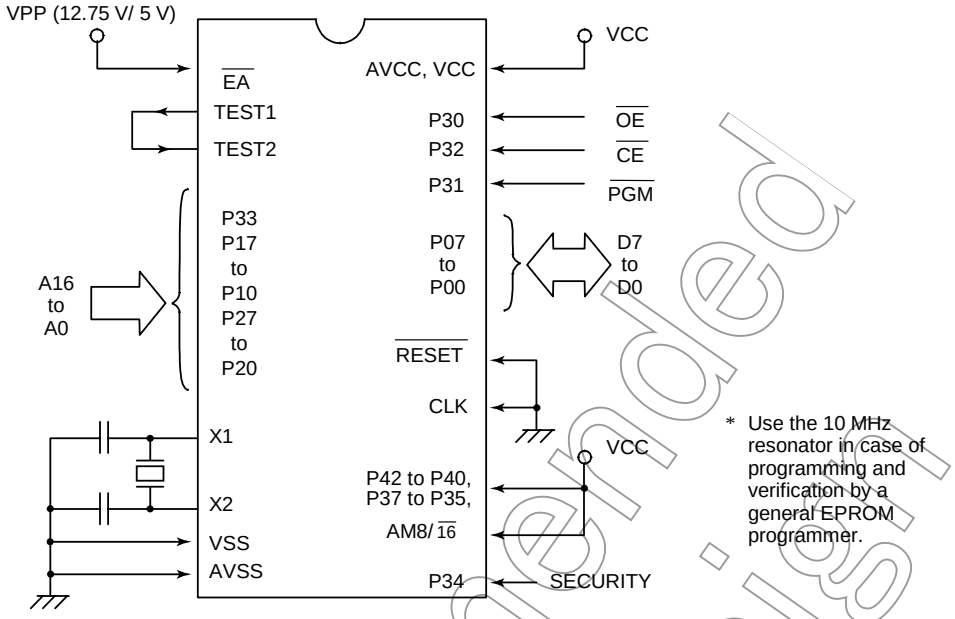


Figure 3.3.1 PROM Mode pin setting

(2) Programming Flow Chart

The programming mode is set by applying 12.75 V (programming voltage) to the VPP pin when the following pins are set as follows; VCC: 6.25 V, $\overline{\text{RESET}}$: L level, CLK: L level. While address and data are fixed and $\overline{\text{CE}}$ pin is set to L level, 0.1 ms of L level pulse is applied to $\overline{\text{PGM}}$ pin to program the data. Then the data in the address is verified. If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin. This programming procedure is repeated until correct data is read from the address. (25 times maximum) Subsequently, all data are programmed in all addresses. The verification for all data is done under the condition of Vpp = Vcc = 5 V after all data were written.

Figure 3.3.2 shows the programming flow chart.

High Speed Program Writing

Flow chart

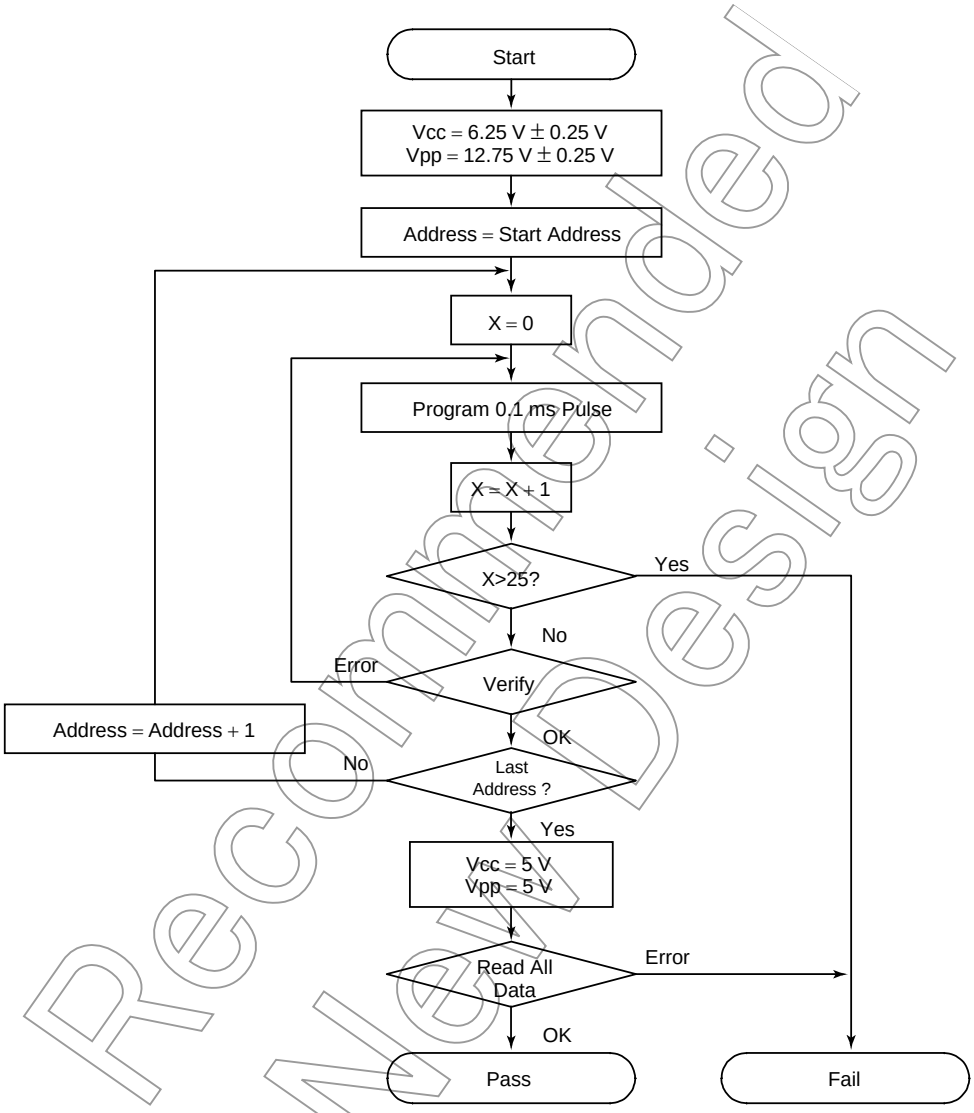


Figure 3.3.2 Flowchart

(3) Security Bit

The TMP91PW11 has a Security Bit in PROM cell. If the Security Bit is programmed to 0, the content of the PROM is disable to be read in PROM mode.

How to program the Security Bit.

- Set the PROM mode.
- Set the security pin (Port 34) to 1.
- Set programming address to 00000H.
- Set programming data to FEH.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

X used in an expression shows a frequency of clock f_{FPH} selected by SYSCR1 <SYSCK>. If a clock gear or a low speed oscillator is selected, a value of X is different. The value as an example is calculated at fc, gear = 1/fc (SYSCR1 <SYSCK, GEAR 2 to 0> = 0000).

Parameter	Symbol	Pin	Rating	Unit
Power Supply voltage	V_{CC}		−0.5 to 6.5	V
Program voltage	U_{PP}	$\overline{EA}$	−0.5 to 13.0	V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5	V
Output Voltage	V_{OUT}	P96, P97, PA0 to A5, P60, P91 to 93 (for open-drain)	−0.5 to V_{CC} + 0.5	V
Output Current (per pin)	I_{OUT1}	only PA0 to A5	20	mA
	I_{OUT2}	except PA0 to A5	2	mA
	I_{OUT3}		−2	mA
Output Current (total)	ΣI_{OUT1}	Total	120	mA
	ΣI_{OUT2}	PA0 to A5	80	mA
	ΣI_{OUT3}	Total	−80	mA
Power Dissipation (Ta = 85°C)	P_D		600	mW
Soldering Temperature	Tsolder		260	°C
Storage Temperature	T_{STG}		−65 to 150	°C
Operating Temperature	T_{opr}		−40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2) (Vss = 0 V, Ta = −40 to 85°C)

Parameter		Symbol	Condition		Min	Typ. (Note 1)	Max	Unit
Power Supply Voltage AVcc = V_{CC} AVss = V_{SS}		VCC	fc = 4 to 25 MHz	fs = 30 to 34 kHz	4.5		5.5	V
			fc = 4 to 12.5 MHz		2.7			
Input Low Voltage	AD0 to 15	VIL	$V_{CC} \geq 4.5$ V		−0.3		0.8	V
			$V_{CC} < 4.5$ V				0.6	
	P20 to 27, P32 to 37, P42, P50 to 57, P60 to 67, P70 to 73, P80 to 86, P93, P96, P97 to 37, PA0 to A7	VIL1	V_{CC} = 2.7 to 5.5 V				0.3 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$, P40 to 41, P87, P90 to 92, P94, P95	VIL2					0.25 V_{CC}	
	$\overline{EA}$, AM8/$\overline{16}$	VIL3					0.3	
	X1	VIL4					0.2 V_{CC}	
Input High Voltage	AD0 to 15	VIH	$V_{CC} \geq 4.5$ V		2.2		V_{CC} + 0.3	V
			$V_{CC} < 4.5$ V		2.0			
	P20 to 27, P32 to 37, P42, P50 to 57, P60 to 67, P70 to 73, P80 to 86, P93, P96, P97 to 37, PA0 to A7	VIH1	V_{CC} = 2.7 to 5.5 V		0.7 V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$, P40 to 41, P87, P90 to 92, P94, P95	VIH2			0.75 V_{CC}			
	$\overline{EA}$, AM8/$\overline{16}$	VIH3			V_{CC} − 0.3			
	X1	VIH4			0.8 V_{CC}			

Note: Typical values are for Ta = 25°C and Vcc = 5 V unless other wise noted.

4.2 DC Characteristic (2/2) (Vss = 0 V, Ta = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Output Low Voltage (except PA0 to PA5)	V_{OL}	I OL = 1.6 mA (V_{CC} = 2.7 to 5.5 V)			0.45	V
Output Low Current (PA0 to 5)	I_{OLA}	VOL = 1.0 V (V_{CC} = 3 V ± 10%)	7			mA
		VOL = 1.0 V (V_{CC} = 5 V ± 10%)	16			
Output High Voltage	V_{OH1}	I OH = –400 μA (V_{CC} = 3 V ± 10%)	2.4			V
	V_{OH2}	I OH = –400 μA (V_{CC} = 5 V ± 10%)	4.2			
Darlington Drive Current (8 Output Pins max.)	I_{DAR} (Note 2)	V EXT = 1.5 V R EXT = 1.1 kΩ (V_{CC} = 5 V ± 10% only)	–1.0		–3.5	mA
Input Leakage Current	I_{LI}	0.0 ≤ V_{IN} ≤ V_{CC}		0.02	±5	μA
Output Leakage Current	I_{LO}	0.2 ≤ V_{IN} ≤ V_{CC} – 0.2		0.05	±10	
Power Down Voltage (at STOP, RAM Back up)	V_{STOP}	VIL2 = 0.2 V_{CC}, VIH 2 = 0.8 V_{CC}	2.0		6.0	V
$\overline{RESET}$ Pull Up Resistor	R_{RST}	V_{CC} = 5 V ± 10%	50		150	kΩ
		V_{CC} = 3 V ± 10%	80		200	
Pin Capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, P40, P41, P87, P90 to 92, P94, P95	V_{TH}		0.4	1.0		V
Programmable Pull Down Resistor	R_{KL}	V_{CC} = 5 V ± 10%	10		80	kΩ
		V_{CC} = 3 V ± 10%	30		150	
Programmable Pull Up Resistor	R_{KH}	V_{CC} = 5 V ± 10%	50		150	
		V_{CC} = 3 V ± 10%	100		300	
NORMAL	I_{CC}	V_{CC} = 5 V ± 10% fc = 25 MHz		45	55	mA
RUN				30	40	
IDLE2				18	30	
IDLE1				3.5	10	
NORMAL		V_{CC} = 3 V ± 10% fc = 12.5 MHz (Typ: V_{CC} = 3.0 V)		13	20	mA
RUN				8	11	
IDLE2				4.8	7.5	
IDLE1				1.1	1.8	
SLOW		V_{CC} = 3 V ± 10% fs = 32.768 kHz (Typ.: Vcc = 3.0 V)		110	200	μA
RUN				30	52	
IDLE2				25	52	
IDLE1				15	40	
STOP		Ta ≤ 50°C, V_{CC} = 2.7 to 5.5 V		0.2	10	μA
		Ta ≤ 70°C			20	
		Ta ≤ 85°C			50	

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unlesss otherwise noted.

Note 2: I-DAR is guranteed for total of up to 8 ports.

4.3 AC Characteristics

(1) Vcc = 5 V ± 10% (fc = 4 to 20 MHz)
(fs = 30 to 34 kHz)

External-bus access isn't supported in over 20 MHz.

No.	Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (=x)	50	33.3 μs	62.5		50		ns
2	t_{CLK}	CLK width	2x – 40		85		60		ns
3	t_{AK}	A0 to 23 Valid→CLK Hold	0.5x – 20		11		5		ns
4	t_{KA}	CLK Valid→A0 to 23 Hold	1.5x – 70		24		5		ns
5	t_{AL}	A0 to 15 Valid→ALE fall	0.5x – 15		16		10		ns
6	t_{LA}	ALE fall→A0 to 15 Hold	0.5x – 20		11		5		ns
7	t_{LL}	ALE High pulse width	x – 40		23		10		ns
8	t_{LC}	ALE fall→ $\overline{RD}$ / $\overline{WR}$ fall	0.5x – 25		6		0		ns
9	t_{CL}	$\overline{RD}$ / $\overline{WR}$ rise→ALE rise	0.5x – 20		11		5		ns
10	t_{ACL}	A0 to 15 Valid→ $\overline{RD}$ / $\overline{WR}$ fall	x – 25		38		25		ns
11	t_{ACH}	A0 to 23 Valid→ $\overline{RD}$ / $\overline{WR}$ fall	1.5x – 50		44		25		ns
12	t_{CA}	$\overline{RD}$ / $\overline{WR}$ rise→A0 to 23 Hold	0.5x – 25		6		0		ns
13	t_{ADL}	A0 to 15 Valid→D0 to 15 input		3.0x – 55		133		95	ns
14	t_{ADH}	A0 to 23 Valid→D0 to 15 input		3.5x – 65		154		110	ns
15	t_{RD}	$\overline{RD}$ fall→D0 to 15 input		2.0x – 60		65		40	ns
16	t_{RR}	$\overline{RD}$ Low pulse width	2.0x – 40		85		60		ns
17	t_{HR}	$\overline{RD}$ rise→D0 to 15 Hold	0		0		0		ns
18	t_{RAE}	$\overline{RD}$ rise→A0 to 15 output	x – 15		48		35		ns
19	t_{WW}	$\overline{WR}$ Low pulse width	2.0x – 40		85		60		ns
20	t_{DW}	D0 to 15 Valid→ $\overline{WR}$ rise	2.0x – 55		70		45		ns
21	t_{WD}	$\overline{WR}$ rise→D0 to 15 Hold	0.5x – 15		16		10		ns
22	t_{AWH}	A0 to 23 Valid→ $\overline{WAIT}$ input (1WAIT +n mode)		3.5x – 90		129		85	ns
23	t_{AWL}	A0 to 15 Valid→ $\overline{WAIT}$ input (1 $\overline{WAIT}$ +n mode)		3.0x – 80		108		70	ns
24	t_{CW}	$\overline{RD}$ / $\overline{WR}$ fall→ $\overline{WAIT}$ Hold (1 $\overline{WAIT}$ +n mode)	2.0x + 0		125		100		ns
25	t_{APH}	A0 to 23 Valid→PORT input		2.5x – 120		36		5	ns
26	t_{APH2}	A0 to 23 Valid→PORT Hold	2.5x + 50		206		175		ns
27	t_{CP}	$\overline{WR}$ rise→PORT Valid		200		200		200	ns

AC Measuring Conditions

- Output Level: High 2.2 V /Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK)
- Input Level: High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

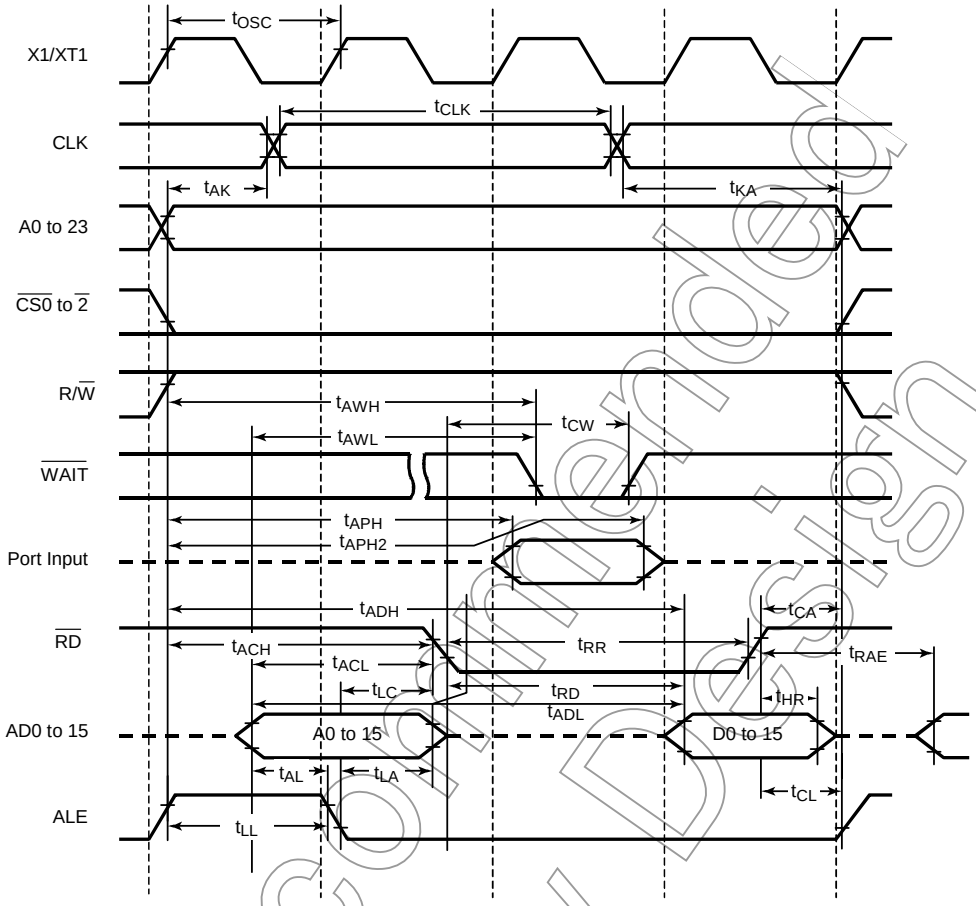
(2) Vcc = 3 V ± 10% (fc = 4 to 12.5 MHz)
(fs = 30 to 34 kHz)

No.	Symbol	Parameter	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (=x)	80	33.3 μs	80		ns
2	t_{CLK}	CLK width	2x – 40		120		ns
3	t_{AK}	A0 to 23 Valid→CLK Hold	0.5x – 30		10		ns
4	t_{KA}	CLK Valid→A0 to 23 Hold	1.5x – 80		40		ns
5	t_{AL}	A0 to 15 Valid→ALE fall	0.5x – 35		5		ns
6	t_{LA}	ALE fall→A0 to 15 Hold	0.5x – 35		5		ns
7	t_{LL}	ALE High width	x – 60		20		ns
8	t_{LC}	ALE fall→$\overline{RD}$ / $\overline{WR}$ fall	0.5x – 35		5		ns
9	t_{CL}	$\overline{RD}$ / $\overline{WR}$ rise→ALE rise	0.5x – 40		0		ns
10	t_{ACL}	A0 to 15 Valid→$\overline{RD}$ / $\overline{WR}$ fall	x – 50		30		ns
11	t_{ACH}	A0 to 23 Valid→$\overline{RD}$ / $\overline{WR}$ fall	1.5x – 50		70		ns
12	t_{CA}	$\overline{RD}$ / $\overline{WR}$ rise→A0 to 23 Hold	0.5x – 40		0		ns
13	t_{ADL}	A0 to 15 Valid→D0 to 15 input		3.0x – 110		130	ns
14	t_{ADH}	A0 to 23 Valid→D0 to 15 input		3.5x – 125		155	ns
15	t_{RD}	$\overline{RD}$ fall→D0 to 15 input		2.0x – 115		45	ns
16	t_{RR}	$\overline{RD}$ Low pulse width	2.0x – 40		120		ns
17	t_{HR}	$\overline{RD}$ rise→D0 to 15 Hold	0		0		ns
18	t_{RAE}	$\overline{RD}$ rise→A0 to 15 output	x – 25		55		ns
19	t_{WW}	$\overline{WR}$ Low pulse width	2.0x – 40		120		ns
20	t_{DW}	D0 to 15 Valid→$\overline{WR}$ rise	2.0x – 120		40		ns
21	t_{WD}	$\overline{WR}$ rise→D0 to 15 Hold	0.5x – 40		0		ns
22	t_{AWH}	A0 to 23 Valid→$\overline{WAIT}$ input (1 $\overline{WAIT}$ + n mode)		3.5x – 130		150	ns
23	t_{AWL}	A0 to 15 Valid→$\overline{WAIT}$ input (1 $\overline{WAIT}$ + n mode)		3.0x – 100		140	ns
24	t_{CW}	$\overline{RD}$ / $\overline{WR}$ fall→$\overline{WAIT}$ Hold (1 $\overline{WAIT}$ + n mode)	2.0x + 0		160		ns
25	t_{APH}	A0 to 23 Valid→PORT input		2.5x – 120		80	ns
26	t_{APH2}	A0 to 23 Valid→PORT Hold	2.5x + 50		250		ns
27	t_{CP}	$\overline{WR}$ rise→PORT Valid		200		200	ns

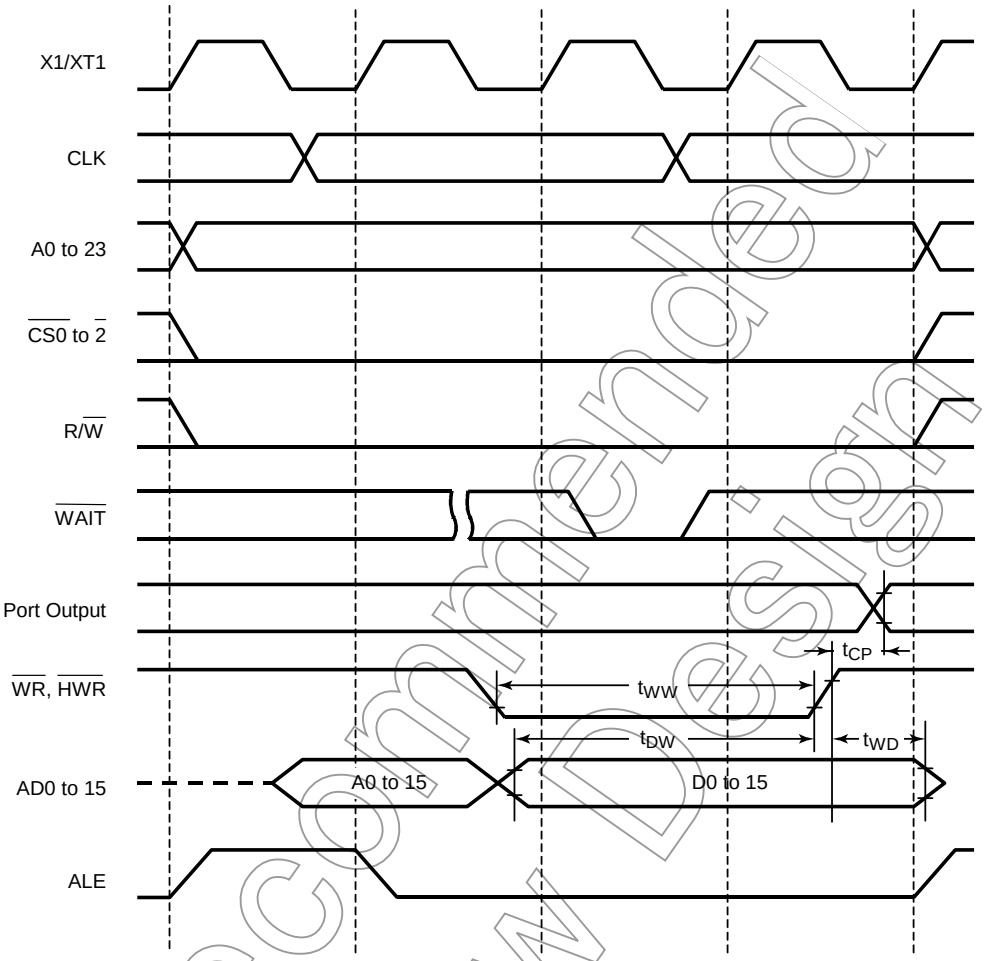
AC Measuring Conditions

- Output Level: High 0.7 Vcc / Low 0.3 Vcc, CL = 50 pF
- Input Level: High 0.9 Vcc / Low 0.1 Vcc

(1) Read Cycle



(2) Write Cycle



4.4 AD Conversion Characteristics

(Vss = 0 V, AVcc = Vcc, AVss = Vss, Ta = –40 to 85 °C)

Vcc = +5 V ± 10%, (fc = 4 to 25 MHz)
Vcc = +3 V ± 10%, (fc = 4 to 12.5 MHz)

Parameter		Symbol	TestConditions	Min	Typ.	Max	Unit
AD analog reference supply voltage (+)		V_{REFH}		Vcc – 0.2		Vcc	V
AD analog reference supply voltage (–)		V_{REFL}		Vss		Vss + 0.2	
Analog reference voltage		AV_{CC}		Vcc – 0.2		Vcc	
Analog reference voltage		AV_{SS}		Vss		Vss + 0.2	
Analog input voltage		V_{AIN}		V_{REFL}		V_{REFH}	
Analog input impedance		R_{AIN}				5	kΩ
Analog reference voltage supply current	<VREFON> = 1	I_{REF}	Vcc = 5 V ± 10%			3.7	mA
			Vcc = 3 V ± 10%			2.2	
	<VREFON> = 0		Vcc = 2.7 to 5.5 V		0.02	5.0	μA
Total tolerance (excludes quantization error)		E_T	Vcc = 5 V ± 10%			±3	LSB
			Vcc = 3 V ± 10%			±3	

Note 1: 1LSB = (VREFH -VREFL)/210[V]

Note 2: Power supply current ICC from the VCC pin includes the power supply current from the AVCC pin.

4.5 Serial Channel Timing (Serial channel 2, 3 and 4)

(1) SCLK Input Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	16X		488 μs		1.28 μs		0.8 μs	
Output Data → Rising edge of SCLK	t_{OSS}	t_{SCY}/2 – 5X – 50		91.5 μs		190 ns		100 ns	
SCLK edge* → Output Data hold	t_{OHS}	5X – 100		152 μs		300 ns		150 ns	
SCLK edge* → Input Data hold	t_{HSR}	0		0		0		0	
SCLK edge* → effective data input	t_{SRD}		t_{SCY} – 5X – 100		336 μs		780 ns		450 ns

* It is rising edge in using rising edge mode and falling edge in using falling edge mode.

(2) SCLK Output Mode

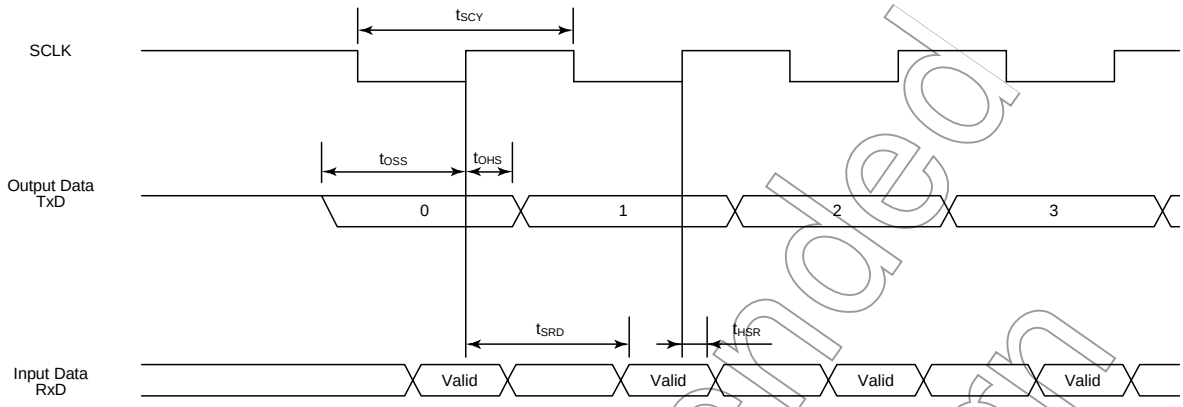
Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.28 μs	655.36 μs	0.8 μs	409.6 μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} – 2X – 150		427 μs		970 ns		550 ns	
SCLK rising edge → Output Data hold	t_{OHS}	2X – 80		60 μs		80 ns		20 ns	
SCLK rising edge → Input Data hold	t_{HSR}	0		0		0		0	
SCLK rising edge → effective data input	t_{SRD}		t_{SCY} – 2X – 150		428 μs		970 ns		550 ns

(3) SCLK Input Mode (UART mode)

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	4X + 20		122 μs		340 ns		220 ns	
Low level SCLK Pulse width	t_{SCYL}	2X + 5		6 μs		165 ns		105 ns	
High level SCLK Pulse width	t_{SCYH}	2X + 5		6 μs		165 ns		105 ns	

Note: fs is used as system clock or input clock to prescaler.

Timing Chart for I/O Interface Mode



Note: SCLK is reversed in SCLK input falling mode.

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		740		500		ns
Low level pulse width	t_{VCKL}	4X + 40		360		240		ns
High levelpulse width	t_{VCKH}	4X + 40		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level pulse width	t_{INTAL}	4X		320		200		ns
$\overline{NMI}$, INT0 High level pulse width	t_{INTAH}	4X		320		200		ns

(2) INT4 to 7

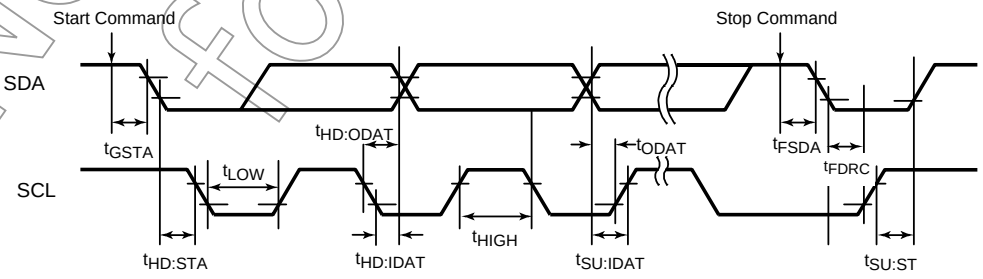
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
INT4 to INT7 Low level pulse width	t_{INTBL}	4X + 100		420		300		ns
INT4 to INT7 High level pulse width	t_{INTBH}	4X + 100		420		300		ns

4.8 Serial Bus Interface Timing

(1) I²C bus Mode

Parameter	Symbol	Variable			Unit
		Min	Typ	Max	
START command → SDA fall	t_{GSTA}	3X			s
Hold time START condition	$t_{HD: STA}$	2^nX			s
SCL Low level pulse width	t_{LOW}	2^nX			s
SCL High level pulse width	t_{HIGH}	$2^nX + 8X$			s
Data hold time (input)	$t_{HD:IDAT}$	0			ns
Data set-up time (input)	$t_{SU:IDAT}$	250			ns
Data hold time (output)	$t_{HD:ODAT}$	7X		11X	s
Data output → SCL Rising edge	t_{ODAT}		$2^nX - t_{HD:ODAT}$		s
STOP command → SDA falling edge	t_{FSDA}	3X			s
SDA Falling edge → SCL Rising edge	t_{FDRC}	2^nX			s
Set-up time STOP condition	$t_{SU:STO}$	$2^nX + 16X$			s

Note: "n" value is set by SBICR1 <SCK2 to 0>



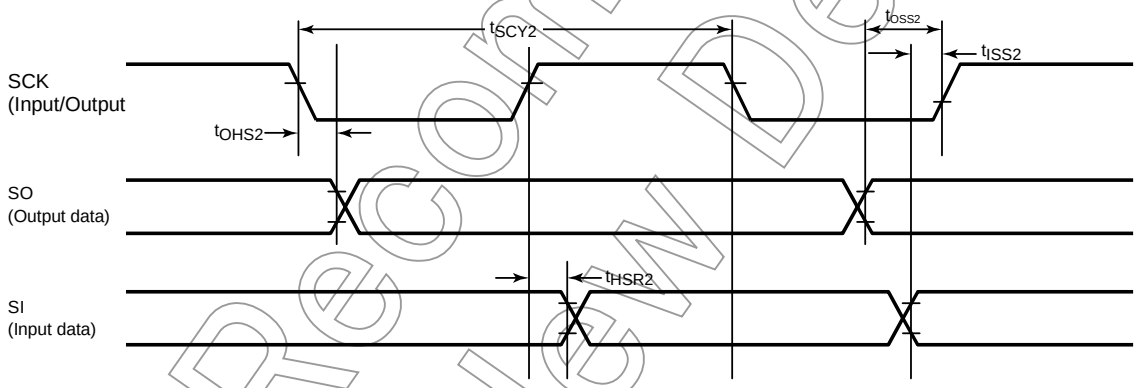
(2) Clocked-synchronous 8-bit SIO Mode

a. SCK Input Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		s
SCK falling edge → Output data hold	t_{OHS2}	6X		s
Output data → SCK rising edge	t_{OSS2}		$t_{SCY2}/2 - 6X$	s
SCK rising edge → Input data hold	t_{HSR2}	6X		ns
Input data → SCK rising edge	t_{ISS2}	0		ns

b. SCK Output Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK falling edge → Output data hold	t_{OHS2}	2X		s
Output data → SCK rising edge	t_{OSS2}		$t_{SCY2}/2 - 2X$	s
SCK rising edge → Input data hold	t_{HSR2}	2X		s
Input data → SCK rising edge	t_{ISS2}	0		ns



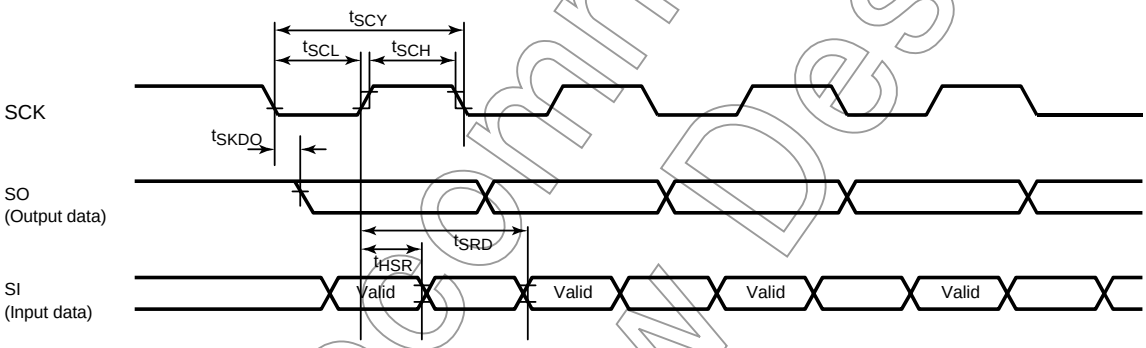
4.9 Timing Chart for Serial Channel 0,1

a. SCK input mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY}	16X		ns
SCK falling edge → Output data hold	t_{SKDO}	6X		ns
SCK rising edge → Effective data input	t_{SRD}		t_{SCY} − 2X	ns
SCK rising edge → Input data hold	t_{HSR}	6X		ns

b. SCK output mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY}	16X		ns
SCK falling edge → Output data hold	t_{SKDO}	2X		ns
SCK rising edge → Effective data input	t_{SRD}		t_{SCY} − 2X	ns
SCK rising edge → Input data hold	t_{HSR}	2X		ns

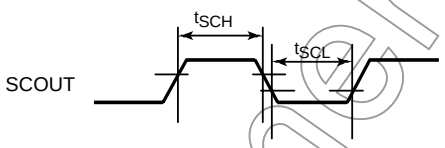


4.10 SCOUT pin AC characteristics

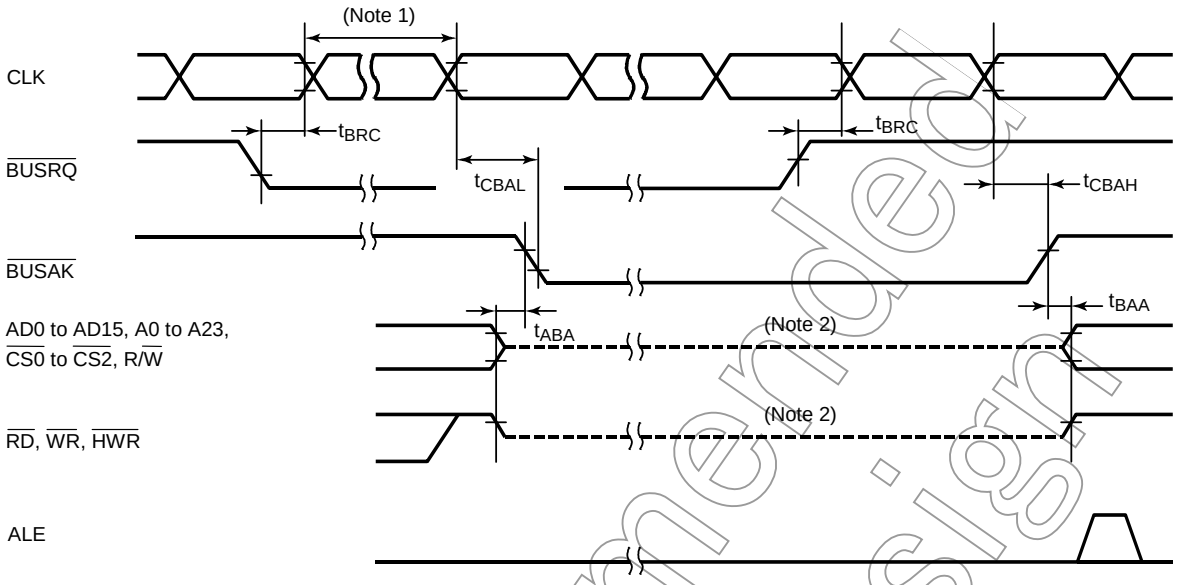
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max		Min	Max	Min	
High-level pulse width VCC = 5 V ± 10%	t_{SCH}	0.5X – 10			30	15		ns
VCC = 3 V ± 10%		0.5X – 20			20	—	—	ns
Low-level pulse width VCC = 5 V ± 10%	t_{SCL}	0.5X – 10			30	15		ns
VCC = 3 V ± 10%		0.5X – 20			20	—	—	ns

Measurement condition

Output level: High 2.2 V / Low 0.8 V, CL = 10 pF



4.11 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ set-up time to CLK	t_{BRC}	120		120		120		ns
CLK → $\overline{BUSAK}$ falling edge	t_{CBAL}		1.5X + 120		240		195	ns
CLK → $\overline{BUSAK}$ rising edge	t_{CBAH}		0.5X + 40		80		65	ns
Output Buffer is off to $\overline{BUSAK}$ ↓	t_{ABA}	0	80	0	80	0	80	ns
$\overline{BUSAK}$ ↑ to Output Buffer is on.	t_{BAA}	0	80	0	80	0	80	ns

Note 1: The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to 0 during Wait cycle.

Note 2: This line shows the output buffer is off-state. It doen't indicate the signal level is fixed.

Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level - fix will be delayed.

The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.

4.12 Read operation in PROM mode

DC/AC characteristics

Ta = 25 ± 5°C Vcc = 5 V ± 10%

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} Read Voltage	V_{PP}	—	4.5	5.5	V
Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	—	2.2	V_{CC} + 0.3	V
Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	—	−0.3	0.8	V
Address to Output Delay	t_{ACC}	C_L = 50 pF	—	2.25TCYC + α	ns

TCYC = 400 ns (10 MHz Clock)

α = 200 ns

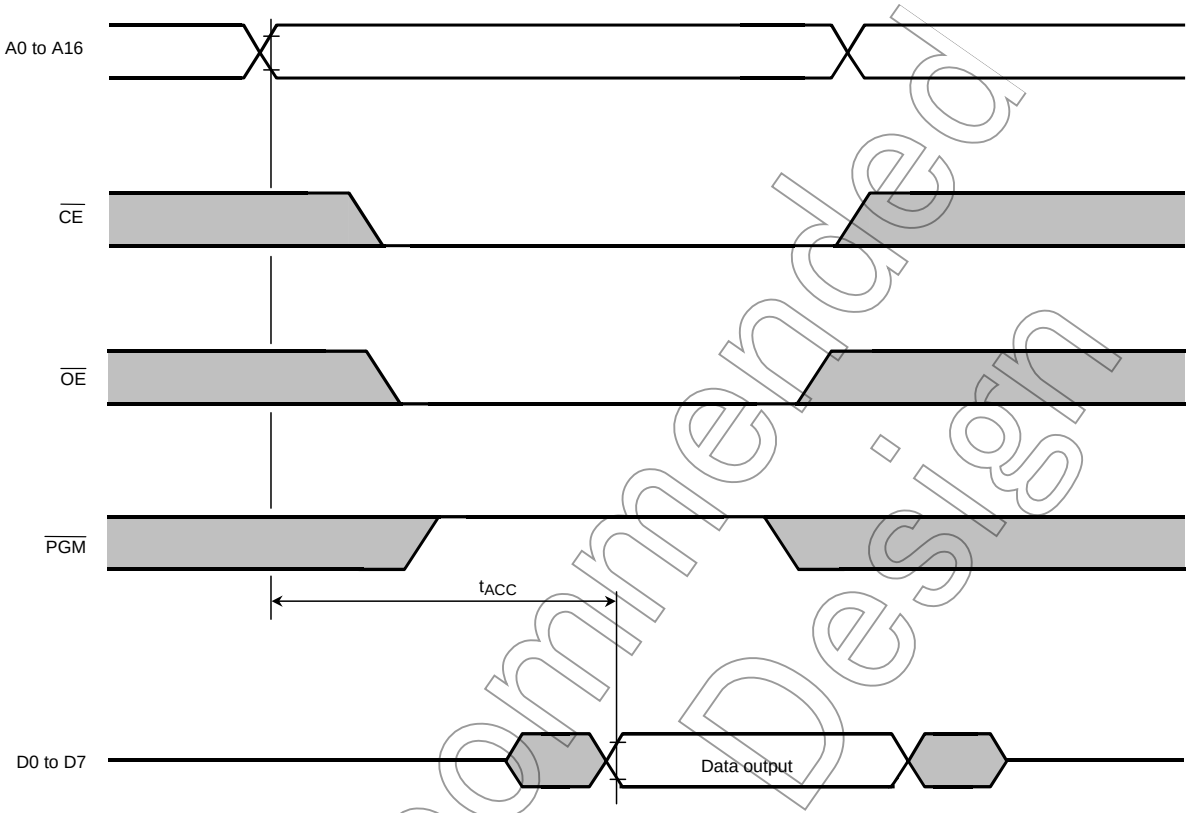
4.13 Program operation in PROM mode

DC/AC characteristics

Ta = 25 ± 5°C Vcc = 6.25 V ± 0.25 V

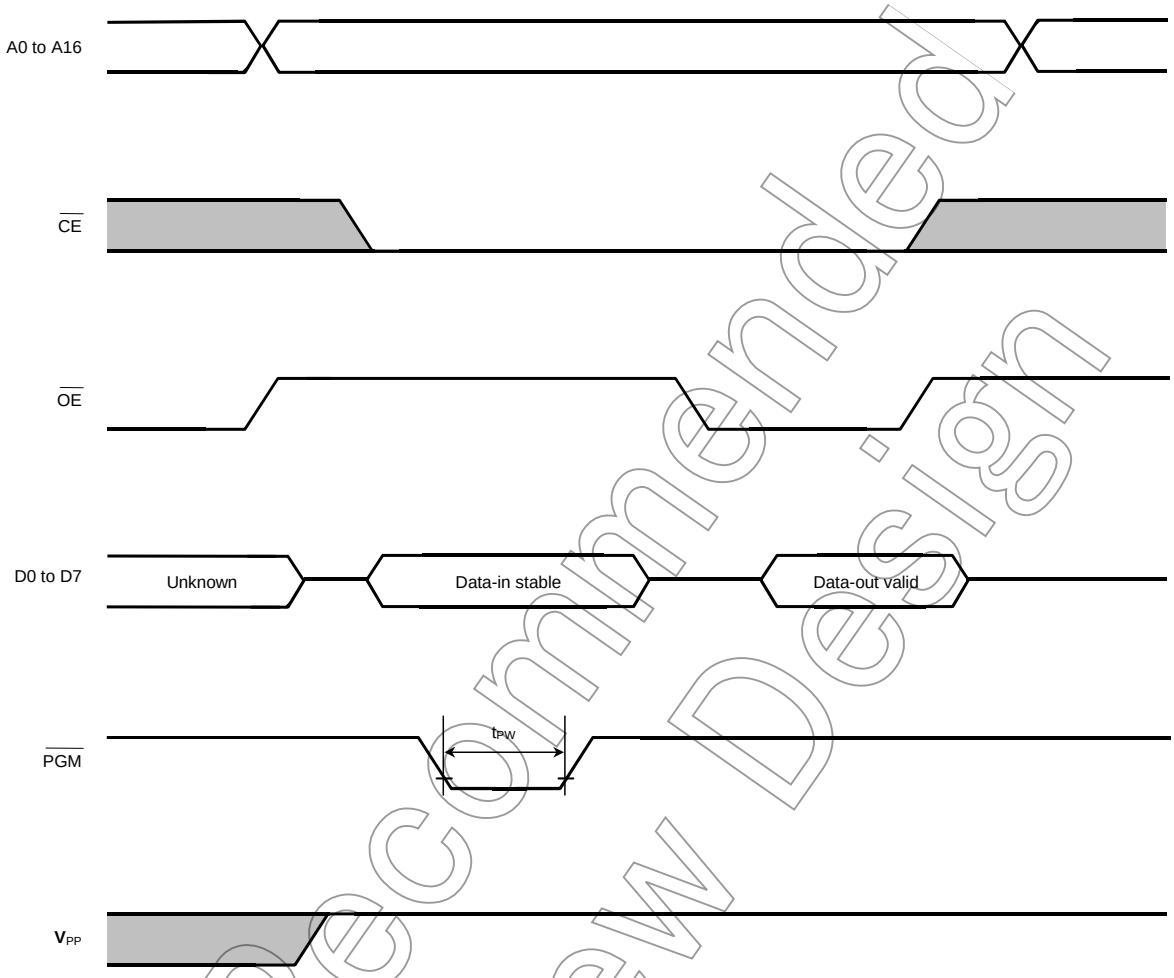
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Programming Supply Voltage	V_{PP}	—	12.50	12.75	13.00	V
Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH}	—	2.6		V_{CC} + 0.3	V
Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL}	—	−0.3		0.8	V
V_{CC} Supply Current	I_{CC}	fc = 10 MHz	—		50	mA
V_{PP} Supply Current	I_{PP}	V_{PP} = 13.00 V	—		50	mA
$\overline{PGM}$ Program Pulse Width	t_{PW}	C_L = 50 pF	0.095	0.1	0.105	ms

4.14 Timing chart of read operation in PROM mode



4.15 Timing chart of program operation in PROM mode

High-Speed Programming formula



Note 1: The power supply of V_{PP} (12.75 V) must be turned on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.

Note 2: The pulling up/down device on condition of V_{PP} = 12.75 V suffers a damage for the device.

Note 3: The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the programming.