TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870 Series

TMP87PS71AFG

TOSHIBA CORPORATION

Semiconductor Company

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87PS71AF	QFP80-P-1420-0.80B	TMP87PS71AFG	QFP80-P-1420-0.80B	—

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

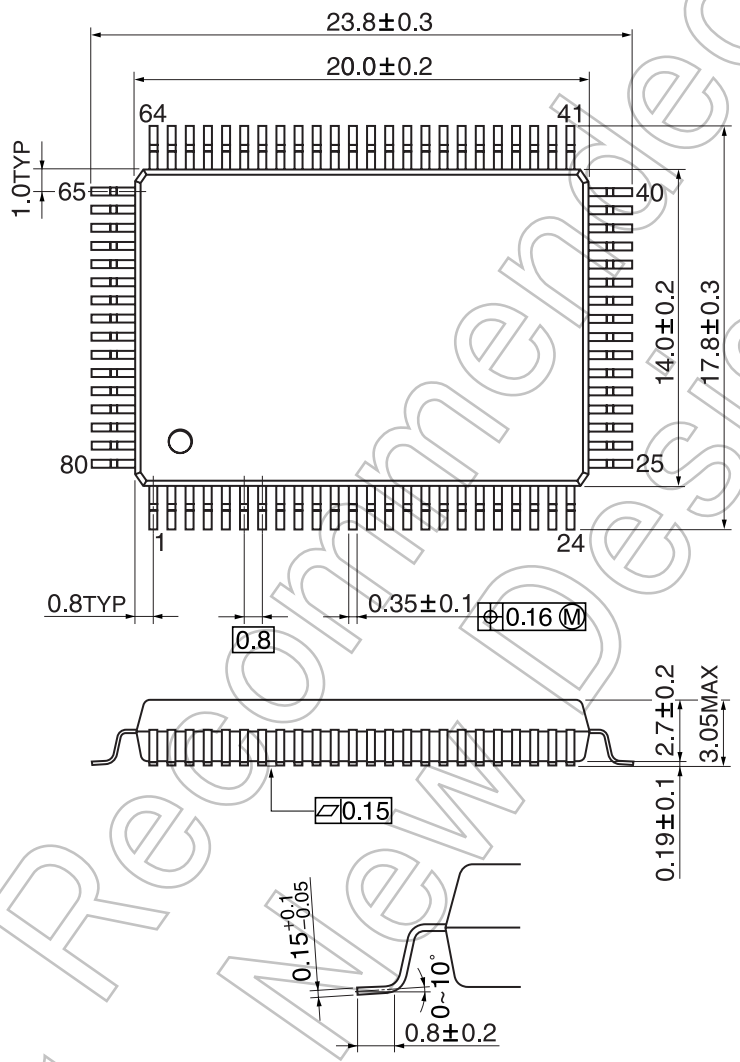
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

QFP80-P-1420-0.80B

Unit: mm



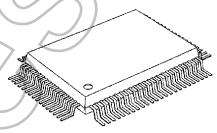
CMOS 8-Bit Microcontroller

TMP87PS71AF

The TMP87PS71A is a One-Time PROM microcontroller with low-power 480 K bits (60 Kbytes) electrically programmable read only memory for the TMP87CS71B system evaluation. The TMP87PS71A is pin compatible with the TMP87CS71B. The operations possible with the TMP87CS71B can be performed by writing programs to PROM. The TMP87PS71A can write and verify in the same way as the TC571000D using an adaptor socket BM11107 and an EPROM programmer.

Product No.	OTP	RAM	Package	Adapter Socket
TMP87PS71AF	60 K × 8 bits	2.0 K × 8 bits	P-QFP80-1420-0.80B	BM11107

P-QFP80-1420-0.80B



TMP87PS71AF

000707EBA1

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  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
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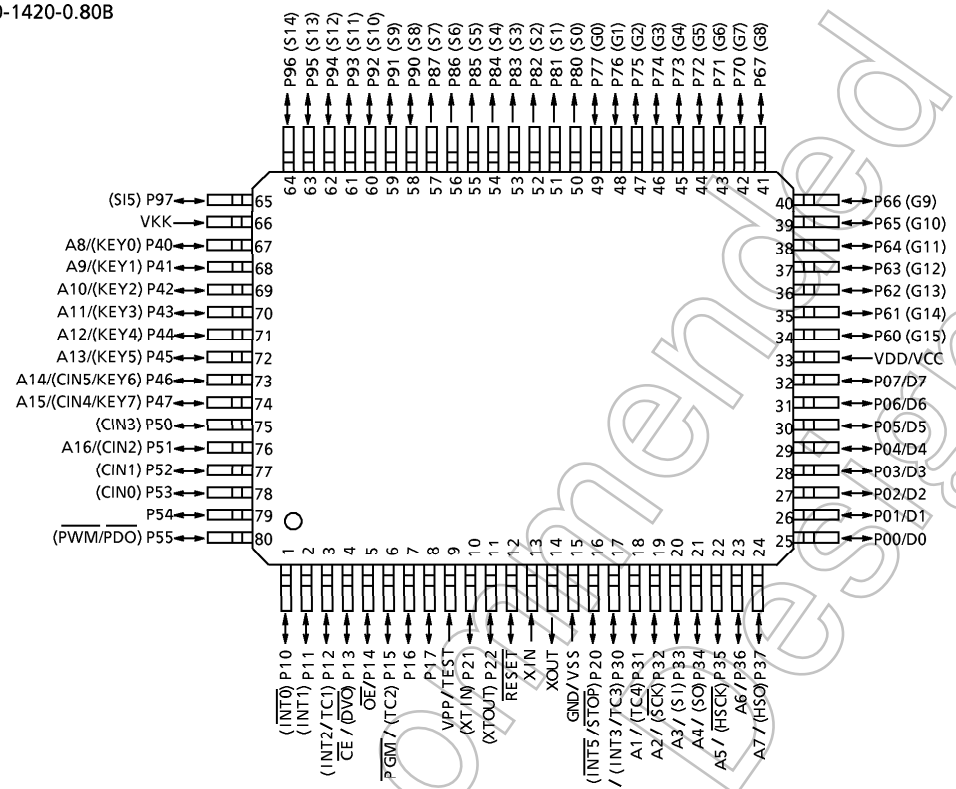
Pin Assignments (Top View)

P-QFP80-1420-0.80B



Pin Functions

The TMP87PS71A has two modes: MCU and PROM.

(1) MCU mode

In this mode, the TMP87PS71A is pin compatible with the TMP87CS71B (fix the TEST pin at low level).

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A16	Input	PROM address inputs	P51
A15 to A8			P47 to P40
A7 to A0			P37 to P30
D7 to D0	I/O	PROM data input/outputs	P07 to P00
$\overline{CE}$	Input	Chip enable signal input (active low)	P13
$\overline{OE}$		Output enable signal input (active low)	P14
$\overline{PGM}$		Program control input (active low)	P15
VPP	Power supply	+ 12.75 V/5 V (Program supply voltage)	TEST
VCC		+ 6.25 V/5 V	VDD
GND		0 V	VSS
P55 to P52	I/O	Pull-down with resistance for input processing	
P11		PROM mode setting pin. Be fixed at high level.	
P21			
P50			
P17, P16		PROM mode setting pin. Be fixed at low level.	
P12, P10			
P22, P20			
$\overline{RESET}$			
XIN	Input	Connect an 8 MHz oscillator to stabilize the internal state.	
XOUT	Output		
VKK	VFT power supply	GND	
P97 to P90	I/O	Open	
P87 to P80	Output		
P77 to P70	I/O		
P67 to P60			

Operational Description

The following explains the TMP87PS71A hardware configuration and operation. The configuration and functions of the TMP87PS71A are the same as those of the TMP87CS71B, except in that a one-time PROM is used instead of an on-chip mask ROM.

The TMP87PS71A is placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. Operating Mode

The TMP87PS71A has two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST/VPP pin at low level.

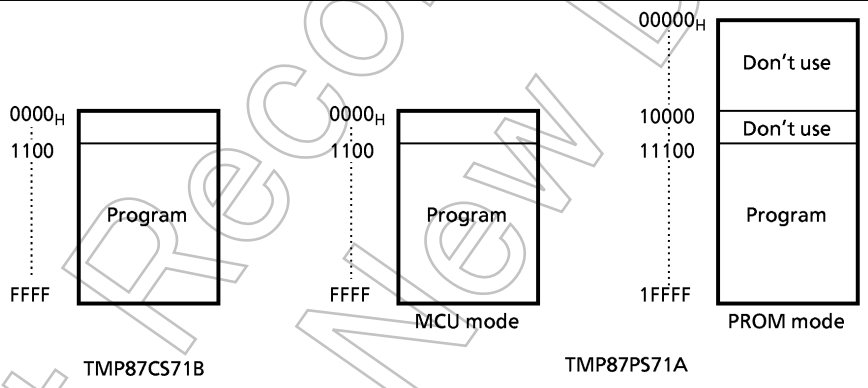
In the MCU mode, operation is the same as with the TMP87CS71B (the TEST/VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program Memory

The TMP87PS71A has a 60 K×8 bits (addresses 1100_H to $FFFF_H$ in the MCU mode, addresses 11100_H to $1FFFF_H$ in the PROM mode) of program memory (OTP).

To use the TMP87PS71A as the system evaluation for the TMP87CS71B, the program should be written to the program memory area as shown in Figure 1-1.

Note: When accessing addresses 00000_H to $110FF_H$ of program memory in the PROM mode, blank, read or verify mode may not be guaranteed the operation; use addresses 11100_H to $1FFFF_H$.



Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

Figure 1-1. Program Memory Area

1.1.2 Data Memory

The TMP87PS71A has an on-chip 2.0 K × 8 bits data memory (static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the TMP87PS71A is the same as those of the TMP87CS71B except that the TEST pin has is no built-in pull-down resistance.

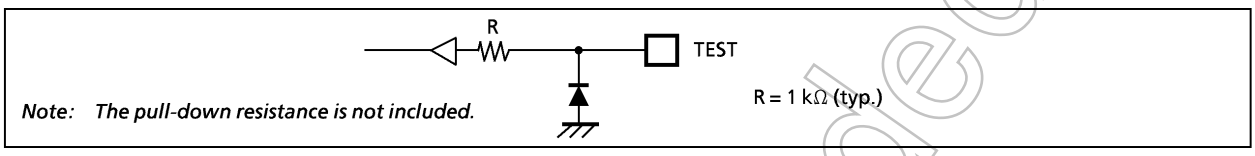


Figure 1-2. TEST Pin

(2) I/O ports

The I/O circuitries of TMP87PS71A I/O ports are the same as the those of TMP87CS71B.

1.2 PROM Mode

The PROM mode is activated by setting the pins TEST, $\overline{\text{RESET}}$ and the ports P17 to P10, P22 to P20 and P50 as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer. The high-speed programming mode can be used for program operation.

The TMP87PS71A is not supported an electric signature mode, so the ROM type must be set to TC571000D.

Set the adaptor socket switchs to "N" and "PS71".

Note: Please set the high-speed programming mode according to each manual of PROM programmer.

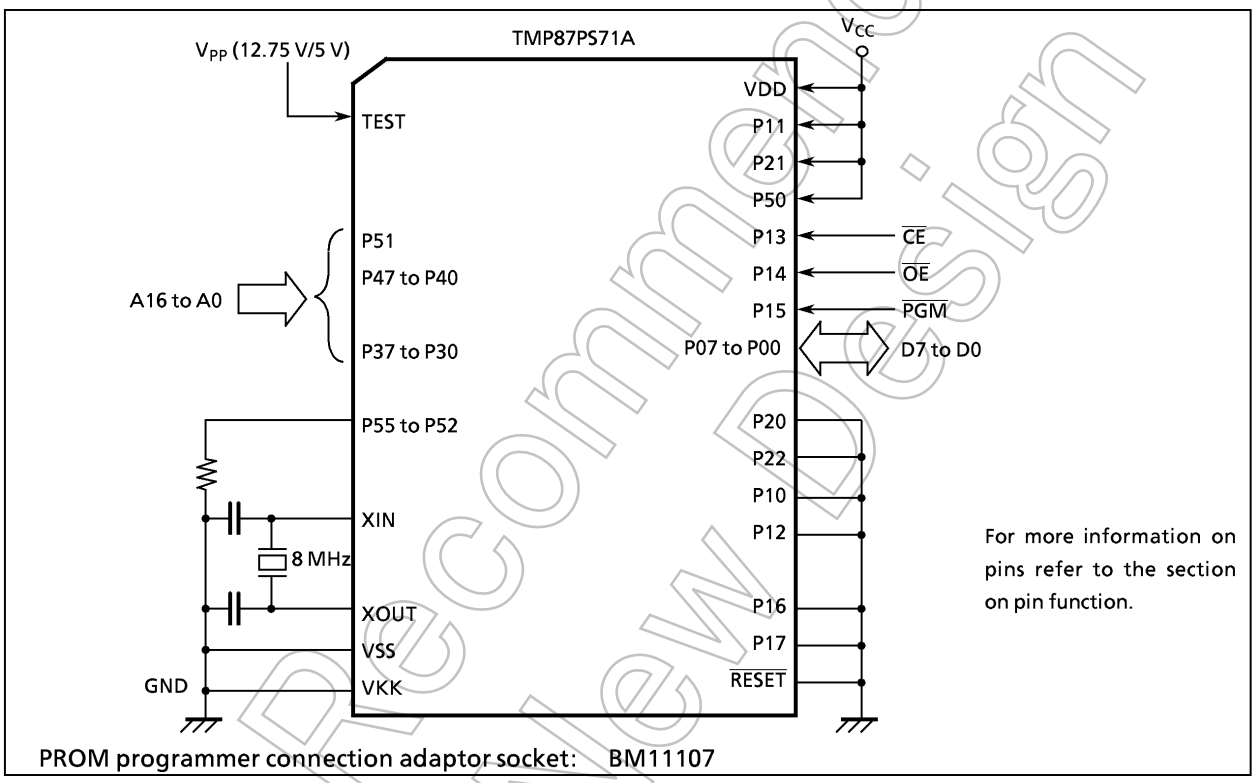


Figure 1-3. Setting for PROM Mode

1.2.1 Programming Flowchart (High-speed Programming Mode)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the VPP pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{PGM}$ input. The programmed data is verified. If incorrect, another 0.1 ms program pulse is applied. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

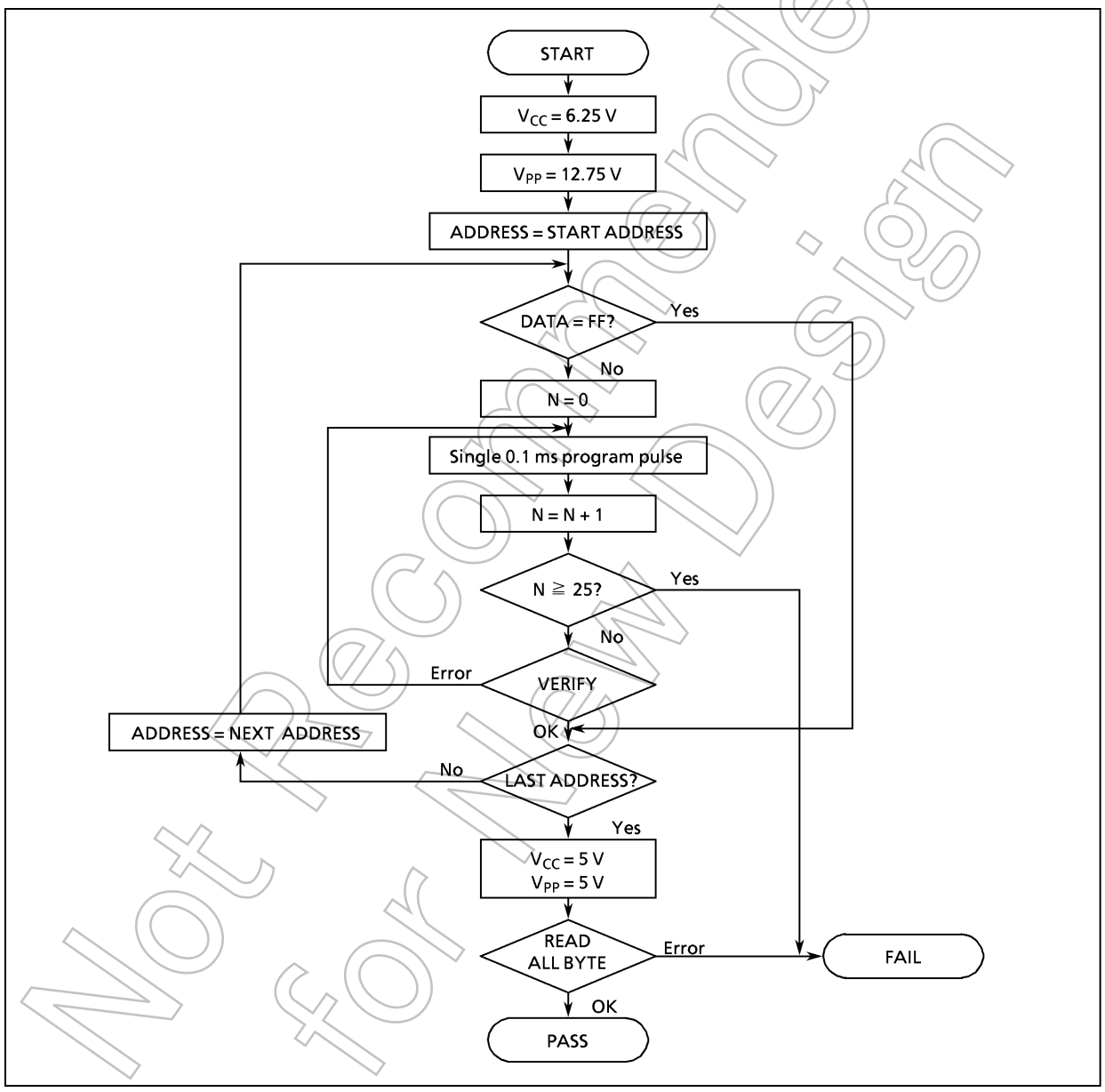


Figure 1-4. Flow Chart of High-Speed Programming

1.2.2 Writing Method for General-purpose PROM Program

(1) Adapters
BM11107: TMP87PS71AF

(2) Adapter setting
Switch (SW1) is set to side N.
Switch (SW2) is set to side PS71.

(3) PROM programmer specifying
i) PROM type is specified to TC571000AD.
Writing voltage: 12.75 V (high-speed program mode)

ii) Data transfer (copy) (note 1)
In the TMP87PS71A, EPROM is within the addresses 11100_H to $1FFFF_H$. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in figure 1-1.

Ex. In the block transfer (copy) mode, executed as below.
ROM capacity of 60KB: transferred addresses 01100_H to $0FFFF_H$ to addresses 11100 to $1FFFF_H$

iii) Writing address is specified. (note 1)
Start address: 11100_H
End address: $1FFFF_H$

(4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1: The specifying method is referred to the PROM programmer description. Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

Note 2: When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.

Note 3: The TMP87PS71A does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12V ± 0.5V to the address pin 9 (A9). The signature must not be used.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	P2, P3, P4, P5, XOUT, $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Source open drain ports	V_{DD} – 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P2, P3, P4, P5	3.2	mA
	I_{OUT3}	P8, P9 (segment outputs)	– 12	
	I_{OUT4}	P6, P7 (digit outputs)	– 25	
Output Current (Total)	ΣI_{OUT1}	P0, P1, P2, P3, P4, P5	120	mA
	ΣI_{OUT2}	P6, P7, P8, P9	– 120	
Power Dissipation [Topr = 70°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 modes			
			fs = 32.768 kHz	SLOW mode	2.7		
				SLEEP mode			
				STOP mode	2.0		
Output Voltage	V_{OUT3}	Source open drain ports			V_{DD} – 38	V_{DD}	V
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	VDD = 4.5 to 5.5V		0.4	8.0	MHz
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL1/2 mode and IDLE1/2 mode.

DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN1}	Port P4 with pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Pull-down Resistance	R_K	Source open drain ports	V_{DD} = 5.5 V, V_{KK} = – 30 V	–	80	–	
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Source open drain ports	V_{DD} = 5.5 V, V_{OUT} = – 32 V	–	–	– 2	
	I_{LO3}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
	V_{OH3}	P8, P9	V_{DD} = 4.5 V, I_{OH} = – 5 mA	2.4	–	–	
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output High current	I_{OH}		V_{DD} = 4.5 V, V_{OH} = 2.4 V	–	– 15	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz fs = 32.768 kHz V_{IN} = 5.3 V/0.2 V	–	12	20	mA
Supply Current in IDLE 1, 2 modes				–	6	10	
Supply Current in SLOW mode			V_{DD} = 3.0 V fs = 32.768 kHz V_{IN} = 2.8 V/0.2 V	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C , V_{DD} = 5 V.

Note 2: Input Current I_{IN1},I_{IN3} ; The current through resistor is not included, when the input resistor (pull-upor pull-down) is contained.

Note 3: Typical current consumption during AD conversion is 1.2 mA.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Analog Input Voltage Range	V_{CIN}	CIN5 to CIN0		V_{SS}	–	V_{DD}	V
Conversion Error			V_{DD} = 5.0 V	–	–	± 1.5	LSB

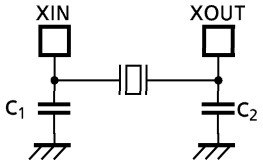
AC Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7/4.5 to 5.5 V, Topr = – 30 to 70°C)

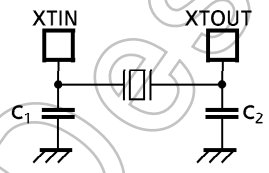
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 2.7/4.5 to 5.5 V, Topr = – 30 to 70°C)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric fieldstress applied for continuous reliable operation.

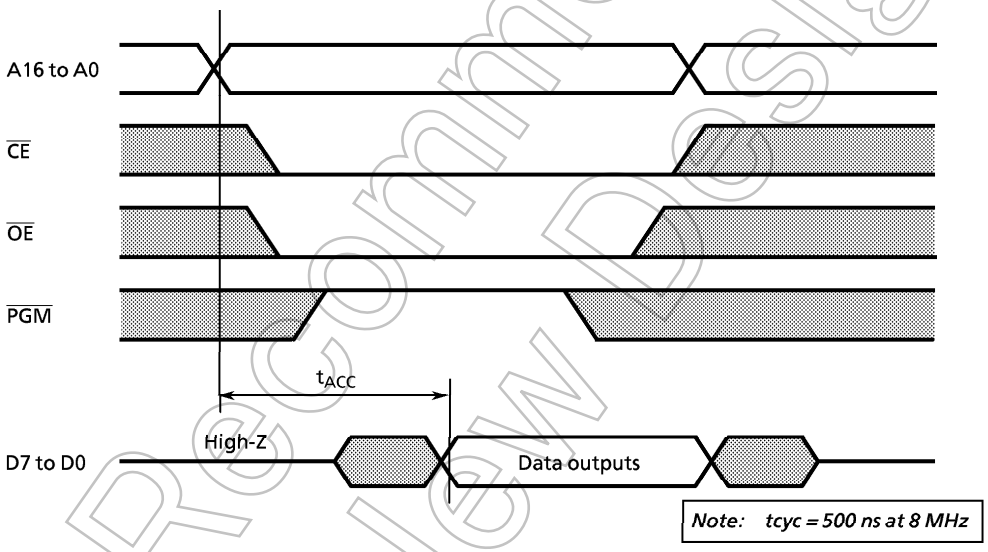
Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.
For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html

DC/AC Characteristics (PROM mode) (V_{SS} = 0 V)

(1) Read Operation

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		2.2	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	0.8	V
Power Supply Voltage	V_{CC}		4.75	5.0	5.25	V
Program Power Supply Voltage	V_{PP}					
Address Access Time	T_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	1.5 tcyc + 300		ns

Note: tcyc = 500 ns at 8 MHz

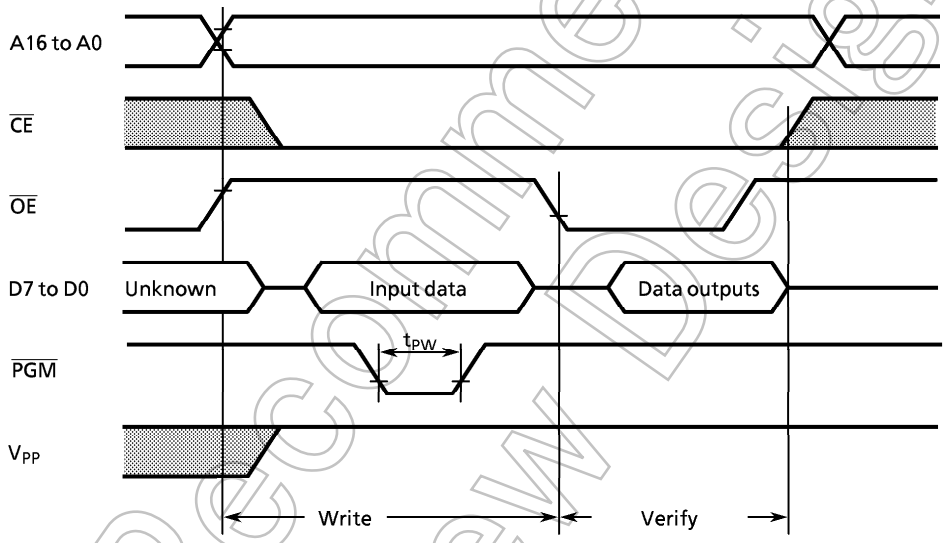


Note: tcyc = 500 ns at 8 MHz

(2) Program Operation (High-Speed program mode) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		2.2	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	0.8	V
Power Supply Voltage	V_{CC}		6.00	6.25	6.5	V
Program Power Supply Voltage	V_{PP}		12.5	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25 V V_{PP} = 12.75 ± 0.25	0.095	0.1	0.105	ms

High-Speed Programing Timing



Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V = V) to the V_{pp} pin as the device is damaged.
Note 3: Do not apply the parameter of program voltage (more than + 13 V) including overshoot to the V_{pp} pin.
Note 4: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.