

November 2010

Dear Customer

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

▶ **Restrictions on Consumer Electronics Control (CEC)** (November 2010)

*If your datasheet is dated 30 September 2010 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA Microcontrollers
TX03 Series

TMPM330FDFG TMPM330FYFG TMPM330FWFG

November 2010

Restrictions on Consumer Electronics Control (CEC)

This is to inform you of restrictions on use of the Consumer Electronics Control (CEC) of the TX03 Series of Toshiba microcontrollers.

If you need any further information, please contact your local Toshiba sales representative.

[Restrictions]

Restrictions are applied when the “low” samplings for noise cancellation, CECRCR1<CECLNC>, is used as the CEC function.

[Detailed restrictions]

1. Set the same values to both “low” samplings for noise cancellation CECRCR1<CECLNC> and the rising timing of data bit CECTCR<CECDTRS>.
2. Set the values of “low” samplings for noise cancellation CECRCR1<CECLNC> between “000” and “011”.

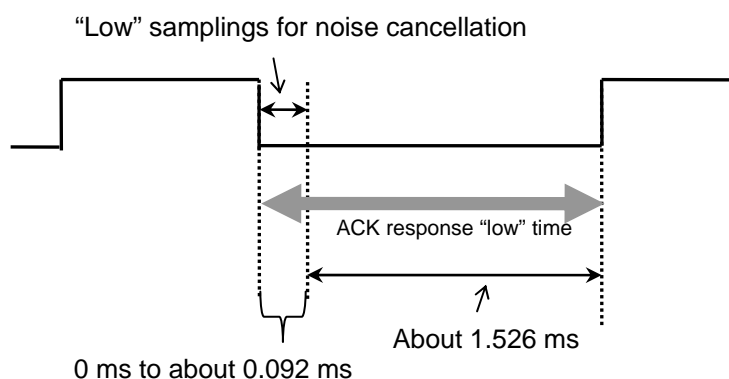
[Description]

Follow the above restrictions when you use the CEC function. In the restricted condition, “low” signal output timing (when a minimum cycle error is detected) and ACK response timing are as follows.

1. ACK response timing

“Low” time at an ACK response is as shown below.

ACK response “Low” time = (“Low” samplings for noise cancellation) + (base time: 1.526 ms)

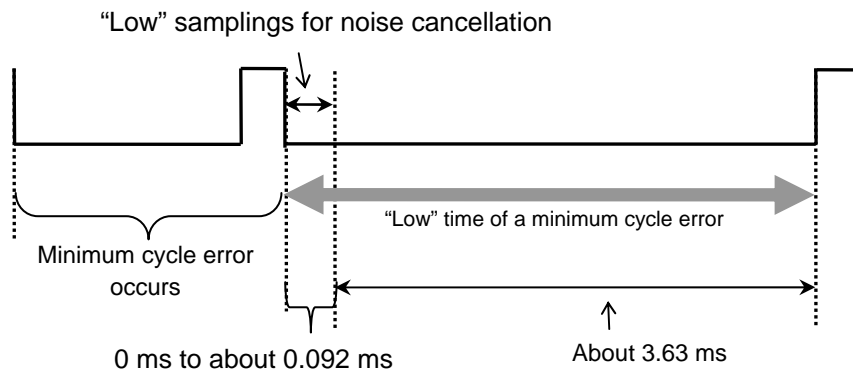


The “low” samplings for noise cancellation and the rising timing of data bit need to be configured the same. Values need to be carefully selected because the configuration of the rising timing of data bit affects “low” time of transmit data

2. "Low" output timing when a minimum cycle error occur

"Low" output timing when a minimum cycle error occurs is as shown below.

Minimum cycle error "Low" time = ("Low" samplings for noise cancellation) + (Base time: 3.63ms)



When a minimum cycle error occurs, "low" signal is output (about 3.63ms) after the elapse of "Low" samplings for noise cancellation.

[Setting Examples]

Setting examples are shown as below.

"Low" samplings for noise cancellation CECRCR1<CECLNC> = "010" 2/fs (about 0.06 ms)

Rising timing of data bit CECTCR<CECDTRS> = "010" Base time - 2/fs (about 0.06 ms)

In the above condition, "low" output periods of ACK, transmit data and a minimum cycle error are as shown below.

- ACK output waveform: 1.587 ms = 1.526 ms + 0.06 ms
- Logical "1" output: 0.54 ms = 0.6 ms - 0.06 ms
- Logical "0" output: 1.44 ms = 1.5 ms - 0.06 ms
- Minimum cycle error "low" output: 3.7 ms = 3.63 ms + 0.06 ms

[Corrected Sections]

□ Corrections on the page of CECRCR1 (Receive control Register 1)

1. The following part has been deleted:
A setting example when the "low" samplings for noise cancellation <CECLNC> are 4/fs (five consecutive fs clocks observed) or higher.
2. A note was added as follows: Use <CECLNC> with the same settings with CECTCR<CECDTRS>.

Bit	Bit Symbol	Type	Function
18-16	CECLNC[2:0]	R/W	The number of "Low" samplings for noise cancellation. 000: None (one time of fs clock observed.) 100: - (Reserved) 001: 1/fs (two consecutive fs clocks observed) 101: - (Reserved) 010: 2/fs (three consecutive fs clocks observed) 110: - (Reserved) 011: 3/fs (four consecutive fs clocks observed.) 111: - (Reserved) Specifies the time of the noise cancellation for each 1/fs when detecting "Low". It is considered as noise if "Low"s of the same number as the specified cycles are not sampled.

Note 4: <CECLNC> must be used under the same setting as CECTCR<CECDTRS>.

□ Corrections on the page of CECTCR (Transmit Control Register)

1. The following part has been deleted:

A setting example when rising timing of data bit<CECDTRS> is the base time $4/f_s$ or higher.

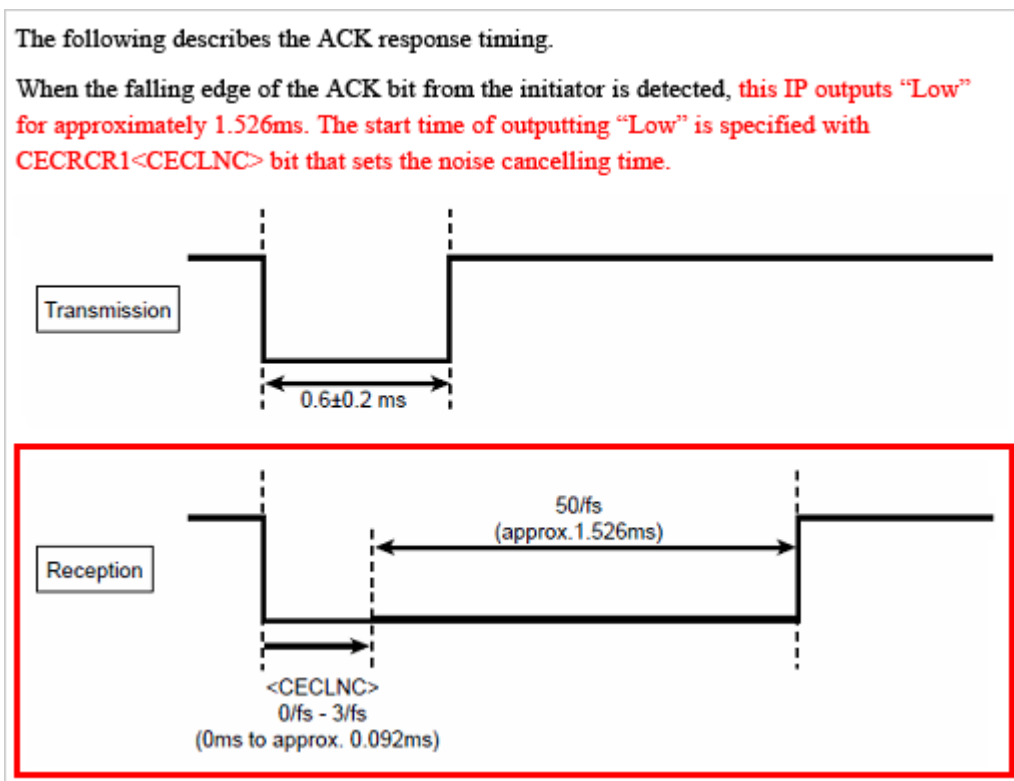
2. A note was added as follows: Use <CECDTRS> with the same settings with CECRCR1<CECLNC>.

Bit	Bit Symbol	Type	Function
14-12	CECDTRS[2:0]	RW	Rising timing of data bit. 000: Base time 100: Reserved 001: Base time- 1/ f_s 101: Reserved 010: Base time- 2/ f_s 110: Reserved 011: Base time- 3/ f_s 111: Reserved Specifies the rising timing of a data bit Base time is $20/f_s$ (approx. 0.610 ms, when logical "1") or $49/f_s$ (approx. 1.495 ms, when logical "0"). Enables to specify it between the ranges 0 to -3/ f_s by the unit of 1/ f_s .

Note: <CECDTRS> must be used under the same setting as CECRCR1<CECLNC>.

□ Corrections on the page of ACK response

Corrections on the description and the figures of "low" output timing when a ACK response is sent.



□ Corrections on the page of cycle error

The following note has been added to the description about the minimum cycle error.

Note: When minimum cycle error is detected, "low" is output after "low" detecting noise cancellation time.