

MOSFETs Silicon N-Channel MOS

# SSM6N55NU

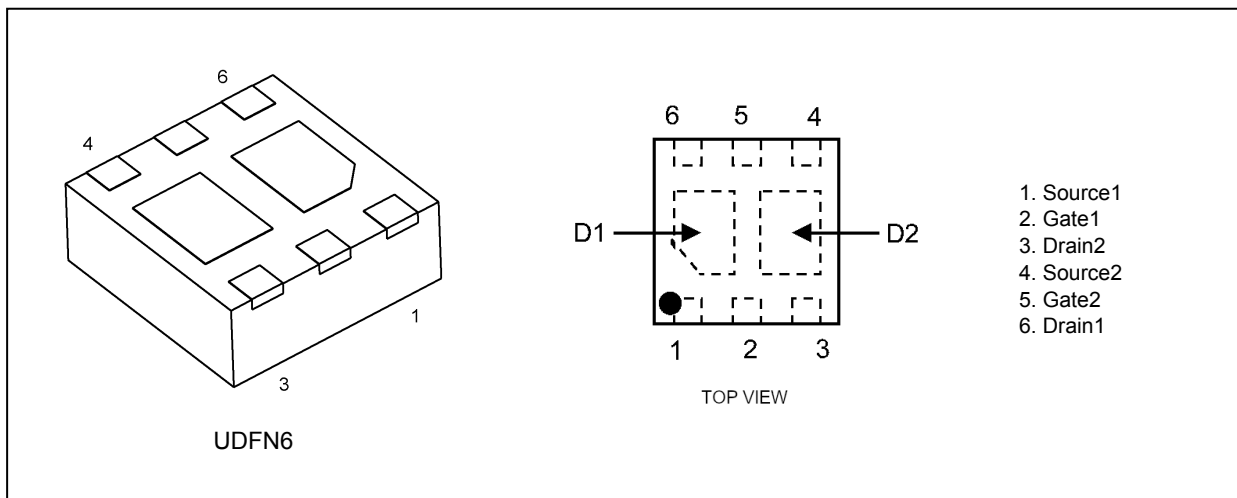
### 1. Applications

- Power Management Switches
- DC-DC Converters

### 2. Features

- (1) 4.5V gate drive voltage.
- (2) Low drain-source on-resistance
  - :  $R_{DS(ON)} = 46 \text{ m}\Omega$  (max) (@ $V_{GS} = 10 \text{ V}$ )
  - $R_{DS(ON)} = 64 \text{ m}\Omega$  (max) (@ $V_{GS} = 4.5 \text{ V}$ )

### 3. Packaging and Pin Assignment



Start of commercial production  
2011-11

### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25^\circ\text{C}$ ) (Q1,Q2 Common)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	30	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	
Drain current (DC) (Note 1)	$I_D$	4.0	A
Drain current (pulsed) (Note 1), (Note 2)	$I_{DP}$	10	
Power dissipation (Note 3)	$P_D$	1	W
Power dissipation $t \leq 10$ s (Note 3)	$P_D$	2	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed  $150^\circ\text{C}$ .

Note 2: Pulse width (PW)  $\leq 10$  ms, duty  $\leq 1\%$

Note 3: Device mounted on a  $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$  FR4 glass epoxy board (total dissipation) (with a dissipating copper surface of  $25.4\text{ mm} \times 25.4\text{ mm}$ )

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Electrical Characteristics

#### 5.1. Static Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified)(Q1,Q2 Common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	—	—	1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	10	—	—	
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 0.1\text{ mA}$	1.3	—	2.5	
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = 4.0\text{ A}, V_{GS} = 10\text{ V}$	—	33	46	m $\Omega$
		$I_D = 2.0\text{ A}, V_{GS} = 4.5\text{ V}$	—	48	64	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 1.0\text{ A}$	3.4	6.8	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (0.1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 5.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified) (Q1,Q2 Common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	280	—	pF
Reverse transfer capacitance	$C_{rss}$		—	20	—	
Output capacitance	$C_{oss}$		—	53	—	
Switching time (turn-on time)	$t_{on}$	$V_{DD} = 15\text{ V}, I_D = 0.5\text{ A}$ $V_{GS} = 0\text{ to }4.5\text{ V}, R_{GS} = 10\ \Omega,$ Duty $\leq 1\%$ , Input: $t_r, t_f < 5\text{ ns}$ Ground source, See Chapter 5.3	—	15	—	ns
Switching time (turn-off time)	$t_{off}$		—	12	—	

#### 5.3. Switching Time Test Circuit

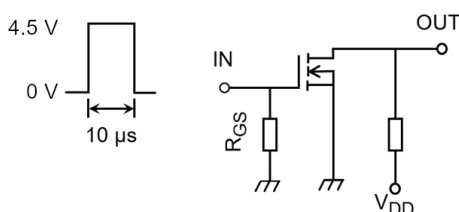


Fig. 5.3.1 Test Circuit of Switching Time

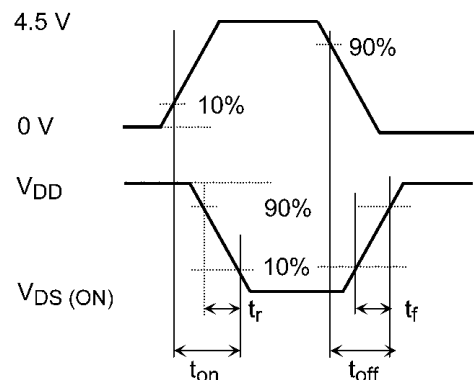


Fig. 5.3.2 Input Waveform/Output Waveform

#### 5.4. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified) (Q1,Q2 Common)

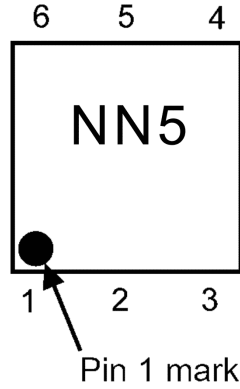
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = 15\text{ V}, V_{GS} = 4.5\text{ V},$ $I_D = 4.0\text{ A}$	—	2.5	—	nC
Gate-source charge 1	$Q_{gs1}$		—	1.6	—	
Gate-drain charge	$Q_{gd}$		—	0.5	—	

### 5.5. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$ unless otherwise specified) (Q1, Q2 Common)

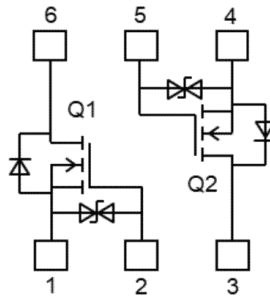
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_{DR} = 4.0\text{ A}$ , $V_{GS} = 0\text{ V}$	—	0.85	1.2	V

Note 1: Pulse measurement.

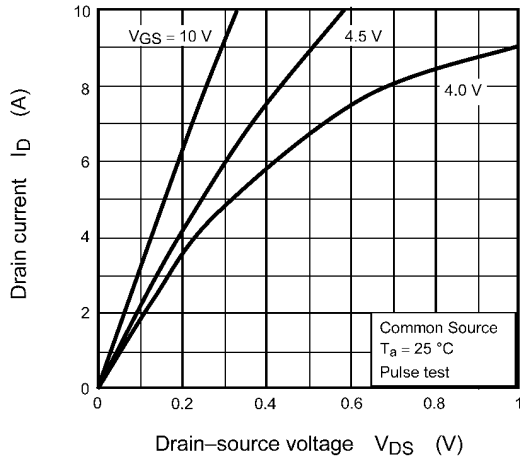
### 6. Marking



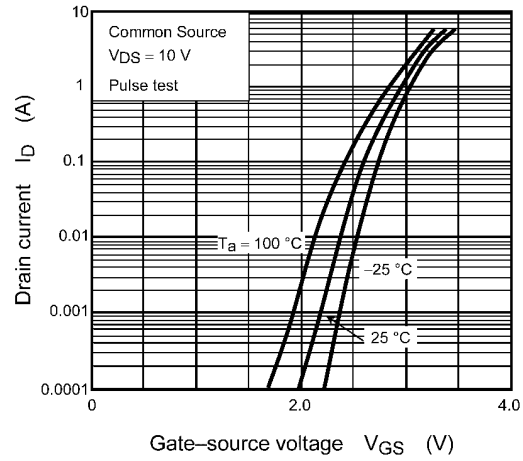
### 7. Internal Circuit



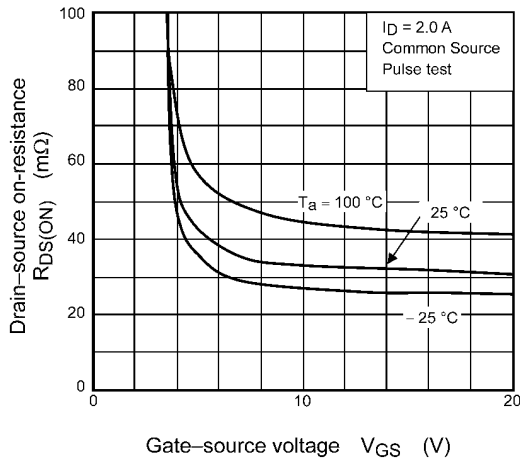
### 8. Characteristics Curves (Note)



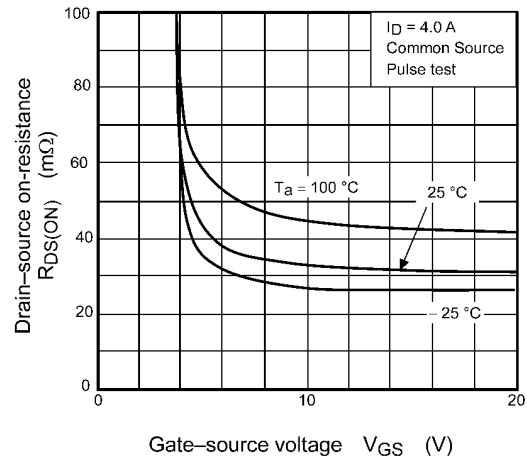
**Fig. 8.1  $I_D - V_{DS}$**



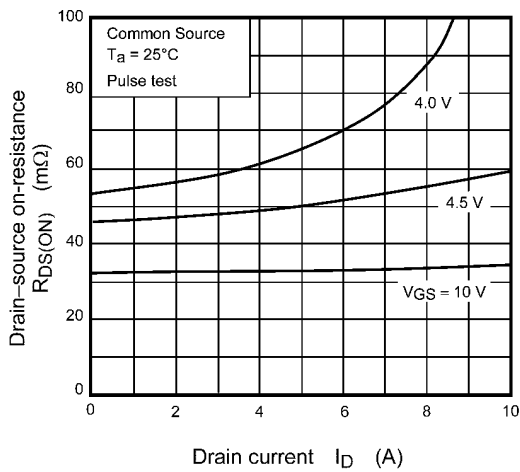
**Fig. 8.2  $I_D - V_{GS}$**



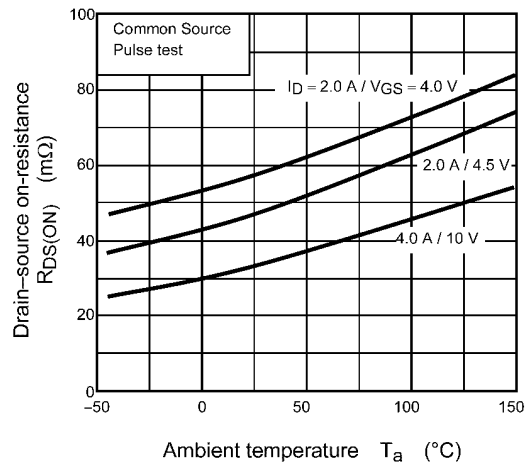
**Fig. 8.3  $R_{DS(ON)} - V_{GS}$**



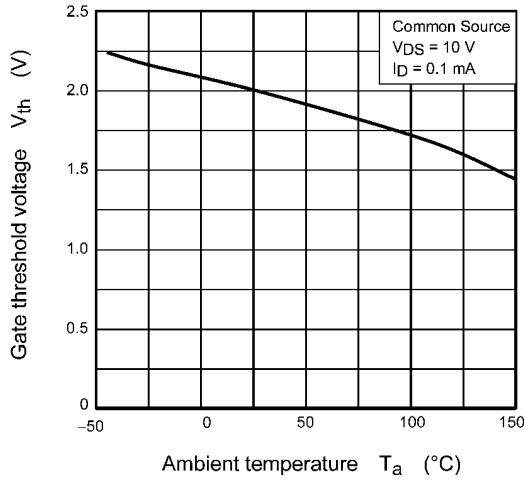
**Fig. 8.4  $R_{DS(ON)} - V_{GS}$**



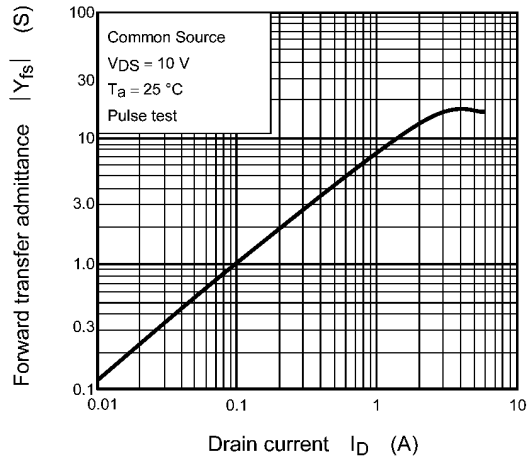
**Fig. 8.5  $R_{DS(ON)} - I_D$**



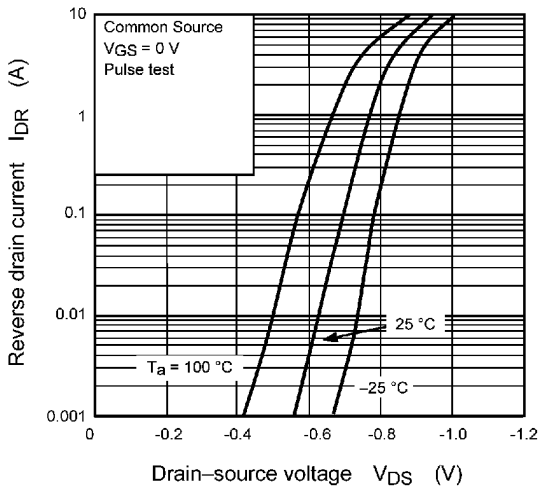
**Fig. 8.6  $R_{DS(ON)} - T_a$**



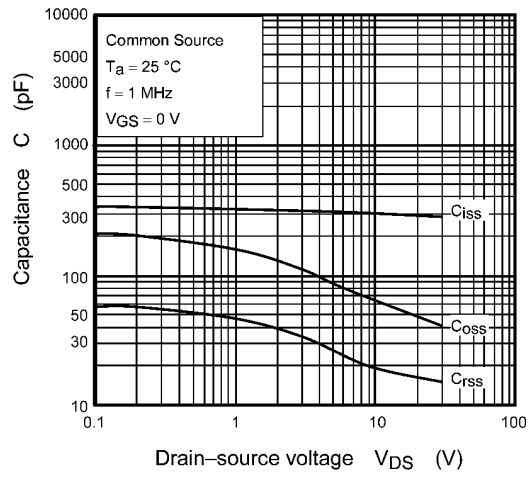
**Fig. 8.7  $V_{th} - T_a$**



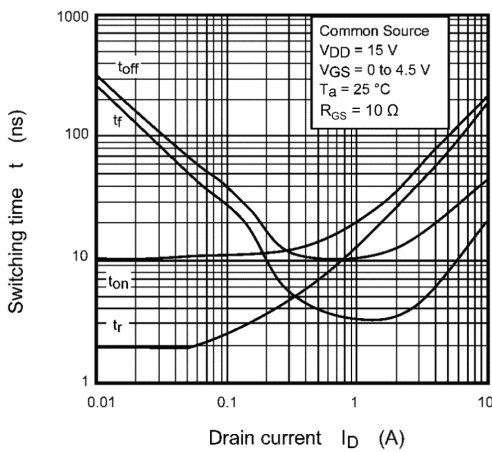
**Fig. 8.8  $|Y_{fs}| - I_D$**



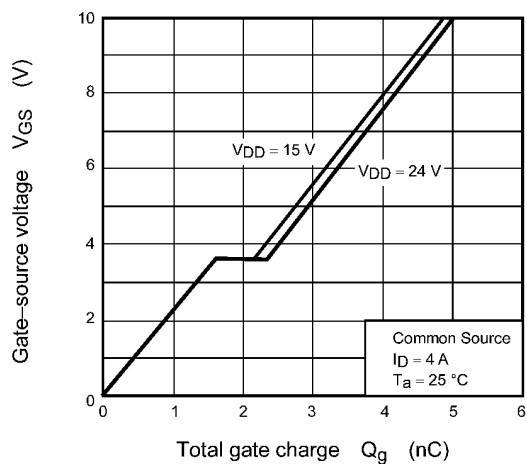
**Fig. 8.9  $I_{DR} - V_{DS}$**



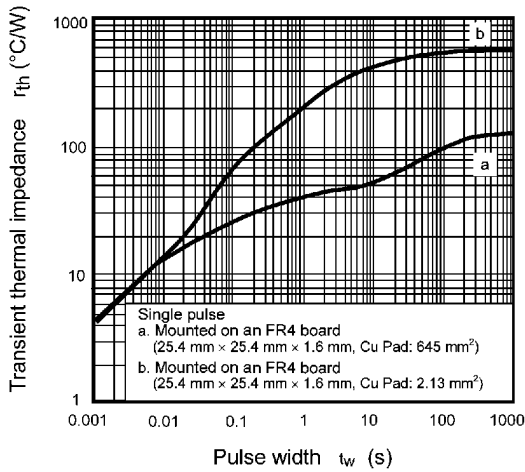
**Fig. 8.10  $C - V_{DS}$**



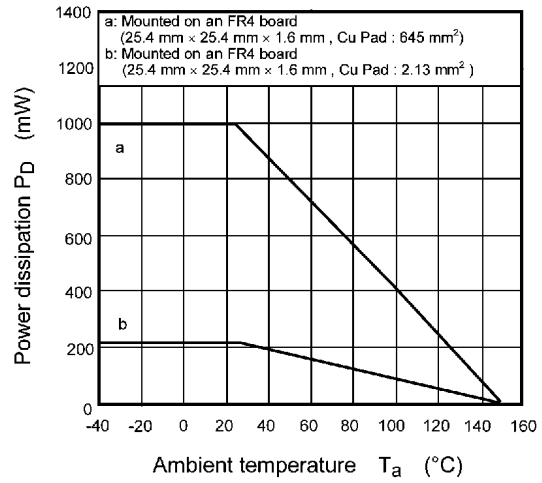
**Fig. 8.11  $t - I_D$**



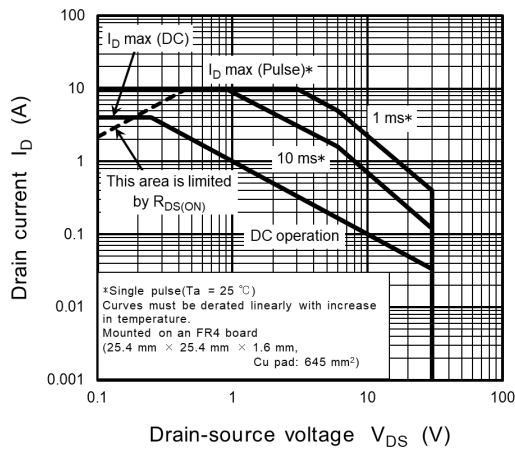
**Fig. 8.12 Dynamic Input/Output Characteristics**



**Fig. 8.13**  $r_{th} - t_w$



**Fig. 8.14**  $P_D - T_a$

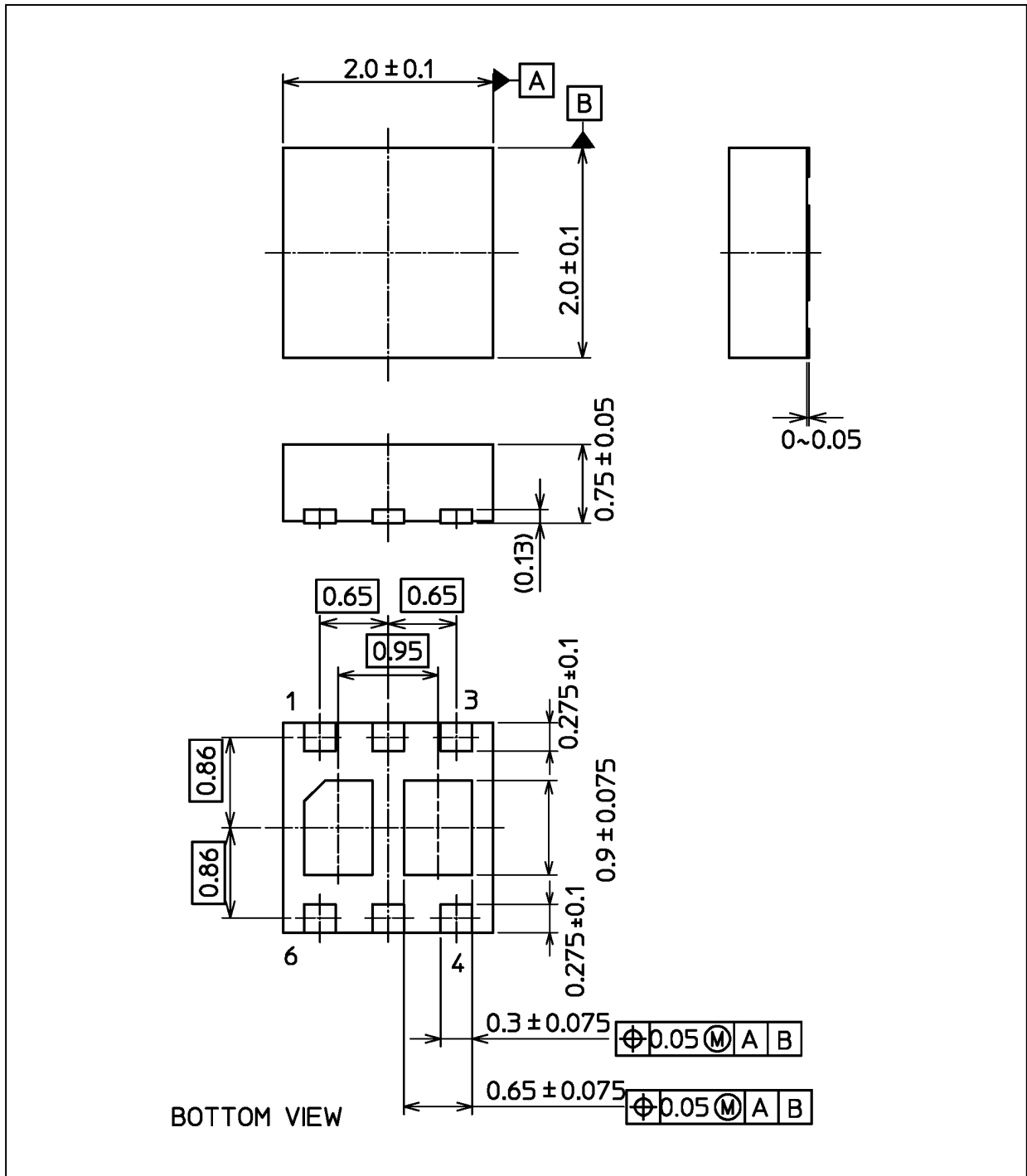


**Fig. 8.15** Safe Operating Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm



Weight: 8.5 mg (typ.)

Package Name(s)
JEDEC: SOT-1118
Nickname: UDFN6



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