Basic Characteristics and Application Circuit Design of Transistor Couplers

Outline

This document outlines the basic characteristics and application design of general-purpose transistor output photocouplers (optical isolators).

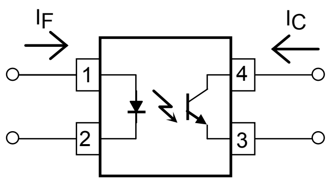
Contents

Photocouplers optically links, via transparent isolating material, a light emitter and a photodetector. Used as an interface between circuits with different ground potentials, photocouplers replace isolation transformers and electromagnetic relays. Traditionally, relays or transformers have been used for isolation interfaces between logic circuits and power line load circuits. Photocouplers not only replace these devices, but also have merits such as elimination of impedance mismatching, improvement in isolation capability between input and output, and ease of noise cutoff. Moreover, while circuits nowadays consist of many more LSIs and microcomputers than before, additional merits of photocouplers include reduction in the area occupied on the printed circuit board, and maintenance-free operation due to improvement in reliability. This section outlines the basic characteristics and application design of general-purpose transistor output photocouplers (optical isolators).

1. Basic Characteristics

1-1. Current Transfer Ratio (CTR)

Figure1.1 shows the pin configuration of TLP785. CTR is defined as the ratio I_C/I_F (expressed as a percentage) of the output-side transistor collector current I_C to the current I_F flowing in the input-side LED. Figure 1.2 shows the CTR distribution for TLP785. CTR varies with I_F. At standard conditions of I_F = 5 mA and V_{CE} = 5 V, CTR is designed to be between 50% to 600%.



CTR =100 x I_C / I_F [%]

Figure 1.1 Pin Configuration of TLP785

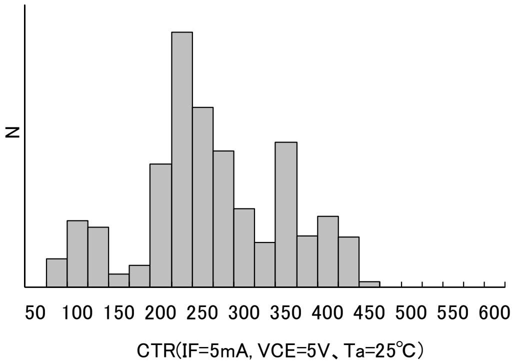


Figure 1.2 CTR Distribution of TLP785

When using transistor couplers, it is necessary to pay particular attention to the following. The section 2-4 shows the example of circuit design for transistor couplers.

(1)CTR degradation

Light output of the LED in the photocoupler decreases gradually over time, contributing to CTR degradation. It is, therefore, advisable to provide a design margin to offset this anticipated CTR degradation.

(2)CTR - I_F dependency

When a transistor coupler is used with low input current, its CTR drops as shown in Figure 1.3. This effect should also be considered during circuit design.

(3)CTR - Ta dependency

At high temperatures, the decrease in LED light emission efficiency is dominant over the increase in h_{FE}, resulting in a reduction of the CTR. Attention should also be paid to this effect during circuit design.(Figure 1.4)

(4) CTR-V_{CE} dependency

As with h_{FE} of general transistors, the rate of change of collector current decreases at saturation. (Figure 1.5)

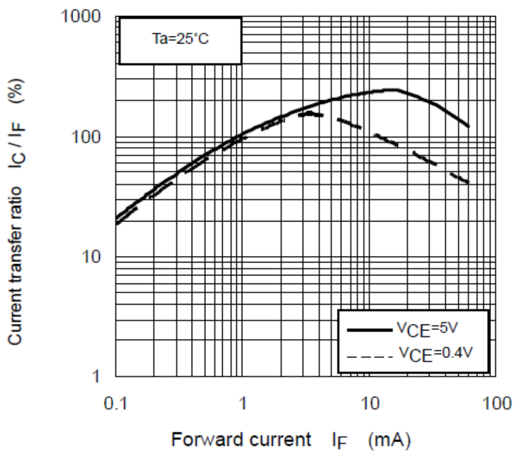


Figure 1.3 CTR (I_C/I_F) - I_F

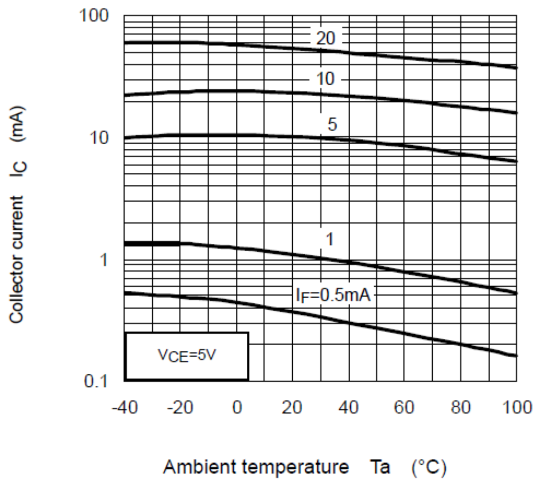


Figure 1.4 I_C -Ta

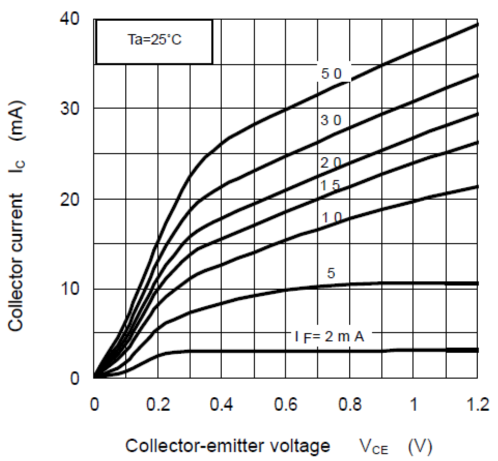


Figure 1.5 I_C -V_{CE}

1-2. Switching Time

When the phototransistor is used in a saturated switching mode, the switching time must be considered. Among a phototransistor's switching time characteristics, fall time (tf), being the longest in duration, is the most significant. It is represented approximately by

tf to 2.2 × C_{ob} × h_{FE} × R_L.

Where,

C_{ob}: collector-to-base capacitance

h_{FE}: DC current gain

R_L: load resistance

Switching time of TLP785 is shown in Figure 1.6. Thus, if an application requires a response speed of 1 kbit/s and above, the design must take into account the transistor coupler's R_L dependency.

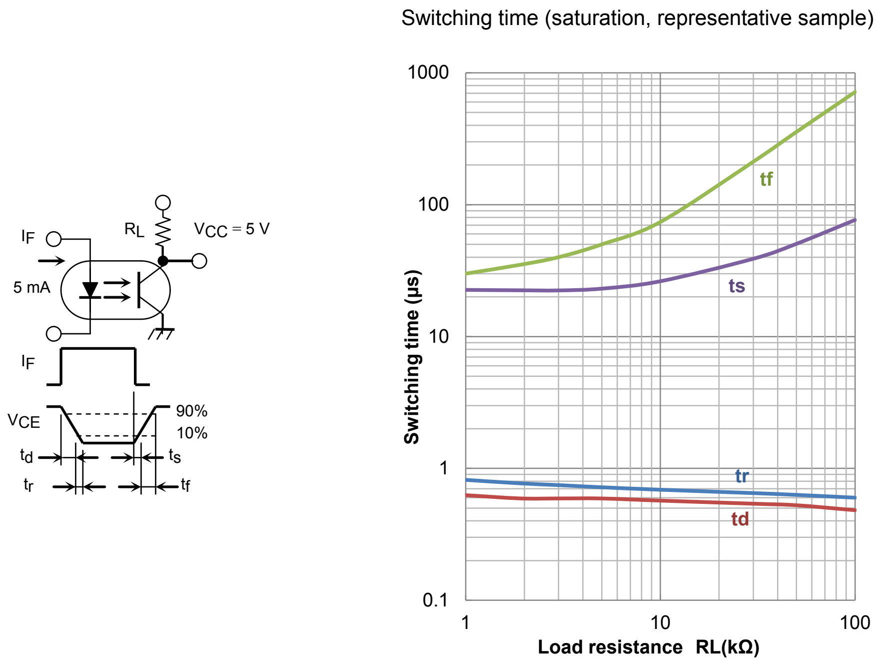


Figure 1.6 Switching Time - R_L

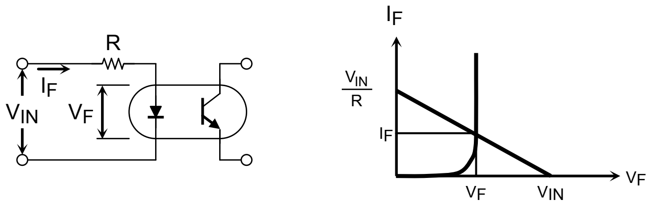
2. How to Use Transistor Couplers

2-1. LED Control Circuits

2-1-1. DC drive

Figure 2.1(a) shows an example of controlling LED drive current by switching the supply voltage V_{IN} on and off.
Figure 2.1(b) indicates a load line in the (a) circuit.
In this case, the resistor R is as follows.

$$R = \frac{V_{IN} - V_F}{I_F}$$



(a) (b)

Figure 2.1

For example, when I_F = 10 mA, $V_{F\ (max)}$ = 1.35 V, and V_{IN} = 5 V,

$$R = \frac{(5 - 1.35)\ V}{10\ mA} = 365\ \Omega$$

Therefore, the resistor should be selected as R = 360 Ω. In the case where V_F = 0.9 V due to the variation in different samples or the influence of operating temperature, the value of I_F is 11.4 mA.

2-1-2. Reverse Voltage Protection

To prevent a reverse surge voltage in the LED, a Si diode (for example, 1SS352) should be connected in reverse parallel with the LED, as shown in Figure 2.2, so that the reverse surge voltage bypasses the LED.

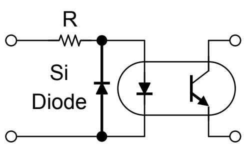


Figure 2.2

2-1-3. Threshold Voltage

When the input voltage V_{IN} is not absolutely zero or some unnecessary current flow is in the data transmission line, the threshold voltage of the LED should be raised up to a certain level by connecting a resistor in parallel with the light-emitting diode. (Figure 2.3)

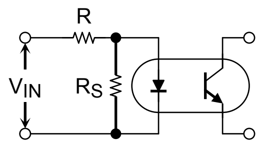


Figure 2.3

If the forward voltage of the LED in the zero-light-emission state V_T, the OFF-level input voltage $V_{IN\ (OFF)}$, and the OFF-level input current $I_{IN\ (OFF)}$ are given as follows.

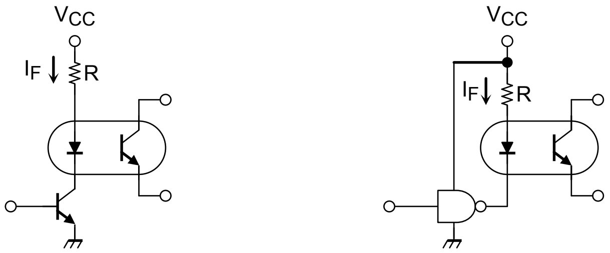
$$V_{IN(OFF)} \simeq V_T + R \cdot \frac{V_T}{R_S} = \left(1 + \frac{R}{R_S}\right) V_T$$

$$I_{IN(OFF)} \simeq \frac{V_T}{R_S}$$

In the case of the Toshiba infrared LED for transistor couplers), the value of V_T is 0.5 V.

2-1-4. Driving by Transistor or IC

Figure 2.4 shows examples of LED drive circuits controlled by (a) a transistor and (a) an IC.



$$R = \frac{V_{CC} - V_F - V_{CE\,(sat)}}{I_F}$$

$$R = \frac{V_{CC} - V_F - V_{OL}}{I_F}$$

(a) LED Drive Circuit Controlled by a Transistor **(b) LED Drive Circuit Controlled by an IC**

Figure 2.4

2-1-5. AC Drive

In this case, a bridge rectifier is used as shown in Figure 2.5.

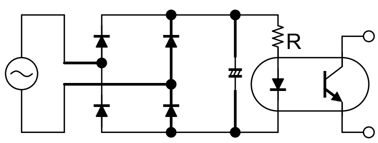
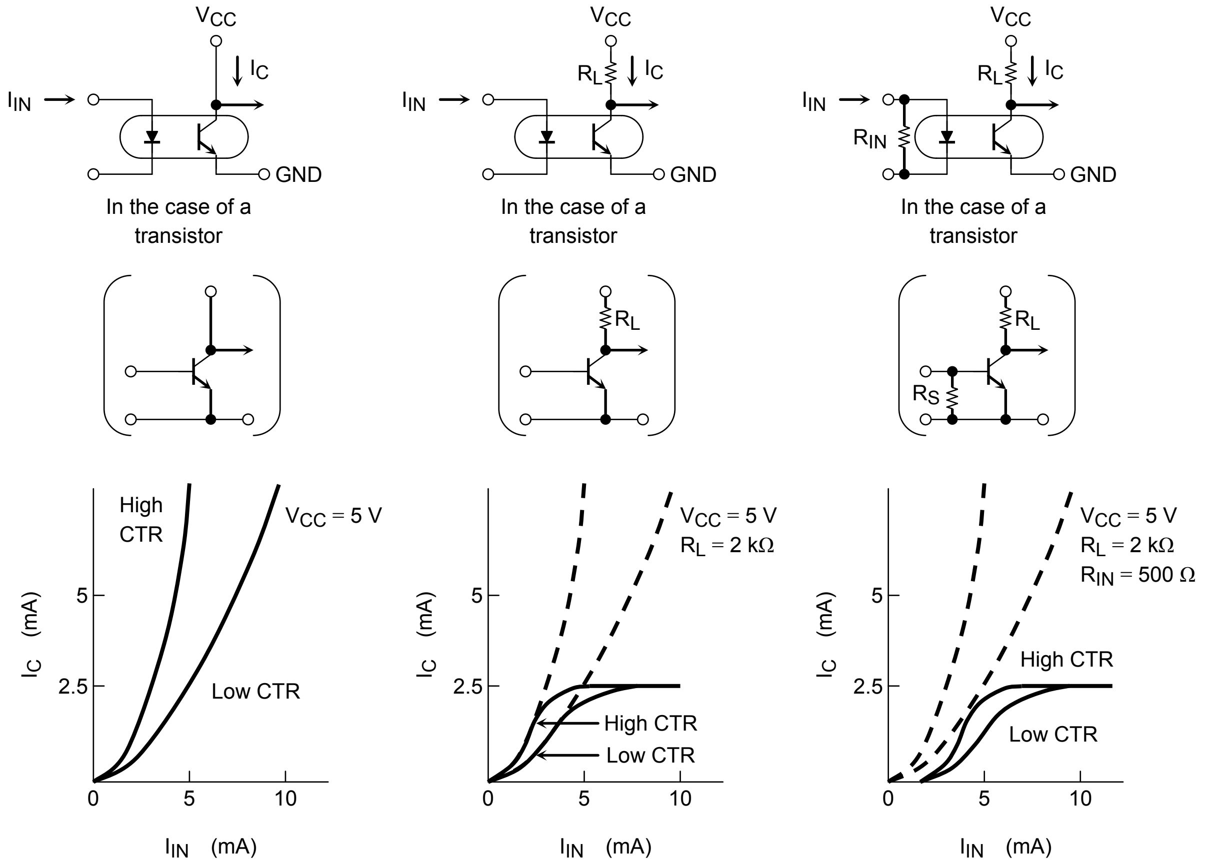


Figure 2.5

2-2. Examples of Application to Signal Transmission

Transistor couplers which have high photosensitivity and high current-transfer ratios are effective as interfaces for signal transmission. However, transmission lines are generally subjected to all kinds of noises, and it is therefore necessary to take countermeasures against these noises at the receiving side. In many cases, transistor couplers designed in a circuit similar to that shown in Figure 2.6 (b). However, this circuit design is vulnerable to certain kinds of interference in signal transmission. While common-mode noise do not pose a problem because of the isolation characteristics of transistor couplers, no measures have been taken against differential noise. Figure 2.6 (c) is an example of a circuit useful for eliminating differential noise. This circuit is the same as that of general-purpose transistors, with the addition of a resistor inserted between the base and the emitter.

High CTR transistor couplers are more effective in signal transmission applications. It can be seen from the graph that for a high CTR product, the cut-off area and the saturation area are closer than that of a low-CTR product. Because of this, it is possible to specify the threshold output voltage level with sufficient margin to allow for ease and flexibility in design. This circuit is recommended for that purpose.



(a) Characteristics of Transistor Couplers

(b) Characteristics with Load Connected

(c) Characteristics for Transmission

Figure 2.6 Load Characteristics of Transistor Couplers

2-3. Transistor Coupler Circuit Design for Signal Transmission

Figure 2.7 shows a basic transistor coupler interface circuit, where collector current I_C flows on the output side as LED current I_F is applied on the input side.

The following points are important in determining the values of the various parameters in the circuit:

(1) $I_{IN} = I_F = 0$ (OFF state)

Only a dark current $I_D(I_{CEO})$ flow at the output transistor in this state. In order to maintain the OFF state, the output voltage $V_{OUT\ (OFF)}$ should be higher than V_H (the required high level voltage) as follows:

$$V_{CC} - I_D \times R_L = V_{OUT\ (OFF)} > V_H$$

Where, V_{CC}: Applied voltage (supply voltage)

The leakage current ID increases as the ambient temperature rises (see Figure 2.8 I_D vs. Ta), so the I_D value will have to be considered at the worst case, here being the maximum operating temperature.

As such, the value of R_L should meet the following formula:

$$R_L < \frac{V_{CC} - V_H}{I_D}$$

(2) $I_{IN} = I_F$ (ON state)

When the collector current $I_{C\ (ON)}$ flows on the output side of the transistor coupler, output $V_{OUT\ (ON)}$ has to be less than V_L (the required low level voltage) as follows:

$$V_{CC} - I_{C\ (ON)} \times R_L = V_{OUT\ (ON)} < V_L$$

Therefore,

$$R_L > \frac{V_{CC} - V_L}{I_{C(ON)}}$$

Generally when the R_L value is large, the switching response time increases, so the R_L value should be kept as small as possible.

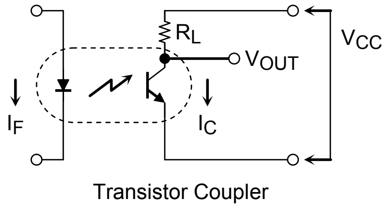


Figure 2.7 Transistor Coupler

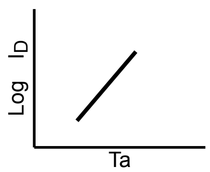


Figure 2.8 I_D vs.Ta

(3) Considerations for input current I_{IN} in the "ON" state

The characteristic curves of I_C vs. I_F, CTR vs. Ta, and CTR vs. t as shown in Figure 2.9, Figure 2.10 and Figure 2.11 respectively can be found in the product technical data sheet.

The transistor coupler CTR test is performed at the specific point ① in Figure 2.9. This point ① is not always the same as the actual operating point, so some compensation work is required to be done by the following procedure;

i) Draw the extrapolated CTR min curve Ⓑ in parallel with the reference curve Ⓐ.

The point of intersection ① shows the "CTR min" specification value.

Where, CTR = I_C/I_F, I_C min = CTR min × I_{F1}

ii) Determine I_{F2} from the intersection point of $I_C = I_{C\ (ON)}$ with curve Ⓑ.

I_{F2} indicates the minimum input current at Ta = 25°C and operating time t = 0 hour. When considering the relationship between CTR and Ta (Figure 2.10), as well as CTR degradation (Figure 2.11), the minimum input current I_{IN} has to conform to the following formula.;

$$I_{IN} > I_{F2} \times \frac{1}{D_{Ta}} \times \frac{1}{D_t} \times \alpha$$

Where, D_{Ta}: Rate of CTR fluctuation within the operating temperature range

D_t: CTR degradation rate after "t" hours of operation

α: System design margin

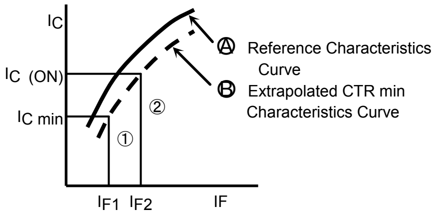
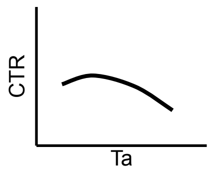


Figure 2.9 I_C vs. I_F



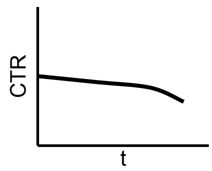


Figure 2.10 CTR vs. Ta **Figure 2.11 CTR vs.t**

2-4. Design Example for Interface Circuit Using Transistor Coupler

Figure 2.12 shows a circuit using a DIP 4 pin transistor coupler as an interface between TTLs. In order to ensure absolute ON/OFF operation of the TTL, the LED current I_F should be set to satisfy I_{OL} which is determined by R_C and I_{IL}.

Example of Design Specifications

Operating temperature T_{opr} : 0 to 70°C
Data transmission rate : 5 kbit/s
Supply voltage : V_{CC} = 5 V ± 5%
Operating life : 10 years (88,000 hours)
System working ratio: 50%

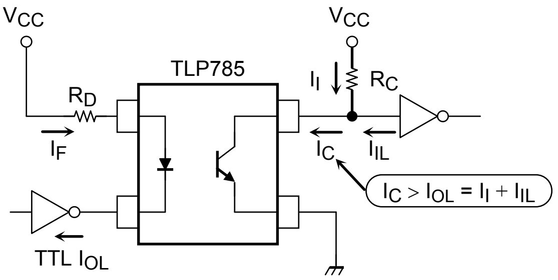


Figure2.12

Interface Circuit between TTLs Using a 4pin Transistor Coupler

TLP785 with CTR free rank is used. Specifications of products TLP785 for designing interface circuits are shown in Table 2.1.

Table 2.1 Principal Characteristics of TLP785

Item	Symbol	Test Condition (Ta = 25°C)		min	typ.	max	Unit
Forward voltage	V_F	I_F = 10 mA		1.0	1.15	1.3	V
Collector to emitter Breakdown voltage	$V_{(BR)\ CEO}$	I_C = 0.5 mA		80	—	—	V
Emitter to collector Breakdown voltage	$V_{(BR)\ ECO}$	I_E = 0.1 mA		7	—	—	V
Collector dark current	I_{CEO}	I_F = 0, V_{CE} = 24 V		—	0.01	0.1	μA
		I_F = 0, V_{CE} = 24 V, Ta = 85°C		—	0.6	50	μA
Current transfer ratio	CTR (I_C/I_F)	I_F = 5 mA, V_{CE} = 5 V	free	50	—	600	%
			GB rank	100	—	600	
			GR rank	100	—	300	
			BL rank	200	—	600	
Collector to emitter Saturation voltage	$V_{CE\ (sat)}$	I_F = 8 mA, I_C = 2.4 mA		—	0.2	0.4	V

2-4-1. Setting of Forward Current I_F

The maximum forward current I_F is typically 16 mA for TTL I_{OL}, and is subjected to the constrain $I_F \leq I_{OL}$. The maximum allowable value of I_F found from Figure 2.13 is 38 mA. However, I_F should be kept as small as possible because CTR degradation increases with the increase of forward current. Figure 2.14 shows the degradation of CTR. In order to realize the design of continuous operating life of 10 years (approximately 88,000 hours, 44,000 at system working ratio 50%), consider the degradation of CTR to be 50% (D_t =0.5). The CTR measurement condition of TLP785 is at I_F =5mA, so forward current should be set at I_F = 5 / 0.5 = 10 mA for the initial design.

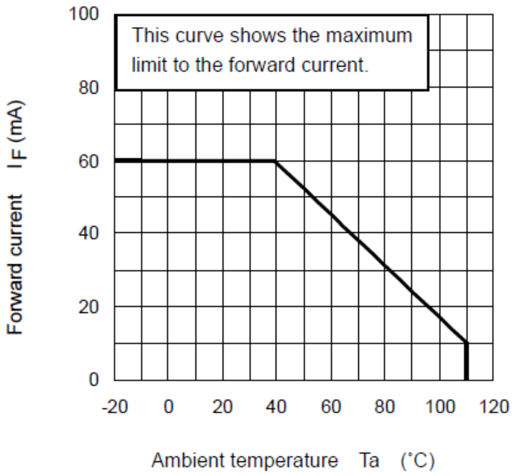


Figure 2.13 Ambient Temperature vs. Allowable Forward Current (TLP785)

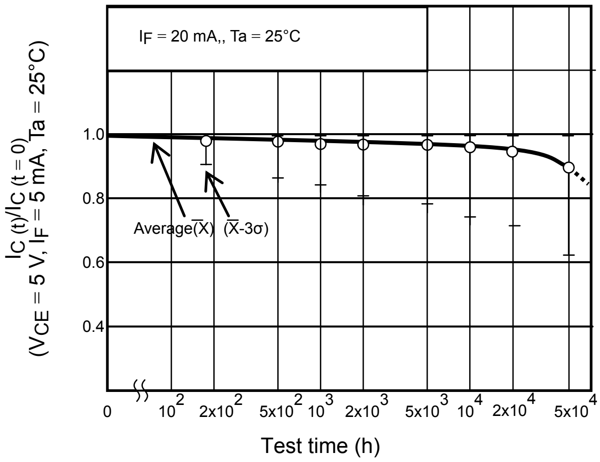


Figure 2.14 Lifetime Test Data *
(CTR degradation)

*This data shows an example of the CTR degradation curve.

Please design the circuit after confirming the reliability information on individual products.

2-4-2. Setting of the I_F Limiting Resistance R_D

Forward current (typ.) is expressed by the following formula:

$$I_{F(typ.)} = \frac{V_{CC} - V_{F(typ.)} - V_{OL}}{R_{D(typ.)}}$$

where $V_{F\ (typ.)}$ is obtained from the technical datasheet. For TLP785,

$V_{F\ (typ.)}$ = 1.15 V (I_F = 10 mA)

R_D is determined as follows:

$$R_D = \frac{5V - 1.15V - 0.4V}{10mA}$$

$$= 345\ \Omega$$

Therefore, R_D = 330 Ω ± 5% will be optimum.

Then $I_{F\ (min)}$ and $I_{F\ (max)}$ should be checked to make sure that actual values of I_F will remain within allowable tolerances:

$$I_{F(min)} = \frac{V_{CC(min)} - V_{F(max)} - V_{OL}}{R_{D(max)}}$$

$$= \frac{4.75V - 1.3V - 0.4V}{347\Omega}$$

$$= 8.8\ mA$$

$$I_{F(max)} = \frac{V_{CC(max)} - V_{F(min)} - V_{OL}}{R_{D(min)}}$$

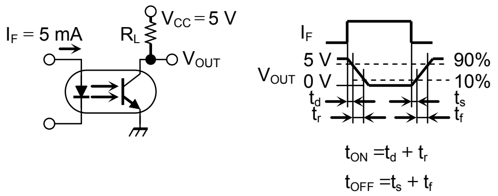
$$= \frac{5.25V - 1.0V - 0.4V}{314\Omega}$$

$$= 12.3\ mA$$

2-4-3. Setting of Pull-up Resistance $R_{C\ (max)}$

$R_{C\ (max)}$ should be set according to the switching time and dark current $I_{CEO\ (max)}$ at the maximum operating temperature of the transistor coupler. Since the design specification for data transmission rate is 5 kbit/s, the total switching time should satisfy the below condition.

$$T = tr + td + tf + ts \leq 200\ \mu s$$



Switching time changes with various conditions, such as CTR (current transfer ratio), R_L (load resistance), and Ta (ambient temperature). R_L should be designed to accommodate these changes in these conditions. Please check the technical datasheet for the influence of change in I_F, V_{CC} etc. Here, T(max) is set at T≤100 μs taking into consideration of a variation margin for I_F, V_{CC} etc.

The switching time t_{OFF} (=t_s + t_f) increases as the CTR rises (see Figure 2.15 CTR vs. Switching time), this is because the h_{FE} of photo-transistor tends to increase as the CTR rises. Therefore, it will be desirable to choose a product with a small CTR rank when a maximum switching time is specified.

Products of CTR free rank (50 to600%) seem suitable for satisfying the condition T≤100 μs. However, we can see from Figure 2.15 that switching time for products of similar rank can vary slightly (t_{OFF} has a difference for about 10 μs on the similar CTR=200% samples). Therefore GR rank (100 to 300%) is selected taking into consideration such variation in characteristics and influences due to other parameter change (Ta, R_L etc).

Next, refer to Figure 2.16 Ta vs. switching time (CTR=300% sample). Switching time is increased by 40% when Ta is raised from 25˚C to 70˚C. Therefore at Ta=70°C, T= 100 / 1.4 < 70μs.

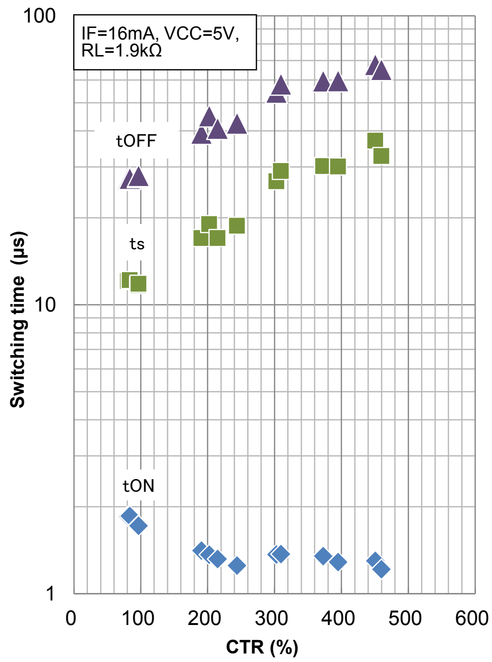


Figure 2.15 CTR vs. Switching time (saturated)

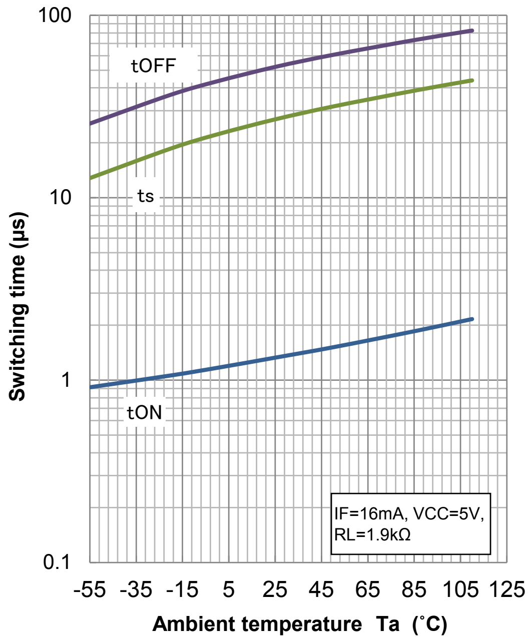


Figure 2.16 Ta vs. Switching time (saturated)

The load resistance R_L is obtained from the switching time characteristic (for saturated operation) in Figure 2.17. Reading off the graph, for T≤70 μs, load resistance should satisfy $R_L \leq 3$ kΩ. R_L can be expressed in terms of R_C and the parallel resistance of the standard TTL input resistance R_{IN} (Figure 2.18). $R_{c(max)}$ is obtained as follows;

$$R_L = R_C // R_{IN}$$

$$R_L = 1 / ((1/ R_C) + (1 / R_{IN})) \leq 3k\Omega$$

As, $R_{IN} = 4k\Omega$

$$R_C \leq 12k\Omega$$

Next, check $R_{C\ (max)}$ with regards to the dark current $I_{CEO\ (max)}$. The relation between $I_{CEO\ (max)}$ and $R_{C\ (max)}$ is shown below;

$$R_{C(max)} = \frac{V_{CC(min)} - V_{IH}}{I_{CEO}}$$

V_{IH} is high level input voltage for TTL.

Here, $I_{CEO(max)}$ is estimated at Ta = 70°C. Temperature dependencies of $I_{CEO(typ.)}$ at alternative parameter values of V_{CE} = 5 V, 10 V, and 24 V are shown in Figure 2.19.

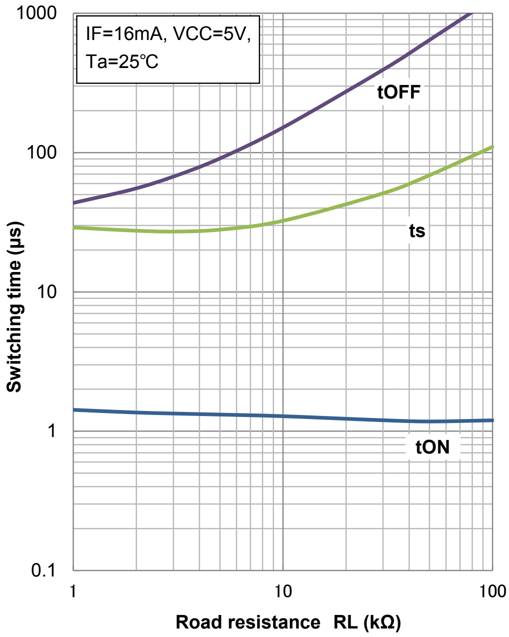


Figure 2.17 R_L vs. Switching Time (Saturated)

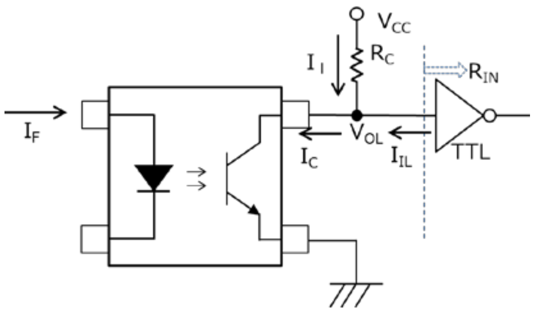


Figure 2.18 R_L can be Expressed by R_{IN} and R_C

In the case of the TLP785 transistor coupler,

$I_{CEO\ (max)}$ = 50 μA at Ta = 85°C and V_{CE} = 24 V (technical datasheet specifications). Taking V_{CE} dependency and Ta dependency into consideration using Figure 2.19, $I_{CEO\ (max)}$ is estimated at Ta = 70°C and V_{CE} = 5 V.

V_{CE} dependency: $I_{CEO\ (typ.)}$ is reduced by 1/3 when V_{CE} is varied from 24 to 5 V.

Ta dependency: $I_{CEO\ (typ.)}$ is reduced by 1/4 when Ta is varied from 85 to 70°C.

Therefore, $I_{CEO\ (max)}$ at Ta = 70°C and V_{CE} = 5 V is estimated to be,

$$I_{CEO} = 50\mu A \times \frac{1}{3} \times \frac{1}{4} = 4.2\mu A$$

At I_{IH} = 40 μA for general TTLs and $R_{C\ (max)}$ will be obtained as follows;

$$R_{C(max)} = \frac{4.75V - 2V}{4.2\mu A + 40\mu A} = 62\,k\Omega$$

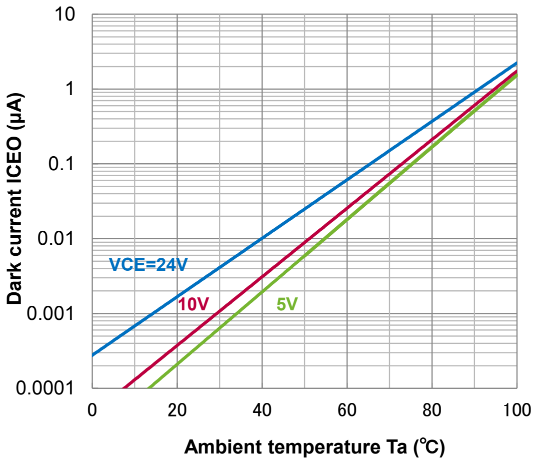


Figure 2.19 I_{CEO} vs. Temperature

Since this is a larger value than 12kΩ set up from switching time, $R_{C\ (max)}$ is set at 12kΩ.

2-4-4. Setting of Pull-up Resistance R_C

Assuming the worst case scenario where the collector current I_C is at its minimum in Figure 2.18, R_C can be expressed by the following relation;

$$R_C \geq \frac{V_{CC(max)} - V_{OL}}{\min I_C - I_{IL}}$$

$$\min I_C = I_{C\ (min)} \times D_{IF} \times D_t \times D_{VCE} \times D_{Ta}$$

Where,

D_t: I_C degradation rate after a certain time has passed.

D_{IF}: I_C change rate at an I_F setting for your designing.

D_{VCE}: I_C drop rate under $V_{CE\ (sat)}$ condition.

D_{Ta}: I_C fluctuation rate with changes in the operating temperature T_{opr}.

These values are obtained from technical data.

In the case of the TLP785:

From Figure 2.14, D_t = 0.5 (t = 44,000 h, 50% operating ratio)

From Figure 2.20, D_{IF} = 2.3 (at I_F = 10 mA)

From Figure 2.21, D_{VCE} = 0.7 (at V_{CE} = 0.4 V)

From Figure 2.22, D_{Ta} = 0.75 (at Ta = 70°C)

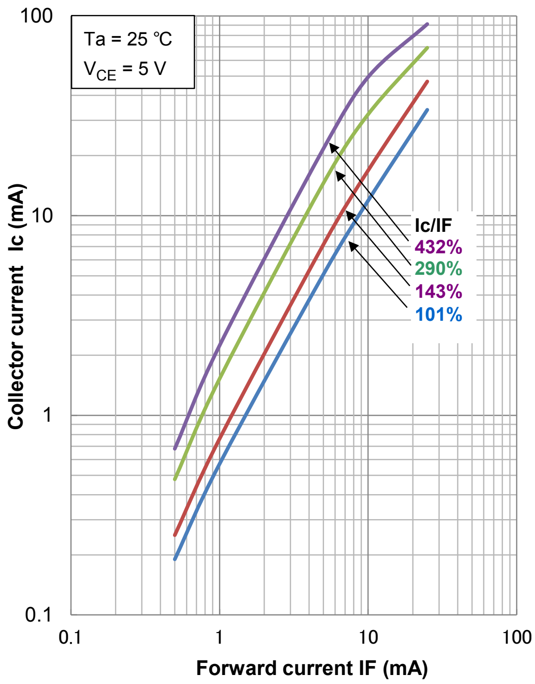


Figure 2.20 I_C vs. I_F Curves Varying According to Different I_C/I_F Rations

On the other hand, GR rank is selected at section 2.4.3 as I_C (min) = 5 mA (at I_F = 5 mA × I_C/I_F (min) = 100%), and

min I_C = 5 mA × 2.3 × 0.5 × 0.7 × 0.75

= 3 mA

Accordingly, I_{IL} is 1.6 mA for general TTLs and R_C (min) can be obtained as follows:

$$R_{C(min)} = \frac{5.25V - 0.4V}{3.0mA - 1.6mA} \simeq 3.5k\Omega$$

In other words, R_C can be set from 3.5 kΩ to 12 kΩ, but it is also necessary to consider the switching speed required by the system and the importance of absolute ON or OFF conditions. If the switching speed is considered to be relatively more important, R_C should be set to a value close to R_C (min). On the other hand, if the certainty of ON and OFF operation is considered to be the most important criterion, a value close to R_C (max) should be selected (the operating life of the device may be defined as the period during which there is certainty of the ON and OFF conditions being properly set.). In this case, since D_t is assumed to be 0.5 with a relatively high margin the switching speed should be considered to be more important. So, R_C is set at 4.7 kΩ.

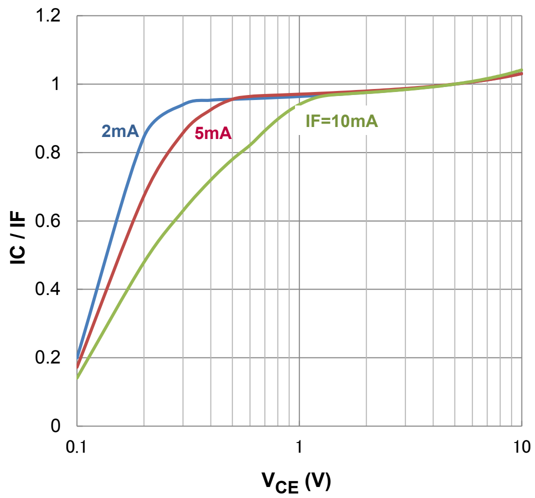


Figure 2.21 I_C/I_F vs. V_{CE}

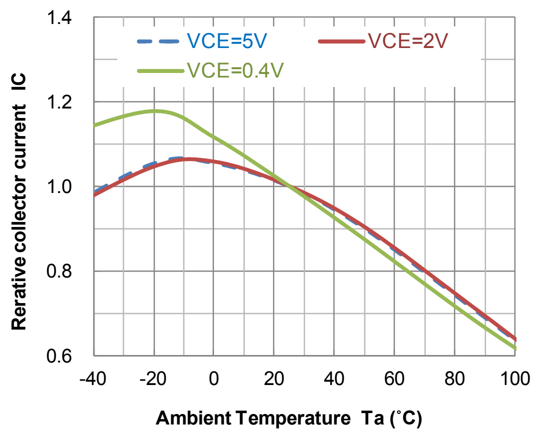


Figure 2.22 Collector Current vs. Ta

R_D = 330 Ω and R_C = 4.7 kΩ are calculated values determined by the procedures above. Please perform a thorough check of the waveform and the operation with your system and redesign a R_D and R_C as necessary. When faster data speed is required for a system, you can also select an IC coupler with guarantee of the maximum switching time. When using a transistor coupler as an interface between CMOS, circuit design can also be conducted in the same way as the above TTLs. Please note that in the case of CMOS, I_{IL} and I_{IH} are smaller than TTLs. Also, the input voltage level of CMOS is different from that of TTLs. As such, please pay careful attention to the characteristics of CMOS during circuit design.

*All of the electrical data on this document is a reference of a representative sample.

3.Terms

(General terms)

Term	Symbol	Description
Absolute Maximum Rating		Maximum value that must not be exceeded even for an instant during operation
Isolation Voltage	BV_S	Isolating voltage between input and output under the specified conditions
Capacitance (Input to Output), Total Capacitance (Input to Output)	C_S	Electrostatic capacitance between the input and output pins
Capacitance (Input), Input Capacitance	C_T C_t	Electrostatic capacitance between the anode and cathode pins of the LED
Forward Current, Input Forward Current	I_F	Rated current that can flow continuously in the forward direction of the LED
Pulse Forward Current, Input Forward Current (Pulsed)	I_{FP}	Rated current that can flow momentarily in the forward direction of the LED
Peak Transient Forward Current	I_{FPT}	Rated current that can flow momentarily in the forward direction of the LED
Reverse Voltage, Input Reverse Voltage	V_R	Rated reverse voltage that can be applied across the LED's cathode and anode
Reverse Current, Input Reverse Current	I_R	Leakage current flowing in the reverse direction of the LED (from cathode to anode)
Forward Voltage, Input Forward Voltage	V_F	Voltage drop across the anode and cathode pins of the LED under the specified forward-current condition
LED Power Dissipaiton, Input Power Dissipaiton	P_D	Rated power that can be dissipated in the LED
Total Power Dissipaiton	P_T	Total rated power that can be dissipated in both the input and output devices
Isolation Resistance	R_S	Resistance between the input and output pins at the specified voltage
Junction Temperature	T_j	Permissible temperature of the junction of the photodetector or LED
Operating Temperature	T_{opr}	Ambient temperature range in which the device can operate without loss of functionality
Lead Soldering Temperature	T_{sol}	Rated temperature at which the device pins can be soldered without loss of functionality
Storage Temperature	T_{stg}	Ambient temperature range in which the device can be stored without operation
Creepage Distance		Shortest distance along the surface of insulation between the path of two conductive parts (input and output)
Clearance(Clearance Distance)		Shortest distance through air between the path of two conductive parts (input and output)
Internal Isolation Thickness, Insulation Thickness		Distance through insulation. Shortest thickness through internal insulation between the path of two conductive parts (input and output)

(Transistor output)

Term	Symbol	Description
Collector Current	I_C	Rated current allowed to flow to collector
Current Transfer Ratio	I_C/I_F (CTR)	Ratio of output current, I_C, to input current, I_F: $I_C/I_F \times 100$ (unit: %)
Collector Dark Current, Dark Current	I_{CEO} I_{DARK}	Leakage current flowing between collector and emitter
OFF-state Collector Curreent	$I_{C(off)}$	Leakage current flowing between collector and emitter when Low voltage is applied to input
Current Gain Factor	h_{FE}	h_{FE} for phototransistor
Base Photo-Current	I_{PB}	Photo-current generated by the specified input current, I_F, in the phototransistor base block
Collector Power Dissipation	P_C	Rated power that can be dissipated in collector
Turn-On Time	t_{ON} t_{on}	Time required for the output waveform to change from 100% (0%) to 10% (90%) when the input is turned off and back on under the specified conditions
Turn-Off Time	t_{OFF} t_{off}	Time required for the output waveform to change from 0% (100%) to 90% (10%) when the input is turned on and back off under the specified conditions
Storage Time	t_S	Time required for the output waveform to change from 0% (100%) to 10% (90%) when input is turned on and back off under the specified conditions
Fall Time	t_f	Time required for the output waveform to change from 90% to 10%
Rise Time	t_r	Time required for the output waveform to change from 10% to 90%
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	Voltage between collector and emitter under the specified saturation conditions
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	Breakdown voltage between collector and base when emitter is open
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	Breakdown voltage between collector and emitter (when base is open)
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	Breakdown voltage between emitter and base when collector is open
Emitter-Collector Breakdown Voltage	$V_{(BR)ECO}$	Breakdown voltage between emitter and collector (when base is open)
Collector-Base Voltage	V_{CBO}	Rated voltage that can be applied across collector and base
Collector-Emitter Voltage	V_{CEO}	Rated voltage that can be applied across collector and emitter
Emitter-Base Voltage	V_{EBO}	Rated voltage that can be applied across emitter and base
Emitter-Collector Voltage	V_{ECO}	Rated voltage which can be applied across emitter and collector
Capacitance (Collector to Emitter), Collector-Emitter Capacitance	C_{CE}	Electrostatic capacitance between the collector and emitter pins

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