CMOS Digital Integrated Circuits Silicon Monolithic

T3GF3WBG

1. Functional Description

- Dual-Supply Bus Transceiver for SD Memory Card

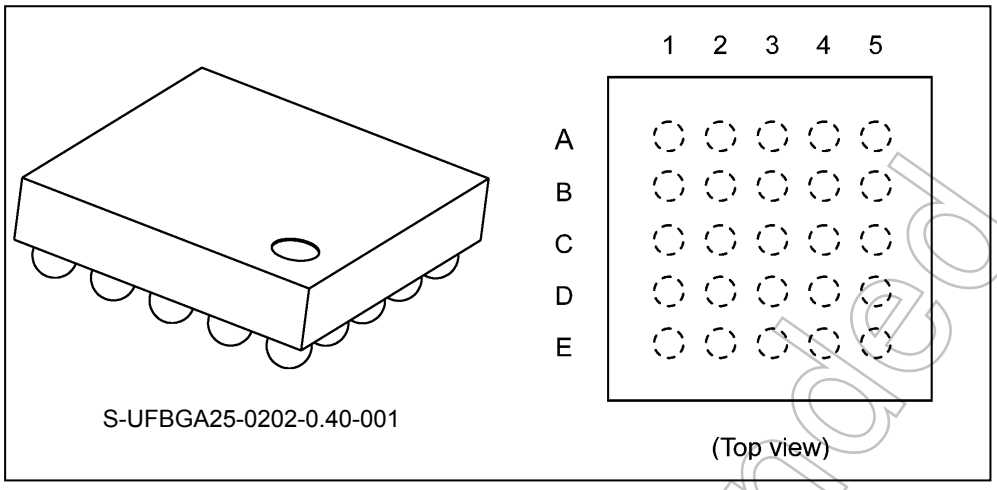
2. General

This device is an advanced high-speed dual-supply bus transceiver fabricated with silicon-gate CMOS technology.
Designed for use as an interface between a 1.8-V bus and a 1.8-V/2.9-V bus in mixed 1.8-V/2.9-V supply systems.
The A-port interfaces with the 1.8-V bus, the B-port with the 1.8-V/2.9-V bus.
The direction of data transmission is determined by the level of the DIR input.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

(1) Compliant with SD specification Part 1 Physical Layer Specification 3.0 (SDR12/SDR25/DDR50)
(2) Bidirectional interface between 1.8-V and 2.9-V buses
(3) High-speed operation: t_{pd} (A to B) = 5.0 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.9 ± 0.1 V)
t_{pd} (B to A) = 5.0 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.9 ± 0.1 V)
t_{pd} (A to B) = 7.0 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 1.8 ± 0.1 V)
t_{pd} (B to A) = 7.0 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 1.8 ± 0.1 V)
(4) Output current: I_{OHB}/I_{OLB} = ±6 mA (min) (V_{CCB} = 2.8 V)
I_{OHA}/I_{OLA} = ±6 mA (min) (V_{CCA} = 1.65 V)
(5) Integrated EMI filter on B-port
(6) Integrated pull-up and pull-down resistors on B-port
(7) Latch-up performance: ±200 mA
(8) ESD performance: Human body model > ±2000 V
IEC61000-4-2 Level 4 (Contact) > ±8 kV (SD card side)
IEC61000-4-2 Level 4 (Air) > ±15 kV (SD card side)
CDM > 500 V
(9) Ultra-small package: WCSP25

4. Packaging and Pin Assignment (Top View)



4.1. Pin Assignment

	1	2	3	4	5
A	Dat2.h	CMD-dir	Dat0-dir	V_{Batt}	Dat2-B
B	Dat3.h	SEL	V_{CCA}	V_{CCB}	Dat3-B
C	Clk.h	Enable	GND	GND	CLK-B
D	Dat0.h	CMD.h	CD	CMD-B	Dat0-B
E	Dat1.h	Clk-f	Dat123-dir	WP	Dat1-B

5. Marking

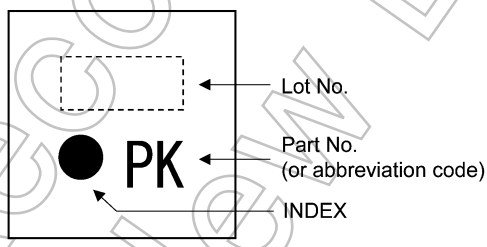


Fig. 5.1 Marking

6. Principle of Operation

6.1. Truth Table

Input Clk.h	Output Clk-f	Output CLK-B
L	L	L
H	H	H

Input CMD-dir	Function CMD.h	Function CMD-B	Outputs
L	Output	Input	CMD.h = CMD-B
H	Input	Output	CMD-B = CMD.h

Input Dat0-dir	Function Dat0.h	Function Dat0-B	Outputs
L	Output	Input	Dat0.h = Dat0-B
H	Input	Output	Dat0-B = Dat0.h

Input Dat123-dir	Function Dat1.h - Dat3.h	Function Dat1-B - Dat3-B	Outputs
L	Output	Input	Datn.h = Datn-B
H	Input	Output	Datn-B = Datn.h

Input Enable	Input SEL	UVLO	Regulator Function
L	X	X	OFF
H	X	Detect	OFF
H	L	Release	2.9 V
H	H	Release	1.8 V

7. Block Diagram

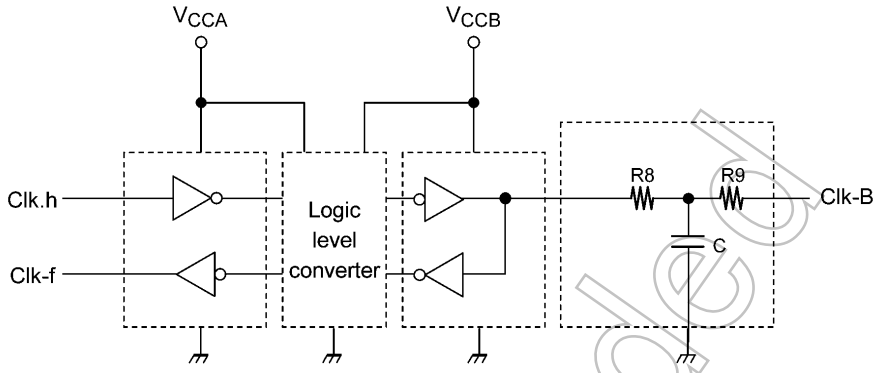


Fig. 7.1 Block Diagram 1

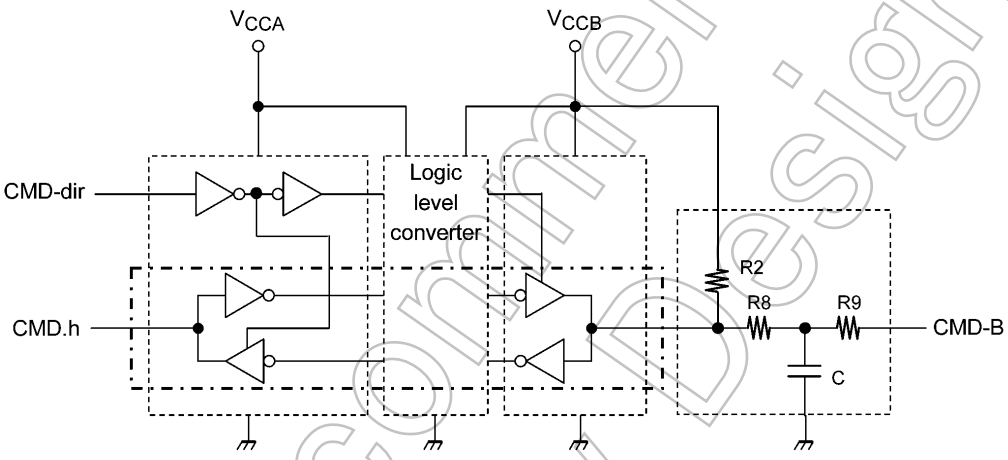


Fig. 7.2 Block Diagram 2

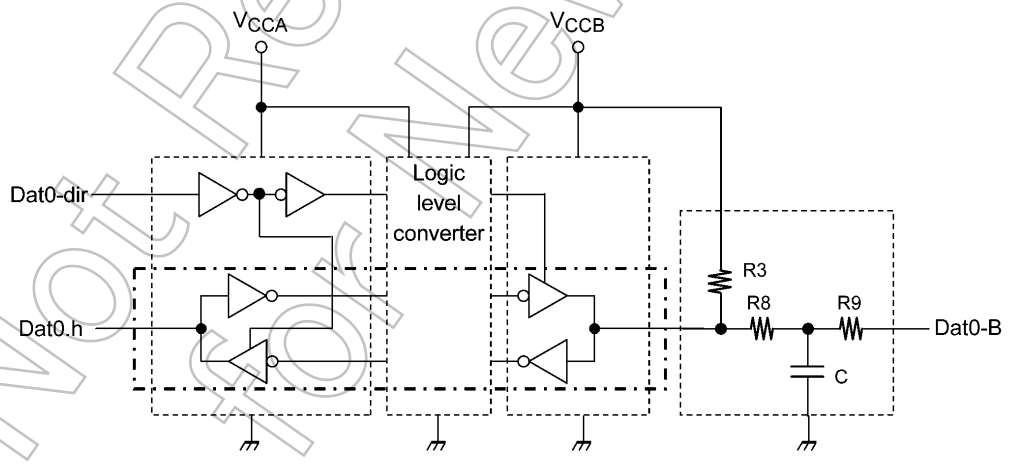


Fig. 7.3 Block Diagram 3

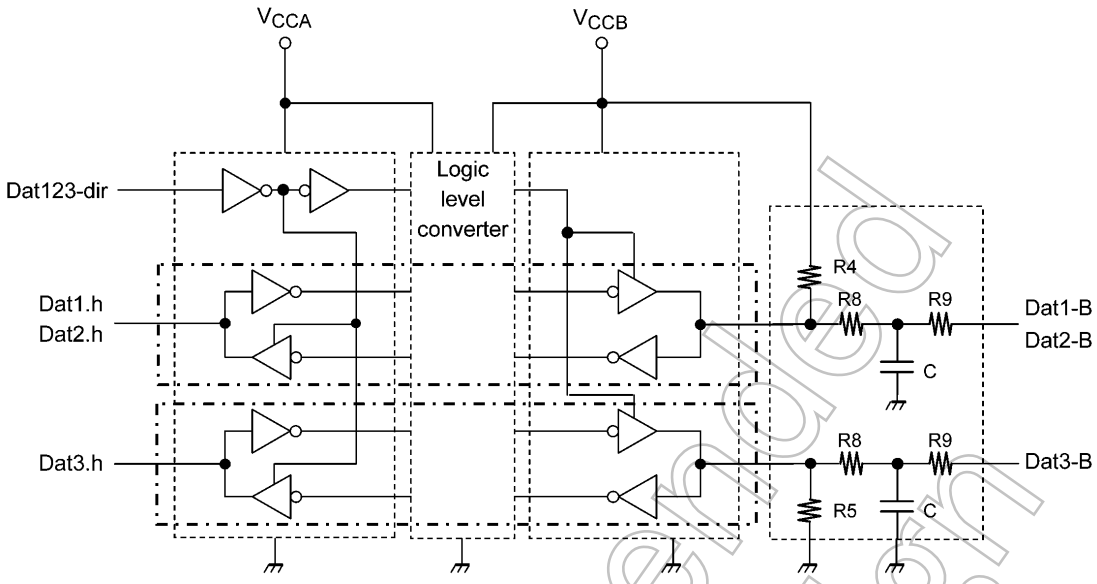
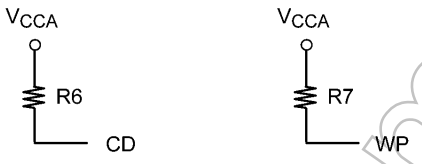
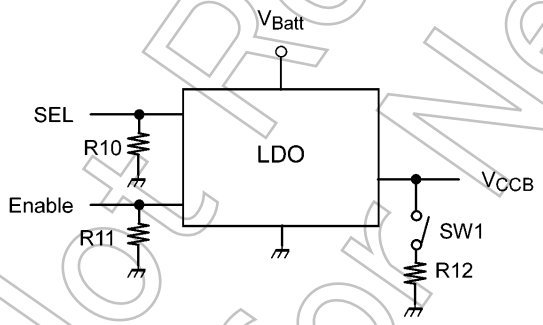


Fig. 7.4 Block Diagram 4



Symbol	Value (typ.)
R3, R4	70 kΩ
R2	15 kΩ
R5	470 kΩ
R6, R7	100 kΩ
R8	5 Ω
R9	35 Ω
R10, R11	200 k to 500 kΩ
R12	80 to 400 Ω
C	35 pF

Fig. 7.5 Block Diagram 5



Enable	UVLO	SW1
H	Release	OFF
H	Detect	ON
L	X	ON

Fig. 7.6 Block Diagram 6

8. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCA}		-0.5 to 3.0	V
	V_{Batt}		5.5	
Input voltage (DIR, Clk.h)	V_{IN}		-0.5 to V_{CCA} +0.5	
Input voltage (Enable, SEL)			-0.5 to 5.5	
Bus I/O voltage	$V_{I/OA}$	(Note 1)	-0.5 to V_{CCA} +0.5	
	$V_{I/OB}$		-0.5 to V_{CCB} +0.5	
Clamp diode current (DIR, Clk.h)	I_{IK}		±25	mA
Clamp diode current (Enable, SEL)			-25	
I/O diode current	$I_{I/OK}$	(Note 2)	±25	
Output current	I_{OUTA}		±25	
	I_{OUTB}		±25	
V_{CC}/ground current per supply pin	I_{CCA}		±50	
Power dissipation	P_D		400	mW
Storage temperature	T_{stg}		-55 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.

Note 2: V_{OUT} < GND, V_{OUT} > V_{CC}

9. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CCA}		—	1.65 to 1.95	V
	V_{Batt}			3.1 to 5.0	
Input voltage (DIR, Clk.h)	V_{IN}			0 to V_{CCA}	
Input voltage (Enable, SEL)				0 to 5.0	
Bus I/O voltage	$V_{I/OA}$	(Note 1)		0 to V_{CCA}	
	$V_{I/OB}$			0 to V_{CCB}	
Output current	I_{OUTA}		V_{CCA} = 1.65 to 1.95 V	±6	mA
	I_{OUTB}		V_{CCB} = 2.8 to 3.0 V, V_{CCB} is supplied from the built-in LDO.	±6	
Operating temperature	T_{opr}		—	85	°C
Input rise time	dt/dv		V_{CCA} = 1.65 V, V_{CCB} = 2.8 V	0 to 10	ns/V
Input fall time				0 to 10	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note: Don't input the signal during the period of changing the output voltage of the LDO.

Note 1: High (H) or Low (L) state.

10. Electrical Characteristics

10.1. DC Characteristics (Note)

(Unless otherwise specified, T_a = -30 to 85°C, 1.65 V ≤ V_{CCA} ≤ 1.95 V)

Characteristics	Symbol	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage (DIR, An)	V_{IHA}	(Note 1)	1.65 to 1.95	1.7 to 3.0	V_{CCA} × 0.65	—	V
High-level input voltage (Bn)	V_{IHB}			2.8 to 3.0	2.0	—	
				1.7 to 1.9	V_{CCB} × 0.65	—	
Low-level input voltage (DIR, An)	V_{ILA}			1.7 to 3.0	—	V_{CCA} × 0.35	
Low-level input voltage (Bn)	V_{ILB}			2.8 to 3.0	—	0.8	
				1.7 to 1.9	—	V_{CCB} × 0.35	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}, I_{OHA} = -100 μA		1.7 to 3.0	V_{CCA} - 0.2	—	
		V_{IN} = V_{IH} or V_{IL}, I_{OHA} = -6 mA	1.65		1.15	—	
	V_{OHB}	V_{IN} = V_{IH} or V_{IL}, I_{OHB} = -100 μA	1.65 to 1.95	2.8 to 3.0	V_{CCB} - 0.2	—	
				1.7 to 1.9	V_{CCB} - 0.2	—	
		V_{IN} = V_{IH} or V_{IL}, I_{OHB} = -6 mA		2.8	2.2	—	
		V_{IN} = V_{IH} or V_{IL}, I_{OHB} = -4 mA		1.7	1.2	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}, I_{OLA} = 100 μA		1.7 to 3.0	—	0.2	
		V_{IN} = V_{IH} or V_{IL}, I_{OLA} = 6 mA	1.65		—	0.3	
	V_{OLB}	V_{IN} = V_{IH} or V_{IL}, I_{OLB} = 100 μA	1.65 to 1.95	2.8 to 3.0	—	0.2	
				1.7 to 1.9	—	0.2	
		V_{IN} = V_{IH} or V_{IL}, I_{OLB} = 6 mA		2.8	—	0.4	
		V_{IN} = V_{IH} or V_{IL}, I_{OLB} = 4 mA		1.7	—	0.3	
Input leakage current	I_{INA}	V_{INA} = V_{CCA} or GND DIR = High V_{CD} = V_{WP} = V_{CCA}		1.7 to 3.0	—	±5.0	μA
	I_{INB}	V_{CMD-B}, V_{DAT0-B}, V_{DAT1-B}, V_{DAT2-B} = V_{CCB} V_{DAT3-B} = GND, DIR = Low V_{CD} = V_{WP} = V_{CCA}			—	±5.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND DIR = High V_{CD} = V_{WP} = V_{CCA}			—	20	

Note: V_{CCB} is supplied from the built-in LDO.

Note 1: An is a host side signal. Bn is a card side signal.

10.2. AC Characteristics (Note)
(Unless otherwise specified, T_a = -30 to 85°C, Input: $t_r = t_f$ = 2.0 ns)

10.2.1. V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.9 ± 0.1 V

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 10.2.1, 10.2.2	—	3.5	5.0	ns
Propagation delay time (An → Bn)				—	3.5	5.0	
Propagation delay time (Clk.h → Clk-f)				1.0	5.7	9.5	
Skew (CLK-f to CMD/DAT)	$t_{skew.f}$		—	-1.8	0.0	3.0	
Output rise/fall time (An)	t_{TLH}/t_{THL}		See Fig. 10.2.1, 10.2.2	—	1.5	—	
Output rise/fall time (Bn)				—	1.5	—	
Output skew	t_{osLH}/t_{osHL}	(Note 1)	See Fig. 10.2.3	—	—	0.5	

Note: An is a host side signal. Bn is a card side signal. V_{CCB} is supplied from the built-in LDO.
Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.2.2. V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 1.8 ± 0.1 V

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}		See Fig. 10.2.1, 10.2.2	—	4.5	7.0	ns
Propagation delay time (An → Bn)				—	5.0	7.0	
Propagation delay time (Clk.h → Clk-f)				1.0	8.0	13.5	
Skew (CLK-f to CMD/DAT)	$t_{skew.f}$		—	-0.8	0.4	1.6	
Output rise/fall time (An)	t_{TLH}/t_{THL}		See Fig. 10.2.1, 10.2.2	—	1.5	—	
Output rise/fall time (Bn)				—	1.5	—	
Output skew	t_{osLH}/t_{osHL}	(Note 1)	See Fig. 10.2.3	—	—	0.5	

Note: An is a host side signal. Bn is a card side signal. V_{CCB} is supplied from the built-in LDO.
Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

10.3. Dynamic Switching Characteristics (Note)
(Unless otherwise specified, T_a = 25°C, Input: $t_r = t_f$ = 2.0 ns, C_L = 15 pF)

Characteristics		Symbol	Note	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	(A → B)	V_{OLP}	(Note 1)	See Fig. 10.3.1 $V_{IH} = V_{CC}$, V_{IL} = 0 V	1.8	2.9	0.35	V
	(B → A)						0.25	
Quiet output minimum dynamic V_{OL}	(A → B)	V_{OLV}					-0.35	
	(B → A)						-0.25	
Quiet output maximum dynamic V_{OH}	(A → B)	V_{OHP}					3.25	
	(B → A)						2.05	
Quiet output minimum dynamic V_{OH}	(A → B)	V_{OHV}					2.55	
	(B → A)						1.55	

Note: An is a host side signal. Bn is a card side signal.
Note 1: Parameter guaranteed by design.

10.4. Capacitive Characteristics (Unless otherwise specified, T_a = 25°C)

Characteristics	Symbol	Note	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Power dissipation capacitance	C_{PDA}	(Note 1)	A → B (DIR = High)	1.8	2.9	24	pF
			B → A (DIR = Low)			22	
	C_{PDB}		A → B (DIR = High)			76	
			B → A (DIR = Low)			28	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.
$I_{CC}(opr) = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6$ (per bit)

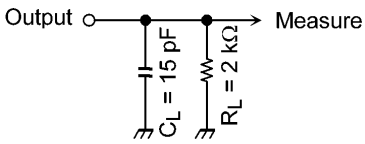


Fig. 10.2.1 Parameter for AC Test Circuit

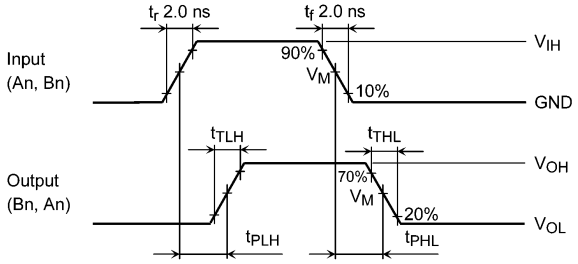
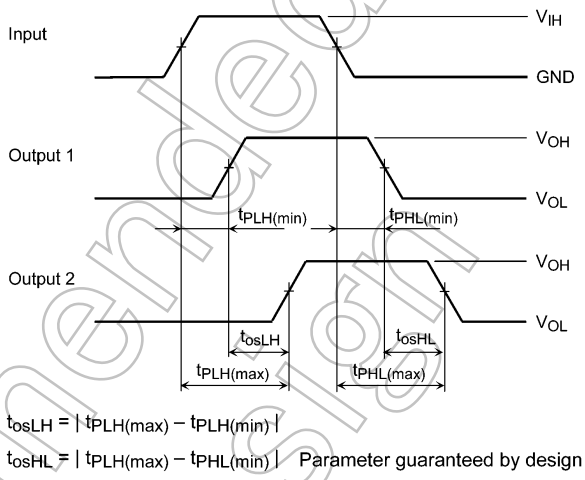


Fig. 10.2.2 AC Waveform t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}



$t_{osLH} = | t_{PLH(max)} - t_{PLH(min)} |$

$t_{osHL} = | t_{PLH(max)} - t_{PHL(min)} |$ Parameter guaranteed by design

Fig. 10.2.3 AC Waveform t_{osLH}, t_{osHL}

Table 10.2.1 AC Waveform Symbols

V_{CC}	Symbol	Value
2.9 ± 0.1 V	V_{IH}	V_{CC}
	V_M	$V_{CC}/2$
1.8 ± 0.15 V	V_{IH}	V_{CC}
	V_M	$V_{CC}/2$

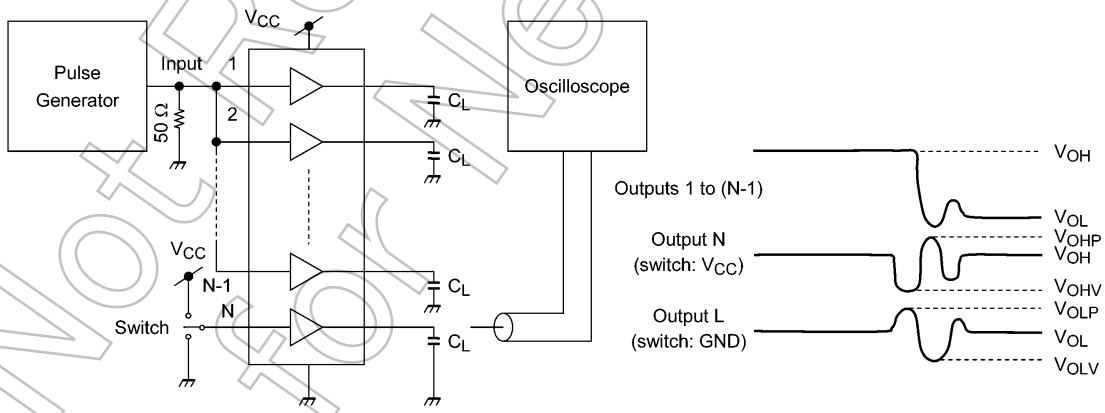


Fig. 10.3.1 Quiet Output Measurement Circuit V_{OHP}, V_{OHV}, V_{OLP}, V_{OLV}

11. Regulator Section

11.1. Electrical Characteristics (Unless otherwise specified, V_{IN} = V_{OUT} + 1 V, I_{OUT} = 1 mA, C_{IN} = 0.1 μF, C_{OUT} = 2.2 μF, T_j = 25°C)

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Supply voltage	V_{Batt}		—	3.1	—	5.0	V
Output voltage	V_{CCB}	(Note 1)	SEL = Low	2.8	2.9	3.0	
			SEL = High	1.7	1.8	1.9	
UVLO detect voltage	V_{UVLO1}		—	—	2.4	2.7	
UVLO release voltage	V_{UVLO2}			—	2.6	2.8	
Line regulation	REG_{Line}		V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.0 V, I_{OUT} = 1 mA	—	3	15	mV
Load regulation	REG_{Load}		1 mA ≤ I_{OUT} ≤ 100 mA	—	—	150	
Quiescent current	$I_{B(ON)}$		I_{OUT} = 0 mA	—	80	160	μA
Standby current	$I_{B(OFF)}$		V_{Enable} = 0 V, V_{SEL} = 0 V	—	0.1	1.0	
Output noise voltage	V_n		V_{IN} = V_{OUT} = + 1 V, I_{OUT} = 10 mA, 10 Hz ≤ f ≤ 100 kHz, T_a = 25°C	—	140	—	μVms
Temperature coefficient of output voltage	T_{CVO}		-30°C ≤ T_{opr} ≤ 85°C	—	100	—	ppm/°C
Ripple rejection	R.R		V_{IN} = V_{OUT} + 1 V, I_{OUT} = 10 mA, f = 1 kHz, V_{Ripple} = 500 mV_{p-p}, T_a = 25°C	—	40	—	dB
High-level input voltage	V_{IH}		Enable, SEL	1.5	—	V_{Batt}	V
Low-level input voltage	V_{IL}			0	—	0.25	
Control current (ON)	$I_{CT(ON)}$		V_{Enable} = 1.5 V	—	—	7.5	μA
Control current (OFF)	$I_{CT(OFF)}$		V_{Enable} = 0 V	—	—	0.1	
Startup time	t_{start}		SEL = Low	—	—	200	μs
Transition time (from 2.9 V to 1.8 V)	t_{trans}		—	—	—	5	ms

Note 1: The relation between the supply voltage and the output voltage is shown in the below figure. This figure shows the representative typical behavior of the LDO.

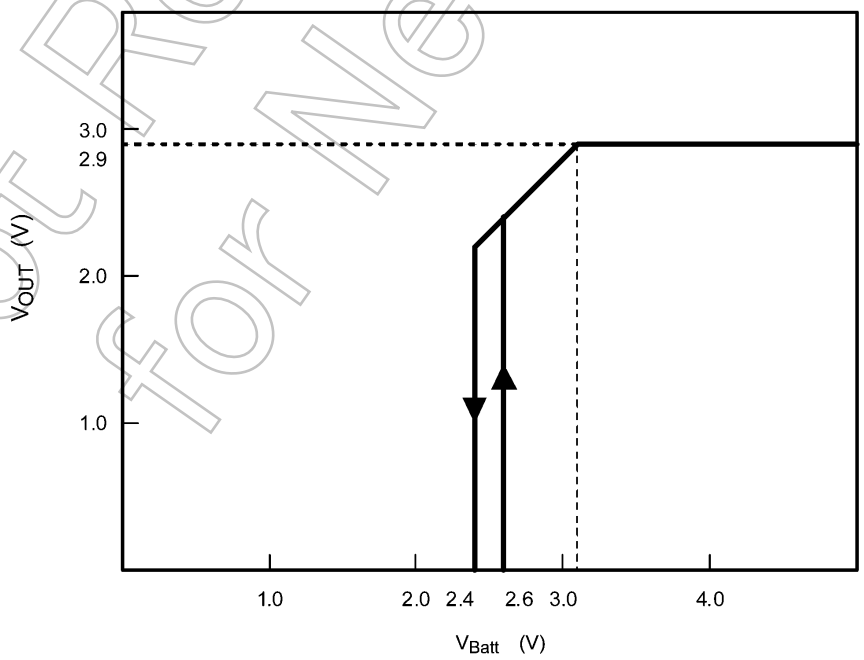


Fig. 11.1.1 UVLO Characteristics

11.2. EMI Filter Response (Typical performance)

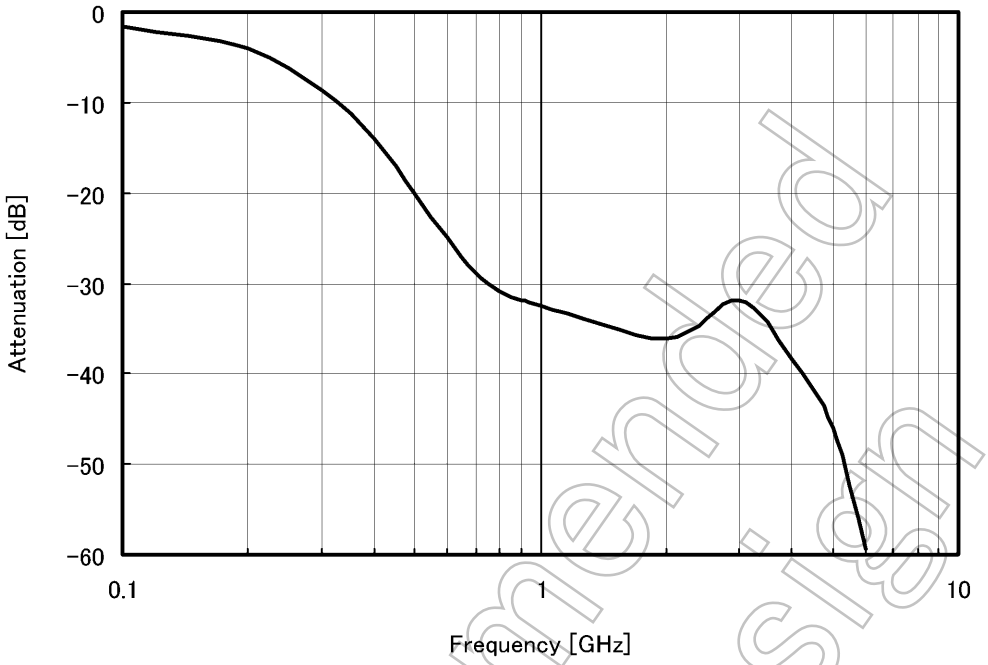
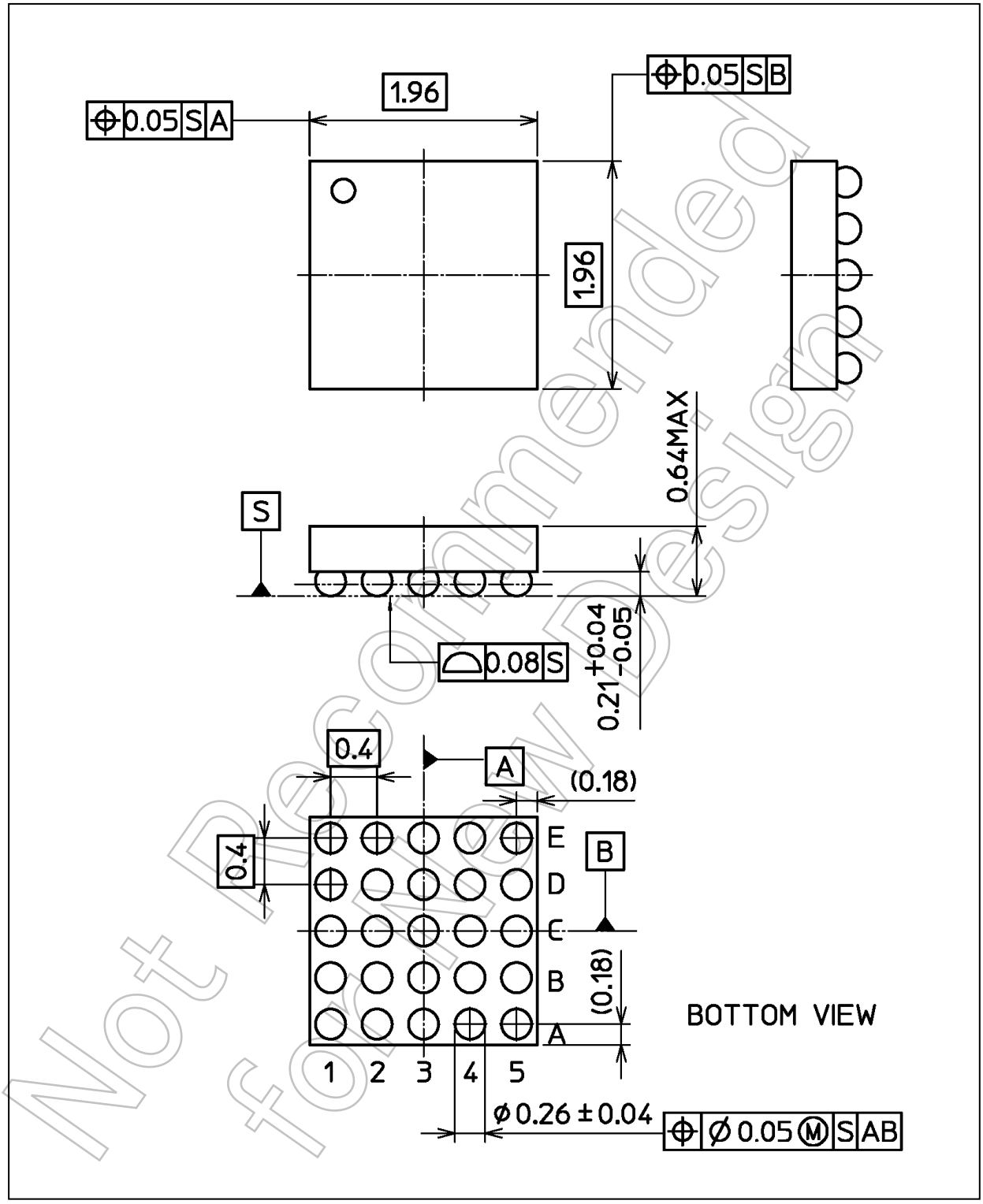


Fig. 11.2.1 EMI Filter Response (Typical performance)

Package Dimensions

Unit: mm



Weight: 0.006 g (typ.)

Package Name(s)
TOSHIBA: S-UFBGA25-0202-0.40-001

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