

# TLP155

## 1. Applications

- Plasma Display Panels (PDPs)
- Transistor Inverters
- MOSFET Gate Drivers
- IGBT Gate Drivers

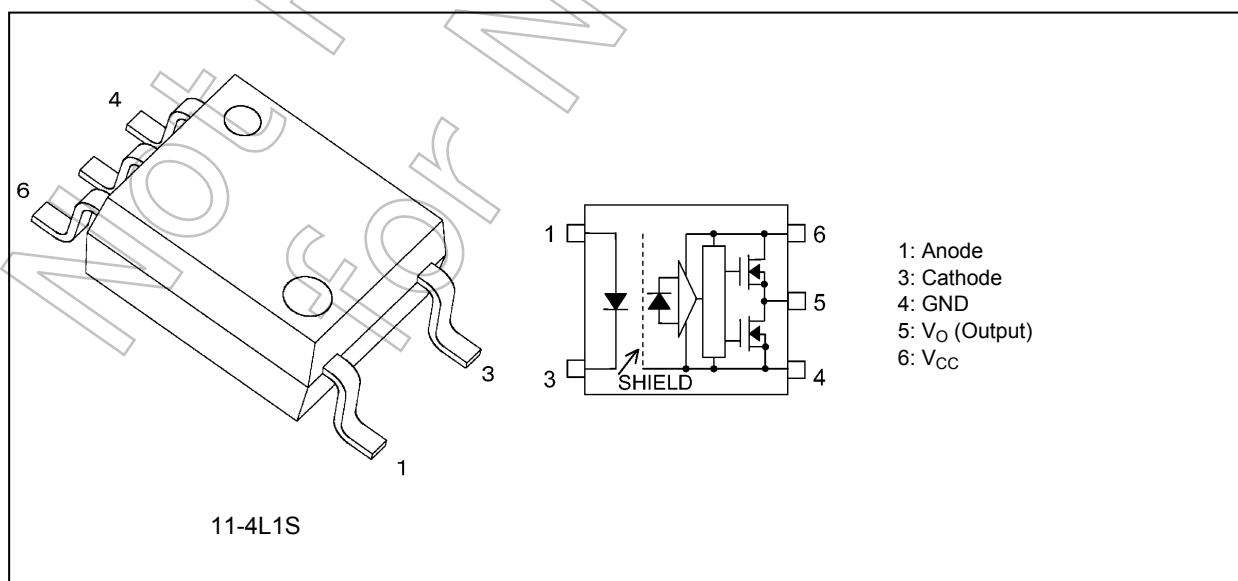
## 2. General

The Toshiba TLP155 consists of a GaAs infrared light-emitting diodes and integrated high gain, high-speed photodetectors. The TLP155 is housed in the SO6 package. The photodetector has an internal Faraday shield that provides a guaranteed Common-mode transient immunity of  $\pm 20$  kV/ $\mu$ s. TLP155 is suitable for direct gate driving circuit for IGBTs or power MOSFETs.

## 3. Features

- (1) Buffer logic type (Totem pole output)
  - (2) Package:SO6
  - (3) Output peak current:  $\pm 0.6$  A (max)
  - (4) Operating temperature:  $-40$  to  $100$  °C
  - (5) Threshold input current:  $7.5$  mA (max)
  - (6) Propagation delay time:  $200$  ns (max)
  - (7) Common-mode transient immunity:  $\pm 20$  kV/ $\mu$ s (min)
  - (8) Propagation delay skew:  $\pm 85$  ns(max)
  - (9) Isolation voltage:  $3750$  Vrms (min)
  - (10) Safety standards
    - UL-approved: UL1577, File No.E67349
    - cUL-approved: CSA Component Acceptance Service No.5A File No.E67349
    - VDE-approved: EN60747-5-5 (**Note 1**)
- Note 1: When an EN60747-5-5 approved type is needed, please designate the **Option (V4)**.

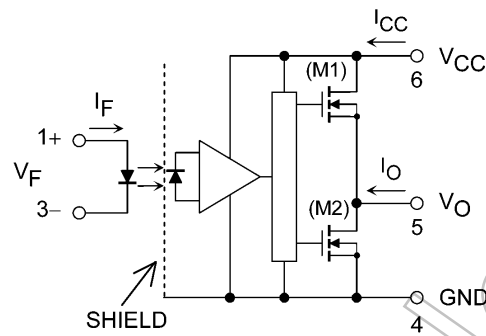
## 4. Packaging and Pin Assignment



Start of commercial production

2011-09

**5. Internal Circuit (Note)**



Note: A 0.1- $\mu$ F bypass capacitor must be connected between pin 6 and pin 4.

**6. Principle of Operation**

**6.1. Truth Table**

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

**6.2. Mechanical Parameters**

Characteristics	Min	Unit
Creepage distances	5.0	mm
Clearance distances	5.0	
Internal isolation thickness	0.4	

**7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T<sub>a</sub> = 25 °C)**

	Characteristics	Symbol	Note	Rating	Unit
LED	Input forward current	I <sub>F</sub>		20	mA
	Input forward current derating (T <sub>a</sub> ≥ 92 °C)	ΔI <sub>F</sub> /ΔT <sub>a</sub>		-0.63	mA/°C
	Peak transient input forward current	I <sub>FPT</sub>	(Note 1)	1	A
	Input reverse voltage	V <sub>R</sub>		5	V
	Input power dissipation	P <sub>D</sub>		40	mW
	Input power dissipation derating (T <sub>a</sub> ≥ 92 °C)	ΔP <sub>D</sub> /ΔT <sub>a</sub>		-1.2	mW/°C
	Junction temperature	T <sub>j</sub>		125	°C
Detector	Peak high-level output current (T <sub>a</sub> = -40 to 100 °C)	I <sub>OPH</sub>	(Note 2)	-0.6	A
	Peak low-level output current (T <sub>a</sub> = -40 to 100 °C)	I <sub>OPL</sub>		+0.6	
	Output voltage	V <sub>O</sub>		35	V
	Supply voltage	V <sub>CC</sub>		35	
	Output power dissipation	P <sub>O</sub>		80	mW
	Output power dissipation derating (T <sub>a</sub> ≥ 85 °C)	ΔP <sub>O</sub> /ΔT <sub>a</sub>		-2.0	mW/°C
	Junction temperature	T <sub>j</sub>		125	°C
Common	Operating temperature	T <sub>opr</sub>		-40 to 100	
	Storage temperature	T <sub>stg</sub>		-55 to 125	
	Lead soldering temperature (10 s)	T <sub>sol</sub>		260	
	Isolation voltage AC, 60 s, R.H. ≤ 60 %	BV <sub>s</sub>	(Note 3)	3750	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) ≤ 1 μs, 300 pps

Note 2: Exponential waveform. Pulse width ≤ 2 μs, f ≤ 10 kHz, V<sub>CC</sub> = 20V, T<sub>a</sub> = -40 to 100 °C

Note 3: This device is considered as a two-terminal device: Pins 1 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

Not for New

**8. Recommended Operating Conditions (Note)**

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Threshold input current (L/H)	$I_{FLH}$	(Note 1)	10	—	15	mA
Threshold input voltage (H/L)	$V_{FHL}$		0	—	0.8	V
Supply voltage	$V_{CC}$	(Note 2)	10	—	30	
Peak high-level output current	$I_{OPH}$		—	—	-0.2	A
Peak low-level output current	$I_{OPL}$		—	—	+0.2	
Operating temperature	$T_{opr}$		-40	—	100	°C
Operating frequency	f	(Note 3)	—	—	250	kHz

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note: A ceramic capacitor (0.1  $\mu$ F) should be connected between pin 6 and pin 4 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: The rise and fall times of the input on-current should be less than 0.5  $\mu$ s.

Note 2: Denotes the operating range, not the recommended operating condition.

Note 3: Exponential waveform.  $I_{OPH} \geq -0.25$  A ( $\leq 80$  ns),  $I_{OPL} \leq 0.25$  A ( $\leq 80$  ns),  $T_a = 100$  °C

**9. Electrical Characteristics (Note)  
(Unless otherwise specified,  $T_a = -40$  to  $100$  °C)**

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	$V_F$		—	$I_F = 10$ mA, $T_a = 25$ °C	1.40	1.57	1.80	V
Input forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$		—	$I_F = 10$ mA	—	-1.8	—	mV/°C
Input reverse current	$I_R$		—	$V_R = 5$ V, $T_a = 25$ °C	—	—	10	$\mu$ A
Input capacitance	$C_t$		—	$V = 0$ V, $f = 1$ MHz, $T_a = 25$ °C	—	60	—	pF
Peak high-level output current	$I_{OPH}$	(Note 1)	Fig. 12.1.1	$I_F = 10$ mA, $V_{CC} = 15$ V, $V_{6-5} = 4$ V	—	-0.5	-0.2	A
				$I_F = 10$ mA, $V_{CC} = 15$ V, $V_{6-5} = 10$ V	—	—	-0.4	
Peak low-level output current	$I_{OPL}$	(Note 1)	Fig. 12.1.2	$I_F = 0$ mA, $V_{CC} = 15$ V, $V_{5-4} = 2$ V	0.2	0.5	—	
				$I_F = 0$ mA, $V_{CC} = 15$ V, $V_{5-4} = 10$ V	0.4	—	—	
High-level output voltage	$V_{OH}$		Fig. 12.1.3	$I_F = 10$ mA, $V_{CC} = 10$ V, $I_O = -100$ mA	6.0	8.4	—	V
Low-level output voltage	$V_{OL}$		Fig. 12.1.4	$V_F = 0.8$ V, $V_{CC} = 10$ V, $I_O = 100$ mA	—	0.3	1.0	
High-level supply current	$I_{CCH}$		Fig. 12.1.5	$I_F = 10$ mA, $V_{CC} = 10$ to $30$ V, $V_O = \text{Open}$	—	1.5	3.0	mA
Low-level supply current	$I_{CCL}$		Fig. 12.1.6	$I_F = 0$ mA, $V_{CC} = 10$ to $30$ V, $V_O = \text{Open}$	—	1.5	3.0	
Threshold input current (L/H)	$I_{FLH}$		—	$V_{CC} = 15$ V, $V_O > 1$ V	—	1.0	7.5	
Threshold input voltage (H/L)	$V_{FHL}$		—	$V_{CC} = 15$ V, $V_O < 1$ V	0.8	—	—	V
Supply voltage	$V_{CC}$		—	—	10	—	30	

Note: All typical values are at  $T_a = 25$  °C.

Note: This device is designed for low power consumption, making it more sensitive to ESD than its predecessors. Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1:  $I_O$  application time  $\leq 50$   $\mu$ s, single pulse.

**10. Isolation Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	$C_S$	(Note 1)	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	—	0.8	—	pF
Isolation resistance	$R_S$	(Note 1)	$V_S = 500\text{ V}$ , R.H. $\leq 60\%$	$1 \times 10^{12}$	$10^{14}$	—	$\Omega$
Isolation voltage	$BV_S$	(Note 1)	AC, 60 s	3750	—	—	Vrms
			AC, 1 s in oil	—	10000	—	
			DC, 60 s in oil	—	10000	—	Vdc

Note 1: This device is considered as a two-terminal device: Pins 1 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

**11. Switching Characteristics (Note)  
(Unless otherwise specified,  $T_a = -40\text{ to }100\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	$t_{pLH}$	(Note 1)	Fig. 12.1.7	$I_F = 0 \rightarrow 10\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $R_g = 30\ \Omega$ , $C_g = 1\text{ nF}$ , $T_a = 25\text{ }^\circ\text{C}$	—	120	170	ns
Propagation delay time (H/L)	$t_{pHL}$	(Note 1)		$I_F = 10 \rightarrow 0\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $R_g = 30\ \Omega$ , $C_g = 1\text{ nF}$ , $T_a = 25\text{ }^\circ\text{C}$	—	120	170	
Propagation delay time (L/H)	$t_{pLH}$	(Note 1)		$I_F = 0 \rightarrow 10\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $R_g = 30\ \Omega$ , $C_g = 1\text{ nF}$	50	120	200	
Propagation delay time (H/L)	$t_{pHL}$	(Note 1)		$I_F = 10 \rightarrow 0\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $R_g = 30\ \Omega$ , $C_g = 1\text{ nF}$	50	120	200	
Propagation delay skew (device to device)	$t_{psk}$	(Note 1) (Note 4)		$I_F = 0 \leftrightarrow 10\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $R_g = 30\ \Omega$ , $C_g = 1\text{ nF}$	-85	—	85	
Pulse width distortion	$ t_{pHL} - t_{pLH} $	(Note 1)		$I_F = 0 \leftrightarrow 10\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $R_g = 30\ \Omega$ , $C_g = 1\text{ nF}$	—	5	50	
Rise time	$t_r$	(Note 1)		$I_F = 0 \rightarrow 10\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $R_g = 30\ \Omega$ , $C_g = 1\text{ nF}$	—	35	—	
Fall time	$t_f$	(Note 1)		$I_F = 10 \rightarrow 0\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $R_g = 30\ \Omega$ , $C_g = 1\text{ nF}$	—	15	—	
Common-mode transient immunity at output high	$CM_H$	(Note 2)	Fig. 12.1.8	$V_{CM} = 1000\text{ V}_{p-p}$ , $I_F = 10\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $T_a = 25\text{ }^\circ\text{C}$ , $V_{O(min)} = 16\text{ V}$	$\pm 20$	—	—	kV/ $\mu\text{s}$
Common-mode transient immunity at output low	$CM_L$	(Note 3)		$V_{CM} = 1000\text{ V}_{p-p}$ , $I_F = 0\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $T_a = 25\text{ }^\circ\text{C}$ , $V_{O(max)} = 1\text{ V}$	$\pm 20$	—	—	

Note: All typical values are at  $T_a = 25\text{ }^\circ\text{C}$ .

Note 1: Input signal ( $f = 250\text{ kHz}$ , duty = 50%,  $t_r = t_f = 5\text{ ns}$  or less).

CL is approximately 15 pF which includes probe and stray wiring capacitance.

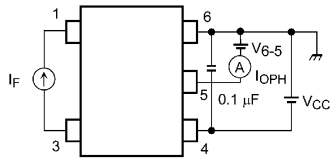
Note 2:  $CM_H$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ( $V_O > 16\text{ V}$ ).

Note 3:  $CM_L$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O < 1\text{ V}$ ).

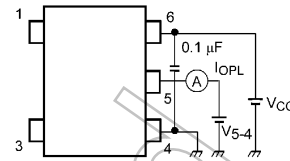
Note 4: The propagation delay skew,  $t_{psk}$ , is equal to the magnitude of the worst-case difference in  $t_{pHL}$  and/or  $t_{pLH}$  that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

**12. Test Circuits and Characteristics Curves**

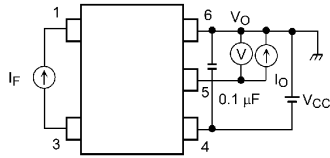
**12.1. Test Circuits**



**Fig. 12.1.1 IO<sub>PH</sub> Test Circuit**

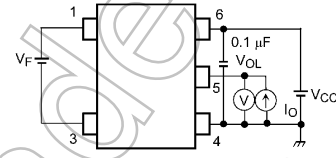


**Fig. 12.1.2 IO<sub>PL</sub> Test Circuit**

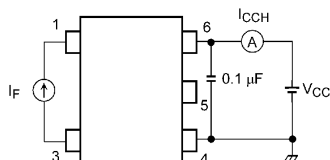


$V_{OH} = V_{CC} - V_O$

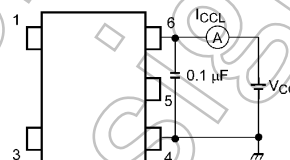
**Fig. 12.1.3 V<sub>OH</sub> Test Circuit**



**Fig. 12.1.4 V<sub>OL</sub> Test Circuit**

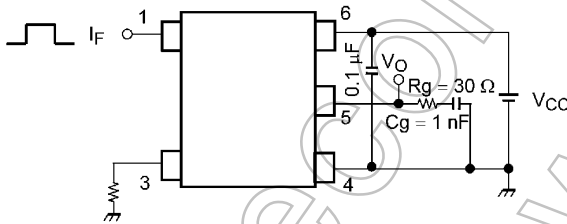


**Fig. 12.1.5 I<sub>CCH</sub> Test Circuit**



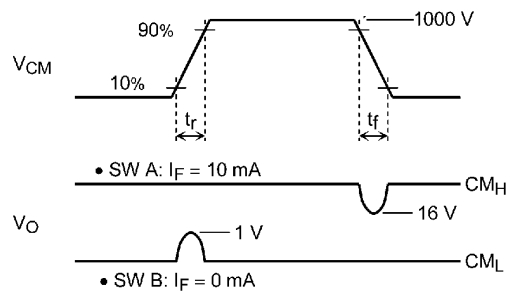
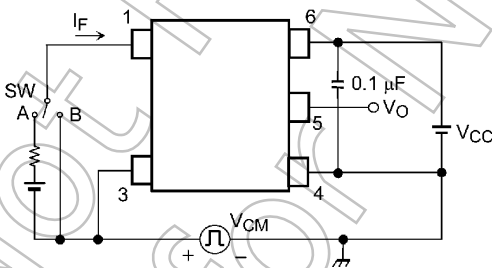
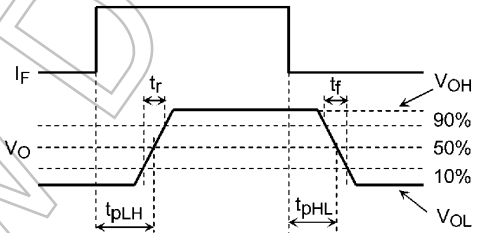
**Fig. 12.1.6 I<sub>CCL</sub> Test Circuit**

$I_F = 10 \text{ mA (P.G.)}$   
 $(f = 250 \text{ kHz, duty} = 50\%, t_r = t_f = 5 \text{ ns})$



P.G. : Pulse generator

**Fig. 12.1.7 Switching Time Test Circuit and Waveform**



$CM_L = \frac{800 \text{ V}}{t_r (\mu\text{s})}$

$CM_H = -\frac{800 \text{ V}}{t_f (\mu\text{s})}$

**Fig. 12.1.8 Common-Mode Transient Immunity Test Circuit and Waveform**

**13. Soldering and Storage**

**13.1. Precautions for Soldering**

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

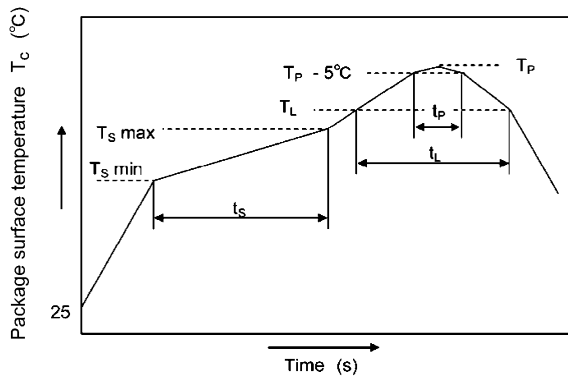
- When using soldering reflow.

The soldering temperature profile is based on the package surface temperature.

(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



	Symbol	Min	Max	Unit
Preheat temperature	$T_s$	150	200	°C
Preheat time	$t_s$	60	120	s
Ramp-up rate ( $T_L$ to $T_P$ )			3	°C/s
Liquidus temperature	$T_L$	217		°C
Time above $T_L$	$t_L$	60	150	s
Peak temperature	$T_P$	260		°C
Time during which $T_c$ is between ( $T_P - 5$ ) and $T_P$	$t_p$	30		s
Ramp-down rate ( $T_P$ to $T_L$ )			6	°C/s

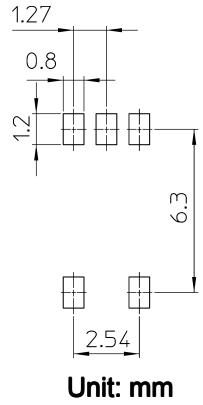
**An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used**

- When using soldering flow  
Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.  
Mounting condition of 260 °C within 10 seconds is recommended.  
Flow soldering must be performed once.
- When using soldering Iron  
Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C  
Heating by soldering iron must be done only once per lead.

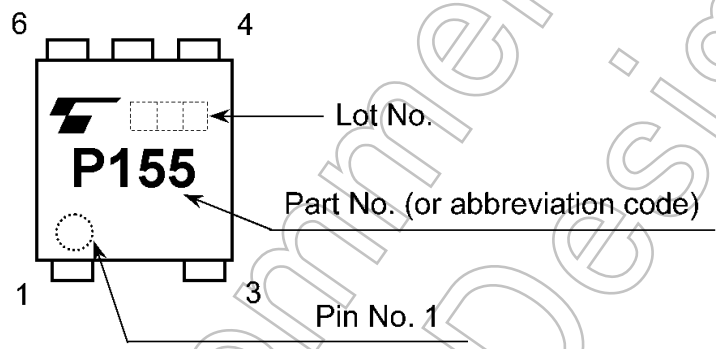
**13.2. Precautions for General Storage**

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

**14. Land Pattern Dimensions for Reference Only**



**15. Marking**

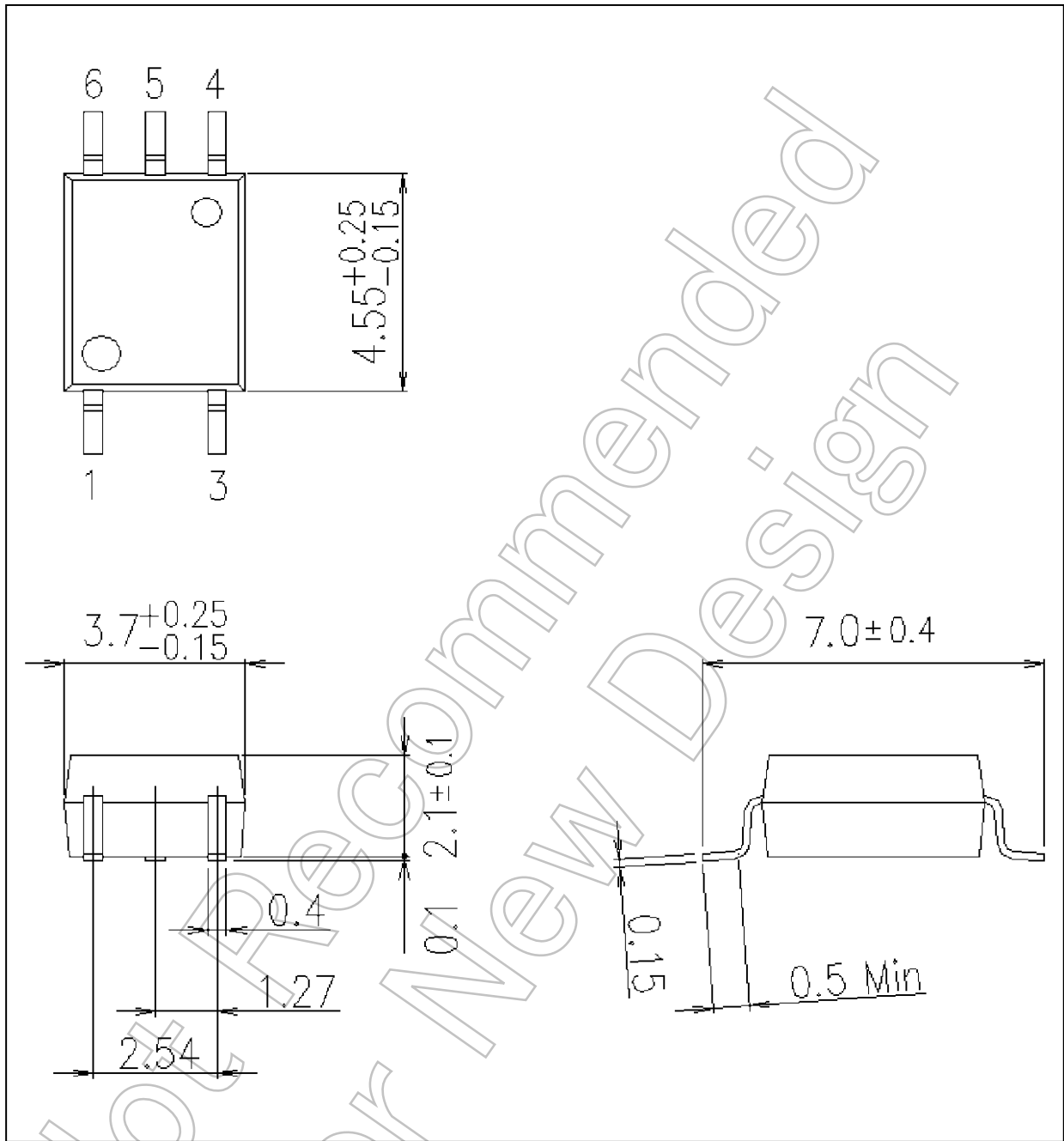


Not Recommended for New Design



**Package Dimensions**

Unit: mm



Weight: 0.08 g (typ.)

Package Name(s)
TOSHIBA: 11-4L1S

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