Basics of Low-Dropout (LDO) Regulator ICs

Outline:

LDO (low-drop-out) regulators, which are used as PoLs for mobile and IoT devices, are optimal power supply ICs for analog circuits that require high voltage accuracy and low noise.

This document describes key features, the operation of the built-in protective function, and the efficiency.

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1. Introduction

Various semiconductor components are used to reduce the size and enhance the performance of increasingly sophisticated mobile and other electronic devices. To accommodate the need for these electronic devices, demand is growing for highly regulated low-noise and high-quality power supplies for semiconductor components.

Low-dropout regulator ICs (hereinafter “LDOs”) are physically smaller, generate less noise, and are easier to design with than switched-mode DC-DC converters, making them ideal for use as point-of-load (POL) regulators that are placed in the vicinity of the target semiconductor components.

This application note describes the basics of LDOs, including their overview, electrical characteristics, and usage considerations.

Application notes that provide more details on the characteristics and applications of LDOs are also available to help you select and use LDOs properly.

2. Electrical characteristics to be noted when selecting LDOs

There are various guidelines for selecting LDOs that satisfy system requirements. The following describes major electrical characteristics to be noted when selecting LDOs.

(1) Input voltage

In the case of battery-operated devices, the battery voltage decreases as the battery supplies electricity to a load. It is necessary to select an LDO, taking the minimum battery voltage and dropout voltage into consideration, in order to ensure that the input voltage of the LDO remains higher than the sum of its output and dropout voltages even at the minimum battery voltage so that the following IC or circuitry is supplied with a regulated voltage.

(References: Input voltage range, dropout voltage)

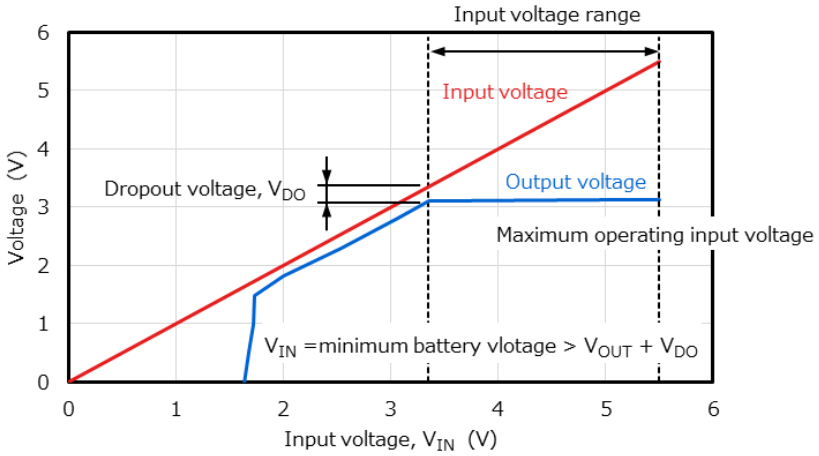


Figure 2.1 Input voltage range and dropout voltage of linear regulators

To perform a parametric search of low dropout voltage type LDOs → Click Here

To perform a parametric search of low input voltage type (up to 5.5V) LDOs → Click Here

To perform a parametric search of high input voltage type (up to 36V) LDOs → Click Here

(2) Output voltage

Select LDOs that provide sufficient output voltage accuracy as well as an output voltage that falls within the operating voltage range of the IC or circuitry connected as a load even when the input voltage or output current varies.

(References: Output voltage, output voltage accuracy, line regulation, load regulation, load transient response)

(3) Output current (load current)

It is necessary to select LDOs whose output current does not exceed the specified operating range even in the event of output current transients.

To perform a parametric search of LDOs with an output current of 150 mA → Click Here

To perform a parametric search of LDOs with an output current of 200 mA → Click Here

To perform a parametric search of LDOs with an output current of 300 mA → Click Here

To perform a parametric search of LDOs with an output current of 420 mA → Click Here

To perform a parametric search of LDOs with an output current of 500 mA → Click Here

To perform a parametric search of LDOs with an output current of 800 mA → Click Here

To perform a parametric search of LDOs with an output current of 1300 mA → Click Here

To perform a parametric search of LDOs with an output current of 1500 mA → Click Here

(4) Power dissipation and maximum junction temperature of LDOs

The power dissipation of an LDO is calculated as $P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_B$. Its maximum junction temperature is calculated as $T_{j(max)} = P_D \times R_{th(j-a)} + Ta$. It is necessary to ensure that both power dissipation and junction temperature do not exceed the absolute maximum rated values under actual usage conditions. Special care should be exercised as to junction temperature because thermal resistance depends on the mounting area and metal thickness of a printed circuit board. If the junction temperature exceeds the absolute maximum rated temperature, an LDO trips thermal shutdown (TSD), possibly becoming unable to provide a normal output level.

(References: Power dissipation and maximum junction temperature)

(5) Quiescent current and standby current

In battery-operated devices, the LDO consumes a small amount of standby current during standby mode, in addition to the bias current during operation mode. It is necessary to select LDOs with low quiescent and standby current in order to conserve battery life.

(References: Quiescent current, standby current)

To perform a parametric search of LDOs with low quiescent current → Click Here

(6) Ripple rejection ratio, output noise voltage

If a system incorporates CMOS sensors and/or high-precision analog circuits, its performance is greatly affected by the quality of power supplies such as the amount of noise on the power supplies. For systems requiring low-noise power supplies, it is necessary to select LDOs with a high ripple rejection ratio and low output noise voltage.

(References: Ripple rejection ratio, output noise voltage)

To perform a parametric search of low-noise LDOs → Click Here

To perform a parametric search of LDOs with a high ripple rejection ratio → Click Here

(7) Control voltage

The control voltage is the voltage required to turn on the LDO. In recent years, low-voltage interface signals and control signals have been increasingly used to reduce the power consumption of devices. Our company offers a lineup of products with control voltages ranging from low control voltage products compatible with 1.2V I/O and a minimum of 0.8V, to products compatible with general-purpose lines of 1.8V and above.

To perform a parametric search of low control voltage LDOs → Click Here

(8) Package

We offer a wide range of packages, including ultra-compact WCSP types with high power dissipation suitable for high-density mounting, as well as general-purpose types that are easy to handle, available in various sizes. You can select the most suitable option according to your usage conditions.

To perform a parametric search of WCSP4E / 4F (0.645 mm x 0.645 mm) LDOs → Click Here

To perform a parametric search of SDFN4 / 4E (0.8 mm x 0.8 mm) LDOs → Click Here

To perform a parametric search of DFN4D / 4E / 4F (1.0 mm x 1.0 mm) LDOs → Click Here

To perform a parametric search of WCSP6F (1.2 mm x 0.8 mm) LDOs → Click Here

To perform a parametric search of DFN5B (1.2 mm x 1.2 mm) LDOs → Click Here

To perform a parametric search of SOT-553 (ESV) (1.6 mm x 1.6 mm) LDOs → Click Here

To perform a parametric search of SOT-353F (UFV) (2.0 mm x 2.1 mm) LDOs → Click Here

To perform a parametric search of SOT-25 (SMV) (2.9 mm x 2.8 mm) LDOs → Click Here

3. Power supply sequencing of LDOs

3.1. Single-power-supply LDOs

In the case of single-power-supply LDOs, the supply voltage from the V_{IN} pin is supplied to the internal control circuitry. For an LDO to work properly, V_{IN} must be fully powered up to a nominal voltage level prior to the application of control voltage (V_{CT}). Power off the LDO in the order opposite to the power-up sequence. Also use the LDO within the operating voltage range so that V_{CT} does not exceed V_{IN}. The power supply sequence, the magnitude relationship between V_{IN} and V_{CT}, and the operating voltage range might differ from LDO to LDO. For details on power supply sequencing, see the datasheets for individual LDOs.

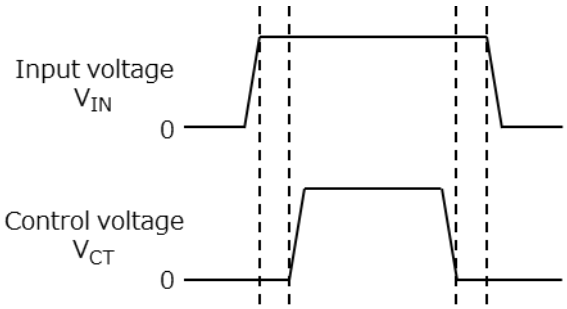


Figure 3.1 Power supply sequence of single-power-supply LDOs

3.2. Dual-power-supply LDOs

In the case of dual-power-supply LDOs, the supply voltage is supplied to the internal control circuitry from the bias voltage pin (V_{BIAS} or V_{BAT}). Therefore, V_{BIAS} or V_{BAT} must be fully powered up to a nominal voltage level first, followed by the application of input voltage (V_{IN}) and then control voltage (V_{CT}). Power off the LDO in the order opposite to the power-up sequence. The power supply sequence might differ from LDO to LDO. For details on power supply sequencing, see the datasheets for individual LDOs.

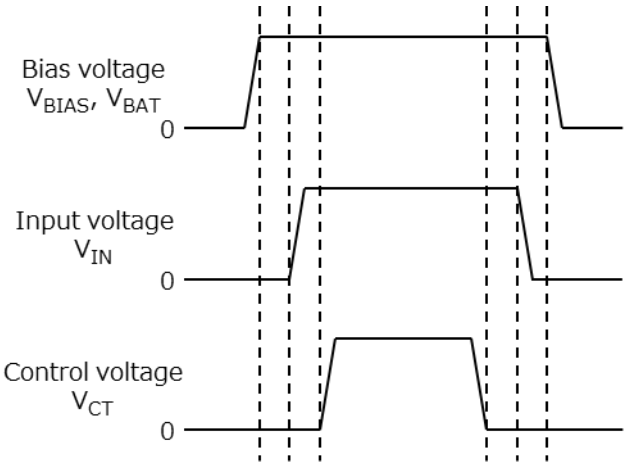


Figure 3.2 Power supply sequence of dual-power-supply LDOs

4. External capacitors

An LDO requires external capacitors to remove noise and power supply ripple. These capacitors greatly affect an LDO's performance as a power supply, including load transient response and oscillation immunity. Therefore, care should be exercised as to the types and specifications of the capacitors. Toshiba's LDOs are designed for use with multilayer ceramic capacitors (MLCCs). In this section, the use of multilayer ceramic capacitors (hereinafter referred to as "ceramic capacitors") is assumed. Ensure that an LDO is stable when used with capacitors with capacitance values higher than those shown in the datasheet.

4.1. Input capacitor, C_{IN}

The input capacitor (C_{IN}) filters out the noise superimposed on the input voltage. In the event of a drop in the input voltage due to an instantaneous change in output current, C_{IN} also prevents the malfunction of an LDO and compensates for a loss of output current.

4.2. Bias capacitor, C_{BIAS}

The bias capacitor (C_{BIAS}) filters out the noise superimposed on bias voltage and helps supply stable voltage to the internal control circuitry of an LDO.

4.3. Output capacitor, C_{OUT}

The output capacitor (C_{OUT}) compensates for a loss of output current in the event of an instantaneous change in output current, improving load transient response. C_{OUT} also provides phase compensation for a feedback loop.

4.4. Considerations for using ceramic capacitors

Ceramic capacitors are ideal for use with LDOs since high-capacitance-value ceramic capacitors are becoming available with small size and low effective series resistance (ESR). However, the values of ceramic capacitors depend on voltage and temperature as shown in Figure 4.1 and Figure 4.2. In particular, the value of the output capacitor greatly affects the stability of an LDO. Be sure to fully evaluate ceramic capacitors, taking voltage and temperature into consideration.

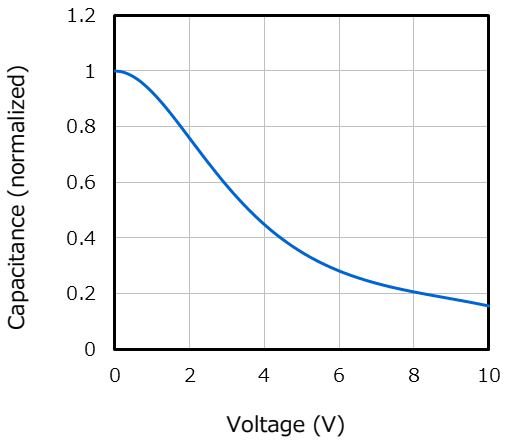


Figure 4.1 Example of a capacitance-vs-voltage curve of a ceramic capacitor

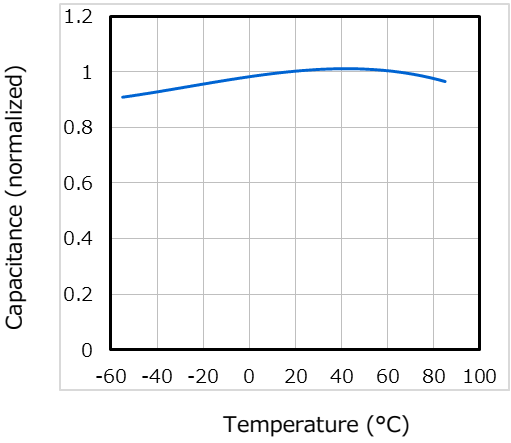


Figure 4.2 Example of a capacitance-vs-temperature curve of a ceramic capacitor

5. Overview of linear regulators

5.1. What is a linear regulator?

Also called series regulators, linear regulators incorporate an active component such as a pass transistor connected in series between an input power source and a load as shown in Figure 5.1. Controlled via a control signal, this active component acts as a variable resistor to maintain a constant output voltage.

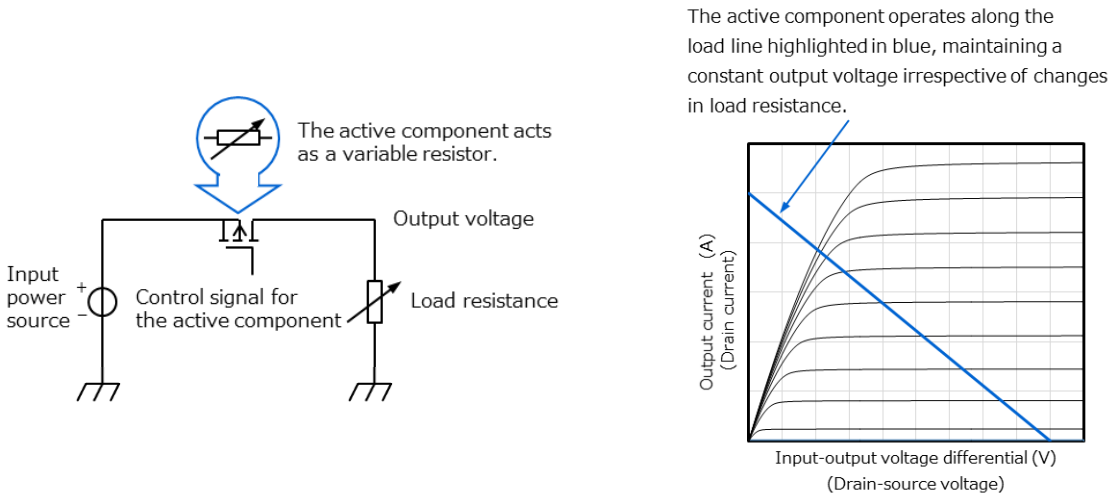


Figure 5.1 Operation of a linear regulator

5.2. Dropout voltage of LDOs

The input-output voltage differential of a linear regulator is called the dropout voltage. The input voltage necessary to obtain a regulated output voltage is expressed by Equation 5-1:

$$V_{IN} = V_{OUT} + V_{DROP} \tag{5-1}$$

Generally, linear regulators with a dropout voltage of less than 1 V or so are called LDOs. Figure 5.2 shows an LDO with a P-channel MOS pass transistor. The gate-source voltage of the LDO can be up to V_{IN}. Since the LDO can operate in the linear region shown in Figure 5.3, the relationship between the input and output voltages can be expressed by Equation 5-2.

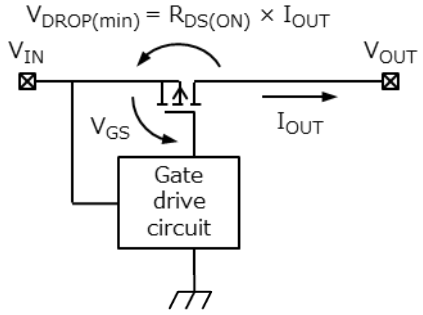


Figure 5.2 Dropout voltage of an LDO with a P-channel MOS pass transistor

$$\begin{aligned} V_{IN(min)} &= V_{OUT} + V_{DROP(min)} \\ &= V_{OUT} + R_{DS(ON)} \times I_{OUT} \end{aligned} \tag{5-2}$$

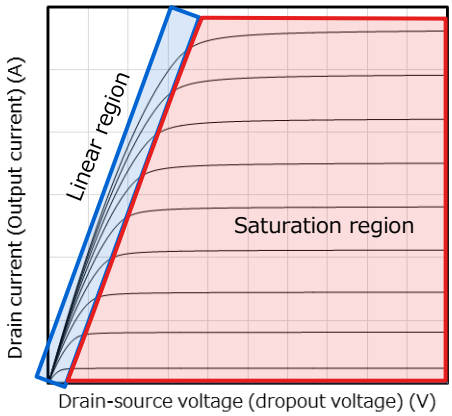


Figure 5.3 Regions of MOSFET operation

Figure 5.4 shows a standard linear regulator with an N-channel MOS pass transistor. Equation 5-3 holds because $V_{DROP(min)} = V_{GS}$. Hence, the dropout voltage cannot be lower than V_{GS}.

$$V_{IN(min)} = V_{OUT} + V_{GS} \quad (5\text{-}3)$$

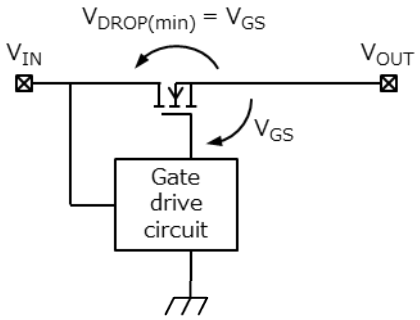
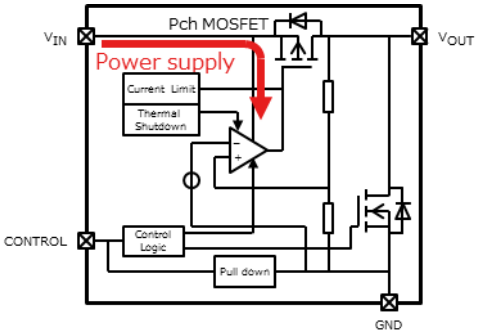
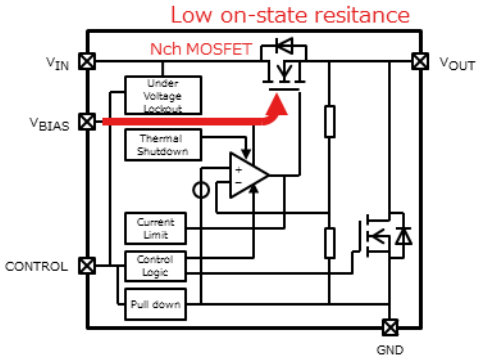
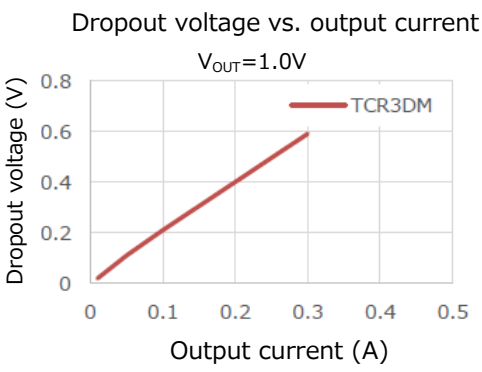
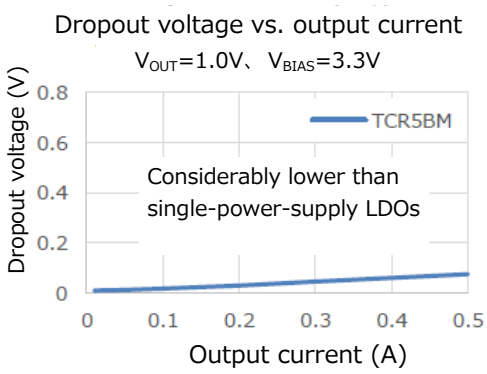


Figure 5.4 Dropout voltage of a standard linear regulator with an N-channel MOS pass transistor

As described above, in the case of single-power-supply LDOs, LDOs with a P-channel MOS pass transistor provide less dropout voltage than those with an N-channel MOS pass transistor.

However, since single-power-supply LDOs with a P-channel MOS pass transistor drive the gate of the MOS output transistor from V_{IN}, the gate drive voltage becomes insufficient at low V_{IN}, making it impossible to obtain a regulated output voltage. In contrast, dual-power-supply LDOs with the V_{IN} and V_{BIAS} pins incorporate an N-channel MOS output transistor that is more suitable for reducing on-resistance. Since these LDOs drive the gate of the MOS output transistor from the V_{BIAS} pin, the dropout voltage decreases because the gate voltage is independent of V_{IN}. This makes it possible to obtain a regulated output voltage even at low V_{IN}, considerably reducing power loss. Table 5.1 compares single- and dual-power-supply LDOs.

Table 5.1 Comparison of single- and dual-power-supply LDOs

Types of LDOs	Single-power-supply LDOs	Dual-power-supply LDOs
Polarity of the MOS output transistor	P-channel MOSFET	N-channel MOSFET
Power supplies required	Only V_{IN}	V_{IN} and V_{BIAS}
Dropout characteristics	The gate voltage of the MOS output transistor is supplied from the V_{IN} pin.	The gate voltage of the MOS output transistor is supplied from the V_{BIAS} pin to reduce on-resistance and dropout voltage.
		
Dropout voltage characteristics When V_{OUT} = 1.0 V		

6. Major characteristics of LDOs

This section describes each electrical characteristic of LDOs, referring to actual datasheets.

6.1. Input voltage (V_{IN})

V_{IN} is the input voltage range in which an LDO is guaranteed to operate properly and provide the specified electrical characteristics. In the event of an input undervoltage condition, LDOs with the undervoltage lockout (UVLO) function shut down the output to prevent the subsequent IC or circuitry from malfunctioning in order to avoid system failure or instability.

Datasheet example: TCR3UF series (300 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Input voltage	V_{IN}	I_{OUT} = 1 mA	1.5	–	5.5	1.5	5.5	V

6.2. Bias voltage (V_{BIAS}, V_{BAT})

The bias voltage supplied via the V_{BIAS} pin is used as a power supply for the internal control and protection circuits of the LDO as well as for the gate drive of the MOS output transistor and the error amplifier for output voltage detection. V_{BIAS} and V_{BAT} are the bias voltage range in which these circuits are guaranteed to operate properly to provide the specified electrical characteristics. The V_{BIAS} pin does not incorporate an undervoltage lockout (UVLO) function. For the power-up and power-down sequence of V_{BIAS} and V_{IN}, see Section 3, "Power supply sequencing of LDOs."

Datasheet example: TCR13AGADJ (1.3 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Bias voltage	V_{BIAS}	V_{OUT} ≤ 1.1 V, I_{OUT} = 1 mA	2.5	–	5.5	2.5	5.5	V
		V_{OUT} > 1.1 V, I_{OUT} = 1 mA	V_{OUT} +1.4 V	–	5.5	V_{OUT} +1.4 V	5.5	

6.3. Output voltage accuracy, output voltage (V_{OUT})

V_{OUT} is the accuracy of output voltage regulation under the test conditions specified in a datasheet.

Datasheet example: TCR8BM series (800 mA LDO)

Characteristics	Symbol	Test Condition		T_j = 25°C			T_j = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Output voltage accuracy	V_{OUT}	I_{OUT} = 50 mA	V_{OUT} < 1.8 V	-18	–	+18	–	–	mV
			1.8 V ≤ V_{OUT}	-1.0	–	+1.0	–	–	%

6.4. Adjustable voltage (V_{ADJ})

V_{ADJ} is specified for LDOs with adjustable output voltage. V_{ADJ} is the reference voltage for the error amplifier for output voltage detection. The error amplifier compares the reference voltage with the voltage at the midpoint of a resistor voltage divider between V_{OUT} and GND and accordingly controls the MOS output transistor so that the output maintains the regulated voltage. Among the TCR15AG series, the TCR15AGADJ is the adjustable output type.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Adjustable voltage	V_{ADJ}	–	0.588	0.60	0.612	–	–	V

6.5. Quiescent current (I_B, $I_{B(ON)}$)

I_B and $I_{B(ON)}$ are the quiescent current of the internal circuitry minus the pull-down current of the CONTROL pin flowing out of the GND pin when an LDO is operating under the test conditions specified in a datasheet. I_B and $I_{B(ON)}$ are specified under a zero-load current (I_{OUT} = 0 mA).

Datasheet example: TCR3UF series (300 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Quiescent current	$I_{B(ON1)}$	I_{OUT} = 0 mA, $V_{OUT} \leq$ 1.5 V	—	0.34	—	—	0.58	μA
	$I_{B(ON2)}$	I_{OUT} = 0 mA, 1.5 V < $V_{OUT} \leq$ 5 V	—	0.38	—	—	0.68	μA

6.6. Quiescent current ($I_{IN(ON)}$, $I_{BIAS(ON)}$)

$I_{IN(ON)}$ and $I_{BIAS(ON)}$ are the quiescent currents flowing into the V_{IN} pin and V_{BIAS} pin when an LDO is operating under the test conditions specified in a datasheet. $I_{IN(ON)}$ and $I_{BIAS(ON)}$ are specified under a zero-load current (I_{OUT} = 0 mA).

Datasheet example: TCR8BM series (800 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Quiescent current	$I_{IN(ON)}$	I_{OUT} = 0 mA, V_{IN} current	–	3	–	–	6	μA
	$I_{BIAS(ON)}$	I_{OUT} = 0 mA, V_{BIAS} current	–	20	–	–	36	μA

6.7. Standby current ($I_{B(OFF)}$, $I_{IN(OFF)}$, $I_{BIAS(OFF)}$)

$I_{B(OFF)}$, $I_{IN(OFF)}$, and $I_{BIAS(OFF)}$ are the current flowing through the V_{IN} and V_{BIAS} pins when an LDO is in standby mode. LDOs in a battery-operated device draw standby current from a battery while it is in standby mode. Therefore, $I_{B(OFF)}$, $I_{IN(OFF)}$, and $I_{BIAS(OFF)}$ are important characteristics to conserve battery life.

Datasheet example: TCR3UM series (300 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Standby current	$I_{B\ (OFF1)}$	V_{CT} = 0 V, V_{IN} = 2.5 V	—	0.03	—	—	0.16	μA
	$I_{B\ (OFF2)}$	V_{CT} = 0 V, V_{IN} = 5.5 V	—	0.03	—	—	0.20	

6.8. ADJ pin current (I_{ADJ})

I_{ADJ} is the input current to an error amplifier connected to the V_{ADJ} pin.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
ADJ pin current	I_{ADJ}	V_{ADJ} = 0.6 V	–	0	0.1	–	–	μA

6.9. Control voltage (ON) ($V_{CT(ON)}$), Control voltage (HIGH) (V_{CTH})

$V_{CT(ON)}$/ V_{CTH} are the voltage required at the CONTROL pin to turn on an LDO. When a voltage in the range specified in a datasheet is applied to the CONTROL pin, output voltage appears at the V_{OUT} pin. Do not apply voltage higher than the V_{IN} or V_{BIAS} to the CONTROL pin. For details, see the datasheets for individual LDOs.

Datasheet example: TCR3EM series (300 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Control voltage (HIGH)	V_{CTH}	CONTROL pin input voltage “HIGH”	–	–	–	0.8	5.5	V

6.10. Control voltage (OFF) ($V_{CT(OFF)}$), Control voltage (LOW) (V_{CTL})

$V_{CT(OFF)}$/ V_{CTL} is the voltage required at the CONTROL pin to turn off an LDO. When a voltage in the range specified in a datasheet is applied to the CONTROL pin, the output voltage is shut down. Ensure that negative voltage is not applied to the CONTROL pin.

Datasheet example: TCR3EM series (300 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Control voltage (LOW)	V_{CTL}	CONTROL pin input voltage "LOW"	–	–	–	–	0.4	μA

6.11. Control pull-down current (I_{CT})

A pull-down MOSFET is internally connected between the CONTROL and GND pins as shown in Figure 3.1 so that the voltage of the internal control circuitry will not become unstable in the event of the CONTROL pin becoming open. A MOSFET is used as a pull-down device to keep I_{CT} constant as shown by the I_{CT} – V_{CT} curve in Figure 6.2 even when the voltage at the CONTROL pin increases.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Control pull-down current	I_{CT}	–	–	0.03	–	–	–	μA

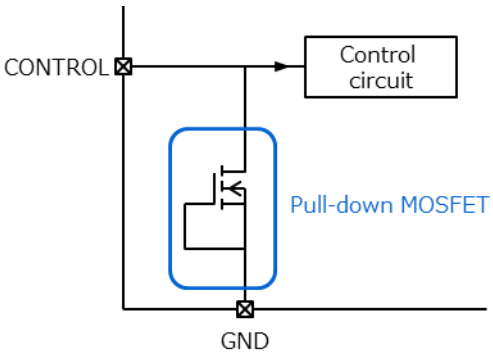


Figure 6.1 Equivalent circuit for the internal circuitry of the CONTROL pin

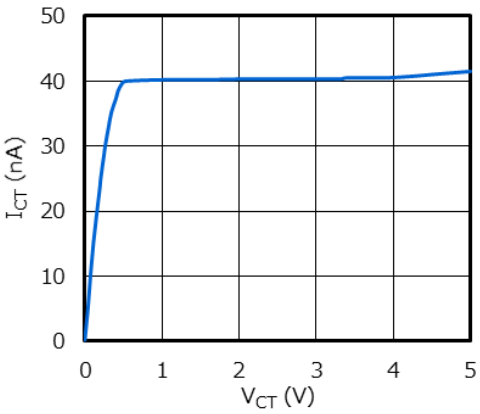


Figure 6.2 I_{CT} – V_{CT} curve (reference)

6.12. Line regulation (Reg·line)

Line regulation (Reg·line) is an amount of change of V_{OUT} with respect to V_{IN} when I_{OUT} is kept constant. Reg·line can be calculated using Equation 6-1.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Line regulation	Reg·line	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 1 mA	–	0	15	–	–	mV

$$Reg \cdot line = \Delta V_{OUT} \tag{6-1}$$

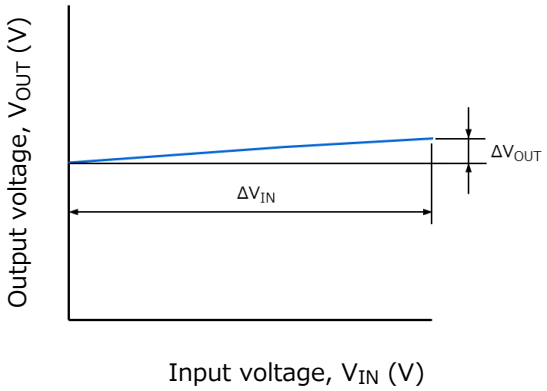


Figure 6.3 Line regulation (Reg·line)

LDOs with a smaller Reg·line value have a higher ability to maintain a regulated output voltage (V_{OUT}) despite changes to the input voltage (V_{IN}). If the input voltage range is wide, it is necessary to use an LDO with a small Reg·line value.

6.13. Load regulation (Reg·load)

Load regulation (Reg·load) is an amount of change of V_{OUT} with respect to I_{OUT} when V_{IN} is kept constant. Reg·load can be calculated using Equation 6-2.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Load regulation	Reg·load	0.01 A ≤ I_{OUT} ≤ 1.5 A	–	3	–	–	–	mV

$$Reg \cdot load = \Delta V_{OUT} \tag{6-2}$$

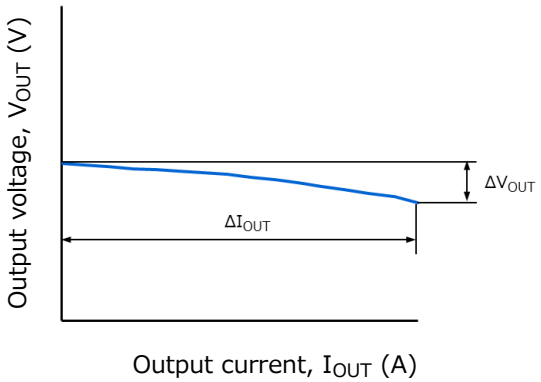


Figure 6.4 Load regulation (Reg·load)

LDOs with a smaller Reg·load value have a higher ability to maintain a regulated output voltage (V_{OUT}) despite changes to the output current (I_{OUT}). If the output current range is wide, it is necessary to use an LDO with a small Reg·load value.

6.14. Dropout voltage (V_{DO}) (input-output voltage differential)

Also called the input-output voltage differential, the dropout voltage (V_{DO}) is a difference between input and output voltages necessary to maintain output voltage regulation. The dropout voltage of an LDO with a MOS output transistor is specified under the conditions in which the MOS output transistor is operating in the linear region. In this region, the dropout voltage depends on on-resistance and output current as indicated by Equation 6-3.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Dropout voltage	V_{DO}	I_{OUT} = 1.5 A, V_{BIAS} = 3.3 V	–	120	–	–	216	mV

$$V_{DO} = V_{DS(ON)}$$
$$= R_{DS(ON)} \times I_{OUT} \quad (6\text{-}3)$$

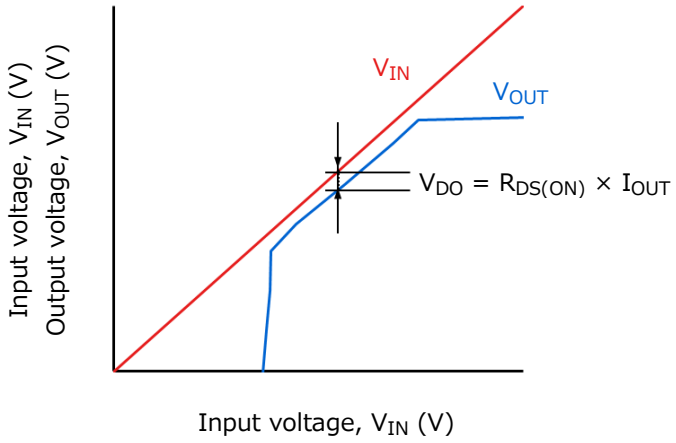


Figure 6.5 Dropout voltage (V_{DO})

6.15. Output Current limit (I_{CL})

I_{CL} is the threshold at which an LDO begins limiting excessive output current caused by a short-circuited load or other condition. Toshiba defines I_{CL} as the output current that an LDO provides when the output voltage drops to V_{OUT} typical × 0.9 in the event of overcurrent protection being tripped.

Datasheet example: TCR3EM series (300 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Output current limit	I_{CL}	V_{OUT} = $V_{OUT(NOM)}$*90%	–	–	–	310	550	mA

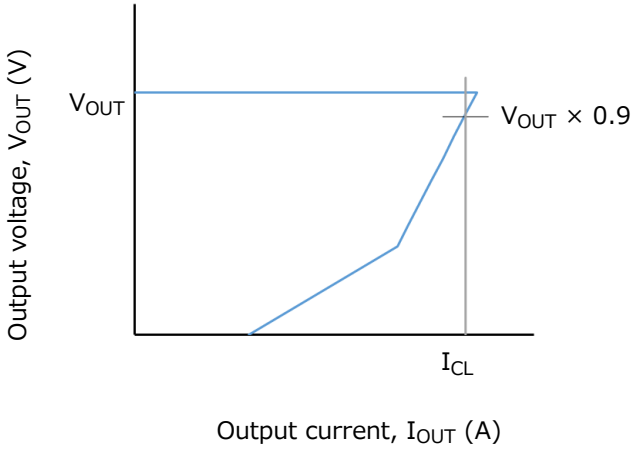


Figure 6.6 Current limit (I_{CL})

Toshiba's LDOs provide overcurrent protection called foldback. Foldback is a current-limiting feature that reduces the output current as the output voltage decreases in the event of an overcurrent condition. When V_{OUT} has decreased to 0 V, the current is limited to an internally set constant value. This feature is called foldback because the V_{OUT}–I_{OUT} curve folds back as shown in Figure 6.7 when the output current is limited. When a fault condition causing overcurrent disappears, an LDO automatically recovers from overcurrent protection, returning the output voltage to the normal level.

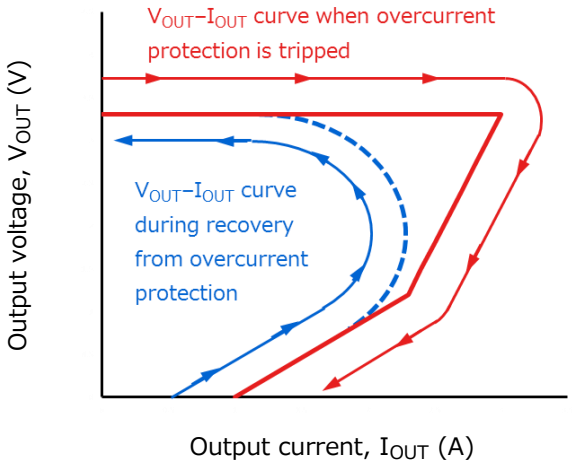


Figure 6.7 Foldback current curves

6.16. Undervoltage lockout (V_{UVLO})

In the event of an input undervoltage condition, the output voltage might drop below the minimum operating voltage of the subsequent IC or circuitry, causing system failure. V_{UVLO}, an undervoltage lockout threshold voltage, is an input voltage at which an LDO turns off to prevent system malfunction.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Undervoltage lockout	V_{UVLO}	Input voltage	–	0.5	–	–	0.65	V

Undervoltage lockout has hysteresis. When the input voltage rises back above the recovery threshold with the high-level CONTROL voltage being applied, the output voltage automatically returns to the normal level.

The undervoltage lockout feature compares the input voltage with the internal reference voltage of an LDO as shown in Figure 6.8. When the input voltage drops below reference voltage V_1, the comparator output toggles, turning off the output voltage. At the same time, the N-channel MOSFET for reference voltage selection turns off, switching the reference voltage to a higher level (V_2). Thereafter, when the input voltage rises back above V_2, the comparator toggles again, turning on the output voltage.

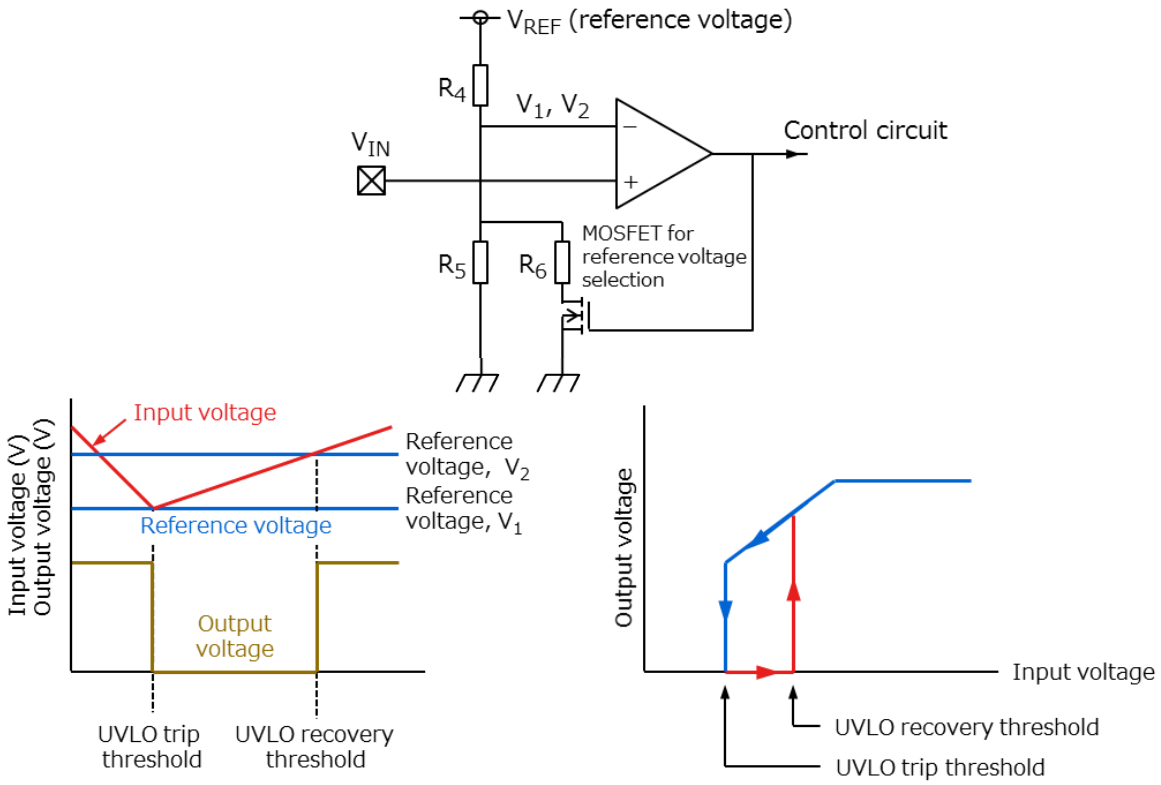


Figure 6.8 Undervoltage lockout circuit

UVLO trip threshold $V_1 = V_{REF} \times \frac{R_5 R_6}{R_4 R_5 + R_4 R_6 + R_5 R_6}$ (6-4)

UVLO recovery threshold $V_2 = V_{REF} \times \frac{R_4 R_5}{R_4 + R_5}$ (6-5)

6.17. Temperature coefficient (T_{CVO})

T_{CVO} is a rate of change of the output voltage with respect to a change of 1°C in ambient temperature under the test conditions specified in a datasheet. LDOs with lower T_{CVO} have a higher ability to maintain the regulated output voltage despite changes in temperature.

Datasheet example: TCR8BM series (800 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Temperature coefficient	T_{CVO}	- 40°C ≤ T_{opr} ≤ 85°C	–	70	–	–	–	ppm/°C

6.18. Output noise voltage (V_{NO})

V_{NO} is the magnitude of noise that occurs at the output of an LDO. It is defined as the sum of all types of noise in the frequency range specified as a test condition.

Datasheet example: TCR8BM series (800 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Output noise voltage	V_{NO}	V_{BIAS} = 3.3 V V_{IN} = V_{OUT} + 0.5 V I_{OUT} = 10 mA 10 Hz ≤ f ≤ 100 kHz	–	40	–	–	–	μV_{rms}

The output noise is broadly divided into two categories. The first category is the internal noise intrinsic to an LDO and includes the following:

1) 1/f noise

Also called flicker noise or pink noise, 1/f noise is considered to be caused by defects on the semiconductor surface, etc. It is called 1/f noise because the noise level is inversely proportional to frequency.

2) Popcorn noise

Also called burst noise, popcorn noise is considered to be caused by lattice defects in the semiconductor, etc. It is called popcorn noise because it produces an acoustic noise that sounds like popping popcorn when it enters an audio speaker. Popcorn noise has considerable adverse effects on applications that are very sensitive to noise such as CMOS sensors.

3) White noise

Also called thermal noise, white noise is caused by the thermal movement of electrons. It is not dependent on frequency. The white noise voltage is expressed as Equation 6-6:

$$V_n = \sqrt{4k \cdot T \cdot R \cdot B} \quad \text{(V)} \qquad \text{(6-6)}$$

k:	Boltzmann constant (1.38×10^{-23})	(J/K)
T:	Absolute temperature	(K)
R:	Resistance	(Ω)
B:	Noise bandwidth	(Hz)

4) Shot noise

Shot noise occurs whenever carriers cross the potential barrier of a p-n junction. It is generated because the resulting current flow is discontinuous. As is the case with white noise, shot noise is not dependent on frequency, and is expressed as Equation 6-7:

$$I_n = \sqrt{2q \cdot I \cdot B} \quad \text{(A)} \qquad \text{(6-7)}$$

q:	Elementary charge (1.602×10^{-19})	(C)
I:	Average current	(A)
B:	Noise bandwidth	(Hz)

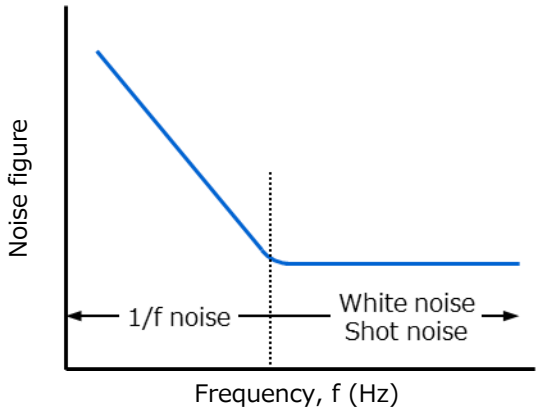


Figure 6.9 Noise frequency characteristics

The other type of noise source is the ripple noise superimposed on the input voltage (supply voltage) of an LDO. Although an LDO internally suppresses ripple noise, some ripple still appears at the output. The ability of an LDO to suppress ripple in the input voltage to its output is called the ripple rejection ratio.

6.19. Ripple rejection ratio (R.R. (V_{IN}), R.R. (V_{BIAS}))

The ripple rejection ratio is the ability of an LDO to suppress ripple in the input or bias voltage to its output under the test conditions specified in a datasheet. It is expressed in dB.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Ripple rejection ratio	R.R. (V_{IN})	V_{BIAS} = 3.3 V V_{IN} = V_{OUT} + 1 V I_{OUT} = 10 mA, f = 1kHz $V_{IN\ Ripple}$ = 200 mV_{p-p}	–	95	–	–	–	dB
	R.R. (V_{BIAS})	V_{BIAS} = 3.3 V V_{IN} = V_{OUT} + 1 V I_{OUT} = 10 mA, f = 1kHz $V_{BIAS\ Ripple}$ = 200 mV_{p-p}	–	60	–	–	–	

The ripple rejection ratio (R.R.) is calculated as shown below. R.R. is dependent on frequency. As frequency increases, R.R. decreases. In cases where an LDO is preceded by a DC–DC converter, an LDO with a higher R.R. is more suitable for the sensor and other analog circuits that are very sensitive to noise because a high-R.R. LDO provides an excellent noise suppression capability. The ripple rejection ratio is also called the power supply rejection ratio (PSRR) or the supply voltage rejection ratio (SVRR).

$$R.R. = 20 \cdot \log \frac{V_{IN\ ripple}}{V_{OUT\ ripple}} \quad \text{(dB)} \qquad (6\text{-}8)$$

$V_{IN\ ripple}$: Ripple voltage superimposed on the input voltage (V_{IN}) (V)

$V_{OUT\ ripple}$: Ripple voltage superimposed on the output voltage (V_{OUT}) (V)

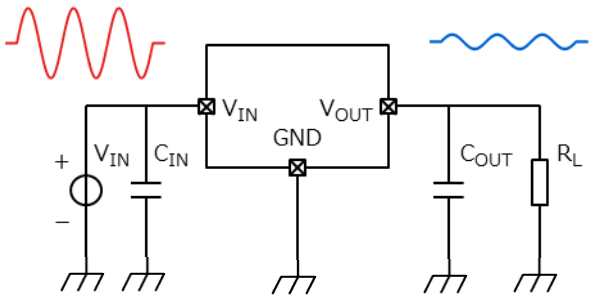


Figure 6.10 Ripple rejection

For more details on the ripple rejection ratio and how to improve it, see Simple Guide to Improving Ripple Rejection Ratio of LDO Regulators.

To download the application note above→ Click Here

6.20. Load transient response (ΔV_{OUT})

The load transient response (ΔV_{OUT}) is an amount of change in the undershoot and overshoot of the output voltage for a load current step change. LDOs with poor load transient response might affect the correct operation of the subsequent IC or circuitry because they are susceptible to large output voltage transients and require a long time for the output voltage to return to the normal level.

Datasheet example: TCR8BM series (800 mA LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Load transient response	ΔV_{OUT}	I_{OUT} = 1 mA → 800 mA	–	-100	–	–	–	mV
		I_{OUT} = 800 mA → 1 mA	–	100	–	–	–	

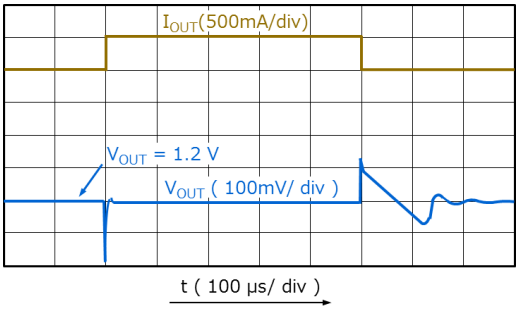


Figure 6.11 V_{OUT} waveform of an LDO with poor load transient response

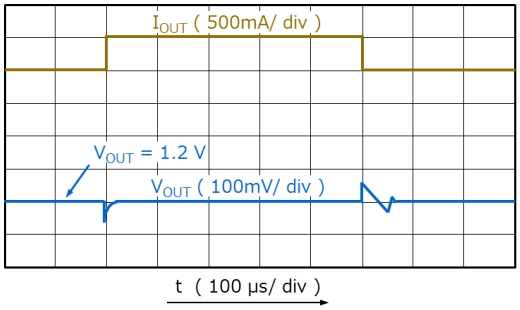


Figure 6.12 V_{OUT} waveform of an LDO with good load transient response

Load transient response characteristics are determined as follows.

1) In the event of a sharp increase in output current

Suppose that an LDO connected to the load impedance (Z_{L1}) has constant output voltage and current, with the MOS output transistor operating at ① in Figure 6.14. Let the drain-source and gate-source voltages at this time be V_{DS1} and V_{GS1}, respectively. When the MOS pass transistor turns on, causing a sharp increase in the output current from I_{OUT1} to I_{OUT2}, the internal error amplifier of the LDO initiates a feedback operation to regulate the output voltage. However, the output voltage does not return to the normal level immediately, depending on the frequency characteristics of the feedback loop, producing a drop in the output voltage as indicated by ② in Figure 6.14. At this time, the operating point (Q point) of the MOS output transistor moves from V_{DS1} (①) to V_{DS2} (②). However, the gate-source voltage (V_{GS}) does not increase to the V_{GS2} level necessary to provide I_{OUT2}. The feedback operation continues, causing V_{GS} to move to V_{GS2} at the Q point indicated by ③, making it possible for the LDO to provide I_{OUT2}. As a result, the output voltage ceases to decrease and begins to return to the normal level.

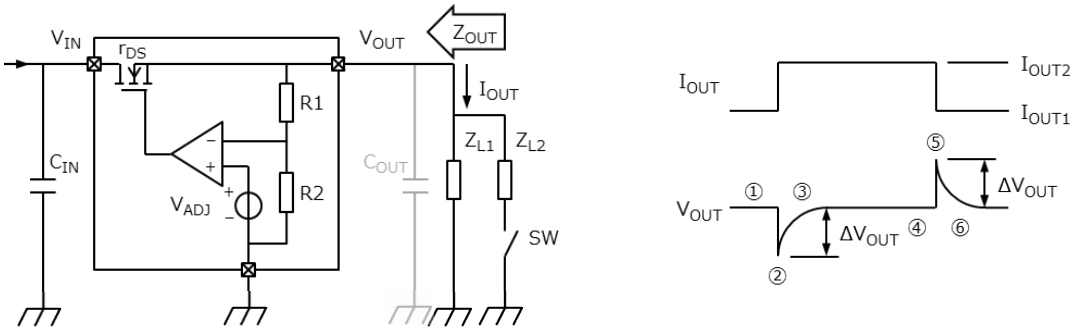


Figure 6.13 Test circuit for load transient response and operating waveforms

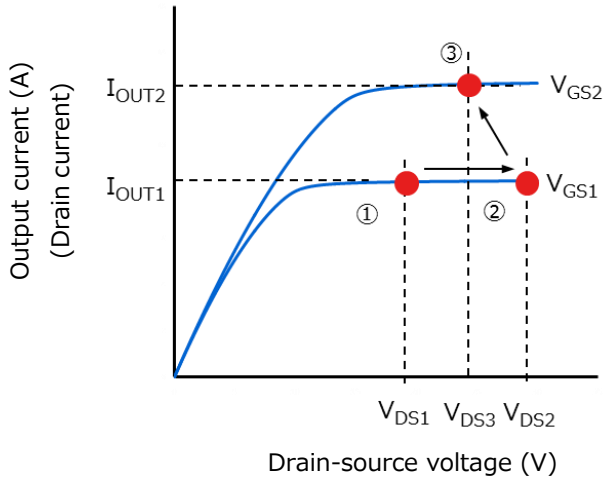


Figure 6.14 Q points in the event of a sharp increase in output current

The output impedance (Z_{OUT}) seen from the V_{OUT} pin of the LDO is:

$$Z_{OUT} = r_{DS} // R_F // Z_L \quad (6\text{-}9)$$

r_{DS}:	Drain resistance of the P-channel MOS output transistor	(Ω)
R_F:	Feedback resistance (R1+R2)	(Ω)
Z_L:	Load impedance (Z_{L1}+Z_{L2})	(Ω)

When a feedback response cannot catch up with an extremely sharp (high-slew-rate) change in output current, the change in output voltage (ΔV_{OUT}) can be calculated by Equation 6-10:

$$\Delta V_{OUT} = \frac{\Delta I_{OUT}}{C_{OUT}} \times \Delta t \quad (6\text{-}10)$$

ΔV_{OUT}:	Change in output voltage	(V)
ΔI_{OUT}:	Change in output current	(A)
Δt:	Response time of the feedback loop	(s)
C_{OUT}:	Output capacitor value	(F)

If the feedback loop has excellent frequency response, the output voltage of the LDO returns to the normal level without dropping as much as calculated by Equation 6-10.

Equation 6-11 also indicates that a high-value output capacitor helps reduce the drop in output voltage.

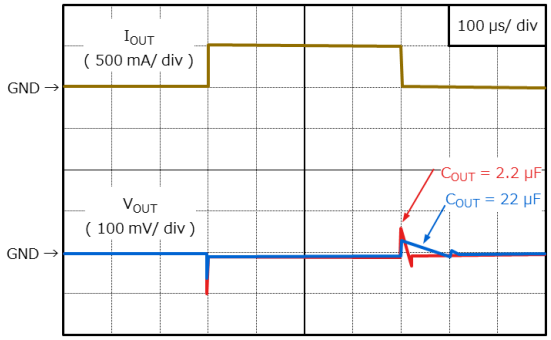


Figure 6.15 Load transient response vs. output capacitor values

2) In the event of a sharp decrease in output current

Suppose that the MOS output transistor is operating at ④ in Figure 6.14, maintaining a regulated output voltage, with the output current I_{OUT2} flowing through the load impedances (Z_{L1} and Z_{L2}) connected to the LDO. Let the drain-source and gate-source voltages at this time be V_{DS2} and V_{GS2}, respectively. When the MOS pass transistor turns off, causing a sharp decrease in the output current from I_{OUT2} to I_{OUT1}, the internal error amplifier of the LDO initiates a feedback operation to regulate the output voltage. However, the output voltage does not return to the normal level immediately, depending on the frequency characteristics of the feedback loop, producing a rise in the output voltage as indicated by ⑤ in Figure 6.14. At this time, the Q point of the MOS output transistor moves from V_{DS2} (④) to V_{DS1} (⑤) as shown in Figure 6.17. However, the gate-source voltage (V_{GS}) does not decrease to the V_{GS1} level necessary to provide I_{OUT1}. The feedback operation continues, causing V_{GS} to move to V_{GS1} at the Q point indicated by ⑥, making it possible for the LDO to reduce the output current to I_{OUT1}. As a result, the output voltage ceases to increase and begins to return to the normal level.

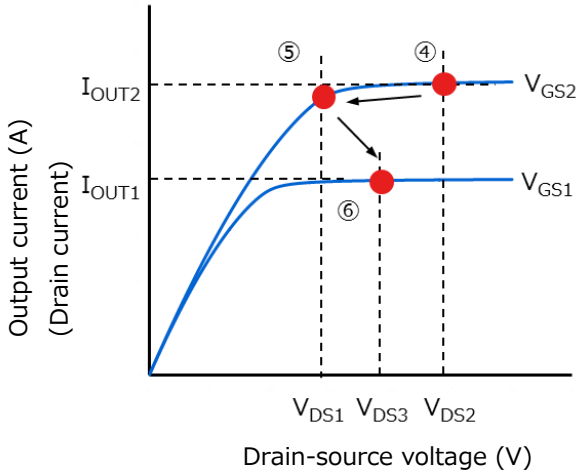


Figure 6.16 Q points in the event of a sharp decrease in output current

For the mechanism of load transient response and how to improve it, see Load Transient Response of LDO and Methods to Improve it.

To download the application note above → Click Here

6.21. Output discharge on-resistance (R_{SD})

R_{SD} is the on-resistance of the internal N-channel MOSFET for discharging the output capacitor connected between the V_{OUT} and GND pins of an LDO. When the LDO output turns off, the N-channel MOSFET turns on to discharge the output capacitor. This MOSFET helps reduce the time required to discharge even a large output capacitor, simplifying system power supply sequencing.

Datasheet example: TCR15AG series (1.5 A LDO)

Characteristics	Symbol	Test Condition	T_j = 25°C			T_j = -40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Output discharge on-resistance	R_{SD}	–	–	10	–	–	–	Ω

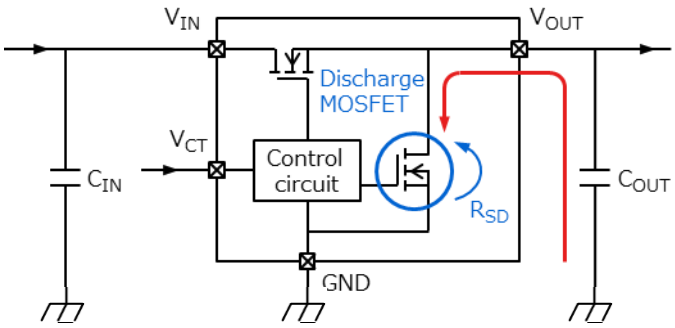


Figure 6.17 Output discharge circuit

6.22. Thermal shutdown temperature (T_{SD}), thermal shutdown temperature hysteresis (T_{SDH})

Thermal shutdown (TSD) is a feature for sensing of the junction temperature to protect an LDO. T_{SD} is the junction temperature at which an LDO turns off its output to prevent self-damage or degradation caused by self-heating due to a sharp increase in ambient temperature, a short-circuited load, a short-to-ground of the V_{OUT} pin, etc. When TSD is tripped, the output turns off, reducing power consumption and thereby the junction temperature. When the junction temperature drops to the specified temperature, the LDO automatically recovers from TSD, turning its output back on. TSD has hysteresis (T_{SDH}), i.e., a difference between the temperature at which the LDO trips TSD to turn off the output and the temperature at which it recovers from TSD. Both the T_{SD} and T_{SDH} values shown in the datasheet are design targets.

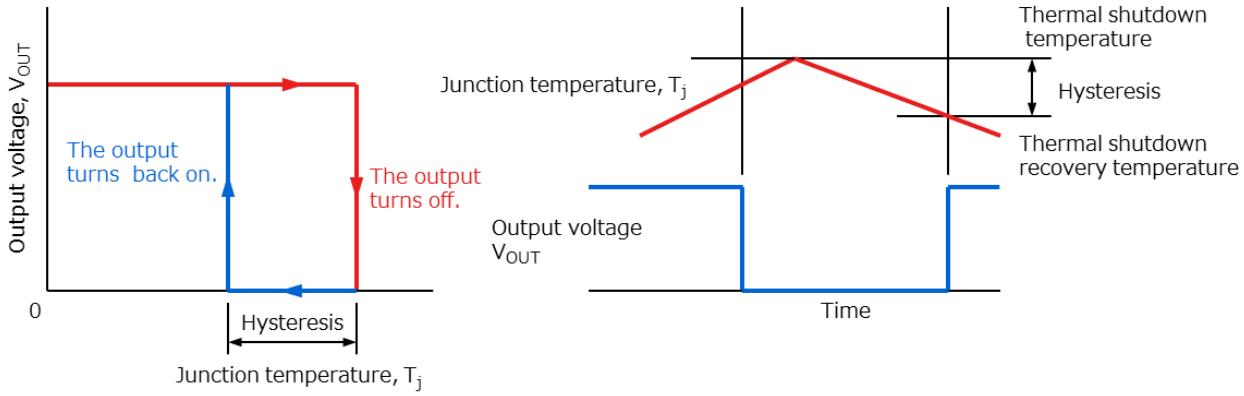


Figure 6.18 Thermal shutdown temperature and thermal shutdown hysteresis

The junction temperature is detected by comparing the reference voltage that changes little with temperature and the forward voltage of a diode, as shown in Figure 6.20. When an LDO is operating properly, the diode's forward voltage is higher than the reference voltage. Since the diode's forward voltage has a temperature coefficient of roughly -2 mV/°C, it becomes lower than the reference voltage when an abnormal load condition causes the junction temperature to increase. The TSD circuit detects this as overheating. In that event, the comparator output toggles, turning off the LDO. At this time, the comparator output is used to switch the reference voltage to a higher level. When the LDO turns off, its power dissipation decreases substantially, causing the junction temperature to decrease and thus the diode's forward voltage to increase. When the diode's forward voltage exceeds the reference voltage, the LDO output automatically turns back on. The thermal shutdown temperature hysteresis (T_{SDH}) is a difference between the temperature at which the LDO trips TSD and the temperature at which it recovers from TSD.

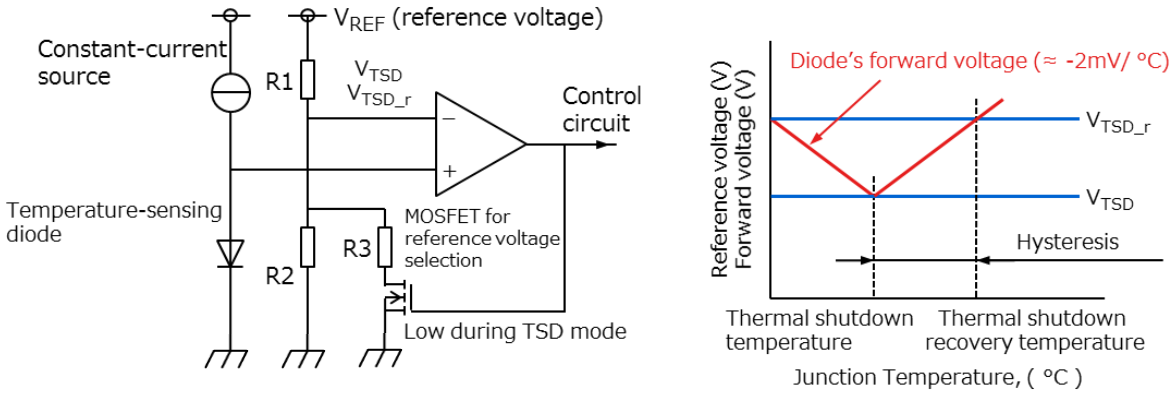


Figure 6.19 TSD circuit and its principle of operation

TSD trip voltage

$$V_{TSD} = V_{REF} \times \frac{R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3} \quad (6\text{-}11)$$

TSD recovery voltage

$$V_{TSD\_r} = V_{REF} \times \frac{R_2}{R_1 + R_2} \quad (6\text{-}12)$$

6.23. Inrush current suppression (slew rate control)

When a logic High is applied to the CONTROL pin, the inrush current suppression feature increases the output voltage slowly to reduce the slew rate of inrush current, thereby preventing system malfunction. When a large output capacitor is connected to an LDO, turning on an LDO during the discharging of the output capacitor causes considerable charge current (inrush current) to flow to the capacitor. At this time, the input voltage might drop instantaneously because of the wire impedance on the input side, causing system malfunction. The inrush current suppression feature uses the foldback circuit for overcurrent protection. A logic High at the CONTROL pin causes the output voltage to rise to the normal level slowly.

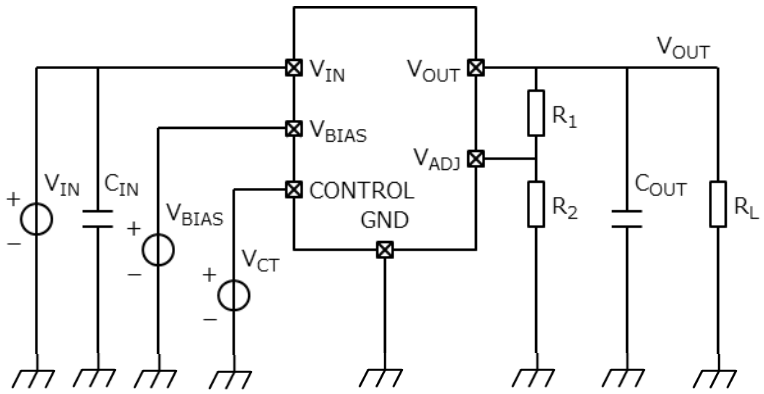
7. Setting the output voltage of an adjustable-output-voltage LDO

For adjustable-output-voltage LDOs, it is necessary to connect two external resistors in series between the V_{OUT} and GND pins. The output voltage can be set by applying the voltage at the midpoint of these resistors to the V_{ADJ} pin.

The values of the voltage-setting resistors can be calculated as follows:

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R_1}{R_2}\right) \quad (7\text{-}1)$$

V_{ADJ}: Internal reference voltage (V)



(R_1 + R_2) and the output capacitor (C_{OUT}) generate a pole at $f_p = \frac{1}{2\,\pi\,C_{OUT}\,(R_1//R_2)}$. If excessively large R_1 and R_2 are used to reduce power consumption, the pole shifts toward a low-frequency region, approaching the pole in the LDO. This might cause the output voltage to oscillate because of a 180° phase rotation.

Use Table 7.1 as a guide to select the values of R_1 and R_2 and perform detailed evaluation.

Table 7.1 Examples of external resistor values for an adjustable-output-voltage LDO (TCR15AGADJ)

Output voltage (typical)	R_1	R_2	Output voltage (typical)	R_1	R_2
0.6 V	0 Ω	Open	1.2 V	24 kΩ	24 kΩ
0.65 V	2 kΩ	24 kΩ	1.3 V	28 kΩ	24 kΩ
0.7 V	4 kΩ	24 kΩ	1.8 V	48 kΩ	24 kΩ
0.8 V	8 kΩ	24 kΩ	2.5 V	76 kΩ	24 kΩ
0.9 V	12 kΩ	24 kΩ	3.0 V	96 kΩ	24 kΩ
1.0 V	16 kΩ	24 kΩ	3.3 V	108 kΩ	24 kΩ
1.1 V	20 kΩ	24 kΩ	3.6 V	120 kΩ	24 kΩ

Output voltage variation can be simulated or calculated as follows based on the variations of V_{ADJ}, R_1, and R_2.

$$v_{OUT} = \sqrt{\left(\frac{R_1}{R_2}+1\right)^2 \cdot {v_{ADJ}}^2 + \left(\frac{V_{ADJ}}{R_2}\right)^2 \cdot {R_1}^2 + \left(\frac{V_{ADJ} \cdot R_1}{{R_2}^2}\right)^2 \cdot {r_2}^2} \quad (7\text{-}2)$$

v_{OUT}:	Output voltage variation	(V)
V_{ADJ}:	Typical internal reference voltage	(V)
v_{ADJ}:	Internal reference voltage variation	(V)
R_1:	Typical R_1 value	(Ω)
r_1:	R_1 variation	(Ω)
R_2:	Typical R_2 value	(Ω)
r_2:	R_2 variation	(Ω)

8. Efficiency of LDOs

The power supply efficiency can be calculated as follows:

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (8\text{-}1)$$

P_{IN}:	Input power	(W)
P_{OUT}:	Output power	(W)

P_{IN} and P_{OUT} can be calculated using Equation 8-2 and Equation 8-3, respectively. CMOS LDOs have very small quiescent current (I_B). Therefore, when $I_{OUT} \gg I_B$, I_B may be ignored as shown by Equation 8-4. In that case, the input current (I_{IN}) and the output current (I_{OUT}) can be considered equal.

$$P_{IN} = V_{IN} \times (I_{IN} + I_B) \quad (8\text{-}2)$$

$$P_{OUT} = V_{OUT} \times I_{OUT} \quad (8\text{-}3)$$

$$P_{IN} \approx V_{IN} \times I_{IN} \quad (\because I_{OUT} \gg I_B) \quad (8\text{-}4)$$

V_{IN}:	Input voltage	(V)
I_{IN}:	Input current	(A)
I_B:	Quiescent current	(A)
V_{OUT}:	Output voltage	(V)
I_{OUT}:	Output current	(A)

Suppose that I_{OUT} » I_B. Then, substituting Equations 8-3 and 8-4 into Equation 8-1, we obtain:

$$\eta = \frac{V_{OUT}}{V_{IN}} \quad (8\text{-}5)$$

Hence, the LDO efficiency can be calculated as the ratio of input voltage to output voltage.

For more detailed calculation of LDO efficiency and how to improve it, see Dual power supply LDO Regulators for Low Drop Out and Low Loss at low Voltage.

To download the application note above → Click Here

9. Calculating the power dissipation and junction temperature of an LDO

9.1. Calculating power dissipation

The power dissipation (P) of an LDO can be calculated by Equation 9-1. The control current (I_{CT}) is negligible since it is much smaller than the quiescent current.

$$P = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_B \quad (9\text{-}1)$$

V_{IN}:	Input voltage	(V)
V_{OUT}:	Output voltage	(V)
I_{OUT}:	Output current	(A)
I_B:	Quiescent current when an LDO is on	(A)

Note: When I_{OUT} » I_B, the V_{IN} × I_B term can be ignored if it is very small.

For example, suppose that V_{IN} = 1.5 V, V_{OUT} = 1 V, I_{OUT} = 200 mA, and I_B = 20 μA. Then, an LDO's power dissipation (P) can be calculated as follows:

$$P = (1.5\,V - 1\,V) \times 0.2\,A + 1.5\,V \times 20 \times 10^{-6}\,A$$

$$= 100.03\,mW$$

$$\approx 100\,mW$$

9.2. Calculating the junction temperature

The junction temperature (T_j) of an LDO can be calculated by Equation 9-2:

$$T_j = P \times R_{th(j-a)} + Ta \quad (9\text{-}2)$$

If $R_{th(j\text{-}a)}$ is not shown in the datasheet, it can be calculated by Equation 9-3 from power dissipation (P_D) and junction temperature (T_j):

$$R_{th(j-a)} = \frac{T_{j(\max)} - T_a}{P_{D(\max)}} \quad (9\text{-}3)$$

$$= \frac{150 - 25}{P_D} \quad (9\text{-}4)$$

P:	Power dissipation of an LDO	(W)
$R_{th(j\text{-}a)}$(Note):	Junction-to-ambient thermal resistance	(°C/W)
$T_{j(max)}$:	Maximum rated junction temperature specified in the datasheet (150°C)	(°C)
$P_{D(max)}$(Note):	Maximum rated power dissipation under the board conditions specified in the datasheet	(W)
T_a:	Ambient temperature at which the absolute maximum ratings are specified in the datasheet (25°C)	(°C)

Note: $R_{th(j-a)}$ and P_D depend on the board size, mounting area, and metal thickness.

Suppose that the power dissipation is roughly 100 mW as calculated in Section 9.1. Also suppose that P_D = 0.6 W and T_a = 60°C. Then, from Equations 9-2 and 9-4, the junction temperature can be calculated as follows:

$$T_j = 0.1\,W \times \frac{150\,°C - 25\,°C}{0.6\,W} + 60\,°C$$

$$\approx 80.8\,°C \quad (9\text{-}5)$$

For more details on thermal design, see Concept of self-heating of LDOs and selection guide.
To download the application note above→ Click Here

10. LDO oscillation and countermeasures

The negative feedback loop of an LDO consists of output voltage-sensing resistors (feedback resistors R_1 and R_2), an error amplifier, a reference voltage source, and a MOS output transistor as shown in Figure 10.1.

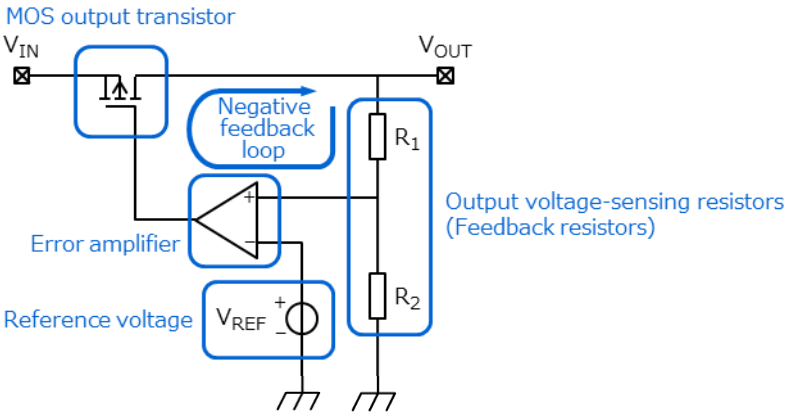


Figure 10.1 Negative feedback loop of an LDO

The negative feedback loop includes time-delay circuits consisting of capacitors (C) and resistors (R). The primary time-delay circuit has a pole at $f_p = \frac{1}{2\pi CR}$. Phase rotation begins at a frequency one order of magnitude lower than f_p, reducing the gain at the rate of 20 dB per decade. The phase rotates by 45° at f_p and eventually by 90°. Therefore, in the secondary time-delay circuit consisting of two stages of CR, the gain decreases at the rate of 40 dB per decade, causing 180° phase rotation. At this time, a gain greater than 0 dB results in positive feedback, causing oscillation.

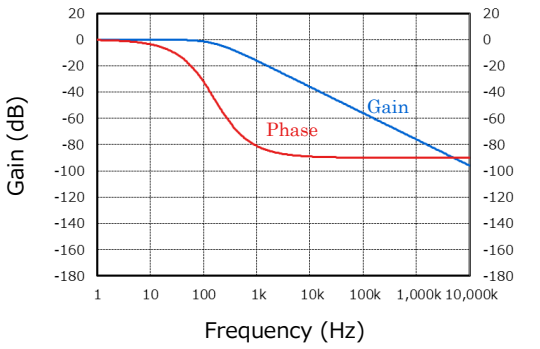


Figure 10.2 Gain and phase of the primary time-delay circuit

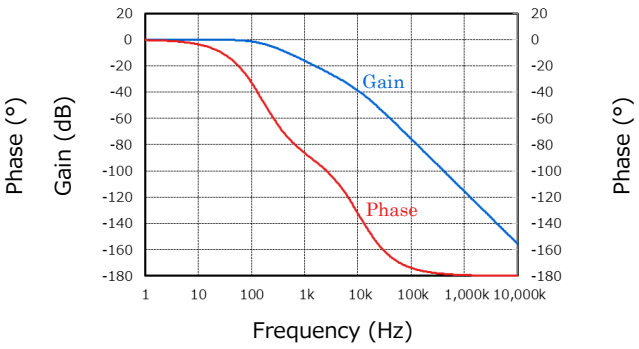


Figure 10.3 Gain and phase of the secondary time-delay circuit

Generally, an error amplifier provides phase compensation and therefore has a single pole.

(1) LDOs with a P-channel MOS output transistor

The drain of the P-channel MOS output transistor is connected to the V_{OUT} pin. The drain resistance of the MOS output transistor is calculated as $r_{DS} = \Delta V_{DS} / \Delta I_D$ as shown in Figure 10.1. Therefore, r_{DS} is relatively high. A pole is generated at the V_{OUT} pin by the drain resistance (r_{ds}), feedback resistor values, and the capacitance and equivalent series resistance of the output capacitor. The pole frequency changes depending on the load conditions. The pole of the V_{OUT} pin is close to that of the error amplifier. Unless the gain becomes lower than 0 dB when the phase rotates by 180°, an LDO goes into oscillation.

(2) LDOs with an N-channel MOS output transistor

The drain of the N-channel MOS output transistor is common drain. Therefore, LDOs with an N-channel MOS output transistor have lower output impedance than those with a P-channel MOS output transistor. As a result, a pole is generated at the V_{OUT} pin at high frequency. This means the pole of the error amplifier is far away from the pole generated at the V_{OUT} pin, making LDOs with an N-channel MOS output transistor less susceptible to oscillation than those with a P-channel MOS output transistor.

To verify system safety, evaluate LDOs, including their neighboring devices, taking into consideration the worst-case conditions for input voltage, output voltage, output current, operating temperature, etc.

If LDOs are found to oscillate, the following measures can be taken to prevent LDO oscillation:

(a) Using the ESR of the output capacitor

All capacitors have equivalent series resistance (ESR). Introduce a zero at $f_z = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$ using the ESR and capacitance of the output capacitor to rotate back the phase in order to make an LDO less susceptible to oscillation.

(b) Using a feedback output capacitor (C_{FB})

For adjustable-output-voltage LDOs, the voltage at the midpoint of two external resistors is applied to the internal error amplifier to set the output voltage. As is the case with the above method, a zero can be introduced at $f_z = \frac{1}{2\pi \times C_{FB} \times R_1}$ by connecting a feedback capacitor in parallel with the upper resistor (R_1 in Figure 10.4). In addition, the feedback capacitor helps increase the ripple rejection ratio and reduce noise.

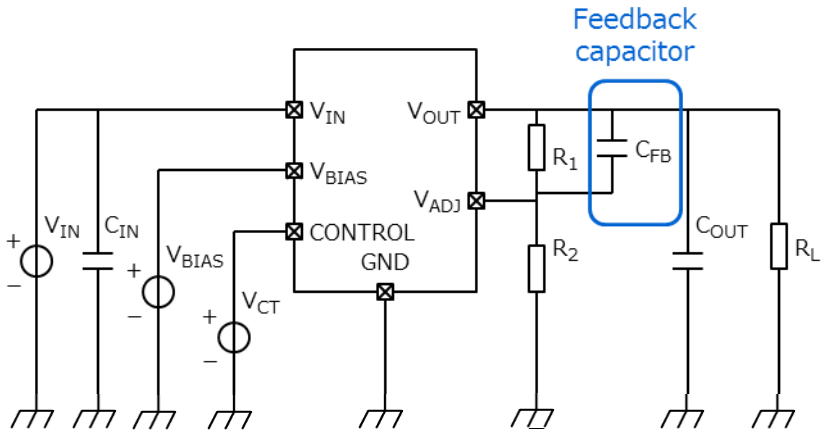


Figure 10.4 Feedback capacitor with adjustable output voltage

For more details on oscillation, see Oscillation Principles and Improvement of Oscillation Resistance of LDO.

To download the application note above→ Click Here

11. Protection against reverse biasing of input and output

If the output voltage of an LDO becomes higher than its input voltage, current flows in the reverse direction from the output capacitor to the LDO, degrading or destroying the LDO. If this could occur, connect a bypass diode between the V_{IN} and V_{OUT} pins as shown in Figure 11.1 or add a reverse-current blocking diode between a power supply and the V_{IN} pin as shown in Figure 11.2.

When you use a reverse-current blocking diode, exercise care as to a voltage drop due to the diode's forward voltage (V_F) in order to ensure that the LDO operates properly over the input voltage range. A diode with low forward voltage and leakage current should be selected, taking the derating of reverse-bias voltage and forward current into consideration.

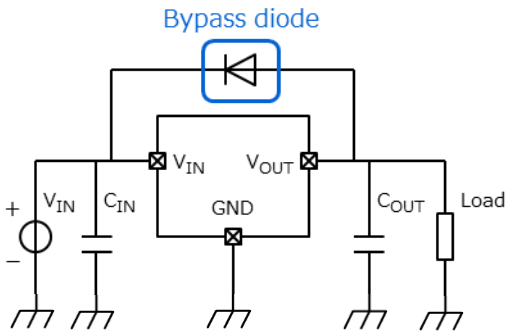


Figure 11.1 Reverse-current protection using a bypass diode

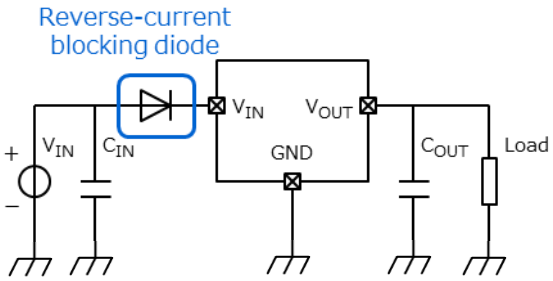


Figure 11.2 Reverse-current protection using a reverse-current blocking diode

When using Schottky barrier diodes (SBDs) for the bypass and reverse-current blocking diodes, select low-leakage SBDs, ensuring sufficient margins for the withstand voltage.

To perform a parametric search of low-leakage SBDs → Click Here

12. Conclusion

This application note has discussed electrical characteristics and protection features of LDOs as well as other basics described in their datasheets. LDOs are one of the easy-to-use power supply ICs. Toshiba provides various LDOs, including low-dropout, physically small, high-PSRR, and low-power-consumption LDOs. We hope that you have found this application note useful in considering the use of Toshiba's LDOs.

To visit a web page on LDOs → Click Here

13. Related Links

- ■ Product Line Ups (Catalog) — Click
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