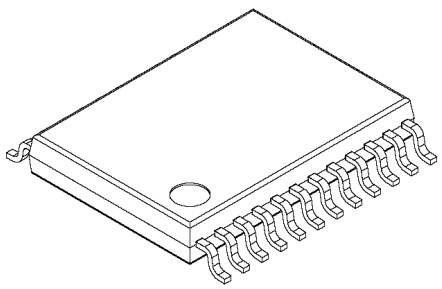
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

# TB9067FNG

Automotive 3-Phase Brushless Motor Pre-Driver



SSOP24-P-300-0.65A

Weight: 0.14 g (typ.)

The TB9067FNG is an automotive three-phase brushless DC motor pre-driver incorporating a 120-degree commutation decoding logic.

## Features

- 3-phase 120-degree rectangular commutation control
- PWM chopper control
- External P-channel/N-channel MOS drive output (3 phases with 6 outputs)
- Internal PWM drive/external direct drive (selectable)
- PWM pulse input control/DC level input control (selectable)
- Forward/Reverse switch capability
- Low-side driver output PWM control
- Overcurrent protection: double detection (current limiter/overcurrent detection)
- 5.12-MHz oscillator
- 5-V regulated voltage
- Operating temperature range: −40 to 125°C
- Compact flat package: 24-pin SSOP (0.65-mm pitch)
- The product(s) is/are compatible with RoHS regulations (EU directive 2011 / 65 / EU) as indicated, if any, on the packaging label ("[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)]]", "RoHS COMPATIBLE" or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV").

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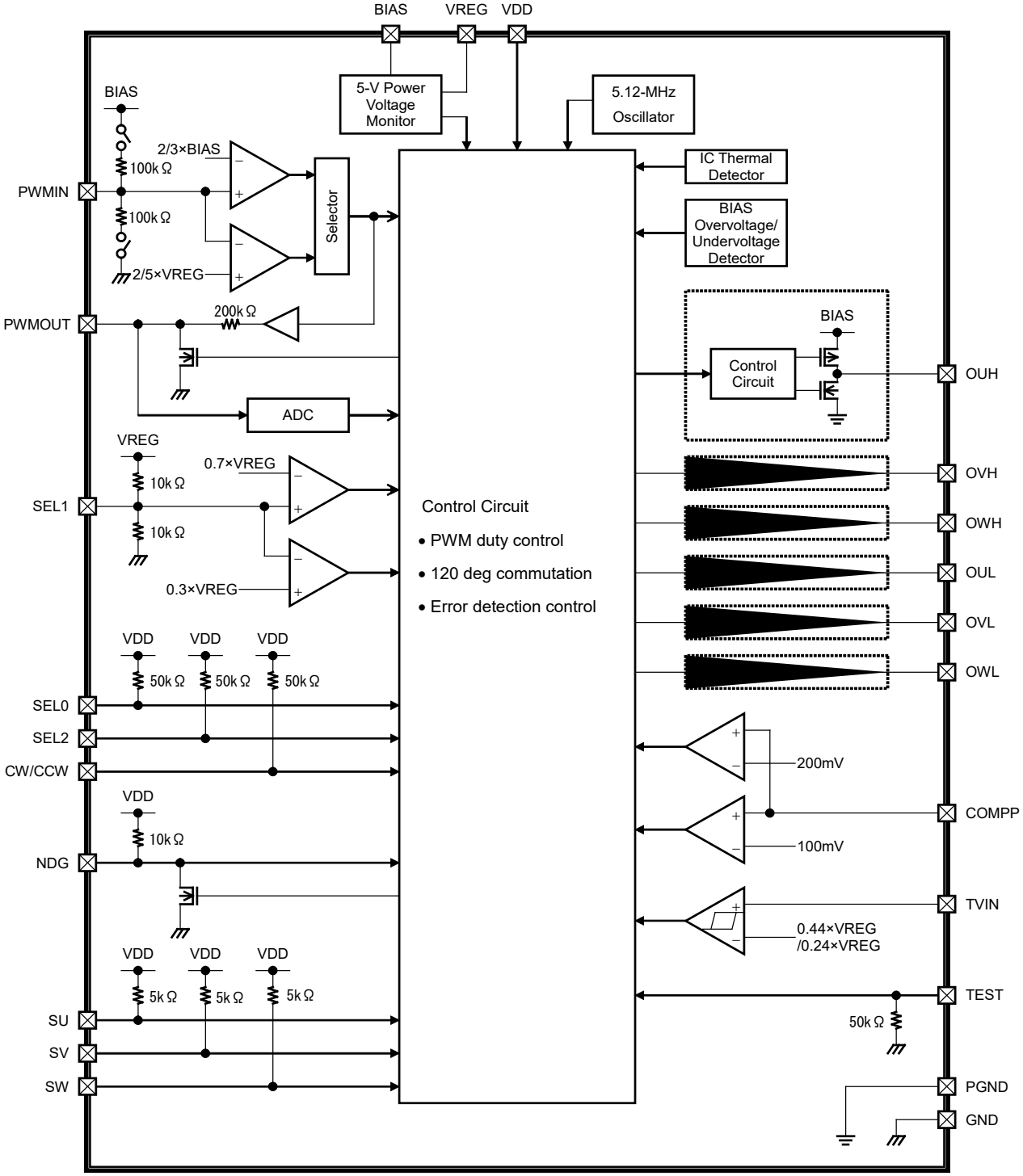
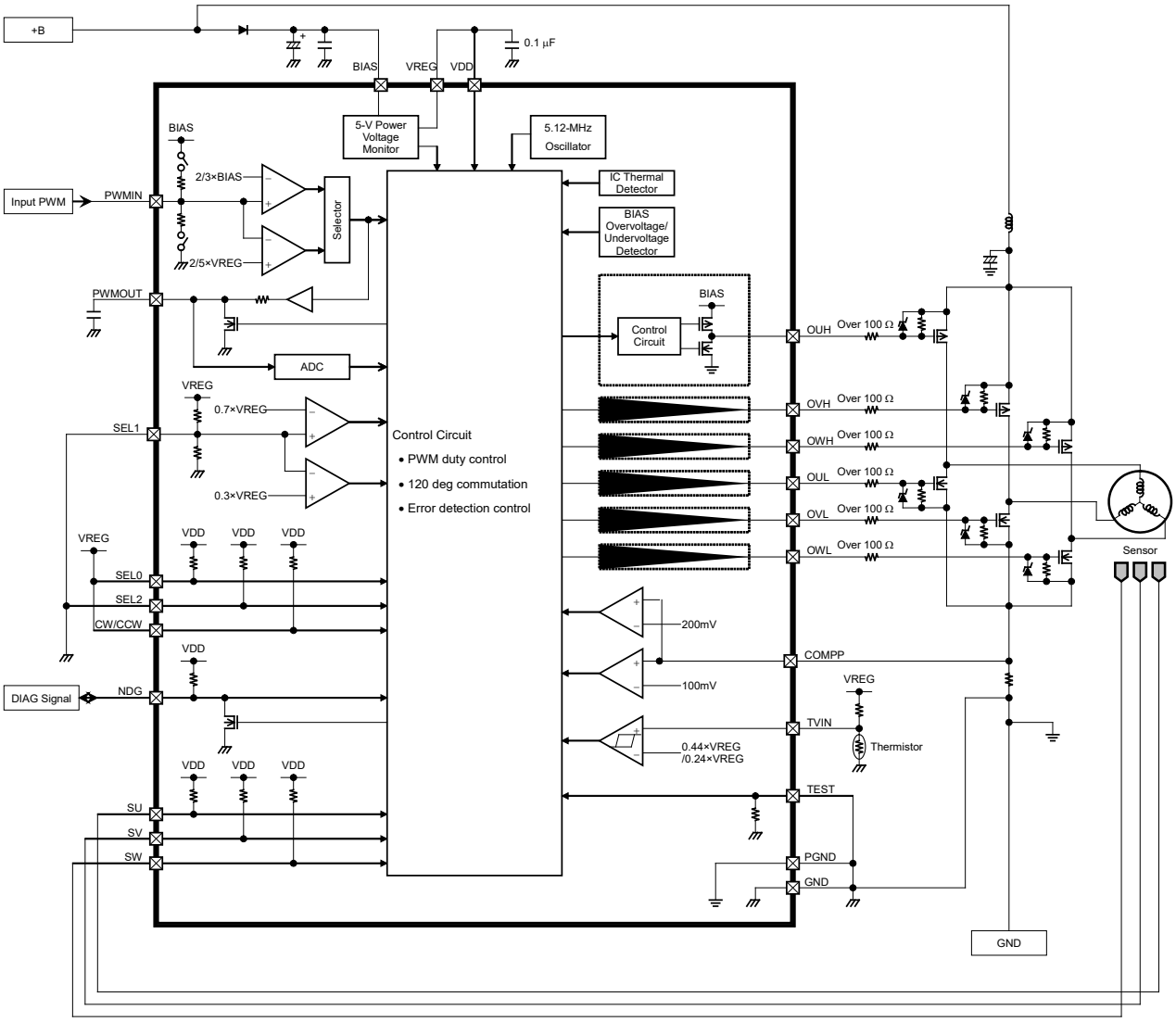
## Block Diagram




Note: In the block diagram, part of the functional blocks or constants may be omitted or simplified for explanatory purposes.

## Application Circuit Example (Operating Mode 1)




Note: In the application circuit example, part of the functional blocks or constants may be omitted or simplified for explanatory purposes.

Note: Ensure that the IC is mounted correctly as specified. Failing to observe the correct mounting procedure or requirements may damage the IC or target equipment.

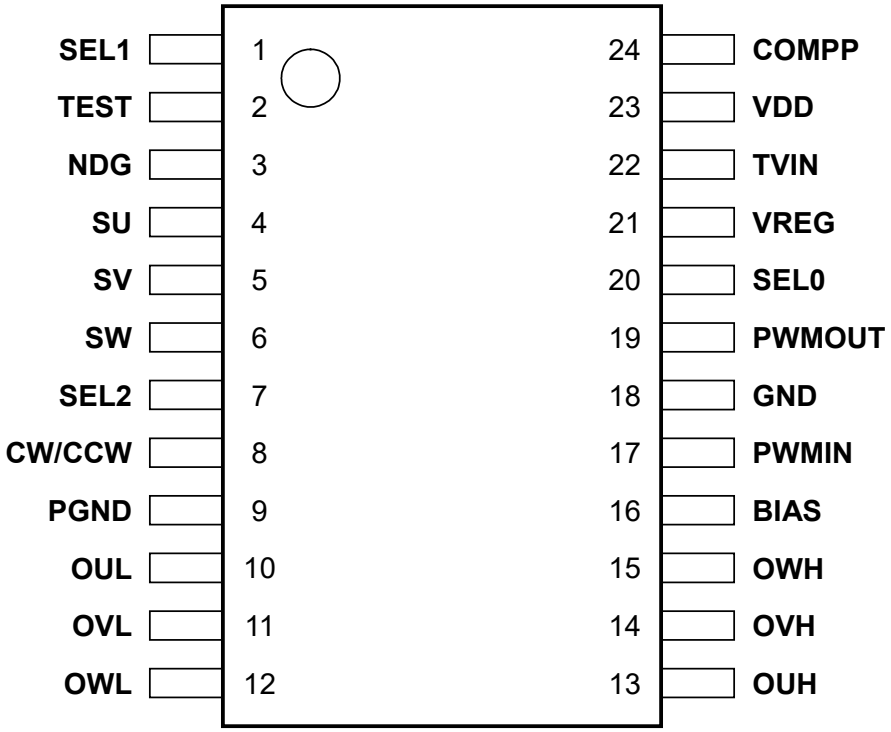
Note: The capacitor connected to the Source pin of the Pch FET is for absorbing disturbance noise, voltage fluctuation by load change, etc. Connect it as close to the Source pin of the Pch FET as possible.

Note: The application circuit shown above is not intended to guarantee mass production. A thorough evaluation is required when designing an application circuit for mass production.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

Note: Utmost care is necessary in the design of the output OUTXX, VB ,VDD and GND lines since the IC may be destroyed in case of a short-circuit across outputs, a short-circuit to power supply, or a short-circuit to ground.

Note: Please use to make a short both VREG and VDD always.
Possibly make a malfunction to potential difference occurs between VREG and VDD.

**Pin Assignment**



## Pin Description

| Pin No. | Symbol | Pin Description |
|---|---|---|
| 1 | SEL1 | Operating mode setting input<br>Low: Mode 1<br>Middle: Mode 2 (including the open state of the pin)<br>High: Mode 3 |
| 2 | TEST | Test mode select input (must be shorted to GND in normal operation)<br>Low: User mode<br>High: Test mode |
| 3 | NDG | Error monitor output/forced off input<br>[Output]<br>Low: Error detected<br>High: Normal state<br>[Input]<br>Low: Pre-driver is forcibly turned off (fixed to High/Low)<br>High: Don't care |
| 4 | SU | U-phase sensor signal input |
| 5 | SV | V-phase sensor signal input |
| 6 | SW | W-phase sensor signal input |
| 7 | SEL2 | Start mode setting input (for the operating mode 1 or 3)<br>Low: Rapid start<br>High: Slow start (normal speed)<br><br>Motor rotation direction setting input (for the operating mode 2)<br>Low: Two-wire control mode<br>High: Single-wire control mode |
| 8 | CW/CCW | Rotation direction control *For additional information, see Chapter 2. Pre-Driver Output Waveforms<br>Low: Reverse<br>High: Forward |
| 9 | PGND | Pre-driver power ground (must be shorted to the GND pin externally) |
| 10 | OUL | U-phase output pin of the low-side pre-driver |
| 11 | OVL | V-phase output pin of the low-side pre-driver |
| 12 | OWL | W-phase output pin of the low-side pre-driver |
| 13 | OUH | U-phase output pin of the high-side pre-driver |
| 14 | OVH | V-phase output pin of the high-side pre-driver |
| 15 | OWH | W-phase output pin of the high-side pre-driver |
| 16 | BIAS | Bias voltage |
| 17 | PWMIN | PWM signal input |
| 18 | GND | IC ground (except for the pre-drivers) |
| 19 | PWMOUT | PWM signal output/DC data input |
| 20 | SEL0 | Full drive enable/disable where PWMIN = Low<br>Low: Enable<br>High: Disable |
| 21 | VREG | 5-V regulated voltage |
| 22 | TVIN | Input signal for monitoring the external analog voltage (high input voltage causes an error detection to be occurred) |
| 23 | VDD | Power supply for the internal logic IC (must be shorted to VREG externally) |
| 24 | COMPP | Input signal for monitoring the external motor driver current (any error is detected if the input marks high voltage) |

## Functional Description

### 1. Basic Operation

The PWM signal is applied to the TB9067FNG as a command signal. The output PWM signal duty cycle generated from the said input PWM activates the three-phase motor driver.

According to the output PWM types, the TB9067FNG has the two drive modes: the internal PWM drive mode and the external direct drive mode. The input PWM signal has the following characteristics ranges:

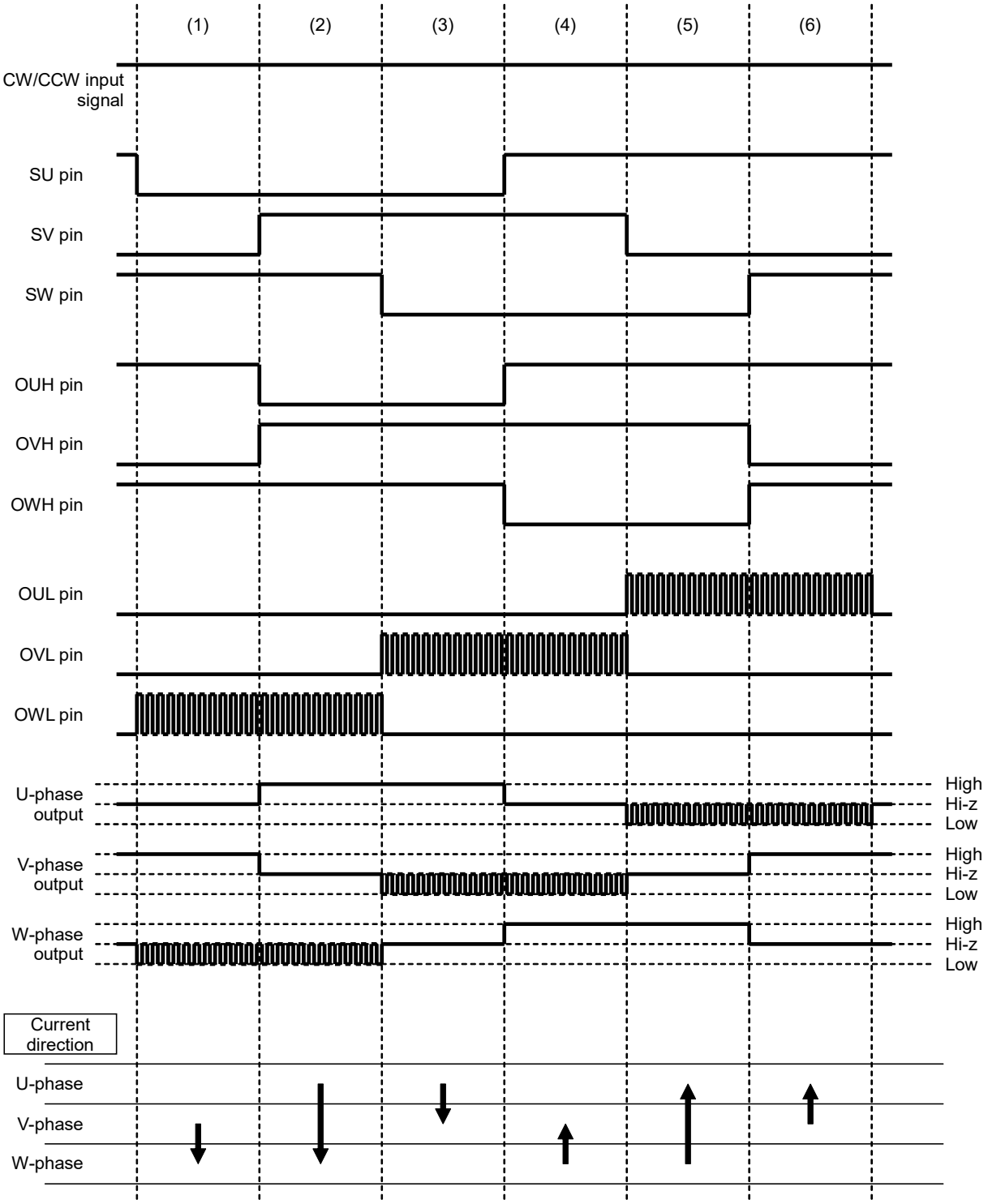
- Frequency: Up to 4 kHz (for internal PWM drive)
  Up to 23 kHz (for external direct drive)
- PWM duty: 0 to 100%
- Voltage amplitude: 0 V to bias voltage

The output PWM signal generated from the input PWM signal is sent out from the pre-drivers according to the sensor signal from the motor. This runs the three-phase brushless motor.

## Functional Description

### 2. Pre-Driver Output Waveforms

(1) Forward rotation mode (CW/CCW input = High)

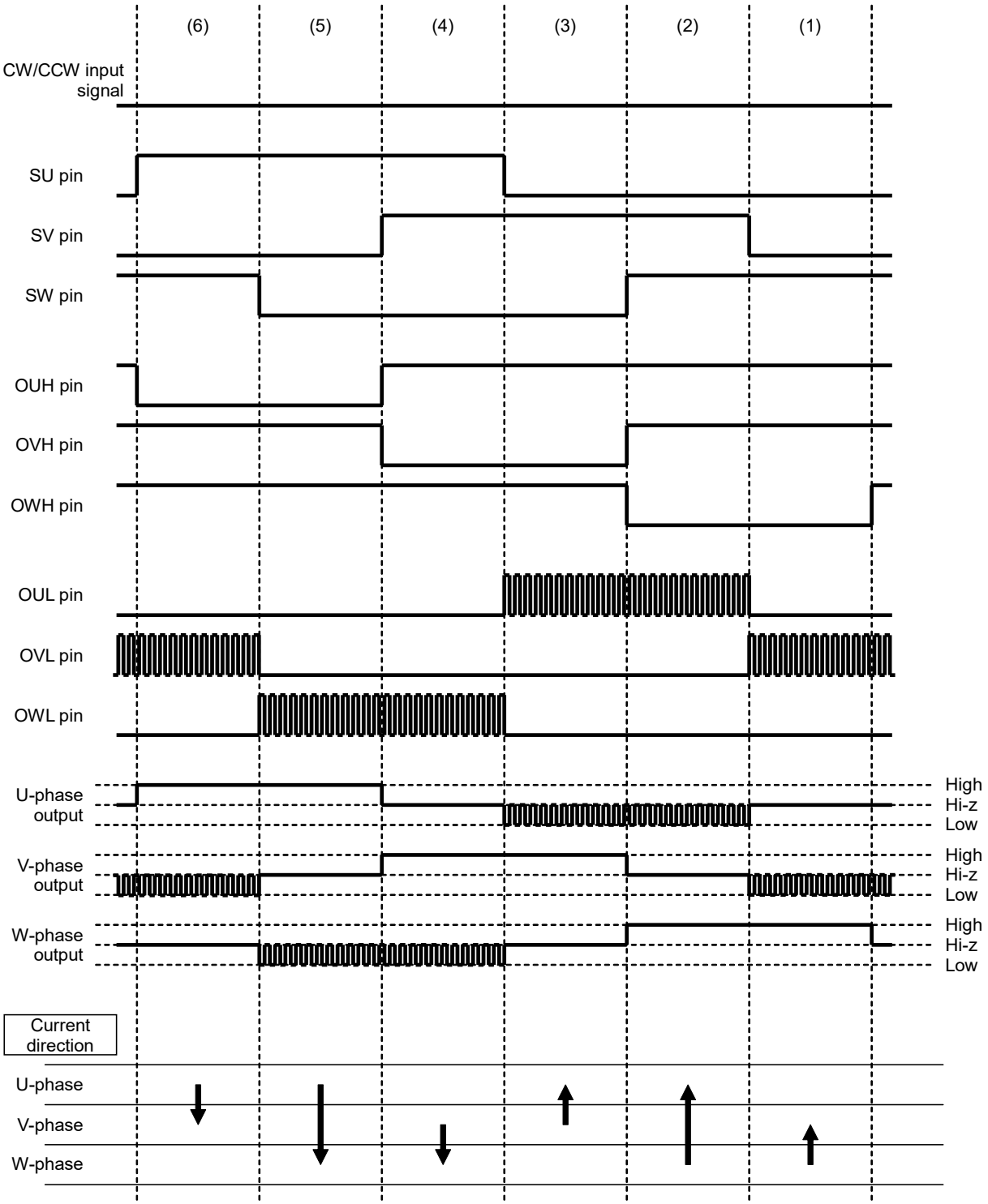



Note: If a combination of the sensor inputs is other than the combination shown above (i.e. all Low or all High), the motor driver is turned off (with the high-side pre-driver output = all High, low-side pre-driver output = all Low).

Note: Timing charts may be simplified to clarify the descriptions of features and operations.

## Functional Description

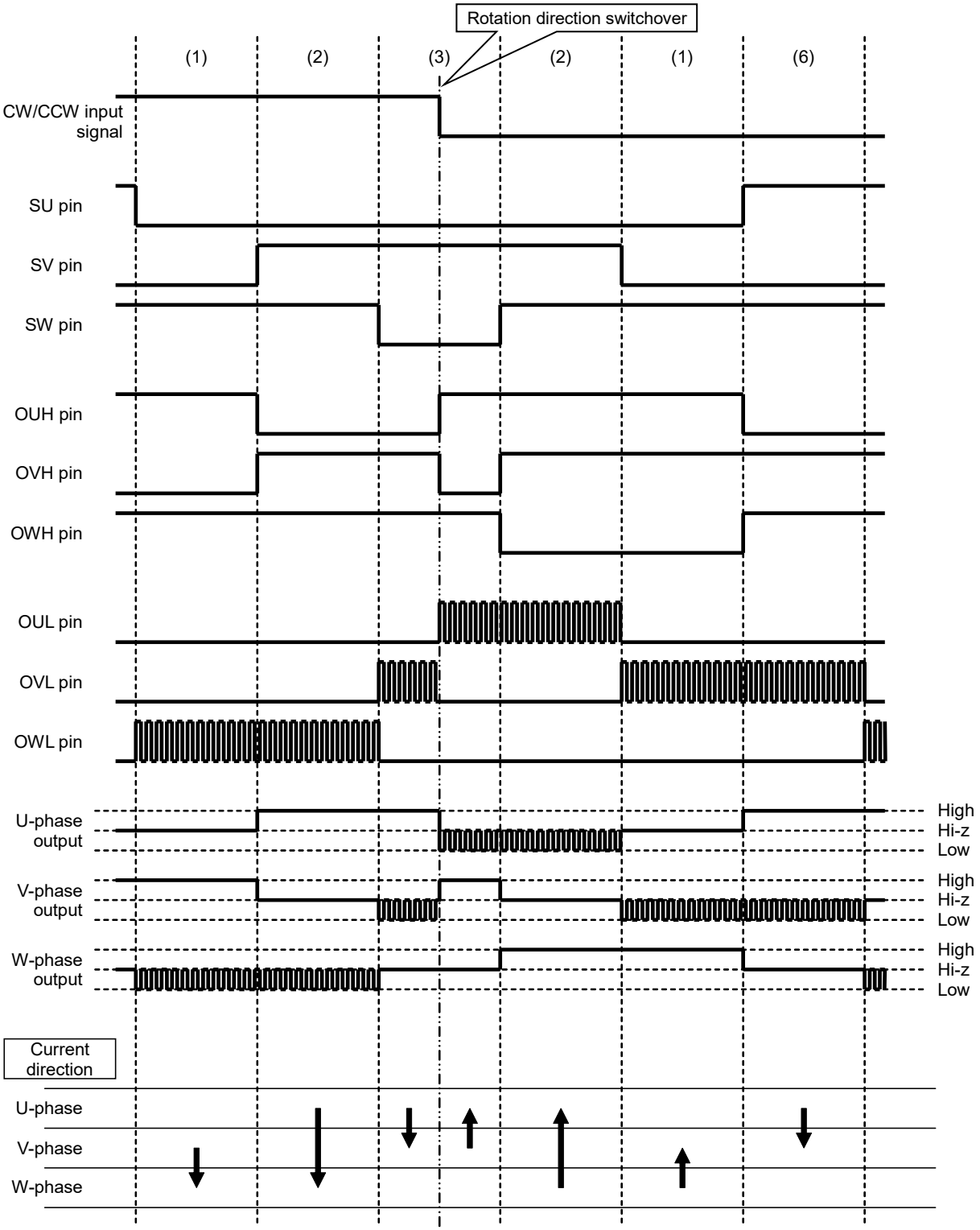
(2) Reverse rotation mode (CW/CCW input = Low)




Note: Timing charts may be simplified to clarify the descriptions of features and operations.

## Functional Description

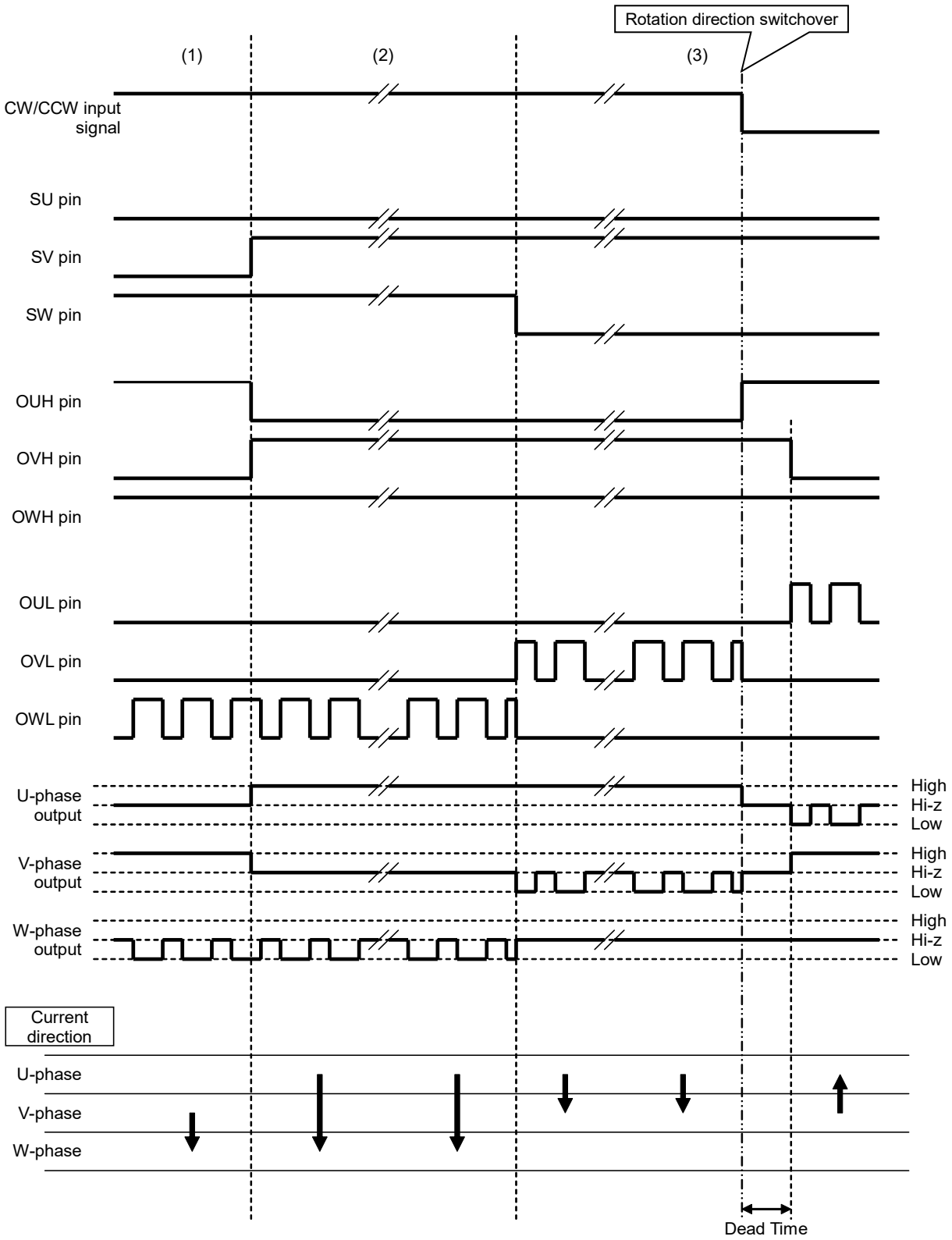
(3) Rotation direction switchover (CW/CCW input = High to Low)




Note: Timing charts may be simplified to clarify the descriptions of features and operations.

## Functional Description

(4) Rotation direction switchover (detailed timing chart)




Note: Timing charts may be simplified to clarify the descriptions of features and operations.

# Functional Description

## 3. Operating Modes

The SEL1 pin and SEL2 pin serve to control the TB9067FNG operating mode setting.

The operating mode is classified into two drive modes as shown below. Each of these two modes is further classified into the two operating modes with the different types of control.

### 3.1 Internal PWM Drive Mode

According to the input PWM duty applied through the PWMIN pin, a PWM waveform is internally generated and sent out from the pre-drivers. The generated PWM waveform has a carrier frequency of 20 kHz typical.

The internal PWM drive mode has the two types of operating mode determined by the active level of the PWMIN input.

1) Operating mode 1 (active-Low)
The input voltages lower than the PWMIN input threshold (2/5 VREG typ.) are the active level in this mode. In operating mode 1, the PWMIN pin will provide a built-in pull-up resistor of 100 kΩ typical.

2) Operating mode 3 (active-High)
The input voltages higher than the PWMIN input threshold (2/3 BIAS typ.) are the active level in this mode. In operating mode 3, the PWMIN pin will provide a built-in pull-down resistor of 100 kΩ typical.

### 3.2 External Direct Drive Mode

The input PWM waveform applied through the PWMIN pin is directly sent out from the pre-drivers. (This operating mode is hereinafter referred to as the Operating Mode 2.)

The operating mode 2 provides the two different ways of controlling the pre-driver ON duty and the rotation direction, according to the input modes.

1) Single-wire control
A PWM duty configuration signal superimposed with motor rotation direction information is applied on the PWMIN pin. The pre-driver ON duty and the rotation direction are thereby determined through a single input. (In this mode, the CW/CCW pin configuration is disabled.)
The PWMIN pin in single-wire control mode will provide both a built-in pull-up resistor of 100 kΩ typical and a built-in pull-down resistor of 100 kΩ typical.

2) Two-wire control
A PWM duty configuration signal is applied to the PWMIN pin while the motor direction control signal is applied to the CW/CCW pin. The pre-driver ON duty and the rotation direction are thereby controlled separately.
The PWMIN pin in this mode provides a built-in pull-up resistor of 100 kΩ typical.

**[Operating Modes]**

| Pin Configuration | | Operating Mode | | Output Frequency of the Pre-Driver | Motor Rotation Direction Control | Active Level of the PWMIN Pin | PWMIN Built-In Resistor |
|---|---|---|---|---|---|---|---|
| SEL1 | SEL2 | | | | | | |
| Low | — | Mode 1 | | Internally generated 20 kHz | Controlled by the CW/CCW input | 2/5 VREG or lower | Pull-up |
| Middle (Open) | High | Mode 2 | Single-wire control | PWMIN pin Direct | Internally generated from the PWMIN input | 2/5 VREG or lower and 2/3 BIAS or higher | Pull-up and pull-down |
| | Low | | Two-wire control | PWMIN pin Direct | Controlled by the CW/CCW input | 2/5 VREG or lower | Pull-up |
| High | — | Mode 3 | | Internally generated 20 kHz | Controlled by the CW/CCW input | 2/3 BIAS or higher | Pull-down |

Note: A hyphen ( — ) indicates Don't care (start mode select function)

## Functional Description

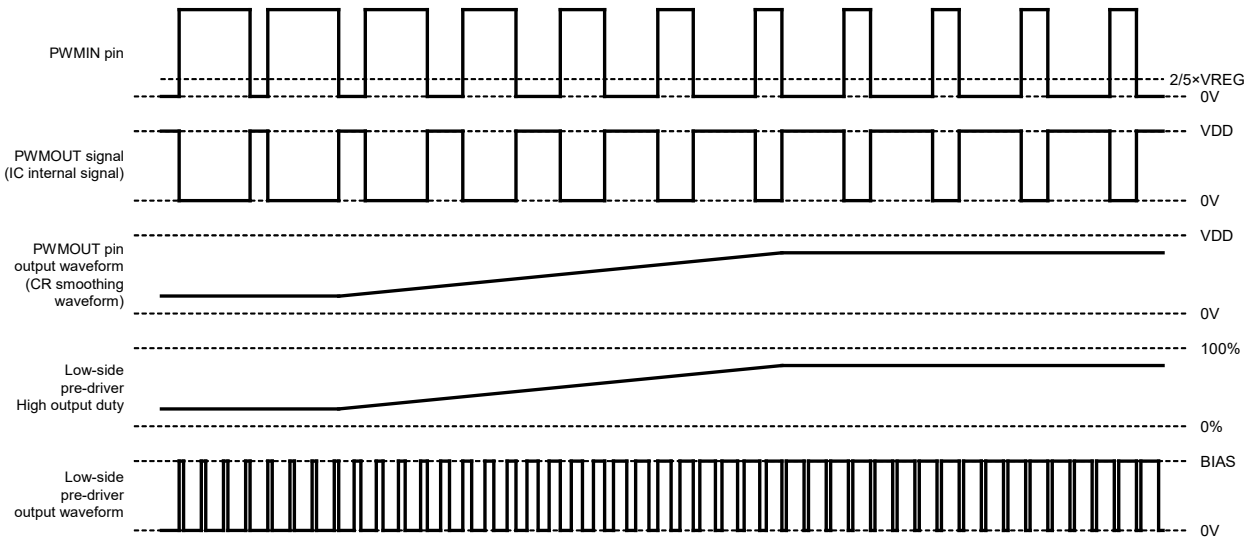
### 3.3 Details of Operating Modes

(1) Operating mode 1

From the Low level input duty of the PWM signal sent on the PWMIN pin, the TB9067FNG internally generates a carrier frequency of 20 kHz typical to run the pre-drivers (active-Low).

The PWM input signal sent on the PWMIN pin is inverted and sent out from the PWMOUT pin. The inverted data is smoothed by the built-in output resistor of 200 kΩ (typ.) at the PWMOUT pin and the external capacitor. The smoothed voltage is then taken into the AD converter and processed through the digital filter to determine the pre-driver ON duty (except for the rapid start mode).

Applying the DC voltage directly to the PWMOUT pin, too, allows the pre-driver ON duty control.



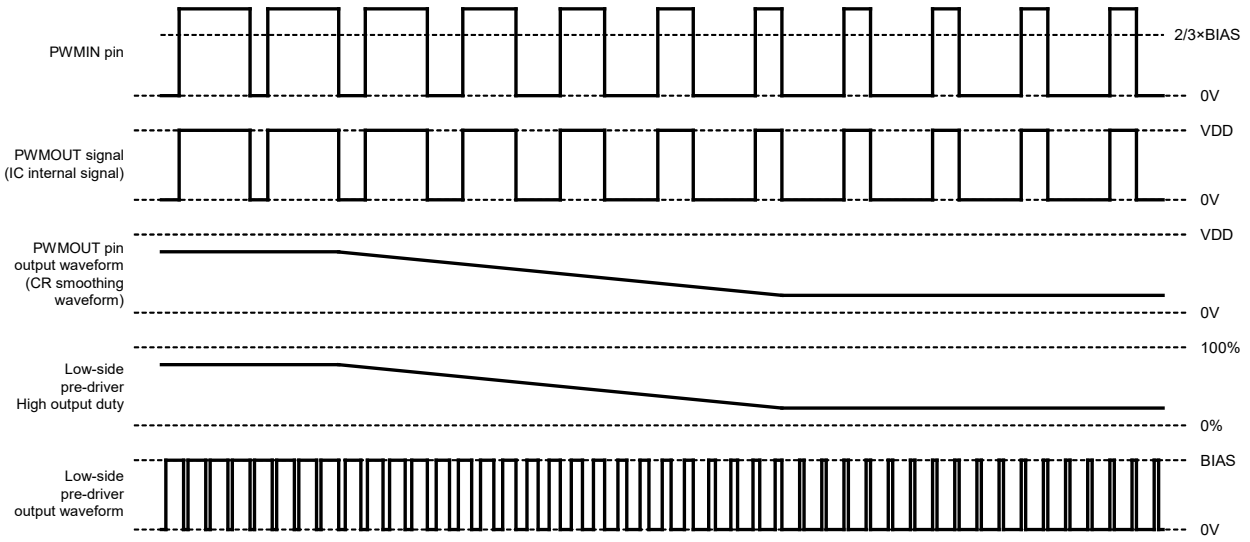

Note: Timing charts may be simplified to clarify the descriptions of features and operations.

(2) Operating mode 3

From the Low level input duty of the PWM signal sent on the PWMIN pin, the TB9067FNG internally generates a carrier frequency of 20 kHz typical to run the pre-drivers (active-High).

The PWM signal sent on the PWMIN pin is sent out on the PWMOUT pin in phase. The said signal is smoothed by the built-in output resistor of 200 kΩ (typ.) at the PWMOUT pin and the external capacitor. The smoothed voltage is then taken into the AD converter and processed through the digital filter to determine the pre-driver ON duty (except for the rapid start mode).

Applying the DC voltage directly to the PWMOUT pin, too, allows the pre-driver ON duty control.




Note: Timing charts may be simplified to clarify the descriptions of features and operations.

## Functional Description

(3) Operating mode 2

The PWM input sent on the PWMIN pin directly runs the pre-drivers in this mode. The pre-driver ON duty and output frequency depend on the said PWM input.

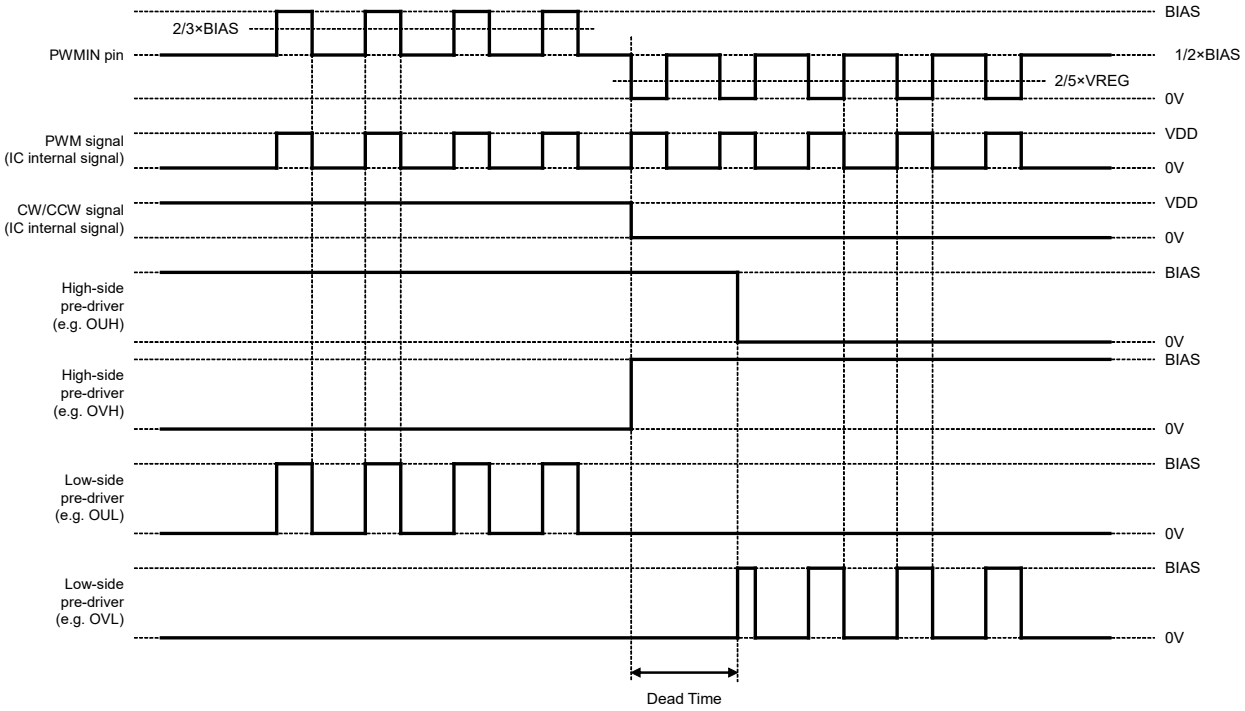
Besides, the TB9067FNG provides the two types of input mode (single- and two-wire controls), depending on how to control the motor rotation direction.

1) Single-wire control

The PWM waveform superimposed with two pieces of information; the pre-driver ON duty and the motor rotation direction, is sent on the PWMIN pin. The TB9067FNG runs the pre-drivers in accordance with each pulse of the High level input (more than 2/3 BIAS typ.) and Low level input (less than 2/5 VREG typ.) of the PWM wave.

The motor rotates forward when the High level input of the PWM wave is detected (like in the case that CW/CCW input = High) while it rotates in reverse direction when a Low level input of the PWM wave is detected (like in the case that CW/CCW input = Low). The CW/CCW pin input should be disabled.

Every time the motor rotation direction is changed, a dead time (50 μs typ.) is automatically inserted.




Note: Timing charts may be simplified to clarify the descriptions of features and operations.

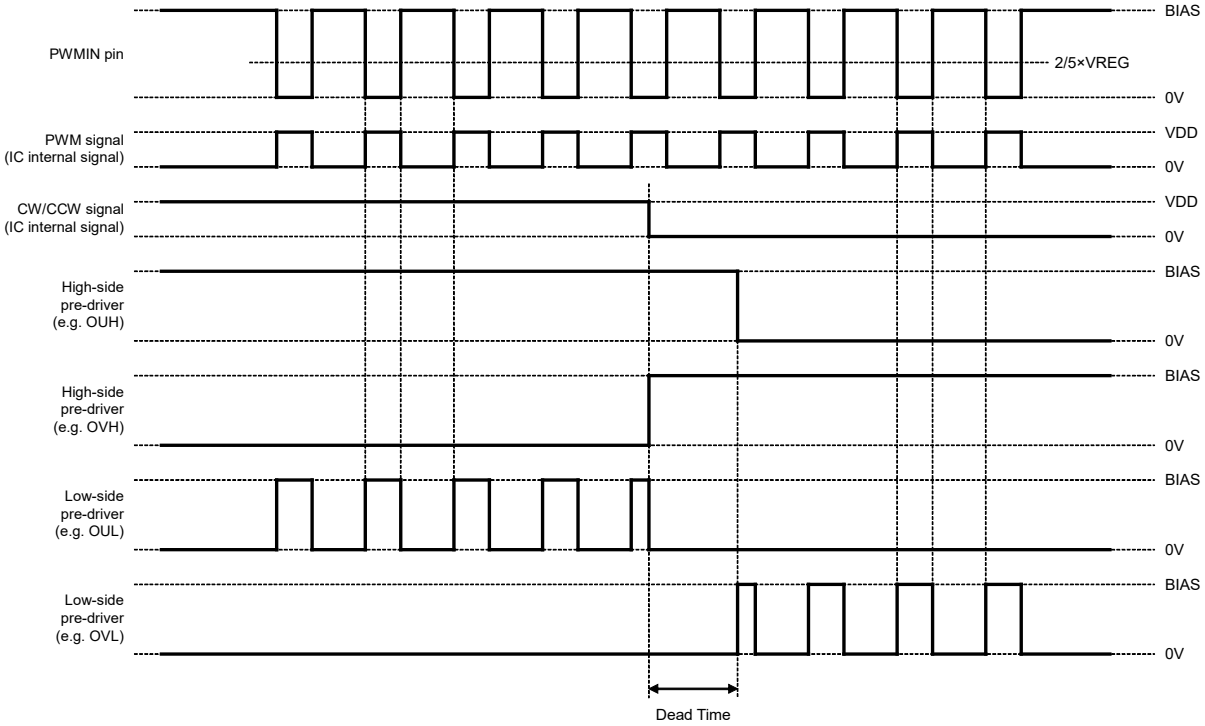
## Functional Description

2) Two-wire control

The pre-driver ON duty information and motor rotation direction information are separately sent in. The pre-driver ON duty is sent in as a PWM signal on the PWMIN pin. The PWM signal Low-level input (less than 2/5 VREG typ.) activates the pre-drivers (active-Low).

On the other hand, the motor rotation direction is configured using the CW/CCW pin.

Every time the motor rotation direction is changed, a dead time (50 μs typ.) is automatically inserted.




Note: Timing charts may be simplified to clarify the descriptions of features and operations.

# Functional Description

## 4. Function Configuration

The SEL0 and SEL2 pins serve to configure the following functions:

- Disabling the full drive (SEL0)
- Motor start mode setting (SEL2)

### 4.1 Disabling the Full Drive (SEL0)

Driving the SEL0 pin High allows disabling the full drive of the motor driver.

In order to protect the motor driver from the excessive PWM duty configuration due to the PWMIN pin destruction (like a grounding fault), the motor driver output gets forced off (with the high-side pre-driver output High, low-side pre-driver output Low) if more than 95% PWM duty (typ.) is applied to the PWMOUT pin.

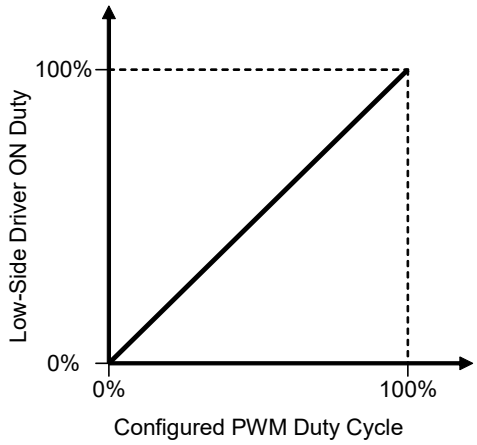
The motor driver resumes the output when the PWM duty cycle drops under 90%.

(For details, refer to 5-7. Full Drive Detection)

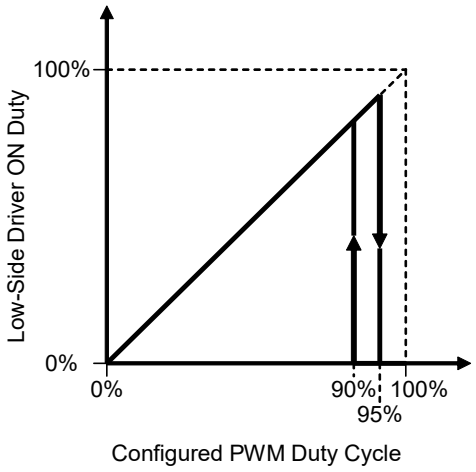
**[Full Drive Disable Configuration]**

| Pin Configuration<br>SEL0 | 100% Drive | Remarks |
|---|---|---|
| Low | Enable | |
| High | Disable | |

**SEL0 = Low**




**SEL0 = High**




Note: Characteristic charts may be simplified to clarify the descriptions of features and operations.

## Functional Description

### 4.2 Motor Start Mode Setting (SEL2)

Pulling the SEL2 pin Low allows the motor to start up in a precipitous curve (Rapid start).

If the SEL2 pin is driven Low upon power-on, a digital filter processing is eliminated for 0.3 sec (typ.) from a release of a detection of the low VREG voltage, and the data converted by the AD converter is thereby used as a PWM duty without being changed.

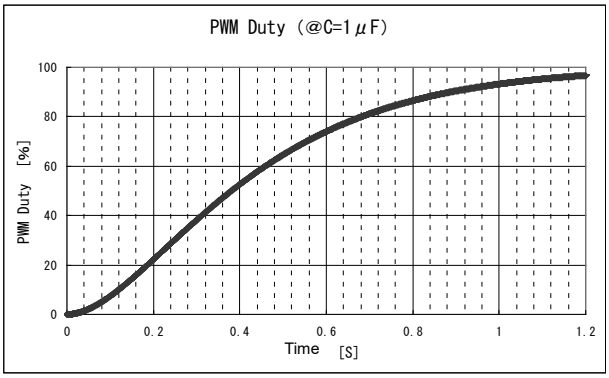
The combination of this capability and the external capacitor at the PWMOUT pin allows the start mode to be selected as shown in the figure below. Provided, however, that this function is available only in operating mode 1 and operating mode 3.

**[Start Mode Configurations]**

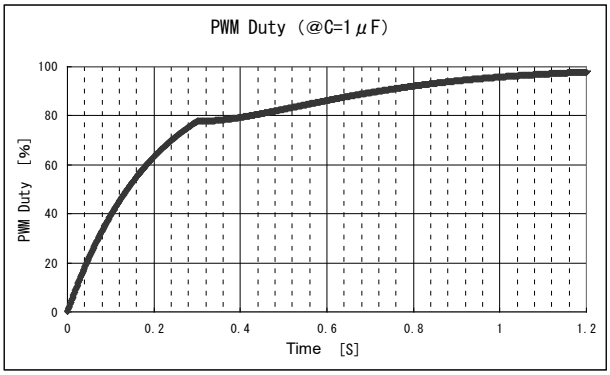
| Pin Configuration | | Operating Mode | Start Mode | Remarks |
|---|---|---|---|---|
| SEL1 | SEL2 | | | |
| Low | Low | Mode 1 | Rapid start | |
| | High | | Normal start | |
| Middle (Open) | Low | Mode 2 | — | Two-wire control where SEL2 = Low |
| | High | | (PWMIN Direct) | Single-wire control where SEL2 = High |
| High | Low | Mode 3 | Rapid start | |
| | High | | Normal start | |

Note:A hyphen ( — ) indicates“ Don’t care”

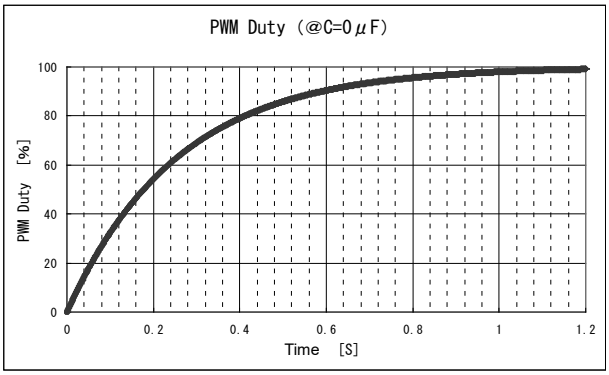
**SEL2 = High, Capacitance = 1 μF**



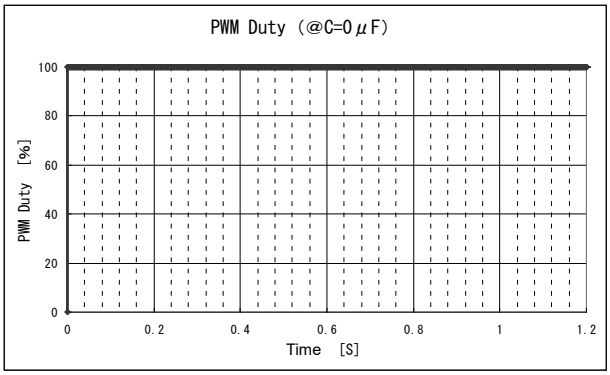

**SEL2 = Low, Capacitance = 1 μF**




**SEL2 = High, Capacitance = 0 μF**




**SEL2 = Low, Capacitance = 0 μF**




Note: The charts shown above present the theoretical figures for the PWMIN pin characteristics when the pin is fixed to High or Low (100% duty cycle). If the pulse input is used, the figures will change.
If pulses are applied to the PWMIN pin, smoothing by the external capacitor at the PWMOUT pin is required.

Note: Timing charts may be simplified to clarify the descriptions of features and operations.

## Functional Description

### 5. Error Detection Capability

The TB9067FNG provides the following eight error detection functions:

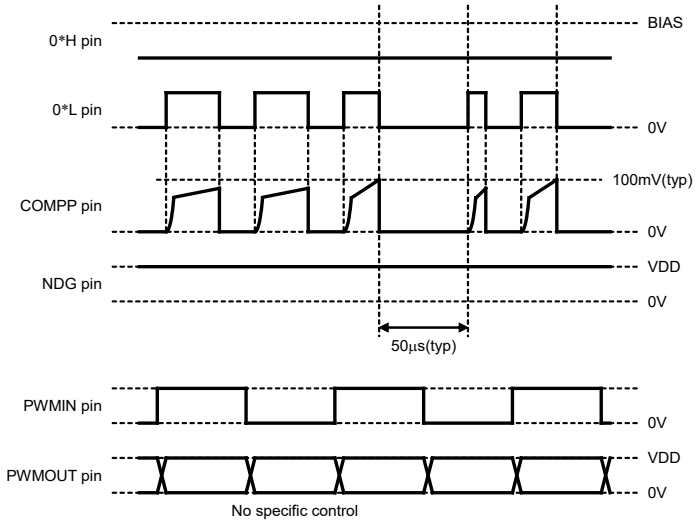
- External overcurrent detection for the motor driver
- External thermal detection for the motor driver
- IC thermal detection
- BIAS overvoltage detection
- BIAS undervoltage detection
- VREG undervoltage detection (5-V output)
- Full drive detection
- External forced off input

#### 5.1 External Overcurrent Detection for the Motor Driver

The external shunt resistor on the motor driver is monitored at its both ends by the COMPP pin to detect the overcurrent state of the motor driver.

The overcurrent detector has two levels of threshold. Their characteristics are as follows:

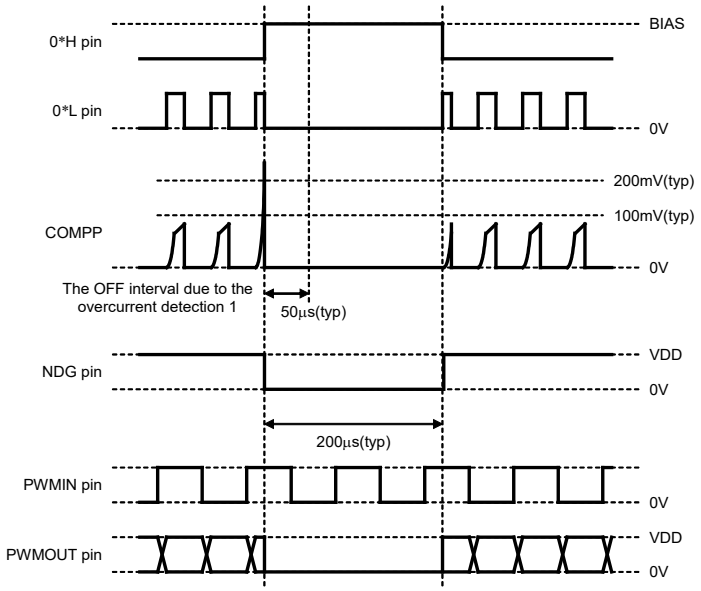
1) Overcurrent detection 1 (motor lock detection)
If once an overcurrent state (more than 100 mV typ.) is detected, the low-side driver gets forced off (the high-side pre-driver maintains its output state while the low-side pre-driver output is changed to Low). After the off state of 50 μs (typ.), the low-side driver resumes the output.
The noise filter mounted on the COMPP pin will be configured with 3 μs (typ.) for this function.

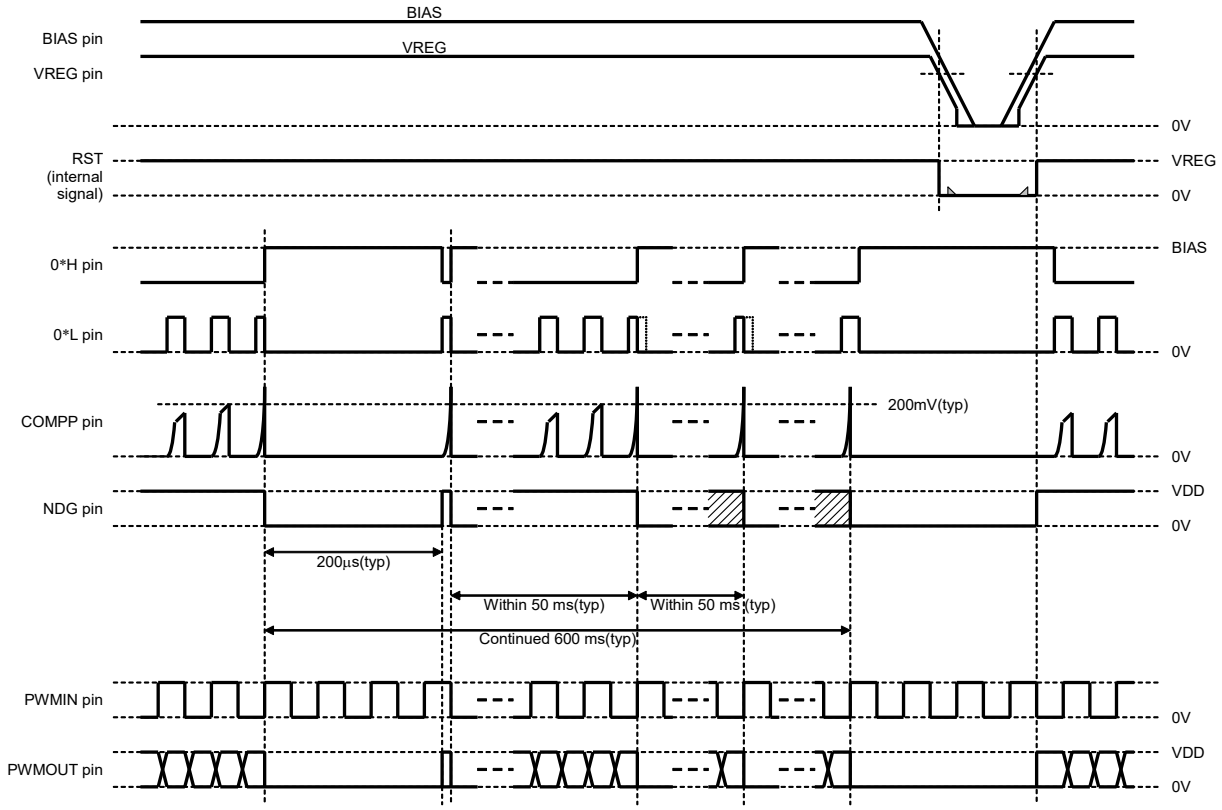



Note: Timing charts may be simplified to clarify the descriptions of features and operations

2) Overcurrent detection 2 (load short-circuit failure detection)
If once an overcurrent state (more than 200 mV typ.) is detected, both the high-side and low-side drivers get forced off (the high-side pre-driver output is changed to High while the low-side pre-driver output is changed to Low). After the off state of 200 μs (typ.), the drivers resume the outputs.
During the overcurrent detection 2, the PWMOUT pin is forcibly fixed to Low, and the NDG pin output is pulled Low.
If the overcurrent is repeatedly detected at intervals of within 50 ms (typ.), the state is recognized as one continuous overcurrent; and if this state continues for 0.6 sec (typ.), the motor driver output is fixed to off.
If the power voltage is turned off (upon undervoltage detection for VREG), the fixed off of the motor driver is released.
The noise filter mounted on the COMPP pin will be configured with 1 μs (typ.) for this function.

## Functional Description




Note: Timing charts may be simplified to clarify the descriptions of features and operations

## Functional Description

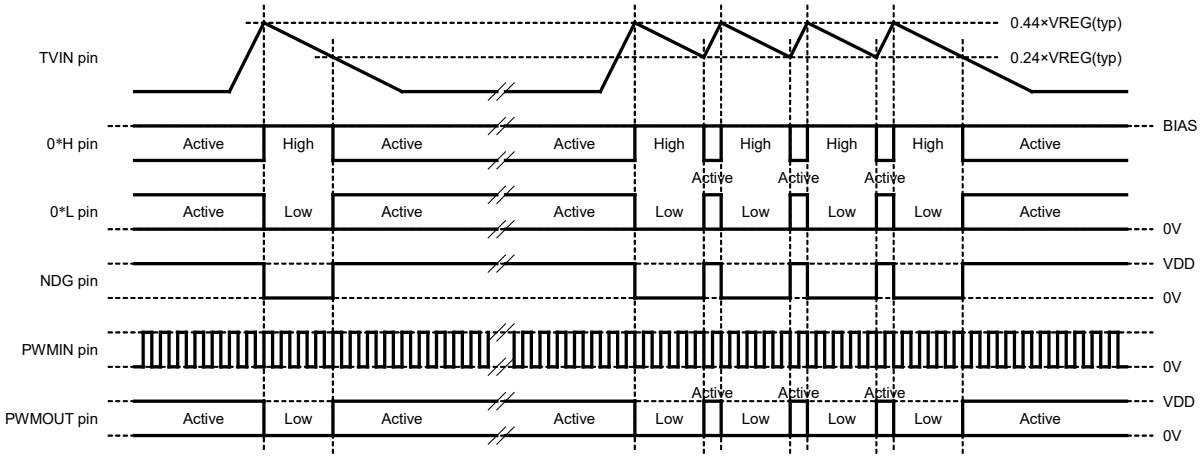
### 5.2 External Thermal Detection for the Motor Driver

The external thermistor on the motor driver is monitored by the TVIN pin to detect the overtemperature state of the motor driver.

Once the overtemperature (more than 0.44 VREG typ.) is detected, both the high-side and low-side drivers are turned off (the high-side pre-driver output is changed to High while the low-side pre-driver output is changed to Low). The drivers resume the outputs if the thermal detection is released due to the lowered temperature.

While the external thermal detection is running, the PWMOUT pin is fixed to Low, and the NDG pin output is pulled Low.

The TVIN pin has a noise filter of 10 μs (typ.).

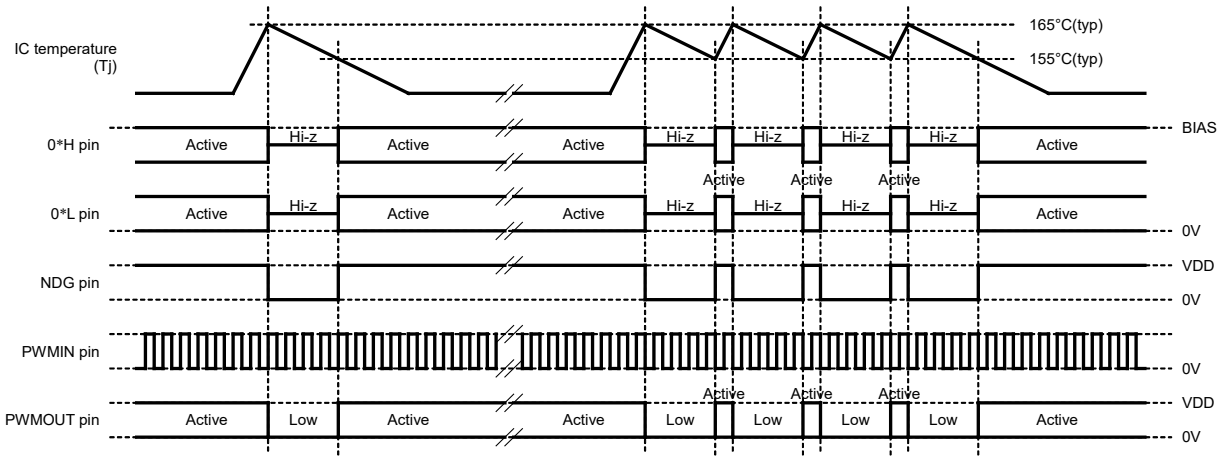



Note: Timing charts may be simplified to clarify the descriptions of features and operations

### 5.3 IC Thermal Detection

Once the overtemperature state (more than 165°C typ.) of the IC is detected, the drivers get turned off (the high- and low-side pre-drivers with Hi-z outputs). The drivers resume the outputs when the thermal detection is released due to the lowered temperature.

During the IC thermal detection, the PWMOUT pin is forcibly fixed to Low, and the NDG pin output is pulled Low.



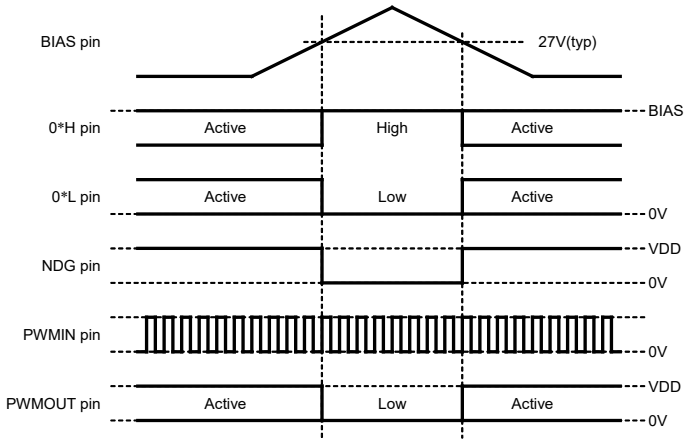

Note: Timing charts may be simplified to clarify the descriptions of features and operations

## Functional Description

### 5.4 BIAS Overvoltage Detection

If once the BIAS overvoltage (more than 27 V typ.) is detected, the drivers are turned off (the high-side pre-driver output is changed to High while the low-side pre-driver output is changed to Low). The drivers resume the outputs when the overvoltage detection is released.

During the BIAS overvoltage detection, the PWMOUT pin is forcibly fixed to Low, and the NDG pin output is pulled Low.

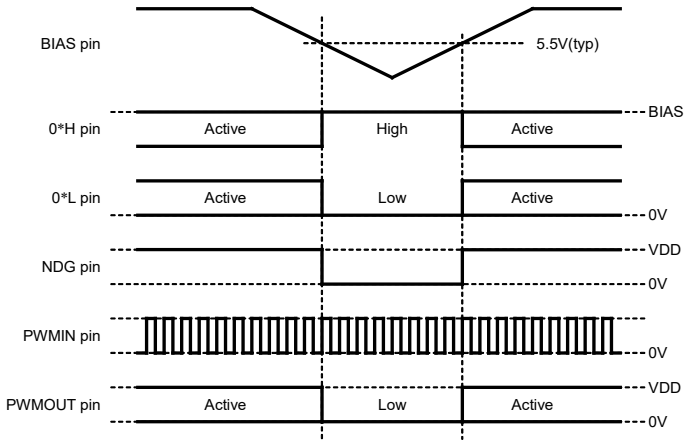



Note: Timing charts may be simplified to clarify the descriptions of features and operations

### 5.5 BIAS Undervoltage Detection

If once the BIAS undervoltage (less than 5.5 V typ.) is detected, the drivers are turned off (the high-side pre-driver output is changed to High while the low-side pre-driver output is changed to Low). The drivers resume the outputs when the undervoltage detection is released.

During the BIAS undervoltage detection, the PWMOUT pin is forcibly fixed to Low, and the NDG pin output is pulled Low.



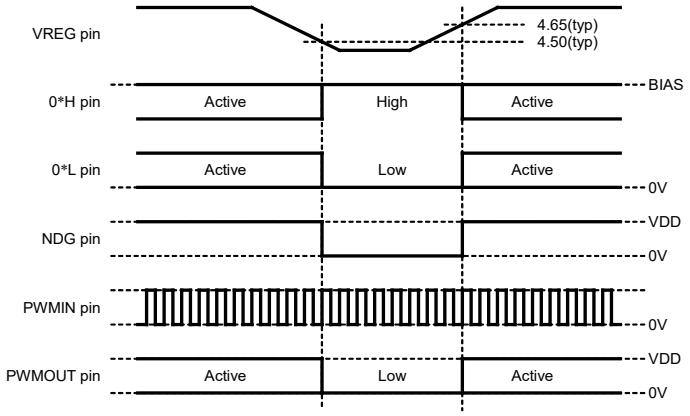

Note: Timing charts may be simplified to clarify the descriptions of features and operations

## Functional Description

### 5.6 VREG Undervoltage Detection (5-V output)

If once the VREG undervoltage (less than 4.5 V typ.) is detected, the control logic is initialized, and the drivers are turned off (the high-side pre-driver output is changed to High while the low-side pre-driver output is changed to Low). The drivers resume the outputs when the VREG undervoltage detection is released.

During the VREG undervoltage detection, the PWMOUT pin is forcibly fixed to Low, and the NDG pin output is pulled Low.



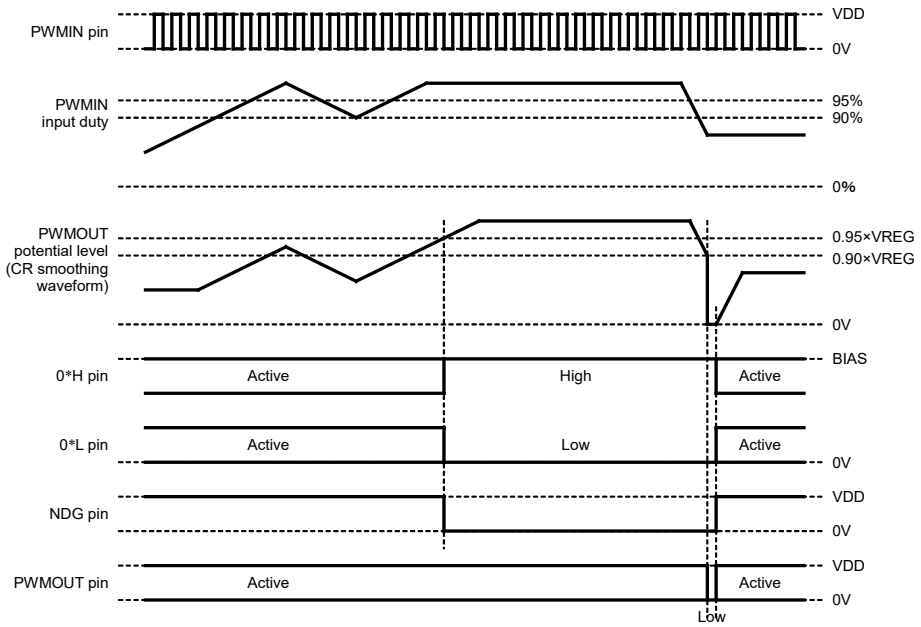

Note: Timing charts may be simplified to clarify the descriptions of features and operations

### 5.7 Full Drive Detection

If the PWMOUT pin potential level exceeds 95% VREG (equivalent to the PWM duty of 95%) when the full drive is configured to Disable (SEL0 = High), the drivers outputs are turned off (the high-side pre-driver output is changed to High while the low-side pre-driver output is changed to Low). The drivers resume the outputs when the VREG potential falls under 90% (typ.).

During the full drive detection, the built-in digital filter on the PWMOUT pin is initialized, and the NDG pin output is pulled Low.

The PWMOUT pin continues behaving normally upon full drive detection, provided that, although for a short time, it is forcibly fixed to Low due to the internal delay of the IC at the time when the full drive disable is released.



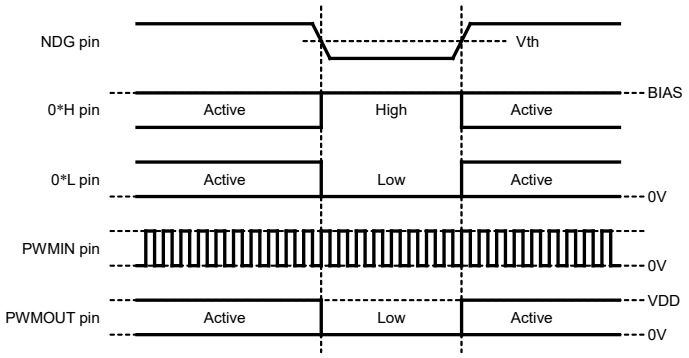

Note: Timing charts may be simplified to clarify the descriptions of features and operations

## Functional Description

### 5.8 External Forced Off Input

Applying the Low input to the NDG pin allows the drivers to be turned off (the high-side pre-driver output is changed to High while the low-side pre-driver output is changed to Low).

During the external forced off input, the PWMOUT pin output is forcibly fixed to Low.




Note: Timing charts may be simplified to clarify the descriptions of features and operations

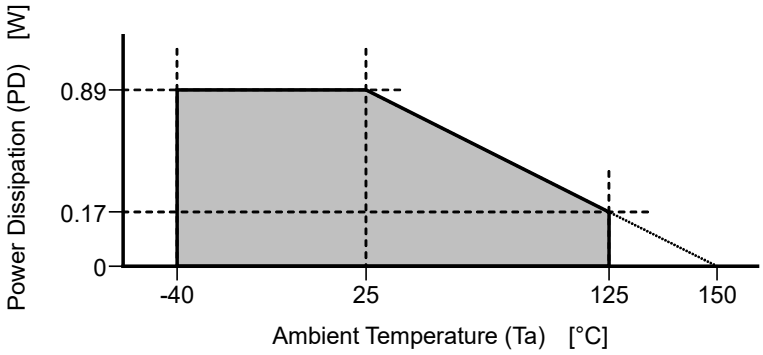
## Absolute Maximum Rating(Ta=25°C)

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

| Characteristics | Symbol | Pin | Ratings | Unit | Remarks |
|---|---|---|---|---|---|
| Power supply voltage | VB1 | BIAS | -0.3 to +40 | V | The rating over +24 V must be within 0.2 s. |
| | VB2 | VREG | -0.3 to +6.0 | V | |
| | VB3 | VDD | -0.3 to +6.0 | V | -0.3 V < VDD-VREG < 0.3 V |
| Input voltage | VIN1 | PWMIN | -0.3 to BIAS+0.3 | V | The rated voltage is less than 40 V. The rating over +24 V must be within 0.2 s. |
| | VIN2 | COMPP | -0.3 to BIAS+0.3 | V | The rated voltage is less than +24 V. |
| | VIN3 | SEL1, TVIN | -0.3 to VREG+0.3 | V | The rated voltage is less than +6.0 V |
| | VIN4 | SEL0, SEL2, NDG, SU, SV, SW, PWMOUT, TEST | -0.3 to VDD+0.3 | V | The rated voltage is less than +6.0 V |
| Output voltage | VOUT1 | OUH, OVH, OWH, OUL, OVL, OWL | -0.3 to BIAS+0.3 | V | The rated voltage is less than 40 V. The rating over +24 V must be within 0.2 s. |
| | VOUT2 | NDG, PWMOUT | -0.3 to VDD+0.3 | V | The rated voltage is less than +6.0 V |
| Output current | IOUT1 | OUH, OVH, OWH, OUL, OVL, OWL | up to ±250 | mA | Must not exceed the Power dissipation. |
| | IOUT2 | NDG, PWMOUT | up to 5 | mA | Must not exceed the Power dissipation. |
| Power dissipation | PD | — | See the figure below. | W | |
| Junction temperature | Tj | — | up to 150 | °C | |
| Operating temperature | Topr | — | -40 to 125 | °C | |
| Storage temperature | Tstg | — | -55 to 150 | °C | |

Note : The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded during operation, even for an instant. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may damage any other equipment. Applications using the device should be designed such that the absolute maximum ratings will never be exceeded in any operating conditions. The device must be used within the specified operating range.

Note : Ratings are presented with the marks; – (minus) and + (plus) indicating the output current from the IC and the input current to the IC respectively, including the symbols.




Note : When mounted on the Toshiba typical board (50 mm × 50 mm × 1.6 mm, Cu = 40%).

## Electrical Characteristics

Unless otherwise specified, Ta = −40 to +125°C, GND = PGND = 0 V, BIAS = 6 to 18 V, VREG and VDD must be shorted.

| Characteristics | Symbol | Pin | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| ♦ Power Consumption | | | | | | | |
| IC power consumption | Ibias | BIAS | TVIN and COMPP are tied to GND. Others have no load. | — | 4.0 | 6.0 | mA |
| ♦ Constant Power Voltage | | | | | | | |
| Constant output voltage | Vreg | VREG | Iveg = 0 to -5 mA | 4.75 | 5.00 | 5.25 | V |
| VREG undervoltage detection threshold | VresL | VREG | | 4.30 | 4.50 | 4.70 | V |
| VREG undervoltage detection hysteresis | VresS | | | 0.10 | 0.15 | 0.20 | V |
| Difference between the constant output voltage and VREG undervoltage detection release threshold | VdifH | | | 0.15 | 0.35 | — | V |
| ♦ Pre-drivers | | | | | | | |
| Internally generated PWM frequency | fpwm | — | | 17.0 | 20.0 | 23.0 | kHz |
| High-side output voltage 1 | VoH_pr1 | OUH, OVH, OWH | Iout = -10 mA | BIAS -0.3 | — | — | V |
| Low-side output voltage 1 | VoL_pr1 | | Iout = 10 mA | — | — | 0.3 | V |
| High-side output voltage 2 | VoH_pr2 | OUL, OVL, OWL | Iout = -10 mA<br>BIAS = 6 to 16 V | BIAS -0.3 | — | — | V |
| | | | Iout = -10 mA<br>BIAS = 16 to 18 V | Vclmp -0.3 | — | — | V |
| Low-side output voltage 2 | VoL_pr2 | | Iout = 10 mA | — | — | 0.3 | V |
| High-side diode-clamp voltage *1 | Vclmp | OUL, OVL, OWL | BIAS = up to 24 V<br>Iout = 0 mA (no load) | 16 *1 | 18 *1 | 20 *1 | V |
| Output off leakage current | Ileak | OUH, OVH, OWH, OUL, OVL, OWL | Vin = 0 V to BIAS on Hi-z output | -10 | — | 10 | μA |
| Output delay time for rising edge | TdlyR | OUL, OVL, OWL | In operating mode 2<br>See Figure 1 | 1 | 4 | 6 | μs |
| Output delay time for falling edge | TdlyF | | In operating mode 2<br>See Figure 1 | — | 3 | 5 | μs |
| Pulse output cycle error | Tdiff | | In operating mode 2<br>See Figure 2 | -1 | 0 | 1 | μs |
| ♦ Sensor Input | | | | | | | |
| High input detection threshold | ViH_si | SU, SV, SW | | — | — | 0.8 ×VREG | V |
| Low input detection threshold | ViL_si | | | 0.2 ×VREG | — | — | V |
| Low input current | IiL_si | SU, SV, SW | VREG = 5 V, Vin = 0 V | -1.5 | -1.0 | -0.5 | mA |
| Noise cancellation time width | Tnc_si | SU, SV, SW | | — | 10 | — | μs |

Note: Ratings are presented with the marks; – (minus) and + (plus) indicating the output current from the IC and the input current to the IC respectively, including the symbols.

*1: The limit reflects the DC characteristics. Any particular event like a rapid fluctuation of the power supply is not considered.

## Electrical Characteristics

Unless otherwise specified, Ta = −40 to +125°C, GND= PGND = 0 V, BIAS = 6 to 18 V, VREG and VDD must be shorted.

| Characteristics | Symbol | Pin | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| ♦ PWM Duty Configuration | | | | | | | |
| High input detection threshold | ViH_pH | PWMIN | | 0.60 ×BIAS | 0.67 ×BIAS | 0.73 ×BIAS | V |
| Low input detection threshold | ViL_pL | | | 0.33 ×VREG | 0.40 ×VREG | 0.47 ×VREG | V |
| PWMIN input frequency | fpin | PWMIN | SEL1= High or Low | — | — | 4.0 | kHz |
| | | | SEL1 = Open or Middle | — | 20 | 23 | kHz |
| High input current 1 | IiH_p1 | PWMIN | SEL1 = High, BIAS = 12 V, Vin = BIAS | 60 | 120 | 240 | μA |
| Low input current 1 | IiL_p1 | | SEL1 = Low, BIAS = 12 V, Vin = 0 V | -240 | -120 | -60 | μA |
| High input current 2 | IiH_p2 | | SEL1 = Open, BIAS = 12 V, Vin = BIAS | 60 | 120 | 240 | μA |
| Low input current 2 | IiL_p2 | | SEL1 = Open, BIAS = 12 V, Vin = 0 V | -240 | -120 | -60 | μA |
| High output current | IoH_po | PWMOUT | When PWMOUT is High active ,VREG = 5.0 V and PWMOUT is 0 V input | -34 | -25 | -18 | μA |
| Low output current | IoL_po | | When PWMOUT is Low active, VREG = 5.0 V and PWMOUT is VREG input. | 18 | 25 | 34 | μA |
| Low output voltage | VoL_po | PWMOUT | Iout = 1 mA where NDG = Low | — | 0.1 | 0.3 | V |
| ♦ Control Input | | | | | | | |
| High input detection threshold 1 | ViH | CW/CCW, SEL0, SEL2 | | — | — | 0.8 ×VREG | V |
| Low input detection threshold 1 | ViL | | | 0.2 ×VREG | — | — | V |
| High input detection threshold 2 | ViH_s1 | SEL1 | | 0.65 ×VREG | 0.70 ×VREG | 0.75 ×VREG | V |
| Low input detection threshold 2 | ViL_s1 | | | 0.25 ×VREG | 0.30 ×VREG | 0.35 ×VREG | V |
| Low input current | IiL_cc | CW/CCW | VREG = 5V, Vin = 0V | -200 | -100 | -50 | μA |
| Low input current | IiL_s0 | SEL0 | VREG = 5V, Vin = 0V | -200 | -100 | -50 | μA |
| High input current | IiH_s1 | SEL1 | VREG = 5V, Vin = VREG | 350 | 500 | 700 | μA |
| Low input current | IiL_s1 | | VREG = 5V, Vin = 0V | -700 | -500 | -350 | μA |
| Low input current | IiL_s2 | SEL2 | VREG = 5V, Vin = 0V | -200 | -100 | -50 | μA |
| Filter pass time on the rapid start | Tpass | SEL2 | | — | 0.3 | — | s |
| Dead time for motor rotation direction switchover | Tdead | CW/CCW | | — | 50 | — | μs |

Note: Ratings are presented with the marks; – (minus) and + (plus) indicating the output current from the IC and the input current to the IC respectively, including the symbols.

## Electrical Characteristics

Unless otherwise specified, Ta = −40 to +125°C, GND = PGND = 0 V, BIAS = 6 to 18 V, VREG and VDD must be shorted.

| Characteristics | Symbol | Pin | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| ♦ Error Detection (the external overcurrent detector for the motor driver) | | | | | | | |
| Overcurrent detection threshold 1 | Vth_c1 | COMPP | | 85 | 100 | 115 | mV |
| Overcurrent detection threshold 2 | Vth_c2 | COMPP | | 170 | 200 | 230 | mV |
| Output off time width for overcurrent detection threshold 1 | Tof_c1 | COMPP | | — | 50 | — | μs |
| Output off time width for overcurrent detection threshold 2 | Tof_c2 | COMPP | | — | 200 | — | μs |
| Required time for determining the fixed output off for overcurrent detection threshold 2 | Toff2 | COMPP | | — | 0.60 | — | s |
| Input current | Iin_cp | COMPP | Vin=0 to 4.5V | -5 | — | 5 | μA |
| Noise cancellation time width for overcurrent detection 1 | Tnc_c1 | COMPP | | — | 3 | — | μs |
| Noise cancellation time width for overcurrent detection 2 | Tnc_c2 | COMPP | | — | 1 | — | μs |
| ♦ Error Detection (the external thermal detector for the motor driver) | | | | | | | |
| Thermal detection threshold | ViH_tv | TVIN | | 0.40 ×VREG | 0.44 ×VREG | 0.48 ×VREG | V |
| Thermal detection release threshold | ViL_tv | | | 0.20 ×VREG | 0.24 ×VREG | 0.28 ×VREG | V |
| Input current | Iin_tv | TVIN | Vin=0 to VREG | -5 | — | 5 | μA |
| Noise cancellation time width for thermal detection | Tnc_tv | TVIN | | — | 10 | — | μs |
| ♦ Error Detection (IC thermal detector) | | | | | | | |
| Thermal detection threshold | TsdH | — | | — | 165 | — | °C |
| Thermal detection threshold hysteresis | TsdS | | | — | 10 | — | °C |
| ♦ Error Detection (BIAS overvoltage and undervoltage detector) | | | | | | | |
| Overvoltage detection threshold | VsdH_H | BIAS | | 24.5 | 27.0 | 29.5 | V |
| Undervoltage detection threshold | VsdL_L | | | 5.2 | 5.5 | 5.9 | V |

Note: Ratings are presented with the marks; – (minus) and + (plus) indicating the output current from the IC and the input current to the IC respectively, including the symbols.

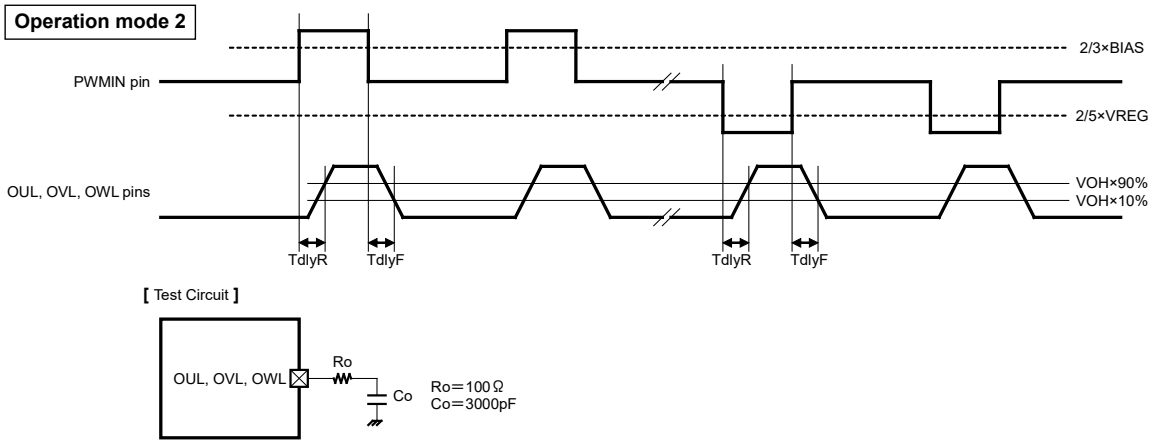
## Electrical Characteristics

Unless otherwise specified, Ta = –40 to +125°C , GND = PGND = 0 V, BIAS = 6 to 18 V, VREG and VDD must be shorted.

| Characteristics | Symbol | Pin | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| ♦ Error Detection (the full drive detector) | | | | | | | |
| 100% duty detection threshold | VdtyH | PWMOUT | PWMOUT pin level | 0.92 ×VREG | 0.95 ×VREG | 0.98 ×VREG | V |
| 100% duty detection release threshold hysteresis | VdtyS | | PWMOUT pin level | — | 0.05 ×VREG | — | V |
| ♦ Error Detection (the external forced off input detector) | | | | | | | |
| High input detection threshold | ViH_nd | NDG | | — | — | 0.8 ×VREG | V |
| Low input detection threshold | ViL_nd | | | 0.2 ×VREG | — | — | V |
| High output voltage | VoH_nd | NDG | Iout = 0 mA (no load) | VDD -0.3 | VDD -0.1 | — | V |
| Low output voltage | VoL_nd | | Iout = 1 mA | — | 0.1 | 0.3 | V |
| Low input current | IiL_nd | NDG | VREG = 5 V, Vin = 0 V | -1000 | -500 | -250 | μA |

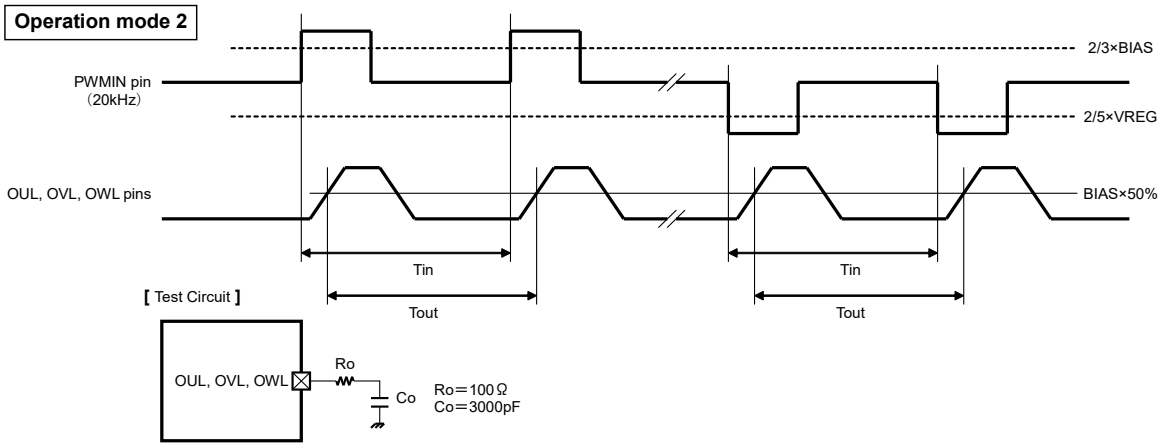
Note: Ratings are presented with the marks; – (minus) and + (plus) indicating the output current from the IC and the input current to the IC respectively, including the symbols.

### Figure 1




Note: Timing charts may be simplified to clarify the descriptions of features and operations

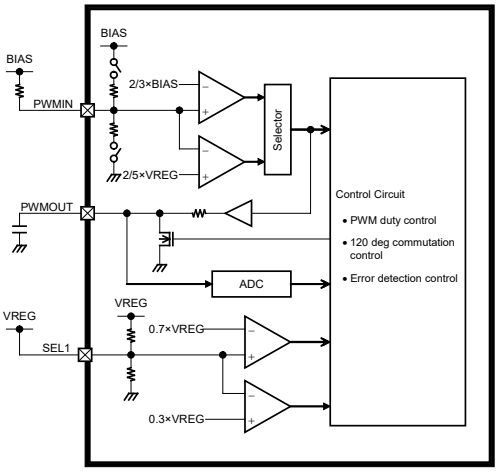
### Figure 2



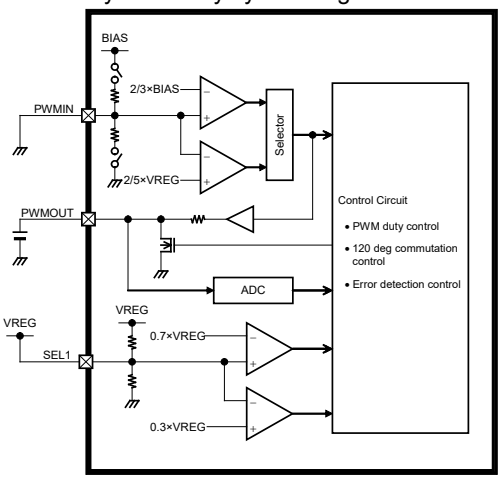

Note: Timing charts may be simplified to clarify the descriptions of features and operations

## Typical Applications for Various Controls

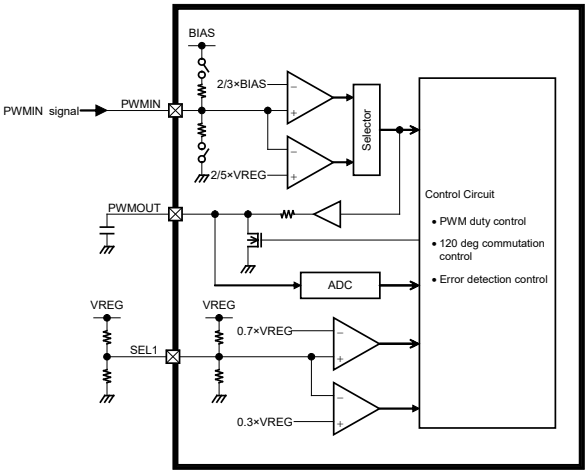
1) When running the motor driver with fixed 100% duty cycle using the internal PWM




2) When running the motor driver with any fixed duty cycle using the internal PWM




3) When running the motor driver using any external input PWM

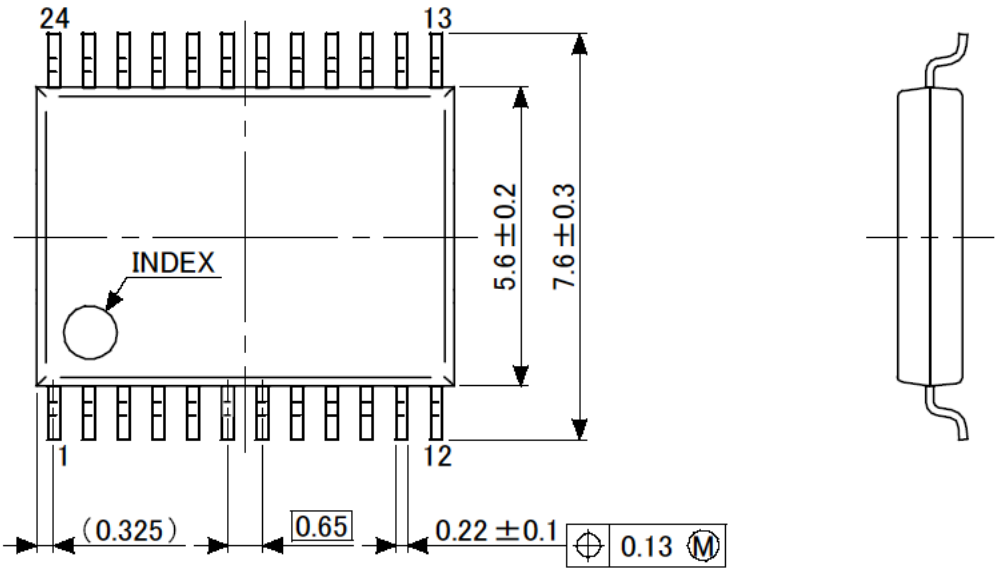



Note: In the application circuit example, part of the functional blocks or constants may be omitted or simplified for explanatory purposes.

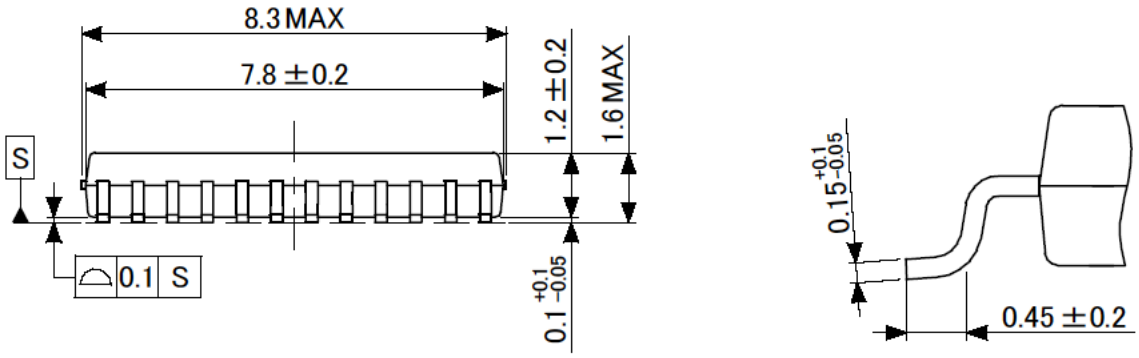
Note: The application circuit shown above is not intended to guarantee mass production. A thorough evaluation is required when designing an application circuit for mass production.

## Package Dimensions

Unit: mm




Expanded View of the Lead Tip




Weight: 0.14 g (typ.)

## Notes

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Note: Timing charts may be simplified for explanatory purposes.

Note: Ensure that the IC is mounted correctly as specified. Failing to observe the correct mounting procedure or requirements may damage the IC or target equipment.

Note: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

Note: Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

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