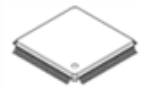
CMOS Digital Integrated Circuit Silicon Monolithic

TMPM3H Group(1)



LQFP144
(20x20 mm, 0.5 mm pitch)
LQFP128
(14x14 mm, 0.4 mm pitch)
LQFP100
(14x14 mm, 0.5 mm pitch)
LQFP80
(12x12 mm, 0.5 mm pitch)
LQFP64
(10x10 mm, 0.5 mm pitch)

LQFP128
(14x20 mm, 0.5 mm pitch)
QFP100
(14x20 mm, 0.65 mm pitch)

General Description

- Arm®Cortex®-M3 core, operating frequency: 1 to 120 MHz, opetating voltage: 2.7 to 5.5V
- Code flash: 256KB to 512KB, Data flash: 32KB
- Package: 64-pin to 144-pin, 7 types of packages are available.

Applications

Widely used for consumer products and industrial products including home appliances, OA equipment, household equipment, AV devices, and motor control devices.

Features

- Arm Cortex-M3 core
  - Operating frequency: 1 to 120 MHz
  - Memory Protection Unit (MPU)
- Operating voltage and Low-power consumption operation
  - Operating voltage: 2.7 to 5.5V
  - Low-power consumption operation: IDLE, STOP1, STOP2
  - Operating temperature: -40 to +105°C
- Internal memory
  - Code flash: 256KB to 512 KB, rewritable up to 100,000 times
  - Data flash: 32 KB, rewritable up to 100,000 times
  - Data flash is rewritable in parallel with instruction execution
  - RAM: 64KB and Backup RAM: 2 KB
    Both RAMs have party bit.
- Clock
  - External High-speed Oscillator: 6 MHz to 12 MHz (Ceramic, Crystal)
  - External High-speed clock input: 6 to 20 MHz
  - Internal High-speed Oscillator (IHOSC1): 10 MHz, user trimming function
  - PLL: 120 MHz output
  - External Low-speed Oscillator: 32.768kHz
- Oscillation Frequency Detector (OFD): Abnormal system clock detection
- Voltage Detection circuit (LVD): 8 level, Generate interrupts and reset outputs
- Interrupt
  - External factors: 12 to 23
    (External pins: 12 to 34 pins with DNF)
  - Internal factors: 128 to 151
- I/O ports: 57 to 135 (Include Input only: 4, Output only: 1)
  - Pull-up/pull-down resistor, Open-drain, 5V-tolerant
- On Chip Debug (JTAG/SW)
- Trigger Selector (TRGSEL)
  - Expand Trigger request for DMAC, Timer counter and so on.
- DMA Controller (DMAC)
  - DMA requests: 2units, 54 to 64 factors, internal/external triggers
- LCD Display Controller (DLCD)
  - Non-Bias Drive: 40 segments × 4 commons (Max)
- Universal Asynchronous Receiver Transmitter (UART): 7 to 8 channels
  - Up to 2.5Mbps, FIFO (Transmission 9bits × 8, Reception 9bits × 8)
- Serial Peripheral Interface (TSPI): 1 to 5 channels
  - SIO/SPI mode, up to 20MHz, FIFO (Transmission 16bits × 8, Reception 16bits × 8), sector/frame mode
- I^2C Interface
  - I^2C interface (I2C): 2 to 4 channels
    Multi Master, Release function for Low Power Mode
  - I^2C interface Version A (EI2C): 2 to 4 channels
    Multi Master, Support 10-bit Slave Addressing
    Release function for Low Power Mode
- Comparator: 1 channel. EMG signal output to A-PMD
- 8-bit DA Converter (DAC): 2 channels
- 12-bit ADC (ADC): 12 to 21 channels analog inputs
  - Built-in sample-and-hold circuit
    Conversion time: 1.5µs@SCLK = 20MHz,
    1.0µs@SCLK = 30MHz
  - Support self-diagnosis function
- Advanced Programmable Motor Control Circuit (A-PMD): 1 channel
  - 3-phase complementary PWM output, Synchronized with 12-bit ADC
  - Emergency stop function by external inputs (EMG0 pin, OVV0 pin)
- Advanced Encoder Input Circuit (A-ENC): 1 channel
  - Encoder/sensor (3 types)/Timer/Phase counter mode
- 32-bit Timer Event Counter (T32A)
  - 8 channels as 32-bit timer, 16 channels as 16-bit timer
  - Interval timer, event counter, input capture, phase difference input, PPG output, sync start, trigger start
- Real Time Clock (RTC): 1 channel
- Watchdog Timer (SIWDT): 1 channel
  - Clock system other than the system clock can be selected
  - Clear window, interrupts and reset output
- Remote Control Signal Preprocessor (RMC): 1 channel
- CRC Calculation Circuit (CRC): 1channel, CRC32, CRC16

Start of commercial production
2022-05

Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, please contact your sales representative.

Table 1.1 Products List (1/2)

Built-in Functions		TMPM3HQFDAFG TMPM3HQFZAFG TMPM3HQFYAFG	TMPM3HPFDAFG TMPM3HPFZAFG TMPM3HPFYAFG	TMPM3HPFDADFG TMPM3HPFZADFG TMPM3HPFYADFG	TMPM3HNFDAFG TMPM3HNFZAFG TMPM3HNFYAFG	TMPM3HNFDADFG TMPM3HNFZADFG TMPM3HNFYADFG
Memory	Code Flash (KB)	512 384 256	512 384 256	512 384 256	512 384 256	512 384 256
	Data Flash (KB)	32	32	32	32	32
	RAM (KB)	64	64	64	64	64
	Backup RAM (KB)	2	2	2	2	2
I/O port	PORT (Pin)	135	119	119	93	93
External interrupt	Factor	23	21	21	18	18
	Pin	34	31	31	19	19
DMA	DMAC (ch)	64	64	64	62	62
Timer function	T32A (ch)	8	8	8	8	8
	RTC (ch)	1	1	1	1	1
Serial communication function	UART (ch)	8	8	8	8	8
	I2C/EI2C (ch)	4/4	4/4	4/4	3/3	3/3
	TSPI (ch)	5	5	5	4	4
Analog function	12-bit ADC (ch)	21	19	19	17	17
	8-bit DAC (ch)	2	2	2	2	2
	Comparator (ch)	1	1	1	1	1
Motor Control peripherals	A-ENC (ch)	1	1	1	1	1
	A-PMD (ch)	1	1	1	1	1
Other peripherals	RMC (ch)	1	1	1	1	1
	CRC (ch)	1	1	1	1	1
	DLCD	40 segments × 4 commons	40 segments × 4 commons	40 segments × 4 commons	32 segments × 4 commons	32 segments × 4 commons
System function	RAMP	1	1	1	1	1
	LVD (ch)	1	1	1	1	1
	SIWDT (ch)	1	1	1	1	1
	OFD (ch)	1	1	1	1	1
	POR	1	1	1	1	1
Debug interface	Debug	JTAG/SW TRACE (4bit)	JTAG/SW TRACE (4bit)	JTAG/SW TRACE (4bit)	JTAG/SW TRACE (4bit)	JTAG/SW TRACE (4bit)
Package	Package type	LQFP144 (20 mm x 20 mm, 0.5 mm pitch)	LQFP128 (14 mm x 14 mm, 0.4 mm pitch)	LQFP128 (14 mm x 20 mm, 0.5 mm pitch)	LQFP100 (14 mm x 14 mm, 0.5 mm pitch)	QFP100 (14 mm x 20 mm, 0.65 mm pitch)

Table 1.2 Products List (2/2)

Built-in Functions		TMPM3HMFDAFG TMPM3HMFZAFG TMPM3HMFYAFG	TMPM3HLFDAUG TMPM3HLFZAUG TMPM3HLFYAUG
Memory	Code Flash (KB)	512 384 256	512 384 256
	Data Flash (KB)	32	32
	RAM (KB)	64	64
	Backup RAM (KB)	2	2
I/O port	PORT (Pin)	73	57
External interrupt	Factor	15	12
	Pin	15	12
DMA	DMAC (ch)	62	54
Timer function	T32A (ch)	8	8
	RTC (ch)	1	1
Serial communication function	UART (ch)	7	7
	I2C/EI2C (ch)	3/3	2/2
	TSPI (ch)	4	1
Analog function	12-bit ADC (ch)	12	12
	8-bit DAC (ch)	2	2
	Comparator (ch)	1	1
Motor Control peripherals	A-ENC (ch)	1	1
	A-PMD (ch)	1	1
Other peripherals	RMC (ch)	1	1
	CRC (ch)	1	1
	DLCD	26 segments × 4 commons	-
System function	RAMP	1	1
	LVD (ch)	1	1
	SIWDT (ch)	1	1
	OFD (ch)	1	1
	POR	1	1
Debug interface	Debug	JTAG/SW TRACE (2bit)	JTAG/SW
Package	Package type	LQFP80 (12 mm x 12 mm, 0.5 mm pitch)	LQFP64 (10 mm x 10 mm, 0.5 mm pitch)

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Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

The following words are terms or abbreviations mainly used in this datasheet.

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
APB	Advanced Peripheral Bus
A-PMD	Advanced Programmable Motor Control Circuit
CG	Clock control and Operation Mode
COMP	Comparator
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
ELOSC	External Low Speed Oscillator
EHOSC	External High-Speed Oscillator
EI2C	I^2C Interface Version A
fsys	Frequency of SYSTEM Clock
I2C	Inter-Integrated Circuit
I2CS	Address Match Wakeup Function
IHOSC	Internal High-speed Oscillator
IA (INTIF)	Interrupt control register A
IB (INTIF)	Interrupt control register B
I-Bus	ICode memory interface
IMN	Interrupt Monitor
INT	Interrupt
IO	IO Bus (32bit Peripheral Bus)
DLCD	LCD Display Control Circuit
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
RAMP	RAM Parity Circuit
RLM	Low Speed Oscillation/Power Supply Control/Reset
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
S-Bus	System interface
SCOUT	Source Clock Output
SIWDT	Clock Selective Watchdog Timer
TPIU	Trace Port Interface Unit
TRGSEL	Trigger Selection Circuit
TRM	Trimming Circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Block Diagram

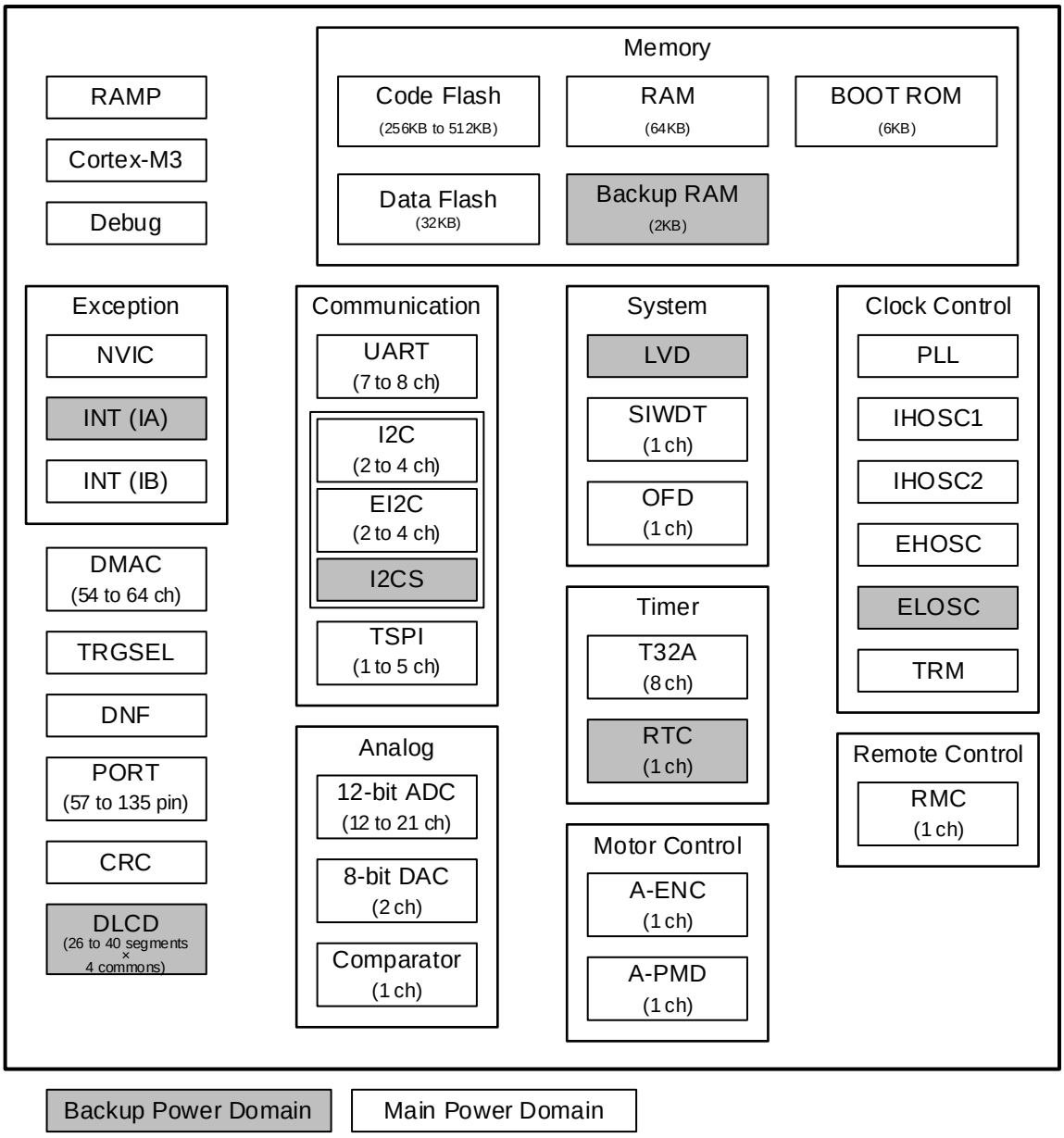
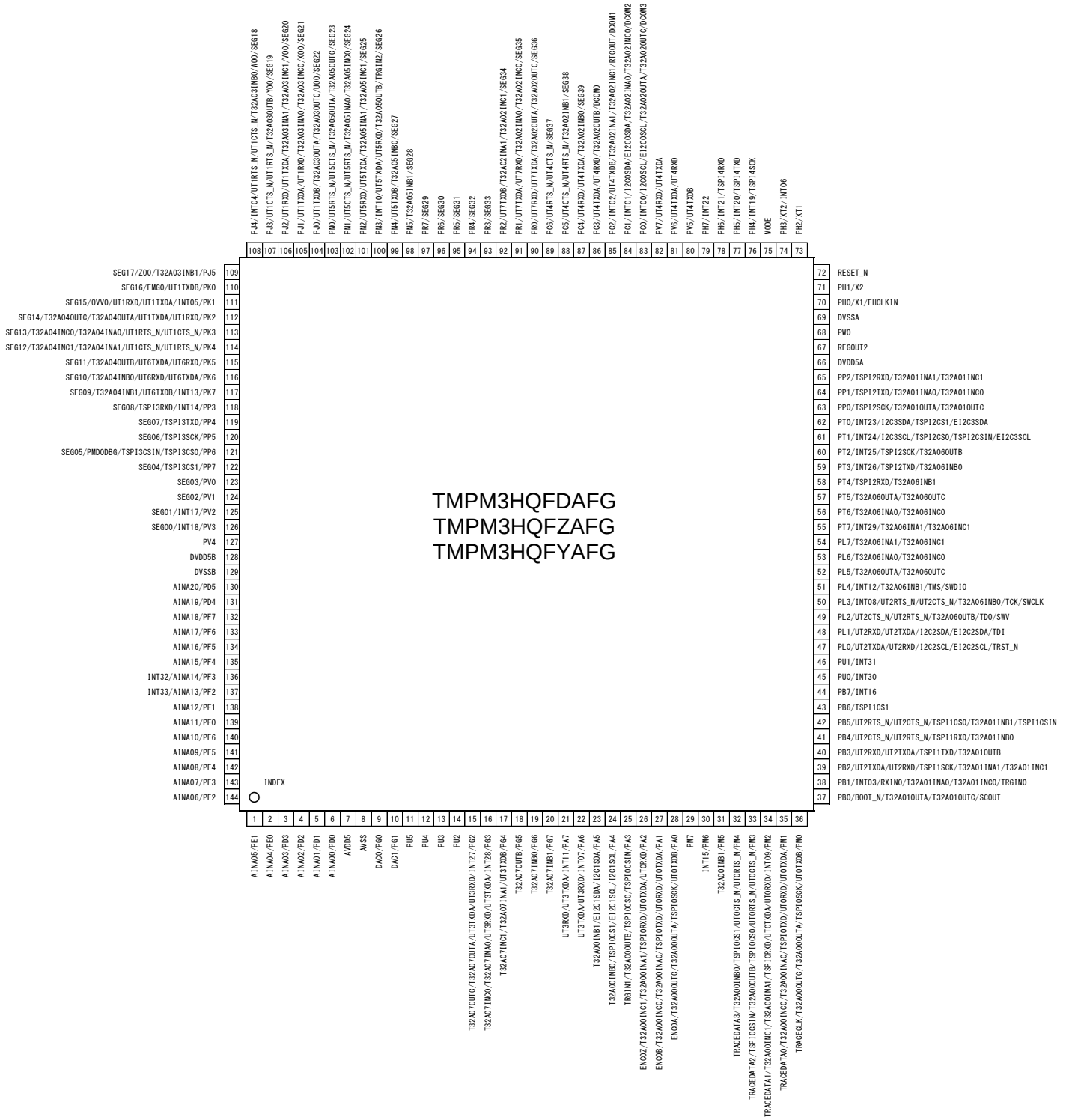


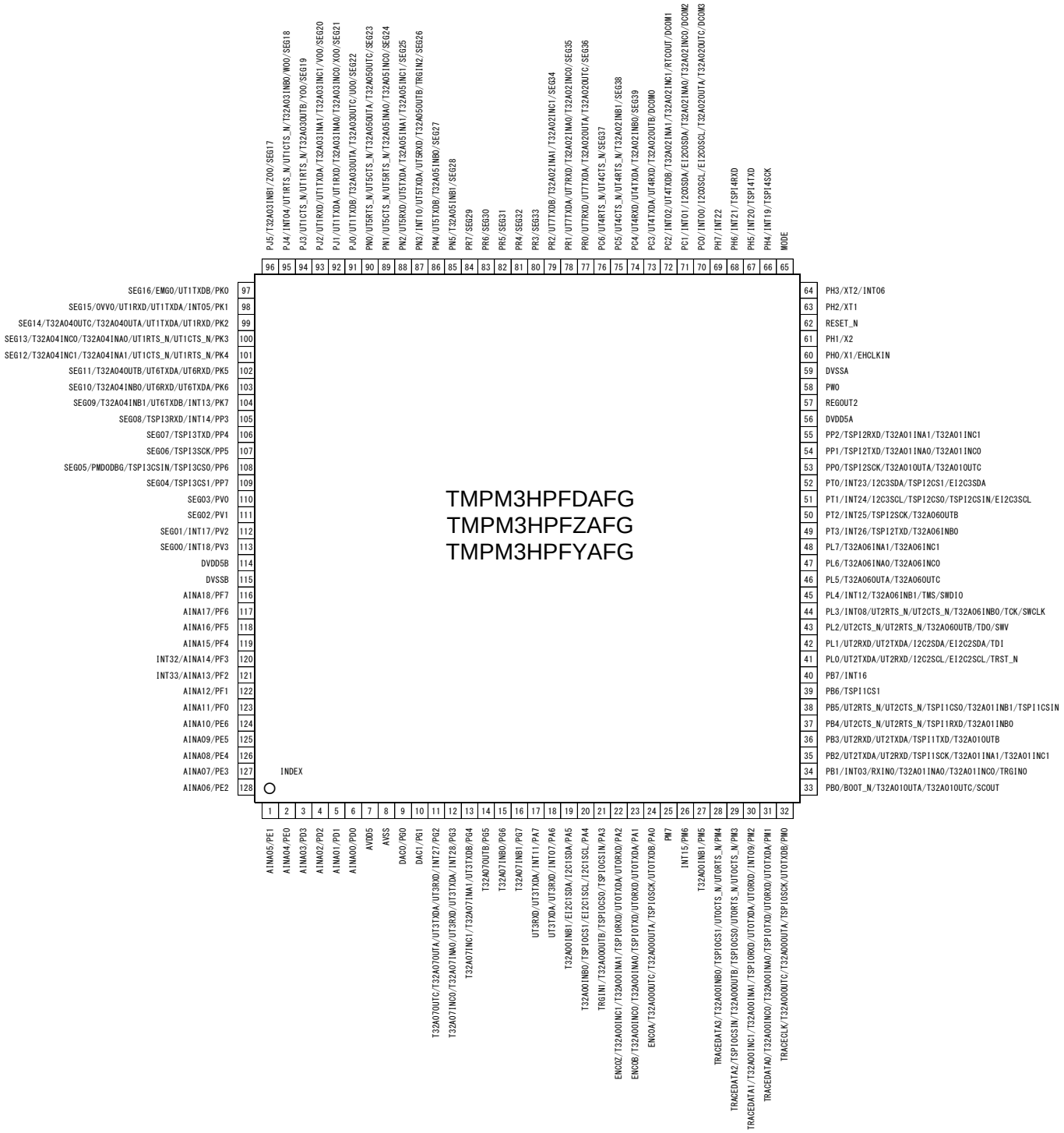
Figure 1.1 Block diagram of the TMPM3H Group(1)

2. Pin Assignment

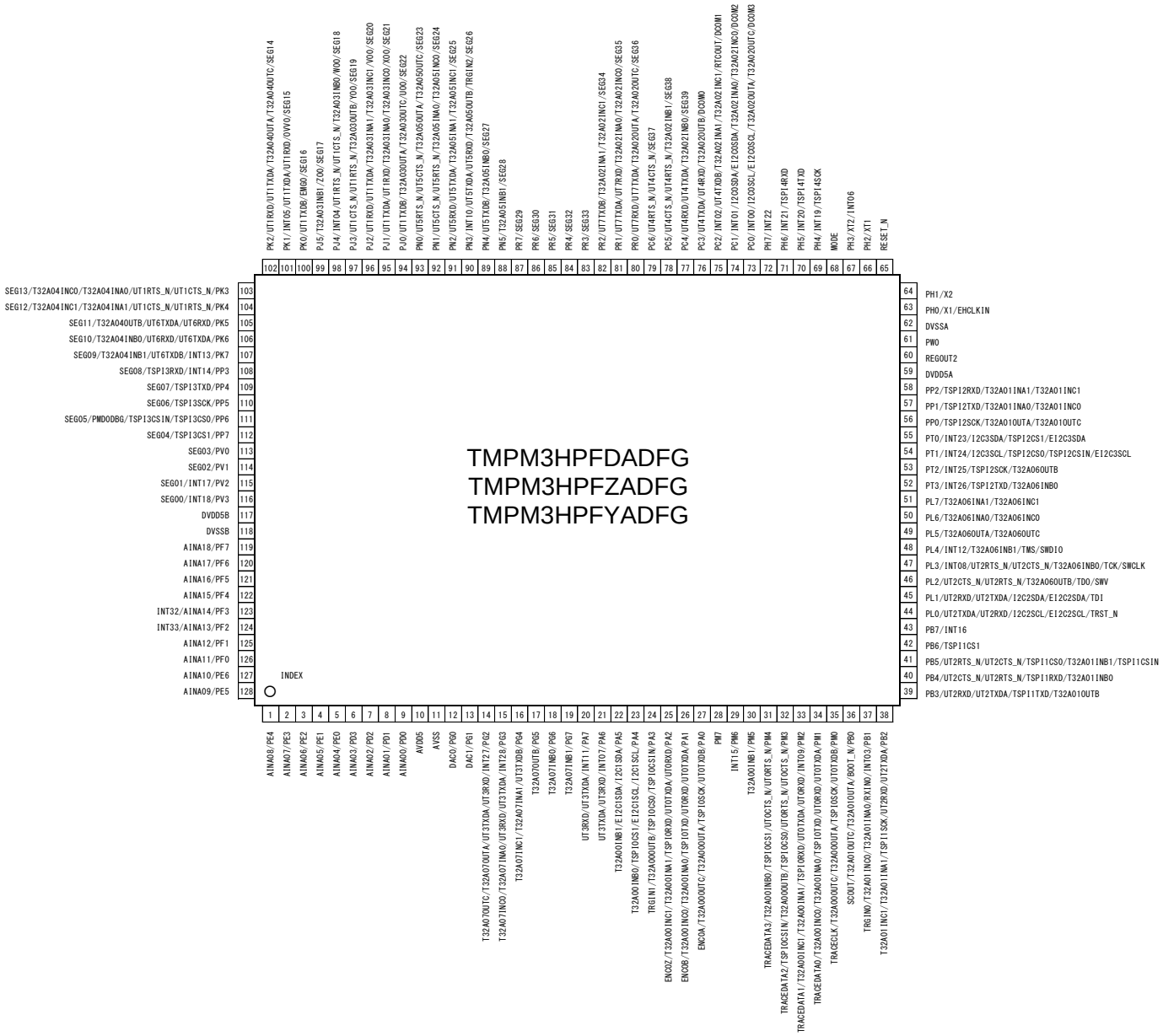
2.1. LQFP144



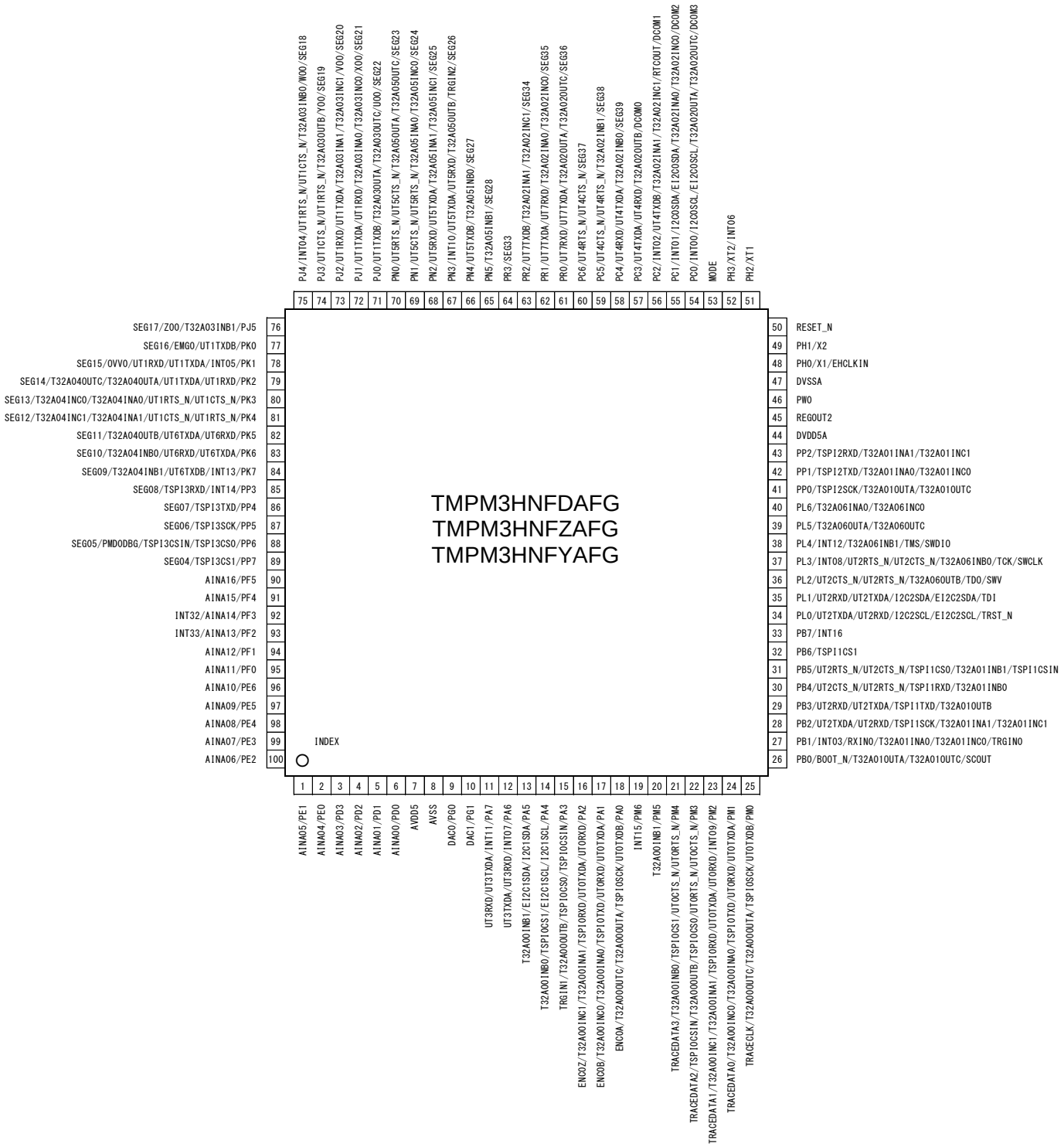
2.2. LQFP128-1414



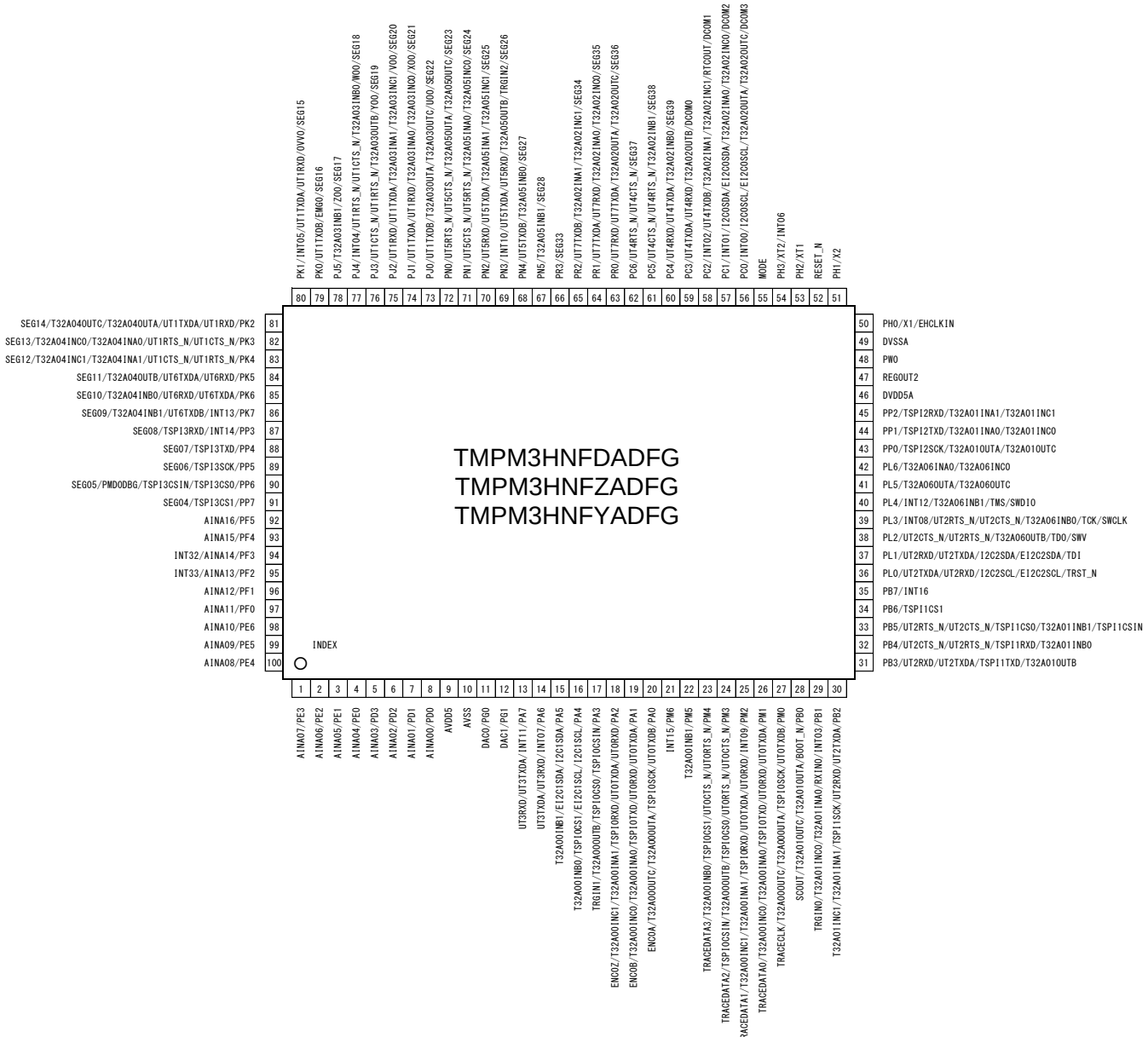
2.3. LQFP128-1420



2.4. LQFP100


TMPM3HNFDAFG
TMPM3HNFZAFG
TMPM3HNFYAFG
INDEX
1 AINA05/PE1
2 AINA04/PE0
3 AINA03/PD3
4 AINA02/PD2
5 AINA01/PD1
6 AINA00/PD0
7 AVDD5
8 AVSS
9 DAC0/PG0
10 DAC1/PG1
11 UT3RXD/UT3TXDA/INT11/PA7
12 UT3TXDA/UT3RXD/INT07/PA6
13 T32A001NB1/EI2C1SDA/I2C1SDA/PA5
14 T32A001NB0/TSPI0CS1/EI2C1SCL/I2C1SCL/PA4
15 TRG1IN1/T32A000UTB/TSPI0CS0/TSPI0CSIN/PA3
16 ENC02/T32A001INC1/T32A001NA1/TSPI0RXD/UT0TXDA/UT0RXD/PA2
17 ENC0B/T32A001INC0/T32A001NA0/TSPI0TXD/UT0RXD/UT0TXDB/PA1
18 ENC0A/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PA0
19 INT15/PM6
20 T32A001NB1/PM5
21 TRACEDATA3/T32A001NB0/TSPI0CS1/UT0CTS_N/UT0RTS_N/PM4
22 TRACEDATA2/TSPI0CSIN/T32A000UTB/TSPI0CS0/UT0RTS_N/UT0CTS_N/PM3
23 TRACEDATA1/T32A001INC1/T32A001NA1/TSPI0RXD/UT0TXDA/UT0RXD/INT09/PM2
24 TRACEDATA0/T32A001INC0/T32A001NA0/TSPI0TXD/UT0RXD/UT0TXDA/PM1
25 TRACECLK/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PM0
26 PB0/BOOT_N/T32A010UTA/T32A010UTC/SCOUT
27 PB1/INT03/RXIN0/T32A011INA0/T32A011INC0/TRGIN0
28 PB2/UT2TXDA/UT2RXD/TSPI1SCK/T32A011INA1/T32A011INC1
29 PB3/UT2RXD/UT2TXDA/TSPI1TXD/T32A010UTB
30 PB4/UT2CTS_N/UT2RTS_N/TSPI1RXD/T32A011INB0
31 PB5/UT2RTS_N/UT2CTS_N/TSPI1CS0/T32A011INB1/TSPI1CSIN
32 PB6/TSPI1CS1
33 PB7/INT16
34 PL0/UT2TXDA/UT2RXD/I2C2SCL/EI2C2SCL/TRST_N
35 PL1/UT2RXD/UT2TXDA/I2C2SDA/EI2C2SDA/TDI
36 PL2/UT2CTS_N/UT2RTS_N/T32A060UTB/TDO/SWV
37 PL3/INT08/UT2RTS_N/UT2CTS_N/T32A061NB0/TCK/SWCLK
38 PL4/INT12/T32A061NB1/TMS/SWDIO
39 PL5/T32A060UTA/T32A060UTC
40 PL6/T32A061NA0/T32A061NC0
41 PP0/TSPI2SCK/T32A010UTA/T32A010UTC
42 PP1/TSPI2TXD/T32A011NA0/T32A011NC0
43 PP2/TSPI2RXD/T32A011NA1/T32A011NC1
44 DVDD5A
45 REGOUT2
46 PW0
47 DVSSA
48 PH0/X1/EHCLKIN
49 PH1/X2
50 RESET_N
51 PH2/XT1
52 PH3/XT2/INT06
53 MODE
54 PC0/INT00/I2C0SCL/EI2C0SCL/T32A020UTA/T32A020UTC/DC0M3
55 PC1/INT01/I2C0SDA/EI2C0SDA/T32A021NA0/T32A021NC0/DC0M2
56 PC2/INT02/UT4TXDB/T32A021NA1/T32A021NC1/RTCOUT/DC0M1
57 PC3/UT4TXDA/UT4RXD/T32A020UTB/DC0M0
58 PC4/UT4RXD/UT4TXDA/T32A021NB0/SEG39
59 PC5/UT4CTS_N/UT4RTS_N/T32A021NB1/SEG38
60 PC6/UT4RTS_N/UT4CTS_N/SEG37
61 PR0/UT7RXD/UT7TXDA/T32A020UTA/T32A020UTC/SEG36
62 PR1/UT7TXDA/UT7RXD/T32A021NA0/T32A021NC0/SEG35
63 PR2/UT7TXDB/T32A021NA1/T32A021NC1/SEG34
64 PR3/SEG33
65 PW5/T32A051NB1/SEG28
66 PW4/UT5TXDB/T32A051NB0/SEG27
67 PW3/INT10/UT5TXDA/UT5RXD/T32A050UTB/TRG1N2/SEG26
68 PW2/UT5RXD/UT5TXDA/T32A051NA1/T32A051NC1/SEG25
69 PW1/UT5CTS_N/UT5RTS_N/T32A051NA0/T32A051NC0/SEG24
70 PW0/UT5RTS_N/UT5CTS_N/T32A050UTA/T32A050UTC/SEG23
71 PJ0/UT1TXDB/T32A030UTA/T32A030UTC/U00/SEG22
72 PJ1/UT1TXDA/UT1RXD/T32A031NA0/T32A031NC0/X00/SEG21
73 PJ2/UT1RXD/UT1TXDA/T32A031NA1/T32A031NC1/V00/SEG20
74 PJ3/UT1CTS_N/UT1RTS_N/T32A030UTB/Y00/SEG19
75 PJ4/INT04/UT1RTS_N/UT1CTS_N/T32A031NB0/W00/SEG18
76 SEG17/Z00/T32A03INB1/PJ5
77 SEG16/EMG0/UT1TXDB/PK0
78 SEG15/OVV0/UT1RXD/UT1TXDA/INT05/PK1
79 SEG14/T32A040UTC/T32A040UTA/UT1TXDA/UT1RXD/PK2
80 SEG13/T32A04INC0/T32A04INA0/UT1RTS_N/UT1CTS_N/PK3
81 SEG12/T32A04INC1/T32A04INA1/UT1CTS_N/UT1RTS_N/PK4
82 SEG11/T32A040UTB/UT6TXDA/UT6RXD/PK5
83 SEG10/T32A041NB0/UT6RXD/UT6TXDA/PK6
84 SEG09/T32A04INB1/UT6TXDB/INT13/PK7
85 SEG08/TSPI3RXD/INT14/PP3
86 SEG07/TSPI3TXD/PP4
87 SEG06/TSPI3SCK/PP5
88 SEG05/PMDODBG/TSPI3CSIN/TSPI3CS0/PP6
89 SEG04/TSPI3CS1/PP7
90 AINA16/PF5
91 AINA15/PF4
92 INT32/AINA14/PF3
93 INT33/AINA13/PF2
94 AINA12/PF1
95 AINA11/PF0
96 AINA10/PE6
97 AINA09/PE5
98 AINA08/PE4
99 AINA07/PE3
100 AINA06/PE2

2.5. QFP100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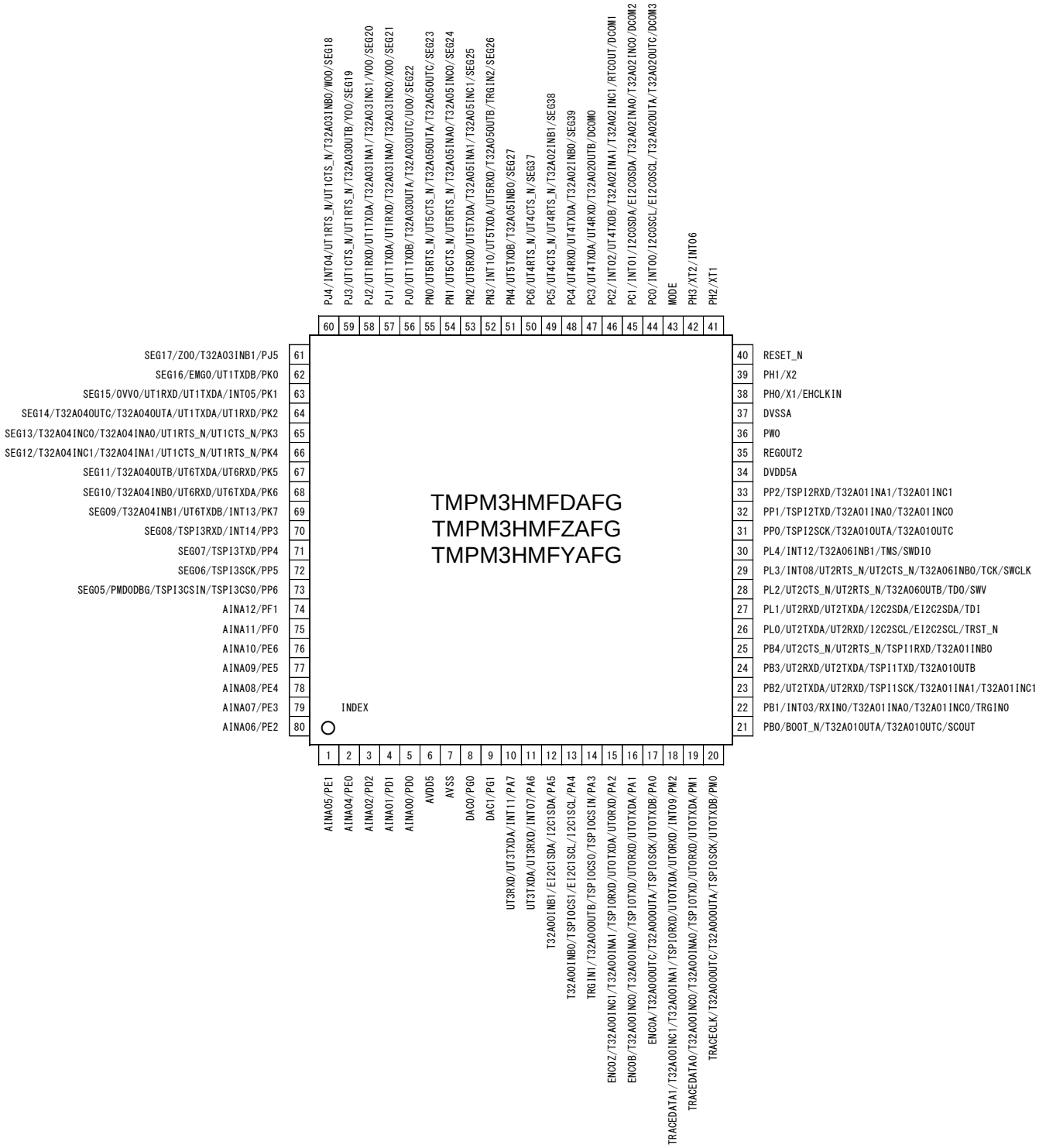
TMPM3HNFZADFG
TMPM3HNFYADFG
INDEX
1 AINA07/PE3
2 AINA06/PE2
3 AINA05/PE1
4 AINA04/PE0
5 AINA03/PD3
6 AINA02/PD2
7 AINA01/PD1
8 AINA00/PD0
9 AVDD5
10 AVSS
11 DAC0/PG0
12 DAC1/PG1
13 UT3RXD/UT3TXDA/INT11/PA7
14 UT3TXDA/UT3RXD/INT07/PA6
15 T32A001NB0/TSPI0CS1/E12C1SDA/I2C1SDA/PA5
16 T32A001NB0/TSPI0CS1/E12C1SCL/I2C1SCL/PA4
17 TRGIN1/T32A000UTB/TSPI0CS0/TSPI0CSIN/PA3
18 ENC02/T32A001NC1/T32A001NA1/TSPI0TXD/UT0TXDA/UT0RXD/PA2
19 ENC0B/T32A001NC0/T32A001NA0/TSPI0TXD/UT0RXD/UT0TXDA/PA1
20 ENC0A/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PA0
21 INT15/PM6
22 T32A001NB1/PM5
23 TRACEDATA3/T32A001NB0/TSPI0CS1/UT0CTS_N/UT0RTS_N/PM4
24 TRACEDATA2/TSPI0CSIN/T32A000UTB/TSPI0CS0/UT0RTS_N/UT0CTS_N/PM3
25 TRACEDATA1/T32A001NC1/T32A001NA1/TSPI0RXD/UT0TXDA/UT0RXD/INT09/PM2
26 TRACEDATA0/T32A001NC0/T32A001NA0/TSPI0TXD/UT0RXD/UT0TXDA/PM1
27 TRACECLK/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PM0
28 SCOUT/T32A010UTC/T32A010UTA/BOOT_N/PB0
29 TRGIN0/T32A011NC0/T32A011NA0/RXIN0/INT03/PB1
30 T32A011NC1/T32A011NA1/TSPI1SCK/UT2RXD/UT2TXDA/PB2
31 PB3/UT2RXD/UT2TXDA/TSPI1TXD/T32A010UTB
32 PB4/UT2CTS_N/UT2RTS_N/TSPI1RXD/T32A011NBO
33 PB5/UT2RTS_N/UT2CTS_N/TSPI1CS0/T32A011NB1/TSPI1CSIN
34 PB6/TSPI1CS1
35 PB7/INT16
36 PL0/UT2TXDA/UT2RXD/I2C2SCL/EI2C2SCL/TRST_N
37 PL1/UT2RXD/UT2TXDA/I2C2SDA/EI2C2SDA/TDI
38 PL2/UT2CTS_N/UT2RTS_N/T32A060UTB/TDO/SWV
39 PL3/INT08/UT2RTS_N/UT2CTS_N/T32A061NBO/TCK/SWCLK
40 PL4/INT12/T32A061NB1/TMS/SWDIO
41 PL5/T32A060UTA/T32A060UTC
42 PL6/T32A061NAO/T32A061NCO
43 PP0/TSPI2SCK/T32A010UTA/T32A010UTC
44 PP1/TSPI2TXD/T32A011NAO/T32A011NCO
45 PP2/TSPI2RXD/T32A011NA1/T32A011NC1
46 DVDD5A
47 REGOUT2
48 PWO
49 DVSSA
50 PH0/X1/EHCLKIN
51 PH1/X2
52 RESET_N
53 PH2/XT1
54 PH3/XT2/INT06
55 MODE
56 PC0/INT00/I2C0SCL/EI2C0SCL/T32A020UTA/T32A020UTC/DCOM3
57 PC1/INT01/I2C0SDA/EI2C0SDA/T32A021NA0/T32A021NC0/DCOM2
58 PC2/INT02/UT4TXDB/T32A021NA1/T32A021NC1/RTCOUT/DCOM1
59 PC3/UT4TXDA/UT4RXD/T32A020UTB/DCOM0
60 PC4/UT4RXD/UT4TXDA/T32A021NBO/SEG39
61 PC5/UT4CTS_N/UT4RTS_N/T32A021NB1/SEG38
62 PC6/UT4RTS_N/UT4CTS_N/SEG37
63 PR0/UT7RXD/UT7TXDA/T32A020UTA/T32A020UTC/SEG36
64 PR1/UT7TXDA/UT7RXD/T32A021NAO/T32A021NCO/SEG35
65 PR2/UT7TXDB/T32A021NA1/T32A021NC1/SEG34
66 PR3/SEG33
67 PM5/T32A051NB1/SEG28
68 PM4/UT5TXDB/T32A051NBO/SEG27
69 PM3/INT10/UT5TXDA/UT5RXD/T32A050UTB/TRGIN2/SEG26
70 PM2/UT5RXD/UT5TXDA/T32A051NA1/T32A051NC1/SEG25
71 PM1/UT5CTS_N/UT5RTS_N/T32A051NAO/T32A051NCO/SEG24
72 PM0/UT5RTS_N/UT5CTS_N/T32A050UTA/T32A050UTC/SEG23
73 PJ0/UT1TXDB/T32A030UTA/T32A030UTC/UO0/SEG22
74 PJ1/UT1TXDA/UT1RXD/T32A031NAO/T32A031NCO/XO0/SEG21
75 PJ2/UT1RXD/UT1TXDA/T32A031NA1/T32A031NC1/YO0/SEG20
76 PJ3/UT1CTS_N/UT1RTS_N/T32A030UTB/YO0/SEG19
77 PJ4/INT04/UT1RTS_N/UT1CTS_N/T32A031NBO/WO0/SEG18
78 PJ5/T32A031NB1/ZO0/SEG17
79 PK0/UT1TXDB/EMG0/SEG16
80 PK1/INT05/UT1TXDA/UT1RXD/OVV0/SEG15
81 SEG14/T32A040UTC/T32A040UTA/UT1TXDA/UT1RXD/PK2
82 SEG13/T32A04INC0/T32A041NAO/UT1RTS_N/UT1CTS_N/PK3
83 SEG12/T32A04INC1/T32A041NA1/UT1CTS_N/UT1RTS_N/PK4
84 SEG11/T32A040UTB/UT6TXDA/UT6RXD/PK5
85 SEG10/T32A04INBO/UT6RXD/UT6TXDA/PK6
86 SEG09/T32A04INB1/UT6TXDB/INT13/PK7
87 SEG08/TSPI3RXD/INT14/PP3
88 SEG07/TSPI3TXD/PP4
89 SEG06/TSPI3SCK/PP5
90 SEG05/PMDODBG/TSPI3CSIN/TSPI3CS0/PP6
91 SEG04/TSPI3CS1/PP7
92 AINA16/PF5
93 AINA15/PF4
94 INT32/AINA14/PF3
95 INT33/AINA13/PF2
96 AINA12/PF1
97 AINA11/PF0
98 AINA10/PE6
99 AINA09/PE5
100 AINA08/PE4

2.6. LQFP80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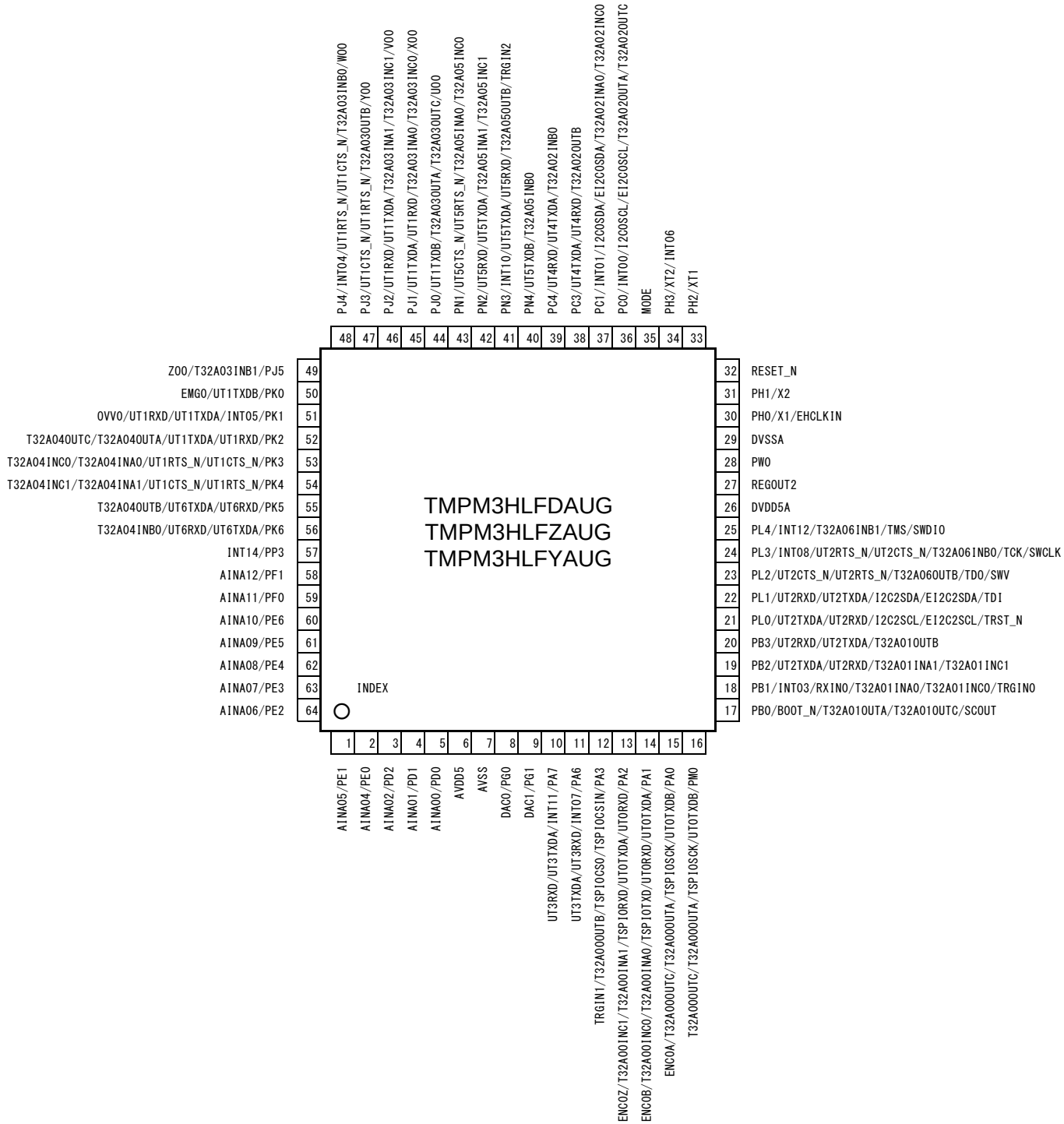
TMPM3HMFZAFG
TMPM3HMFYAFG
INDEX
1 AINA05/PE1
2 AINA04/PE0
3 AINA02/PD2
4 AINA01/PD1
5 AINA00/PD0
6 AVDD5
7 AVSS
8 DAC0/PG0
9 DAC1/PG1
10 UT3RXD/UT3TXDA/INT11/PA7
11 UT3TXDA/UT3RXD/INT07/PA6
12 T32A001NB1/EI2C1SDA/I2C1SDA/PA5
13 T32A001NB0/TSPI0CS1/EI2C1SCL/I2C1SCL/PA4
14 TRGIN1/T32A000UTB/TSPI0CS0/TSPI0CSIN/PA3
15 ENC0Z/T32A001NC1/T32A001INA1/TSPI0RXD/UT0TXDA/UT0RXD/PA2
16 ENC0B/T32A001NC0/T32A001INA0/TSPI0TXD/UT0RXD/UT0TXDA/PA1
17 ENC0A/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PA0
18 TRACEDATA1/T32A001INC1/T32A001INA1/TSPI0RXD/UT0TXDA/UT0RXD/INT09/PM2
19 TRACEDATA0/T32A001INC0/T32A001INA0/TSPI0TXD/UT0RXD/UT0TXDA/PM1
20 TRACECLK/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PM0
21 PB0/BOOT_N/T32A010UTA/T32A010UTC/SCOUT
22 PB1/INT03/RXIN0/T32A01INA0/T32A01INC0/TRGIN0
23 PB2/UT2TXDA/UT2RXD/TSPI1SCK/T32A01INA1/T32A01INC1
24 PB3/UT2RXD/UT2TXDA/TSPI1TXD/T32A010UTB
25 PB4/UT2CTS_N/UT2RTS_N/TSPI1RXD/T32A01INB0
26 PL0/UT2TXDA/UT2RXD/I2C2SCL/EI2C2SCL/TRST_N
27 PL1/UT2RXD/UT2TXDA/I2C2SDA/EI2C2SDA/TDI
28 PL2/UT2CTS_N/UT2RTS_N/T32A06OUTB/TDO/SWV
29 PL3/INT08/UT2RTS_N/UT2CTS_N/T32A06INB0/TCK/SWCLK
30 PL4/INT12/T32A06INB1/TMS/SWDIO
31 PP0/TSPI2SCK/T32A010UTA/T32A010UTC
32 PP1/TSPI2TXD/T32A01INA0/T32A01INC0
33 PP2/TSPI2RXD/T32A01INA1/T32A01INC1
34 DVDD5A
35 REGOUT2
36 PW0
37 DVSSA
38 PH0/X1/EHCLKIN
39 PH1/X2
40 RESET_N
41 PH2/XT1
42 PH3/XT2/INT06
43 MODE
44 PC0/INT00/I2C0SCL/EI2C0SCL/T32A020UTA/T32A020UTC/DCOM3
45 PC1/INT01/I2C0SDA/EI2C0SDA/T32A021INA0/T32A021INC0/DCOM2
46 PC2/INT02/UT4TXDB/T32A021INA1/T32A021INC1/RTCOUT/DCOM1
47 PC3/UT4TXDA/UT4RXD/T32A020UTB/DCOM0
48 PC4/UT4RXD/UT4TXDA/T32A021INB0/SEG39
49 PC5/UT4CTS_N/UT4RTS_N/T32A021INB1/SEG38
50 PC6/UT4RTS_N/UT4CTS_N/SEG37
51 PM4/UT5TXDB/T32A051INB0/SEG27
52 PM3/INT10/UT5TXDA/UT5RXD/T32A050UTB/TRGIN2/SEG26
53 PM2/UT5RXD/UT5TXDA/T32A051INA1/T32A051INC1/SEG25
54 PM1/UT5CTS_N/UT5RTS_N/T32A051INA0/T32A051INC0/SEG24
55 PM0/UT5RTS_N/UT5CTS_N/T32A050UTA/T32A050UTC/SEG23
56 PJ0/UT11TXDB/T32A030UTA/T32A030UTC/UD0/SEG22
57 PJ1/UT11TXDA/UT11RXD/T32A031INA0/T32A031INC0/XO0/SEG21
58 PJ2/UT11RXD/UT11TXDA/T32A031INA1/T32A031INC1/VO0/SEG20
59 PJ3/UT11CTS_N/UT11RTS_N/T32A030UTB/YO0/SEG19
60 PJ4/INT04/UT11RTS_N/UT11CTS_N/T32A031NB0/WO0/SEG18
61 SEG17/ZO0/T32A03INB1/PJ5
62 SEG16/EMG0/UT1TXDB/PK0
63 SEG15/OVV0/UT1RXD/UT1TXDA/INT05/PK1
64 SEG14/T32A040UTC/T32A040UTA/UT1TXDA/UT1RXD/PK2
65 SEG13/T32A04INC0/T32A04INA0/UT1RTS_N/UT1CTS_N/PK3
66 SEG12/T32A04INC1/T32A04INA1/UT1CTS_N/UT1RTS_N/PK4
67 SEG11/T32A040UTB/UT6TXDA/UT6RXD/PK5
68 SEG10/T32A04INB0/UT6RXD/UT6TXDA/PK6
69 SEG09/T32A04INB1/UT6TXDB/INT13/PK7
70 SEG08/TSPI3RXD/INT14/PP3
71 SEG07/TSPI3TXD/PP4
72 SEG06/TSPI3SCK/PP5
73 SEG05/PMDODBG/TSPI3CSIN/TSPI3CS0/PP6
74 AINA12/PF1
75 AINA11/PF0
76 AINA10/PE6
77 AINA09/PE5
78 AINA08/PE4
79 AINA07/PE3
80 AINA06/PE2

2.7. LQFP64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TMPM3HLFZAUG
TMPM3HLFYAUG
INDEX
1 AINA05/PE1
2 AINA04/PE0
3 AINA02/PD2
4 AINA01/PD1
5 AINA00/PD0
6 AVDD5
7 AVSS
8 DAC0/PG0
9 DAC1/PG1
10 UT3RXD/UT3TXDA/INT11/PA7
11 UT3TXDA/UT3RXD/INT07/PA6
12 TRGIN1/T32A00OUTB/TSPI0CS0/TSPI0CSIN/PA3
13 ENC0Z/T32A001INC1/T32A001INA1/TSPI0RXD/UT0TXDA/UT0RXD/PA2
14 ENC0B/T32A001INC0/T32A001INA0/TSPI0TXD/UT0RXD/UT0TXDA/PA1
15 ENC0A/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PA0
16 T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PM0
17 PB0/BOOT_N/T32A010UTA/T32A010UTC/SCOUT
18 PB1/INT03/RXIN0/T32A011INA0/T32A011INC0/TRGIN0
19 PB2/UT2TXDA/UT2RXD/T32A011INA1/T32A011INC1
20 PB3/UT2RXD/UT2TXDA/T32A010UTB
21 PL0/UT2TXDA/UT2RXD/I2C2SCL/EI2C2SCL/TRST_N
22 PL1/UT2RXD/UT2TXDA/I2C2SDA/EI2C2SDA/TDI
23 PL2/UT2CTS_N/UT2RTS_N/T32A060UTB/TDO/SWV
24 PL3/INT08/UT2RTS_N/UT2CTS_N/T32A06INB0/TCK/SWCLK
25 PL4/INT12/T32A06INB1/TMS/SWDIO
26 DVDD5A
27 REGOUT2
28 PW0
29 DVSSA
30 PH0/X1/EHCLKIN
31 PH1/X2
32 RESET_N
33 PH2/XT1
34 PH3/XT2/INT06
35 MODE
36 PC0/INT00/I2C0SCL/EI2C0SCL/T32A020UTA/T32A020UTC
37 PC1/INT01/I2C0SDA/EI2C0SDA/T32A021INA0/T32A021INC0
38 PC3/UT4TXDA/UT4RXD/T32A020UTB
39 PC4/UT4RXD/UT4TXDA/T32A021INB0
40 PN4/UT5TXDB/T32A051INB0
41 PN3/INT10/UT5TXDA/UT5RXD/T32A050UTB/TRGIN2
42 PN2/UT5RXD/UT5TXDA/T32A051INA1/T32A051INC1
43 PN1/UT5CTS_N/UT5RTS_N/T32A051INA0/T32A051INC0
44 PJ0/UT1TXDB/T32A030UTA/T32A030UTC/UO0
45 PJ1/UT1TXDA/UT1RXD/T32A031INA0/T32A031INC0/XO0
46 PJ2/UT1RXD/UT1TXDA/T32A031INA1/T32A031INC1/VO0
47 PJ3/UT1CTS_N/UT1RTS_N/T32A030UTB/YO0
48 PJ4/INT04/UT1RTS_N/UT1CTS_N/T32A031INB0/WO0
49 ZO0/T32A03INB1/PJ5
50 EMG0/UT1TXDB/PK0
51 OVV0/UT1RXD/UT1TXDA/INT05/PK1
52 T32A040UTC/T32A040UTA/UT1TXDA/UT1RXD/PK2
53 T32A04INC0/T32A04INA0/UT1RTS_N/UT1CTS_N/PK3
54 T32A04INC1/T32A04INA1/UT1CTS_N/UT1RTS_N/PK4
55 T32A040UTB/UT6TXDA/UT6RXD/PK5
56 T32A04INB0/UT6RXD/UT6TXDA/PK6
57 INT14/PP3
58 AINA12/PF1
59 AINA11/PF0
60 AINA10/PE6
61 AINA09/PE5
62 AINA08/PE4
63 AINA07/PE3
64 AINA06/PE2

3. Memory Map

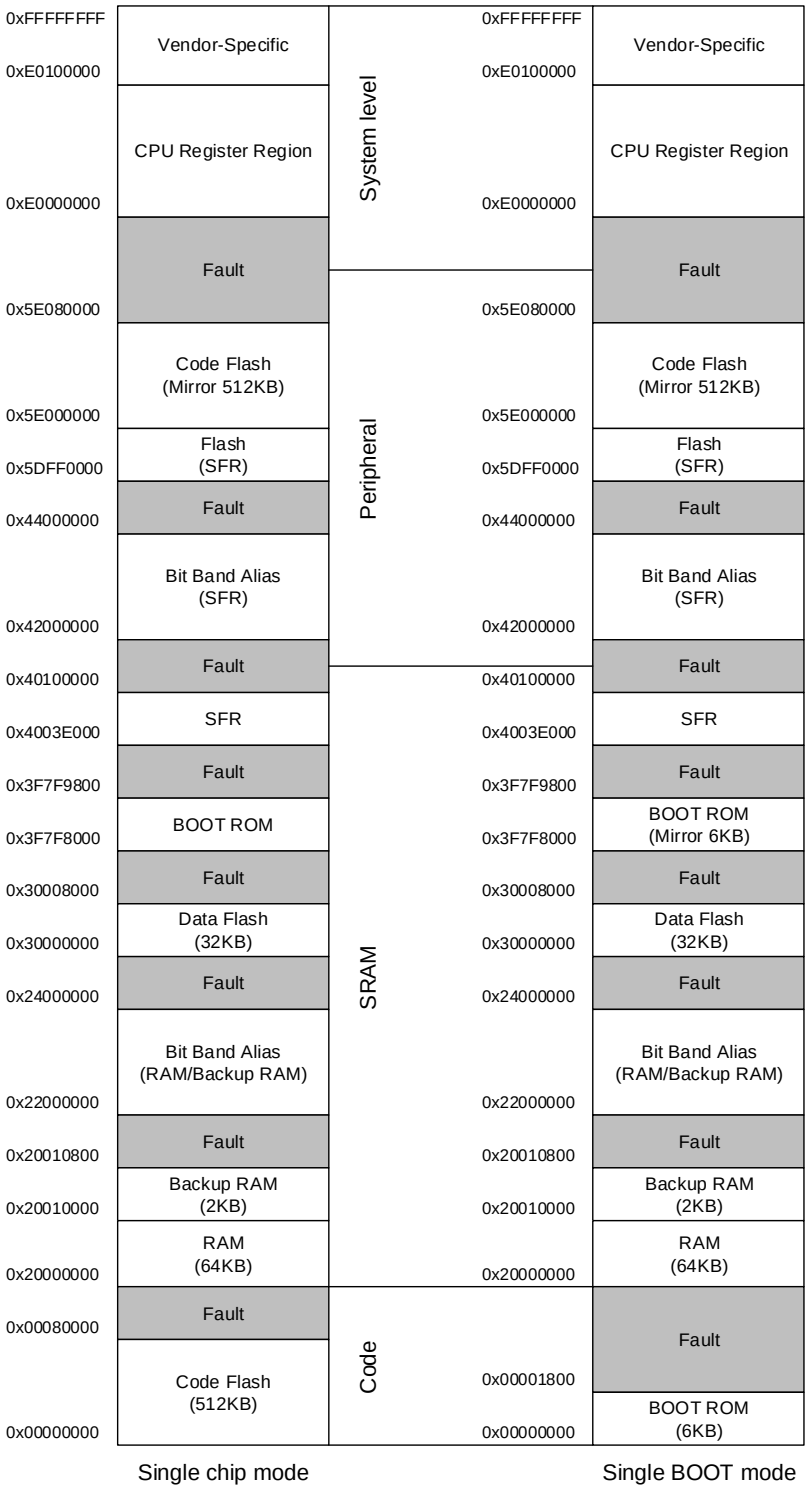


Figure 3.1 Example of the TMPM3HQFDAFG

Note: For detail of Single chip and Single Boot Mode, refer to the reference manual "Flash memory".

3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

Products			TMPM3HQFDAFG TMPM3HPFDAFG TMPM3HPFDADFG TMPM3HNFDAFG TMPM3HNFDADFG TMPM3HMFDAFG TMPM3HLFDAUG	TMPM3HQFZAFG TMPM3HPFZAFG TMPM3HPFZADFG TMPM3HNFZAFG TMPM3HNFZADFG TMPM3HMFZAFG TMPM3HLFZAUG	TMPM3HQFYAFG TMPM3HPFYAFG TMPM3HPFYADFG TMPM3HNFYAFG TMPM3HNFYADFG TMPM3HMFYAFG TMPM3HLFYAUG
Peripheral region	**Code Flash (Mirror)**	Size	512KB	384KB	256KB
		START	0x5E000000	0x5E000000	0x5E000000
		END	0x5E07FFFF	0x5E05FFFF	0x5E03FFFF
SRAM region	**Data Flash**	Size	32KB		
		START	0x30000000		
		END	0x30007FFF		
	Backup RAM	Size	2KB		
		START	0x20010000		
		END	0x200107FF		
	RAM	Size	64KB		
		START	0x20000000		
		END	0x2000FFFF		
Code region	**Code Flash**	Size	512KB	384KB	256KB
		START	0x00000000	0x00000000	0x00000000
		END	0x0007FFFF	0x0005FFFF	0x0003FFFF

4. Pin Description

4.1. Functional Pin Name and Functions

4.1.1. Function Pins of Peripheral

Table 4.1 Pin names and functions of peripheral pins

Peripheral function	Pin name	Input or Output	Function
Clock Control and Operation Mode (CG)	SCOUT	Output	Output pin for the system clock
Interrupt control (IA/IB)	INTx	Input	External interrupt input pin External input pin provides the noise filter (filter width: Typ. 30 ns).
32-bit Timer Event Counter (T32A)	T32AxINA0	Input	16-bit timer-A input capture input pin 0
	T32AxINA1	Input	16-bit timer-A input capture input pin 1
	T32AxOUTA	Output	16-bit timer A output pin
	T32AxINB0	Input	16-bit timer B input capture input pin 0
	T32AxINB1	Input	16-bit timer B input capture input pin 1
	T32AxOUTB	Output	16-bit timer B output pin
	T32AxINC0	Input	32-bit timer input capture input pin 0
	T32AxINC1	Input	32-bit timer input capture input pin 1
	T32AxOUTC	Output	32-bit timer output pin
Serial Peripheral Interface (TSPI)	TSPIxCSIN	Input	TSPI Chip select input pin
	TSPIxCS0	Output	TSPI Chip select output pin 0
	TSPIxCS1	Output	TSPI Chip select output pin 1
	TSPIxRXD	Input	TSPI Data input pin
	TSPIxTXD	Output	TSPI Data output pin
	TSPIxSCK	I/O	TSPI Clock input/output pin
Universal Asynchronous Receiver Transmitter (UART)	UTxRXD	Input	UART Data input pin
	UTxTXDA	Output	UART Data output pin A
	UTxTXDB	Output	UART Data output pin B
	UTxCTS_N	Input	UART Transmission control input pin
	UTxRTS_N	Output	UART Transmission request output pin
I^2C Interface (I2C/EI2C)	I2CxSDA/ EI2CxSDA	I/O	I^2C interface Data input/output pin
	I2CxSCL/ EI2CxSCL	I/O	I^2C interface Clock input/output pin

Peripheral function	Pin name	Input or Output	Function
Advanced Programmable Motor Control Circuit (A-PMD)	EMGx	Input	Emergency state detection input pin
	OVVx	Input	Over voltage detection input
	UOx	Output	U-phase output pin
	VOx	Output	V-phase output pin
	WOx	Output	W-phase output pin
	XOx	Output	X-phase output pin
	YOx	Output	Y-phase output pin
	ZOx	Output	Z-phase output pin
	PMDxDBG	Output	PMD Operation Status output pin
Advanced Encoder Input Circuit (A-ENC)	ENCxA	Input	Encoder input A
	ENCxB	Input	Encoder input B
	ENCxZ	Input	Encoder input Z
Analog to Digital Converter (ADC)	AINAx	Input	Analog input pin
Digital to Analog Converter (DAC)	DACx	Output	DAC output pin
Trigger input	TRGINx	Input	External trigger input pin
Remote control signal preprocessor (RMC)	RXINx	Input	Remote Signaling Data input pin
Real Time clock (RTC)	RTCOUT	Output	1Hz clock output pin
LCD Display control circuit (DLCD)	DCOMx	Output	Common output pin
	SEGx	Output	Segment output pin

Note: "x" means channel number, unit number or interrupt number.

4.1.2. Debug Pins

Table 4.2 Debug pin names and their function

Debug Function	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input pin
	TCK	Input	JTAG serial clock input pin
	TDO	Output	JTAG serial data output pin
	TDI	Input	JTAG serial data input pin
	TRST_N	Input	JTAG test reset input pin
SW	SWDIO	I/O	Serial wire data input/output pin
	SWCLK	Input	Serial wire clock input pin
	SWV	Output	Serial wire viewer output pin
TRACE	TRACECLK	Output	Trace clock output pin
	TRACEDATA0	Output	Trace data output pin 0
	TRACEDATA1	Output	Trace data output pin 1
	TRACEDATA2	Output	Trace data output pin 2
	TRACEDATA3	Output	Trace data output pin 3

4.1.3. Control Pins

Table 4.3 Control pin names and their function

	Pin name	Input or Output	Function
Control Pin	X1	Input	High speed oscillator connection pin
	X2	Output	High speed oscillator connection pin
	XT1	Input	Low speed oscillator connection pin
	XT2	Output	Low speed oscillator connection pin
	EHCLKIN	Input	External high speed Clock input pin
	BOOT_N	Input	BOOT mode control pin The BOOT mode control pin is sampled at the rising edge of the RESET_N pin input. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters the Single Boot Mode. If it is "High", the MCU enters the Single Chip Mode. For details of Single Boot Mode, refer to the reference manual "Flash Memory".
	RESET_N	Input	Reset signal input pin
	MODE	Input	Mode pin This pin must be fixed to "Low" level.

4.1.4. Power Supply Pins

Table 4.4 Power supply pin names and their function

	Pin name	Function
Power Supply	DVDD5A (Note 1) DVDD5B (Note 1)	Power supply pin for digital DVDD5A/B supply the power to the following pins: PA to PC, PG2 to PG7, PH to PW, MODE, RESET_N, BOOT_N A power supply is supplied to an oscillating circuit from a built-in regulator. X1, X2, XT1, XT2
	DVSSA (Note 2) DVSSB (Note 2)	GND pin for digital
	REGOUT2 (Note 3)	Capacitor for a regulator connection pin (Note 4)
	AVDD5	Power supply pin and reference power pin (VREFH) for analog are combination pins. The AVDD5 supplies the power to the following pins: PD, PE, PF, PG0 to 1
	AVSS	GND pin for analog, reference GND (VREFL) for analog are combination pins.

Note 1: Apply the voltage to DVDD5Aand DVDD5B at the same potential except the case that the pins are not provided.

Note 2: Apply the external voltage to DVSSA and DVSSB at the same potential except the case that the pins are not provided.

Note 3: For REGOUT2, do not cause a short circuit with DVDD5A, DVDD5B; or DVSSA, DVSSB.

Note 4: Regarding value of capacitor, refer to "7.13 Regulator".

4.1.5. Capacitors between power supply pins

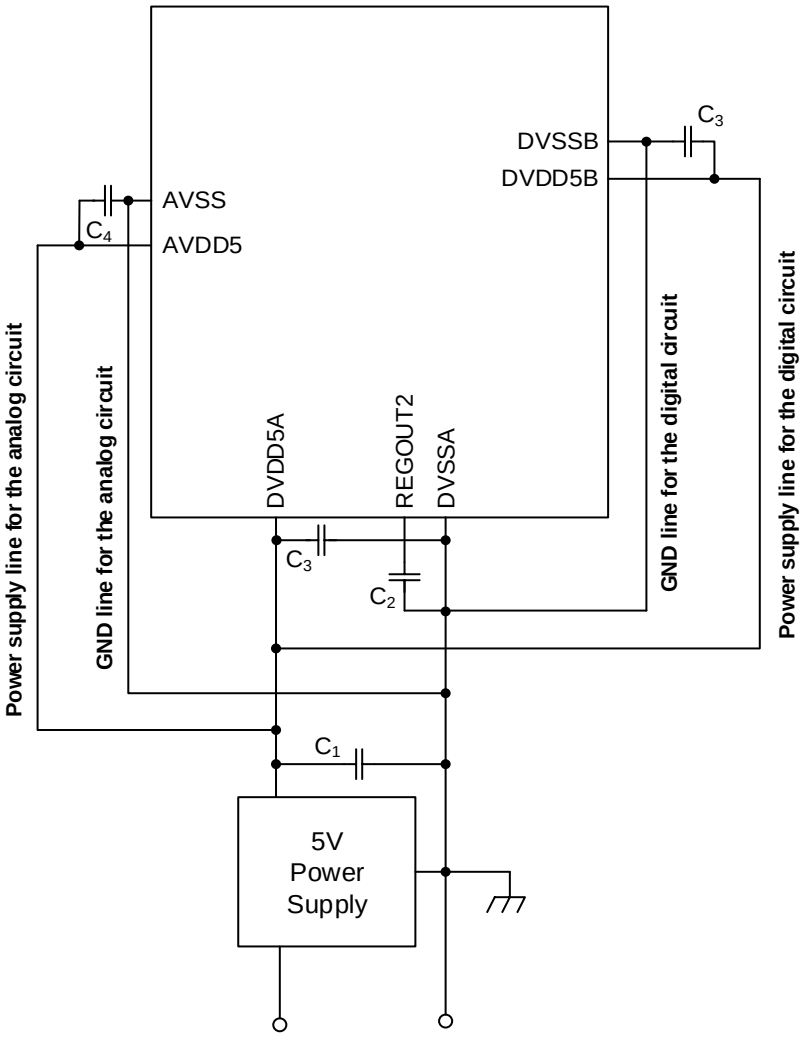


Figure 4.1 Capacitors for power supply pins connection circuit

Note 1: 5V power supply output capacitor (C_1) must be placed on the shortest distance from the output pin of 5V power supply. The power gradient with C_1 must be satisfied V_{PON} and V_{POFF} in "7.7 Characteristics of Internal processing at RESET".

Note 2: Bypass capacitor must be placed between the 5V power supply and GND near each MCU power supply pin. (C_3, C_4:0.01 to 0.1μF)

Note 3: Power stabilizing capacitor of REGOUT2 for built-in regulators must be the capacity (C_2), and ceramic capacitor is recommended for C_2. It must be placed on the shortest distance from DVSSA. Regarding value of capacitor, refer to "7.13 Regulator".

Note 4: Separate the analog power supply line and the digital power supply line near the 5V power supply output pin in order to reduce noise mixing into the analog circuit from the digital power supply.

Note 5: When inserting a filter circuit or pull-up/down resistor at the input/output pin of the analog power supply system to reduce noise mixing from the peripheral circuit to the analog circuit, connect the components that make up these circuits to the analog power supply line.

Note 6: Do not separate the power supply line and the GND line from each other in order to reduce high frequency noise etc., received by the loop circuit of the power supply line, the GND line, and the capacitor.

4.2. Functional Pin and Ports Assignment (Pin Number)

The following table shows a pin number of the port assignment and each product which were seen from the functional pin. "-" means that it does not have a pin or there is no assignment of a function.

Table 4.5 Signal connection List (UART ch0, ch1)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
UT0TXDA	PA1	27	23	26	17	19	16	14
	PA2	26	22	25	16	18	15	13
	PM1	35	31	34	24	26	19	-
	PM2	34	30	33	23	25	18	-
UT0TXDB	PA0	28	24	27	18	20	17	15
	PM0	36	32	35	25	27	20	16
UT0RXD	PA2	26	22	25	16	18	15	13
	PA1	27	23	26	17	19	16	14
	PM2	34	30	33	23	25	18	-
	PM1	35	31	34	24	26	19	-
UT0CTS_N	PM3	33	29	32	22	24	-	-
	PM4	32	28	31	21	23	-	-
UT0RTS_N	PM4	32	28	31	21	23	-	-
	PM3	33	29	32	22	24	-	-
UT1TXDA	PJ1	105	92	95	72	74	57	45
	PJ2	106	93	96	73	75	58	46
	PK1	111	98	101	78	80	63	51
	PK2	112	99	102	79	81	64	52
UT1TXDB	PJ0	104	91	94	71	73	56	44
	PK0	110	97	100	77	79	62	50
UT1RXD	PJ2	106	93	96	73	75	58	46
	PJ1	105	92	95	72	74	57	45
	PK2	112	99	102	79	81	64	52
	PK1	111	98	101	78	80	63	51
UT1CTS_N	PJ3	107	94	97	74	76	59	47
	PJ4	108	95	98	75	77	60	48
	PK3	113	100	103	80	82	65	53
	PK4	114	101	104	81	83	66	54
UT1RTS_N	PJ4	108	95	98	75	77	60	48
	PJ3	107	94	97	74	76	59	47
	PK4	114	101	104	81	83	66	54
	PK3	113	100	103	80	82	65	53

Table 4.6 Signal connection List (URAT ch2, ch3)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
UT2TXDA	PB2	39	35	38	28	30	23	19
	PB3	40	36	39	29	31	24	20
	PL0	47	41	44	34	36	26	21
	PL1	48	42	45	35	37	27	22
UT2RXD	PB3	40	36	39	29	31	24	20
	PB2	39	35	38	28	30	23	19
	PL1	48	42	45	35	37	27	22
	PL0	47	41	44	34	36	26	21
UT2CTS_N	PB4	41	37	40	30	32	25	-
	PB5	42	38	41	31	33	-	-
	PL2	49	43	46	36	38	28	23
	PL3	50	44	47	37	39	29	24
UT2RTS_N	PB5	42	38	41	31	33	-	-
	PB4	41	37	40	30	32	25	-
	PL3	50	44	47	37	39	29	24
	PL2	49	43	46	36	38	28	23
UT3TXDA	PA7	21	17	20	11	13	10	10
	PA6	22	18	21	12	14	11	11
	PG3	16	12	15	-	-	-	-
	PG2	15	11	14	-	-	-	-
UT3TXDB	PG4	17	13	16	-	-	-	-
UT3RXD	PA6	22	18	21	12	14	11	11
	PA7	21	17	20	11	13	10	10
	PG2	15	11	14	-	-	-	-
	PG3	16	12	15	-	-	-	-

Table 4.7 Signal connection List (UART ch4 to 7)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
UT4TXDA	PC3	86	73	76	57	59	47	38
	PC4	87	74	77	58	60	48	39
	PV6	81	-	-	-	-	-	-
	PV7	82	-	-	-	-	-	-
UT4TXDB	PC2	85	72	75	56	58	46	-
	PV5	80	-	-	-	-	-	-
UT4RXD	PC4	87	74	77	58	60	48	39
	PC3	86	73	76	57	59	47	38
	PV7	82	-	-	-	-	-	-
	PV6	81	-	-	-	-	-	-
UT4CTS_N	PC5	88	75	78	59	61	49	-
	PC6	89	76	79	60	62	50	-
UT4RTS_N	PC6	89	76	79	60	62	50	-
	PC5	88	75	78	59	61	49	-
UT5TXDA	PN3	100	87	90	67	69	52	41
	PN2	101	88	91	68	70	53	42
UT5TXDB	PN4	99	86	89	66	68	51	40
UT5RXD	PN2	101	88	91	68	70	53	42
	PN3	100	87	90	67	69	52	41
UT5CTS_N	PN1	102	89	92	69	71	54	43
	PN0	103	90	93	70	72	55	-
UT5RTS_N	PN0	103	90	93	70	72	55	-
	PN1	102	89	92	69	71	54	43
UT6TXDA	PK6	116	103	106	83	85	68	56
	PK5	115	102	105	82	84	67	55
UT6TXDB	PK7	117	104	107	84	86	69	-
UT6RXD	PK5	115	102	105	82	84	67	55
	PK6	116	103	106	83	85	68	56
UT7TXDA	PR1	91	78	81	62	64	-	-
	PR0	90	77	80	61	63	-	-
UT7TXDB	PR2	92	79	82	63	65	-	-
UT7RXD	PR0	90	77	80	61	63	-	-
	PR1	91	78	81	62	64	-	-

Table 4.8 Signal connection List (I2C/EI2C ch0 to 3/TSPI ch0, ch1)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
I2C0SCL	PC0	83	70	73	54	56	44	36
I2C0SDA	PC1	84	71	74	55	57	45	37
I2C1SCL	PA4	24	20	23	14	16	13	-
I2C1SDA	PA5	23	19	22	13	15	12	-
I2C2SCL	PL0	47	41	44	34	36	26	21
I2C2SDA	PL1	48	42	45	35	37	27	22
I2C3SCL	PT1	61	51	54	-	-	-	-
I2C3SDA	PT0	62	52	55	-	-	-	-
EI2C0SCL	PC0	83	70	73	54	56	44	36
EI2C0SDA	PC1	84	71	74	55	57	45	37
EI2C1SCL	PA4	24	20	23	14	16	13	-
EI2C1SDA	PA5	23	19	22	13	15	12	-
EI2C2SCL	PL0	47	41	44	34	36	26	21
EI2C2SDA	PL1	48	42	45	35	37	27	22
EI2C3SCL	PT1	61	51	54	-	-	-	-
EI2C3SDA	PT0	62	52	55	-	-	-	-
TSPI0SCK	PM0	36	32	35	25	27	20	16
	PA0	28	24	27	18	20	17	15
TSPI0TXD	PM1	35	31	34	24	26	19	-
	PA1	27	23	26	17	19	16	14
TSPI0RXD	PM2	34	30	33	23	25	18	-
	PA2	26	22	25	16	18	15	13
TSPI0CS0	PM3	33	29	32	22	24	-	-
	PA3	25	21	24	15	17	14	12
TSPI0CS1	PM4	32	28	31	21	23	-	-
	PA4	24	20	23	14	16	13	-
TSPI0CSIN	PM3	33	29	32	22	24	-	-
	PA3	25	21	24	15	17	14	12
TSPI1SCK	PB2	39	35	38	28	30	23	-
TSPI1TXD	PB3	40	36	39	29	31	24	-
TSPI1RXD	PB4	41	37	40	30	32	25	-
TSPI1CS0	PB5	42	38	41	31	33	-	-
TSPI1CS1	PB6	43	39	42	32	34	-	-
TSPI1CSIN	PB5	42	38	41	31	33	-	-

Table 4.9 Signal connection List (TSPI ch2 to 4)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
TSPI2SCK	PP0	63	53	56	41	43	31	-
	PT2	60	50	53	-	-	-	-
TSPI2TXD	PP1	64	54	57	42	44	32	-
	PT3	59	49	52	-	-	-	-
TSPI2RXD	PP2	65	55	58	43	45	33	-
	PT4	58	-	-	-	-	-	-
TSPI2CS0	PT1	61	51	54	-	-	-	-
TSPI2CS1	PT0	62	52	55	-	-	-	-
TSPI2CSIN	PT1	61	51	54	-	-	-	-
TSPI3SCK	PP5	120	107	110	87	89	72	-
TSPI3TXD	PP4	119	106	109	86	88	71	-
TSPI3RXD	PP3	118	105	108	85	87	70	-
TSPI3CS0	PP6	121	108	111	88	90	73	-
TSPI3CS1	PP7	122	109	112	89	91	-	-
TSPI3CSIN	PP6	121	108	111	88	90	73	-
TSPI4SCK	PH4	76	66	69	-	-	-	-
TSPI4TXD	PH5	77	67	70	-	-	-	-
TSPI4RXD	PH6	78	68	71	-	-	-	-

Table 4.10 Signal Connection List (T32A ch0)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
T32A00OUTA	PA0	28	24	27	18	20	17	15
	PM0	36	32	35	25	27	20	16
T32A00OUTB	PA3	25	21	24	15	17	14	12
	PM3	33	29	32	22	24	-	-
T32A00OUTC	PA0	28	24	27	18	20	17	15
	PM0	36	32	35	25	27	20	16
T32A00INA0	PA1	27	23	26	17	19	16	14
	PM1	35	31	34	24	26	19	-
T32A00INA1	PA2	26	22	25	16	18	15	13
	PM2	34	30	33	23	25	18	-
T32A00INB0	PA4	24	20	23	14	16	13	-
	PM4	32	28	31	21	23	-	-
T32A00INB1	PA5	23	19	22	13	15	12	-
	PM5	31	27	30	20	22	-	-
T32A00INC0	PA1	27	23	26	17	19	16	14
	PM1	35	31	34	24	26	19	-
T32A00INC1	PA2	26	22	25	16	18	15	13
	PM2	34	30	33	23	25	18	-

Table 4.11 Signal connection List (T32A ch1, ch2)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
T32A01OUTA	PB0	37	33	36	26	28	21	17
	PP0	63	53	56	41	43	31	-
T32A01OUTB	PB3	40	36	39	29	31	24	20
T32A01OUTC	PB0	37	33	36	26	28	21	17
	PP0	63	53	56	41	43	31	-
T32A01INA0	PB1	38	34	37	27	29	22	18
	PP1	64	54	57	42	44	32	-
T32A01INA1	PB2	39	35	38	28	30	23	19
	PP2	65	55	58	43	45	33	-
T32A01INB0	PB4	41	37	40	30	32	25	-
T32A01INB1	PB5	42	38	41	31	33	-	-
T32A01INC0	PB1	38	34	37	27	29	22	18
	PP1	64	54	57	42	44	32	-
T32A01INC1	PB2	39	35	38	28	30	23	19
	PP2	65	55	58	43	45	33	-
T32A02OUTA	PC0	83	70	73	54	56	44	36
	PR0	90	77	80	61	63	-	-
T32A02OUTB	PC3	86	73	76	57	59	47	38
T32A02OUTC	PC0	83	70	73	54	56	44	36
	PR0	90	77	80	61	63	-	-
T32A02INA0	PC1	84	71	74	55	57	45	37
	PR1	91	78	81	62	64	-	-
T32A02INA1	PC2	85	72	75	56	58	46	-
	PR2	92	79	82	63	65	-	-
T32A02INB0	PC4	87	74	77	58	60	48	39
T32A02INB1	PC5	88	75	78	59	61	49	-
T32A02INC0	PC1	84	71	74	55	57	45	37
	PR1	91	78	81	62	64	-	-
T32A02INC1	PC2	85	72	75	56	58	46	-
	PR2	92	79	82	63	65	-	-

Table 4.12 Signal connection List (T32A ch3 to 5)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
T32A03OUTA	PJ0	104	91	94	71	73	56	44
T32A03OUTB	PJ3	107	94	97	74	76	59	47
T32A03OUTC	PJ0	104	91	94	71	73	56	44
T32A03INA0	PJ1	105	92	95	72	74	57	45
T32A03INA1	PJ2	106	93	96	73	75	58	46
T32A03INB0	PJ4	108	95	98	75	77	60	48
T32A03INB1	PJ5	109	96	99	76	78	61	49
T32A03INC0	PJ1	105	92	95	72	74	57	45
T32A03INC1	PJ2	106	93	96	73	75	58	46
T32A04OUTA	PK2	112	99	102	79	81	64	52
T32A04OUTB	PK5	115	102	105	82	84	67	55
T32A04OUTC	PK2	112	99	102	79	81	64	52
T32A04INA0	PK3	113	100	103	80	82	65	53
T32A04INA1	PK4	114	101	104	81	83	66	54
T32A04INB0	PK6	116	103	106	83	85	68	56
T32A04INB1	PK7	117	104	107	84	86	69	-
T32A04INC0	PK3	113	100	103	80	82	65	53
T32A04INC1	PK4	114	101	104	81	83	66	54
T32A05OUTA	PN0	103	90	93	70	72	55	-
T32A05OUTB	PN3	100	87	90	67	69	52	41
T32A05OUTC	PN0	103	90	93	70	72	55	-
T32A05INA0	PN1	102	89	92	69	71	54	43
T32A05INA1	PN2	101	88	91	68	70	53	42
T32A05INB0	PN4	99	86	89	66	68	51	40
T32A05INB1	PN5	98	85	88	65	67	-	-
T32A05INC0	PN1	102	89	92	69	71	54	43
T32A05INC1	PN2	101	88	91	68	70	53	42

Table 4.13 Signal connection List (T32A ch6, ch7)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
T32A06OUTA	PL5	52	46	49	39	41	-	-
	PT5	57	-	-	-	-	-	-
T32A06OUTB	PL2	49	43	46	36	38	28	23
	PT2	60	50	53	-	-	-	-
T32A06OUTC	PL5	52	46	49	39	41	-	-
	PT5	57	-	-	-	-	-	-
T32A06INA0	PL6	53	47	50	40	42	-	-
	PT6	56	-	-	-	-	-	-
T32A06INA1	PL7	54	48	51	-	-	-	-
	PT7	55	-	-	-	-	-	-
T32A06INB0	PL3	50	44	47	37	39	29	24
	PT3	59	49	52	-	-	-	-
T32A06INB1	PL4	51	45	48	38	40	30	25
	PT4	58	-	-	-	-	-	-
T32A06INC0	PL6	53	47	50	40	42	-	-
	PT6	56	-	-	-	-	-	-
T32A06INC1	PL7	54	48	51	-	-	-	-
	PT7	55	-	-	-	-	-	-
T32A07OUTA	PG2	15	11	14	-	-	-	-
T32A07OUTB	PG5	18	14	17	-	-	-	-
T32A07OUTC	PG2	15	11	14	-	-	-	-
T32A07INA0	PG3	16	12	15	-	-	-	-
T32A07INA1	PG4	17	13	16	-	-	-	-
T32A07INB0	PG6	19	15	18	-	-	-	-
T32A07INB1	PG7	20	16	19	-	-	-	-
T32A07INC0	PG3	16	12	15	-	-	-	-
T32A07INC1	PG4	17	13	16	-	-	-	-

Table 4.14 Signal connection List (ADC ch0 to 20/DAC ch0, ch1)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
AINA00	PD0	6	6	9	6	8	5	5
AINA01	PD1	5	5	8	5	7	4	4
AINA02	PD2	4	4	7	4	6	3	3
AINA03	PD3	3	3	6	3	5	-	-
AINA04	PE0	2	2	5	2	4	2	2
AINA05	PE1	1	1	4	1	3	1	1
AINA06	PE2	144	128	3	100	2	80	64
AINA07	PE3	143	127	2	99	1	79	63
AINA08	PE4	142	126	1	98	100	78	62
AINA09	PE5	141	125	128	97	99	77	61
AINA10	PE6	140	124	127	96	98	76	60
AINA11	PF0	139	123	126	95	97	75	59
AINA12	PF1	138	122	125	94	96	74	58
AINA13	PF2	137	121	124	93	95	-	-
AINA14	PF3	136	120	123	92	94	-	-
AINA15	PF4	135	119	122	91	93	-	-
AINA16	PF5	134	118	121	90	92	-	-
AINA17	PF6	133	117	120	-	-	-	-
AINA18	PF7	132	116	119	-	-	-	-
AINA19	PD4	131	-	-	-	-	-	-
AINA20	PD5	130	-	-	-	-	-	-
DAC0	PG0	9	9	12	9	11	8	8
DAC1	PG1	10	10	13	10	12	9	9

Table 4.15 Signal connection List (INT 00 to 33)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
INT00	PC0	83	70	73	54	56	44	36
INT01	PC1	84	71	74	55	57	45	37
INT02	PC2	85	72	75	56	58	46	-
INT03	PB1	38	34	37	27	29	22	18
INT04	PJ4	108	95	98	75	77	60	48
INT05	PK1	111	98	101	78	80	63	51
INT06	PH3	74	64	67	52	54	42	34
INT07	PA6	22	18	21	12	14	11	11
INT08	PL3	50	44	47	37	39	29	24
INT09	PM2	34	30	33	23	25	18	-
INT10	PN3	100	87	90	67	69	52	41
INT11	PA7	21	17	20	11	13	10	10
INT12	PL4	51	45	48	38	40	30	25
INT13	PK7	117	104	107	84	86	69	-
INT14	PP3	118	105	108	85	87	70	57
INT15	PM6	30	26	29	19	21	-	-
INT16	PB7	44	40	43	33	35	-	-
INT17	PV2	125	112	115	-	-	-	-
INT18	PV3	126	113	116	-	-	-	-
INT19	PH4	76	66	69	-	-	-	-
INT20	PH5	77	67	70	-	-	-	-
INT21	PH6	78	68	71	-	-	-	-
INT22	PH7	79	69	72	-	-	-	-
INT23	PT0	62	52	55	-	-	-	-
INT24	PT1	61	51	54	-	-	-	-
INT25	PT2	60	50	53	-	-	-	-
INT26	PT3	59	49	52	-	-	-	-
INT27	PG2	15	11	14	-	-	-	-
INT28	PG3	16	12	15	-	-	-	-
INT29	PT7	55	-	-	-	-	-	-
INT30	PU0	45	-	-	-	-	-	-
INT31	PU1	46	-	-	-	-	-	-
INT32	PF3	136	120	123	92	94	-	-
INT33	PF2	137	121	124	93	95	-	-

Table 4.16 Signal connection List (A-PMD/A-ENC/SCOUT/TRGIN/RMC/RTC)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
UO0	PJ0	104	91	94	71	73	56	44
XO0	PJ1	105	92	95	72	74	57	45
VO0	PJ2	106	93	96	73	75	58	46
YO0	PJ3	107	94	97	74	76	59	47
WO0	PJ4	108	95	98	75	77	60	48
ZO0	PJ5	109	96	99	76	78	61	49
EMG0	PK0	110	97	100	77	79	62	50
OVV0	PK1	111	98	101	78	80	63	51
ENC0A	PA0	28	24	27	18	20	17	15
ENC0B	PA1	27	23	26	17	19	16	14
ENC0Z	PA2	26	22	25	16	18	15	13
PMD0DBG	PP6	121	108	111	88	90	73	-
SCOUT	PB0	37	33	36	26	28	21	17
TRGIN0	PB1	38	34	37	27	29	22	18
TRGIN1	PA3	25	21	24	15	17	14	12
TRGIN2	PN3	100	87	90	67	69	52	41
RXIN0	PB1	38	34	37	27	29	22	18
RTCOUT	PC2	85	72	75	56	58	46	-

Table 4.17 Signal connection List (JTAG/SW/TRACE/OSC/BOOT)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
TMS	PL4	51	45	48	38	40	30	25
TCK	PL3	50	44	47	37	39	29	24
TDO	PL2	49	43	46	36	38	28	23
TDI	PL1	48	42	45	35	37	27	22
TRST_N	PL0	47	41	44	34	36	26	21
SWDIO	PL4	51	45	48	38	40	30	25
SWCLK	PL3	50	44	47	37	39	29	24
SWV	PL2	49	43	46	36	38	28	23
TRACECLK	PM0	36	32	35	25	27	20	-
TRACEDATA0	PM1	35	31	34	24	26	19	-
TRACEDATA1	PM2	34	30	33	23	25	18	-
TRACEDATA2	PM3	33	29	32	22	24	-	-
TRACEDATA3	PM4	32	28	31	21	23	-	-
X1	PH0	70	60	63	48	50	38	30
X2	PH1	71	61	64	49	51	39	31
XT1	PH2	73	63	66	51	53	41	33
XT2	PH3	74	64	67	52	54	42	34
EHCLKIN	PH0	70	60	63	48	50	38	30
BOOT_N	PB0	37	33	36	26	28	21	17

Table 4.18 Signal connection List (DLCD)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
DCOM0	PC3	86	73	76	57	59	47	-
DCOM1	PC2	85	72	75	56	58	46	-
DCOM2	PC1	84	71	74	55	57	45	-
DCOM3	PC0	83	70	73	54	56	44	-
SEG00	PV3	126	113	116	-	-	-	-
SEG01	PV2	125	112	115	-	-	-	-
SEG02	PV1	124	111	114	-	-	-	-
SEG03	PV0	123	110	113	-	-	-	-
SEG04	PP7	122	109	112	89	91	-	-
SEG05	PP6	121	108	111	88	90	73	-
SEG06	PP5	120	107	110	87	89	72	-
SEG07	PP4	119	106	109	86	88	71	-
SEG08	PP3	118	105	108	85	87	70	-
SEG09	PK7	117	104	107	84	86	69	-
SEG10	PK6	116	103	106	83	85	68	-
SEG11	PK5	115	102	105	82	84	67	-
SEG12	PK4	114	101	104	81	83	66	-
SEG13	PK3	113	100	103	80	82	65	-
SEG14	PK2	112	99	102	79	81	64	-
SEG15	PK1	111	98	101	78	80	63	-
SEG16	PK0	110	97	100	77	79	62	-
SEG17	PJ5	109	96	99	76	78	61	-
SEG18	PJ4	108	95	98	75	77	60	-
SEG19	PJ3	107	94	97	74	76	59	-
SEG20	PJ2	106	93	96	73	75	58	-
SEG21	PJ1	105	92	95	72	74	57	-
SEG22	PJ0	104	91	94	71	73	56	-
SEG23	PN0	103	90	93	70	72	55	-
SEG24	PN1	102	89	92	69	71	54	-
SEG25	PN2	101	88	91	68	70	53	-
SEG26	PN3	100	87	90	67	69	52	-
SEG27	PN4	99	86	89	66	68	51	-
SEG28	PN5	98	85	88	65	67	-	-
SEG29	PR7	97	84	87	-	-	-	-
SEG30	PR6	96	83	86	-	-	-	-
SEG31	PR5	95	82	85	-	-	-	-
SEG32	PR4	94	81	84	-	-	-	-

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
SEG33	PR3	93	80	83	64	66	-	-
SEG34	PR2	92	79	82	63	65	-	-
SEG35	PR1	91	78	81	62	64	-	-
SEG36	PR0	90	77	80	61	63	-	-
SEG37	PC6	89	76	79	60	62	50	-
SEG38	PC5	88	75	78	59	61	49	-
SEG39	PC4	87	74	77	58	60	48	-

Table 4.19 Signal connection List (PORT/CONTROL/POWER)

Combination function pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
-	PM7	29	25	28	-	-	-	-
-	PU2	14	-	-	-	-	-	-
-	PU3	13	-	-	-	-	-	-
-	PU4	12	-	-	-	-	-	-
-	PU5	11	-	-	-	-	-	-
-	PV4	127	-	-	-	-	-	-
-	PW0	68	58	61	46	48	36	28
RESET_N	-	72	62	65	50	52	40	32
MODE	-	75	65	68	53	55	43	35
AVDD5	-	7	7	10	7	9	6	6
AVSS	-	8	8	11	8	10	7	7
DVDD5A	-	66	56	59	44	46	34	26
DVDD5B	-	128	114	117	-	-	-	-
DVSSA	-	69	59	62	47	49	37	29
DVSSB	-	129	115	118	-	-	-	-
REGOUT2	-	67	57	60	45	47	35	27

4.3. Ports

The symbols of each table of the port have the following meanings.

The right-hand side of the port shows specification with the symbol.

- Input/Output: Input and/or Output of Port
  Input: Input port
  Output: Output port
  I/O: Input/Output port

- PU/PD: Programmable pull-up/pull-down
  PU: Programmable pull-up is selectable
  PD: Programmable pull-down is selectable

- OD: Programmable open-drain output
  Yes: Support
  No: Not support

- 5V_T: 5V-tolerant
  Yes: Support
  N/A: Not available

- SMT/CMOS: Input gate
  SMT: Schmitt trigger input
  CMOS: CMOS input

- Under Reset: Port state under Reset
  Hi-Z: High impedance
  PU: Pull-up
  PD: Pull-down

- After Reset: Port state after Reset
  Hi-Z: High impedance
  PU: Pull-up
  PD: Pull-down

4.3.1. Port Specifications Table

Table 4.20 Port names, and specifications of Port A, B, C, D, E

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/CMOS	Under Reset	After Reset
PA0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA4	I/O	PU/PD	YES	YES	SMT	Hi-Z	Hi-Z
PA5	I/O	PU/PD	YES	YES	SMT	Hi-Z	Hi-Z
PA6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB0	Output	PU/PD (Note)	YES	N/A	SMT	Hi-Z (Note)	Hi-Z
PB1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Note: combination with BOOT_N. When RESET_N pin is "Low" level, pull-up resistor is enabled. When RESET_N pin is "High" level, the pin state is Hi-Z with internal reset.

Table 4.21 Port names, and specifications of Port F, G, H, J, K

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/CMOS	Under Reset	After Reset
PF0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH0	Input	PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH1	Input	PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH2	Input	PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH3	Input	PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Table 4.22 Port names, and specifications of Port L, M, N, P, R

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/CMOS	Under Reset	After Reset
PL0	I/O	PU/PD	YES	N/A	SMT	PU (Note)	PU (Note)
PL1	I/O	PU/PD	YES	N/A	SMT	PU (Note)	PU (Note)
PL2	I/O	PU/PD	YES	N/A	SMT	Hi-Z (Note)	Hi-Z (Note)
PL3	I/O	PU/PD	YES	N/A	SMT	PD (Note)	PD (Note)
PL4	I/O	PU/PD	YES	N/A	SMT	PU (Note)	PU (Note)
PL5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Note: It is assigned to a debug pin in the state of the initial stage.
(PL4: TMS/SWDIO, PL3:TCK/SWCLK, PL2:TDO/SWV, PL1:TDI, PL0:TRST_N)

Table 4.23 Port names, and specifications of Port T, U, V, W

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/CMOS	Under Reset	After Reset
PT0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PW0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

5. Functional Description and Operation Description

5.1. Reference Manuals

For more information on the product of TMPM3H Group(1), please refer to Reference Manuals below.

Table 5.1 Reference Manuals for TMPM3H Group(1)

Reference Manual	IP Symbol	Category
Port (TMPM3H Group(1))	PORT-M3H(1)	System
Exception (TMPM3H Group(1))	EXCEPT-M3H(1)	System
Clock Control and operation mode (TMPM3H Group(1))	CG-M3H(1)-D	System
Product Information (TMPM3H Group(1))	PINFO-M3H(1)	System
Flash Memory (Code Flash: 512KB/384KB/256KB/128KB and Data Flash: 32KB)	FLASH512UD32-B	Peripheral
Trimming Circuit	TRM-B	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-D	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
DMA Controller	DMAC-B	Peripheral
Universal Asynchronous Receiver Transmitter	UART-C	Peripheral
Serial Peripheral Interface	TSPI-E	Peripheral
I^2C interface	I2C-B	Peripheral
I^2C interface Version A	EI2C-A	Peripheral
8-bit Digital to Analog Converter	DAC-B	Peripheral
12-bit Analog to Digital Converter	ADC-G	Peripheral
Comparator	COMP-C	Peripheral
Advanced Programmable Motor Control Circuit	A-PMD-B	Peripheral
Advanced Encoder Input Circuit	A-ENC-A	Peripheral
LCD Display control Circuit	DLCD-A	Peripheral
32-bit Timer Event Counter	T32A-B	Peripheral
Real Time Clock	RTC-A	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
Remote control signal preprocessor	RMC-A	Peripheral
CRC calculation circuit	CRC-A	Peripheral
RAM Parity	RAMP-A	Peripheral

5.2. Processor Core

The TMPM3H Group(1) incorporates a high-performance 32-bit processor core (Arm Cortex-M3 core).

For the operation of the processor core, refer to the Arm documentation set of the Arm "Cortex-M" series processor. This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M3 core revision used in the TMPM3H Group(1) is shown as below:

For details of the CPU core and the architecture, refer to the Arm documentation on Arm's website.

Table 5.2 Core revision

Group name	Core revision
TMPM3H Group(1)	r2p1

5.2.2. Configurable Options

In the Cortex-M3 core, some blocks can be selected to implement. The following table shows the configurations of the TMPM3H Group(1).

Table 5.3 Configurable options and their implementations

Configurable option	Implementation
FPB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace Macrocell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/serial wire
Bit band	Available
Sequential control of AHB	Not available

5.3. Clock Control and Operation mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operation modes. Power consumption can be decreased by mode transition.

The outline of the clock control circuit is as follows:

- Internal high-speed oscillation circuit: 10MHz
- Selectable from the external high speed oscillation circuit or internal high-speed oscillation circuit.
- PLL (Clock Multiplication Circuit): Capable of 120 MHz output by changing the multiplication ratio according to the frequency of the high-speed oscillation circuit
- Clock gear: The high-speed clock can be divided by 1, 2, 4, 8, or 16 and the clock is used as the system clock (fsys).
- Low-power consumption mode:
  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can be enabled or disabled operation in the IDLE mode.
  STOP1: Except some peripheral circuits, all the internal circuits including the internal oscillator are brought to a stop in STOP1 mode. The low frequency clock can be supplied to RTC, RMC and DLCD by corresponding setting.
  STOP2: This mode halts voltage supply, retaining some peripheral circuits operation. The low frequency clock can be supplied to RTC and DLCD by the corresponding setting. The address match wakeup function on I^2C interface can be used.

5.4. Flash Memory (Code FLASH, Data FLASH)

The cord flash stores instruction code, and CPU read instruction code and executes. The data flash stores data, and even if a power supply is off, data can be kept.

The flash memory has the dual mode that possible to write and erase a data flash while executing instruction on a code flash, and it's also possible to continue executing an application program while writing or erasing data flash.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by outsiders.

5.5. Oscillation Circuit

- External High-Speed Oscillator (EHOSC):
  Connect crystal oscillator or ceramic resonator to terminals. Use clock source for System clock.
- External Low Speed Oscillator (ELOSC):
  Connect crystal oscillator (32.768 kHz) to terminals. Use clock source for Real Time Clock or Power consumption mode.
- Internal High-Speed Oscillator 1 (IHOSC1):
  Oscillation frequency is 10MHz. Use clock source for System clock.
- Internal High-Speed Oscillator 2 (IHOSC2):
  Oscillation frequency is 10MHz. Use clock source for OFD and SIWDT.

Table 5.4 Built-in Oscillator

	M3HQ	M3HP	M3HN	M3HM	M3HL
EHOSC	✓	✓	✓	✓	✓
ELOSC	✓	✓	✓	✓	✓
IHOSC1	✓	✓	✓	✓	✓
IHOSC2	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The trimming function can adjust the frequency of the internal high-speed oscillator1 (IHOSC1).

Table 5.5 Built-in TRM

	M3HQ	M3HP	M3HN	M3HM	M3HL
TRM	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.7. Oscillation Frequency Detector (OFD)

The oscillation frequency detector (OFD) is a function that detects an abnormal state of the clock. It measures the external high-speed oscillation (f_{EHOSC}), or high-speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.

The upper limit and the lower limit of detection frequency ranges can be specified.

Table 5.6 Built-in OFD

	M3HQ	M3HP	M3HN	M3HM	M3HL
OFD	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be chosen from eight kinds. LVD is set to enable from the Reset state at the Power-on.

Table 5.7 Built-in LVD

	M3HQ	M3HP	M3HN	M3HM	M3HL
LVD	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.9. Digital Noise Filter (DNF)

The digital noise filter circuit can eliminate the noise of input signals from external interrupt pins at a certain range. The noise of the "High" level/"Low" level input of the external interrupt signal INTx is removed.

Table 5.8 Number of External Interrupts (Built-in DNF)

	M3HQ	M3HP	M3HN	M3HM	M3HL
Number of External Interrupt	34	31	19	15	12

5.10. Debug Interface (DEBUG)

TMPM3H Group(1) contains interfaces to connecting debug tool, which are the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N). These are connected with the debug tool and used for program development. And also, it contains the trace clock (TRACECLK) and data output (TRACEDATA 0 to 3) to reduce the debug process.

Table 5.9 Built-in Debug Interface

Debug Pin (Signal Name)	Port	M3HQ	M3HP	M3HN	M3HM	M3HL
SWDIO	PL4	✓	✓	✓	✓	✓
TMS						
SWCLK	PL3	✓	✓	✓	✓	✓
TCK						
SWV	PL2	✓	✓	✓	✓	✓
TDO						
TDI	PL1	✓	✓	✓	✓	✓
TRST_N	PL0	✓	✓	✓	✓	✓
TRACECLK	PM0	✓	✓	✓	✓	-
TRACEDATA0	PM1	✓	✓	✓	✓	-
TRACEDATA1	PM2	✓	✓	✓	✓	-
TRACEDATA2	PM3	✓	✓	✓	-	-
TRACEDATA3	PM4	✓	✓	✓	-	-

Note: ✓: Available, -: N/A

5.11. DMA Controller (DMAC)

The DMAC is the peripheral function to move the data between peripheral functions and the memory, or between memories. These operations are performed separately from the CPU control; thus, the Load of CPU can greatly be reduced by using the DMA.

TMPM3H Group(1) have two units DMA controller (DMAC), DMAC has 32 channels of DMA requests per unit.

Table 5.10 Built-in DMAC

Unit	M3HQ	M3HP	M3HN	M3HM	M3HL
UNIT A	✓	✓	✓	✓	✓
UNIT B	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.12. Universal Asynchronous Receiver Transmitter (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first/LSB first and reversal of data polarity can be performed, and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8-stage at transmission, and on 8-stage at reception.

The telecommunication control by CTS/RTS and half clock mode are supported.

Table 5.11 Built-in UART

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓	✓
Channel 4	✓	✓	✓	✓	✓
Channel 5	✓	✓	✓	✓	✓
Channel 6	✓	✓	✓	✓	✓
Channel 7	✓	✓	✓	-	-

Note 1: ✓: Available, -: N/A

Note 2: External pins are not the same by the product. Please refer to the section "2 Pin Assignment".

5.13. Serial Peripheral Interface (TSPI)

The TSPI supports two communication methods and enables to perform serial communication between this device and other devices at high speed. The SPI bus type, which uses a CS (Chip Select) signal at communications, and SIO bus type, which does not use a CS signal at communications can be selected.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There are an 8-stage 16-bit FIFO for reception and transmission, each. The TSPI supports master and slave communications.

It can support frame mode (frame length (8 to 32 bit)) or sector mode (8 to 128 bit of frame length is configured in 2 to 4 sectors).

Table 5.12 Built-in TSPI

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	-
Channel 2	✓	✓	✓	✓	-
Channel 3	✓	✓	✓	✓	-
Channel 4	✓	✓	-	-	-

Note 1: ✓: Available, -: N/A

Note 2: External pins are not the same by product. Please refer to the section "2 Pin Assignment ".

5.14. I²C Interface

The following table shows the List of Built-in I²C Interface.

I2C and EI2C assigned to the same channel, and they cannot be used simultaneously at the same pin.

Table 5.13 Built-in I²C

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0 (Note 2)	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	-
Channel 2	✓	✓	✓	✓	✓
Channel 3	✓	✓	-	-	-

Note 1: ✓: Available, -: N/A

Note 2: The slave address match wake up function is available.

5.14.1. I²C Interface (I2C)

I2C is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports STD mode (Max 100kHz), Fast mode (Max 400kHz).7-bit Slave addressing is supported.

Depending on the setting, the MCU can receive data even in low power consumption mode including IDLE, STOP1, or STOP2 mode.

Channel 0 provides the address match wakeup function. It can return from low power consumption mode to normal mode by the slave address match.

5.14.2. I²C Interface Version A (EI2C)

I²C Interface Version A (EI2C) is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports STD mode (Max 100kHz), Fast mode (Max 400kHz), Fast mode plus (Max 1MHz), and 7-bit slave addressing and more 10-bit slave addressing.

Depending on the setting, the MCU can receive data even in low power consumption mode including IDLE, STOP1, or STOP2 mode.

Channel 0 provides the address match wakeup function. It can return from low power consumption mode to normal mode by the slave address match.

5.15. 8-bit Digital to Analog Converter (DAC)

The DAC is an R-2R type 8-bit digital to analog converter that can output the specified voltage. A buffer amplifier is not incorporated.

Channel0 (DAC0) can be used also as the reference voltage (VREFC) of a comparator (COMP).

Table 5.14 Built-in DAC

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.16. 12-bit Analog to Digital Converter (ADC)

The ADC is a successive-approximation analog to digital converter. It supports maximum 21 analog inputs. The combination of a conversion result register and analog input can be programmed in each startup trigger of AD conversion. A startup trigger for analog to digital conversion can be selected from software or peripheral functions (A-PMD trigger outputs, timer/event counter outputs, port inputs).

A motor is easily controllable by cooperating especially with A-PMD.

The monitor function is also available, and it can generate an interrupt request when the compare conditions are matched. 2 types of Sampling time setting are available and can be selected for each AIN channel.

Table 5.15 Built-in ADC

UNIT	M3HQ	M3HP	M3HN	M3HM	M3HL
UNIT A	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Table 5.16 Number of analog inputs for ADC

	M3HQ	M3HP	M3HN	M3HM	M3HL
Analog Inputs Pin count	21	19	17	12	12

5.17. Comparator (COMP)

The comparator compares an Analog Input value with Output value of Built-in 8-bits DAC, and the compared result is outputted to EMG input of A-PMD.

Table 5.17 Built-in Comparator

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.18. Advanced Programmable Motor Control Circuit (A-PMD)

The advanced programmable motor control circuit (A-PMD) enables users to control brushless DC motors easily. It incorporates the three-phase pulse modulation circuit and dead-time circuit, and easily generates waveforms for motor control by operating with the ADC in a coordinated fashion.

It also provides over-voltage detection input and abnormal detection input to support safety measures.

Table 5.18 Built-in A-PMD

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.19. Advanced Encoder Input Circuit (A-ENC)

The advanced encoder input circuit (A-ENC) supports an incremental encoder to acquire the motor position easily. The noise canceller is installed in the input pins, so that the signals from an incremental encoder or Hall sensor can be input directly.

The A-ENC provides six operation modes: encoder mode, sensor modes (3 kinds), timer mode, and phase counter mode.

Table 5.19 Built-in A-ENC

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.20. LCD Display Control Circuit (DLCD)

The LCD display control circuit (DLCD) is a segment display type LCD display control circuit that supports the non-bias driving system. It can drive up to 40-seg × 4-com LCD panel.

Table 5.20 Built-in DLCD List

	M3HQ	M3HP	M3HN	M3HM	M3HL
Segment configuration	40 segments × 4 commons	40 segments × 4 commons	32 segments × 4 commons	26 segments × 4 commons	-
Control type	Non-bias driving system				-

5.21. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit Timer or two 16-bit Timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A has an interval timer, event counter, input capture, 2-phase counter input, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.21 Built-in T32A

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓	✓
Channel 4	✓	✓	✓	✓	✓
Channel 5	✓	✓	✓	✓	✓
Channel 6	✓	✓	✓	✓	✓
Channel 7	✓	✓	✓	✓	✓

Note 1:✓: Available, -: N/A

Note 2: External pins are not the same by product. Please refer to section "2 Pin Assignment".

5.22. Real Time Clock (RTC)

The RTC is a peripheral function that has a second counter, clock function, and leap-year calendar function. It also has the alarm function that generates an interrupt request on a specified time and date.

Since the RTC operates on a low-speed external oscillation clock, it can operate in low-power consumption mode such as IDLE, STOP1 or STOP2 mode according to the setting. In addition, the MCU can be returned from low-power consumption mode by an interrupt request of the RTC.

The RTC easily corrects a gain/loss of the clock caused by an error of low-speed oscillation frequency using the clock correction function.

Table 5.22 Built-in RTC

	M3HQ	M3HP	M3HN	M3HM	M3HL
RTC	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.23. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock (fsys/4), internal oscillator1 (f_{IHOSC1}), or internal oscillator2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, the change of a register can be forbidden until the reset starts by setting to protected mode. (the count-clear function is possible)

Table 5.23 Built-in SIWDT

	M3HQ	M3HP	M3HN	M3HM	M3HL
SIWDT	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.24. Remote control signal preprocessor (RMC)

The RMC is a peripheral function that receives signals excluding carrier signal from remote control reception signals. The RMC detects a leader signal to receive 72 bits data in a lump. Two data formats can be received: synchronous format and fixed-synchronous phase format.

In addition, it contains a digital noise canceller to avoid external noise.

Since the RMC operates on a low-frequency clock, it can operate in low power consumption mode, such as IDLE or STOP1 mode according to the setting (except STOP2). The MCU can also be returned from low-power consumption mode by an interrupt request of the RMC.

Table 5.24 Built-in RMC

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.25. CRC calculation circuit (CRC)

This product has the Hardware calculation circuit for CRC32 and CRC16.

It can be used for detecting a memory and communication data error.

Table 5.25 Built-in CRC calculation circuit

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.26. RAM Parity (RAMP)

A RAM parity function generates and (8-bit unit) stores even parity data at the time of the writing to RAM, and performs a parity judging at the time of reading from RAM.

The interrupt is generated when it becomes an error by judgment. The Status and Address which the error generated are known.

A parity error is detectable in real time, since parity generating/judgment is hardware.

Table 5.26 Built-in RAM parity circuit

	M3HQ	M3HP	M3HN	M3HM	M3HL
RAMP	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

6. Equivalent Circuit

The port equivalent circuit diagram is basically written using the same gate symbol as the standard CMOS logic IC [74HCxx] series.

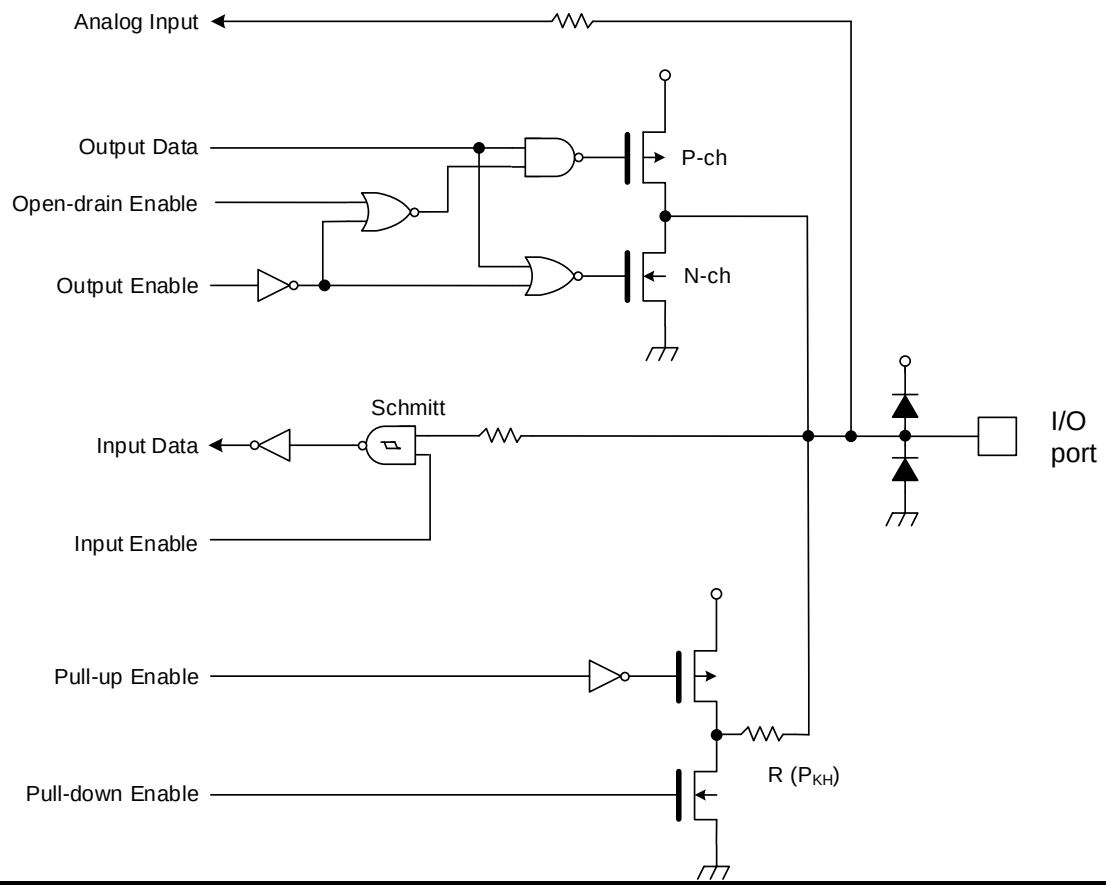
The input protection resistance ranges from several tens of Ω to several hundred of Ω. Damping resistor are shown with a typical value.

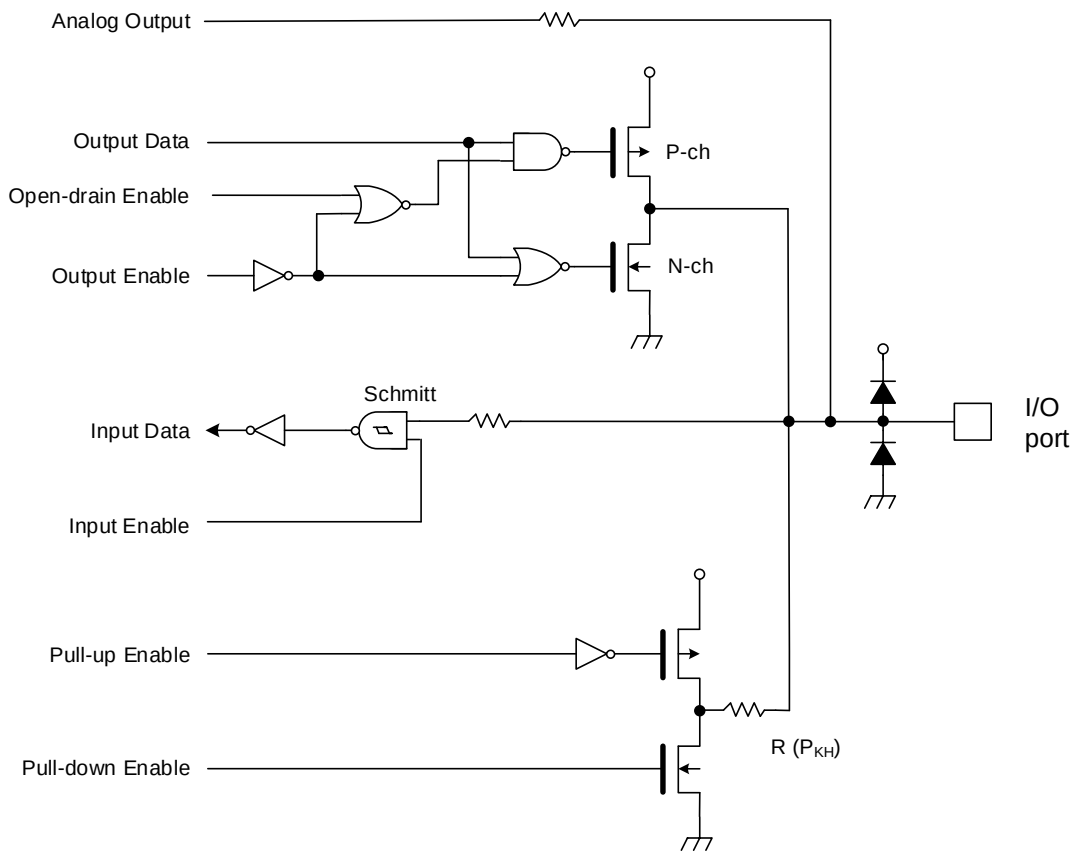
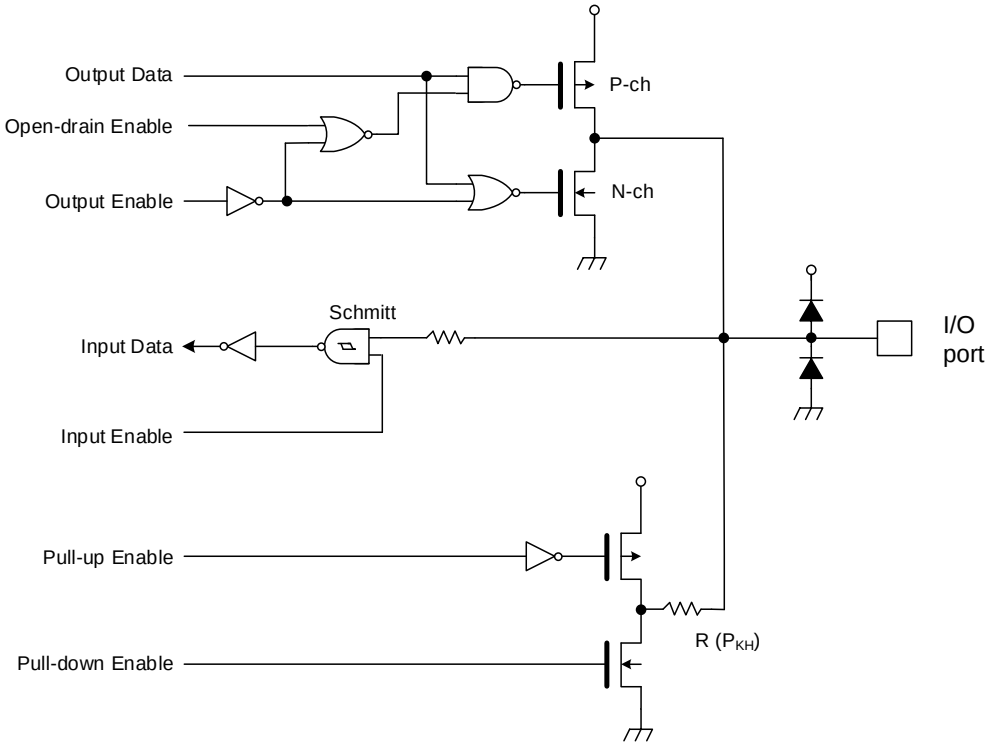
Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

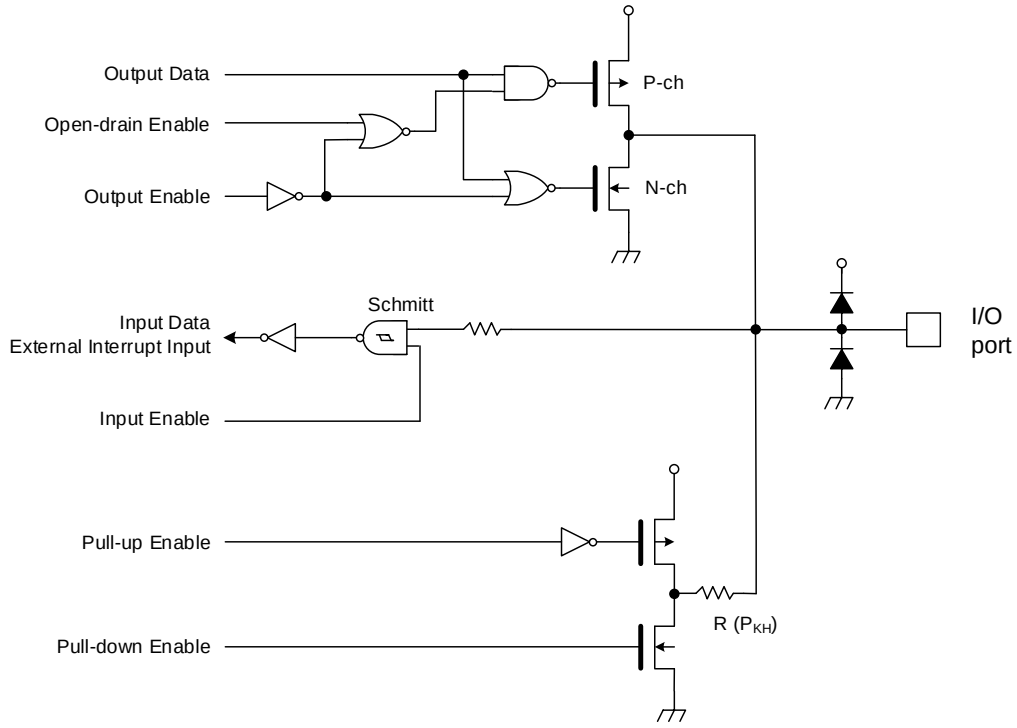
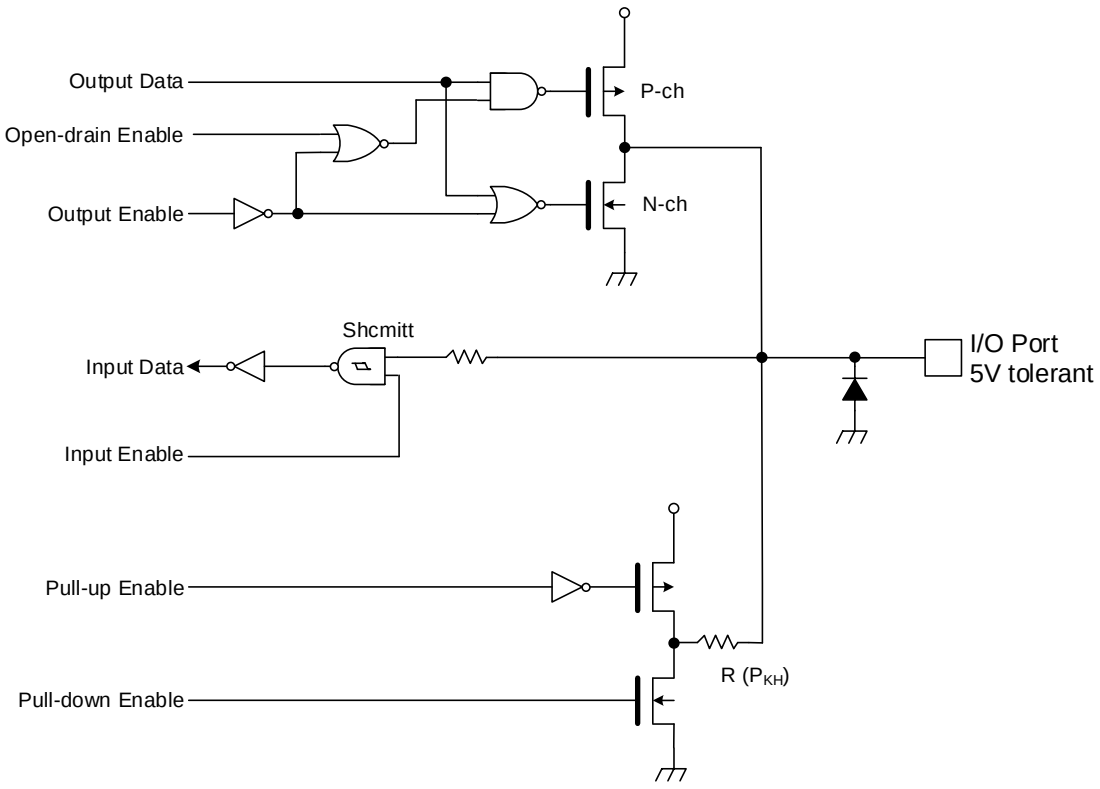
6.1. Port

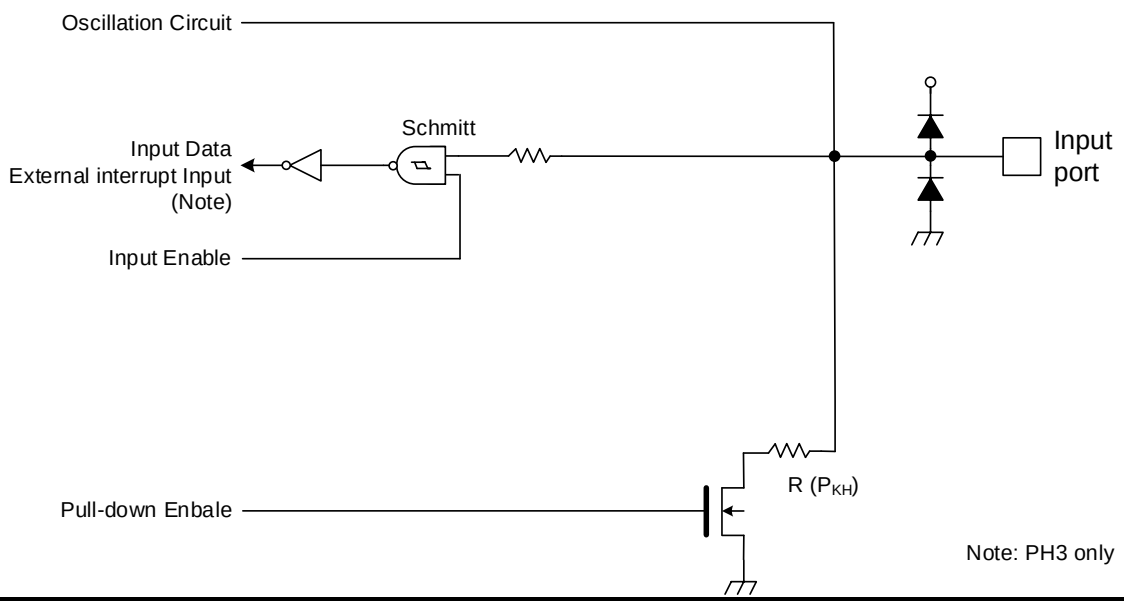
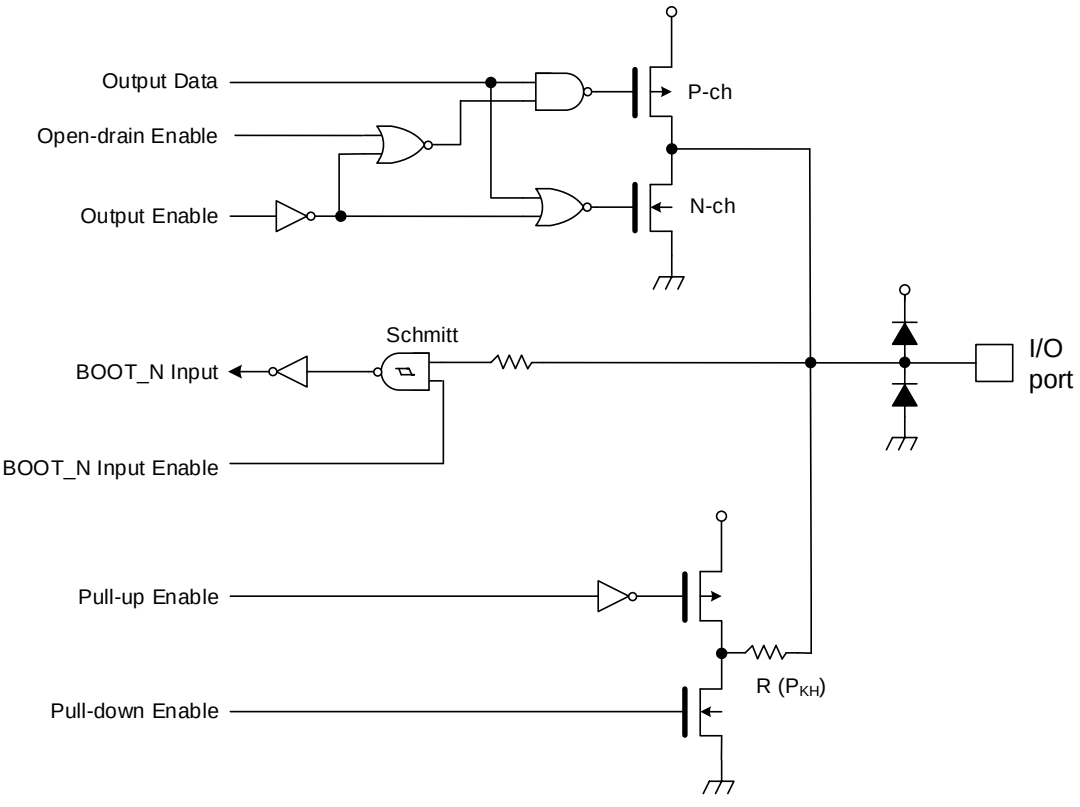
PD0 to 5
PE0 to 6
PF0 to 7

(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt input, Analog input)

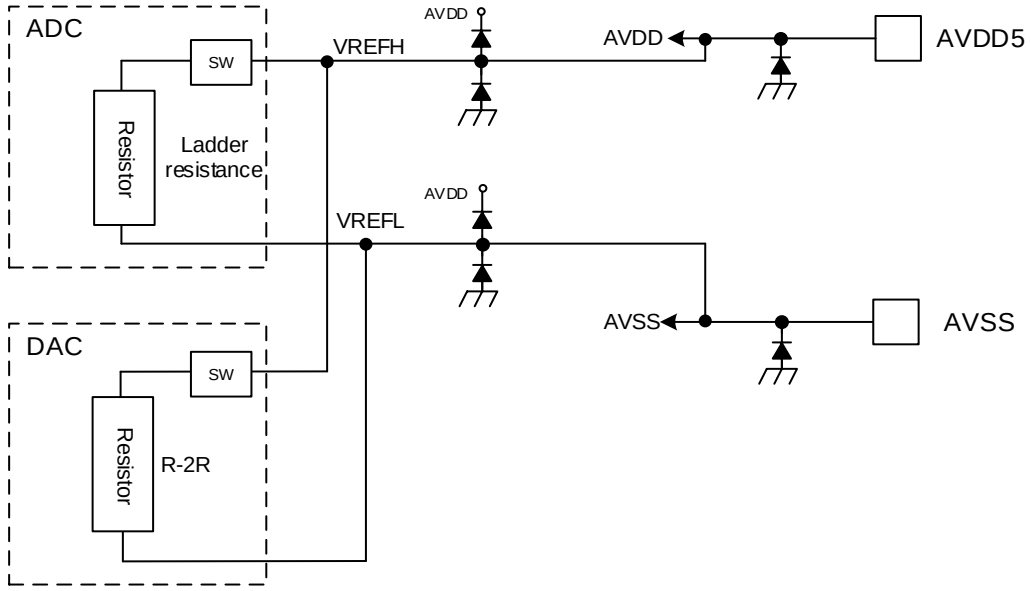


PG0, PG1	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt input, Analog Output) 
PA0 to 3 PB2 to 6 PC3 to 6 PG4 to 7 PJ0 to 3 PJ5, PK0 PK2 to 6 PL0 to 2, PL5 to 7 PM0, PM1 PM3 to 5 PM7 PN0 to 2, PN4, PN5 PP0 to 2 PP4 to 7 PR0 to 7 PT4 to 6 PU2 to 5 PV0, PV1 PV4 to 7 PW0	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input) 

PA6, PA7, PB1, PB7, PC0, PC1, PC2, PG2, PG3, PH4, PH5, PH6, PH7, PJ4, PK1, PK7, PL3, PL4, PM2, PM6, PN3, PP3, PT0, PT1, PT2, PT3, PT7, PU0, PU1, PV2, PV3	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, External Interrupt Input) 
PA4, PA5	(5V tolerant, Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt Input) 

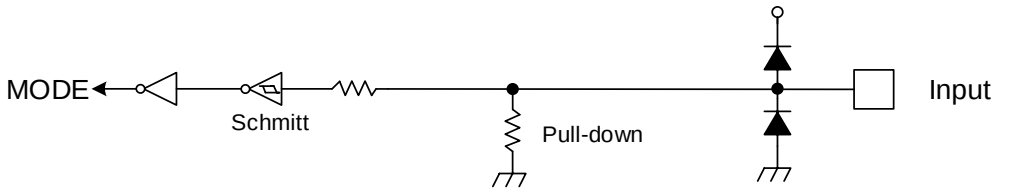
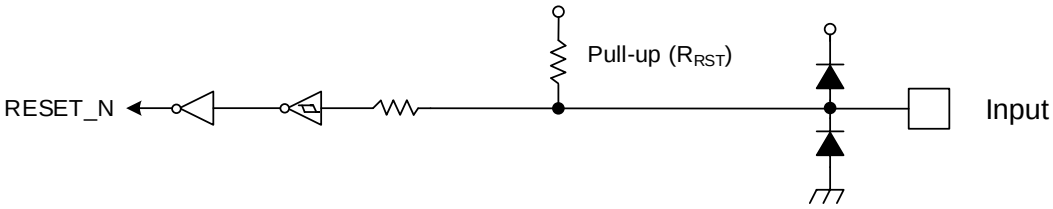
PH0 to 3	(Programmable Pull-down, Schmitt Input, Oscillation Circuit) 
PB0/BOOT_N	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, BOOT_N input) 

6.2. Analog Power pin

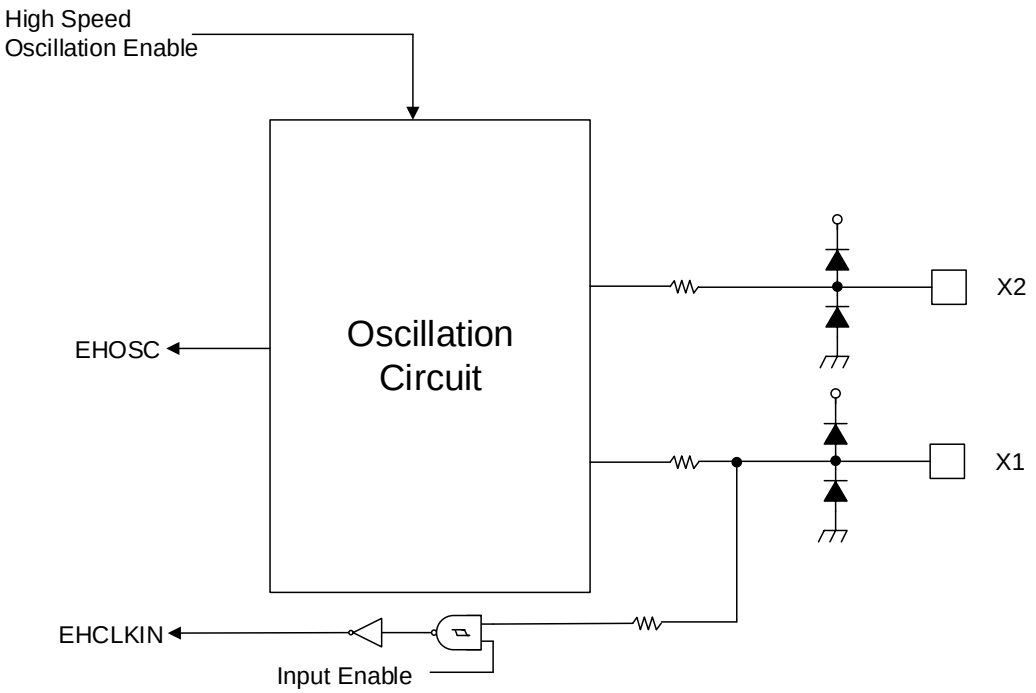
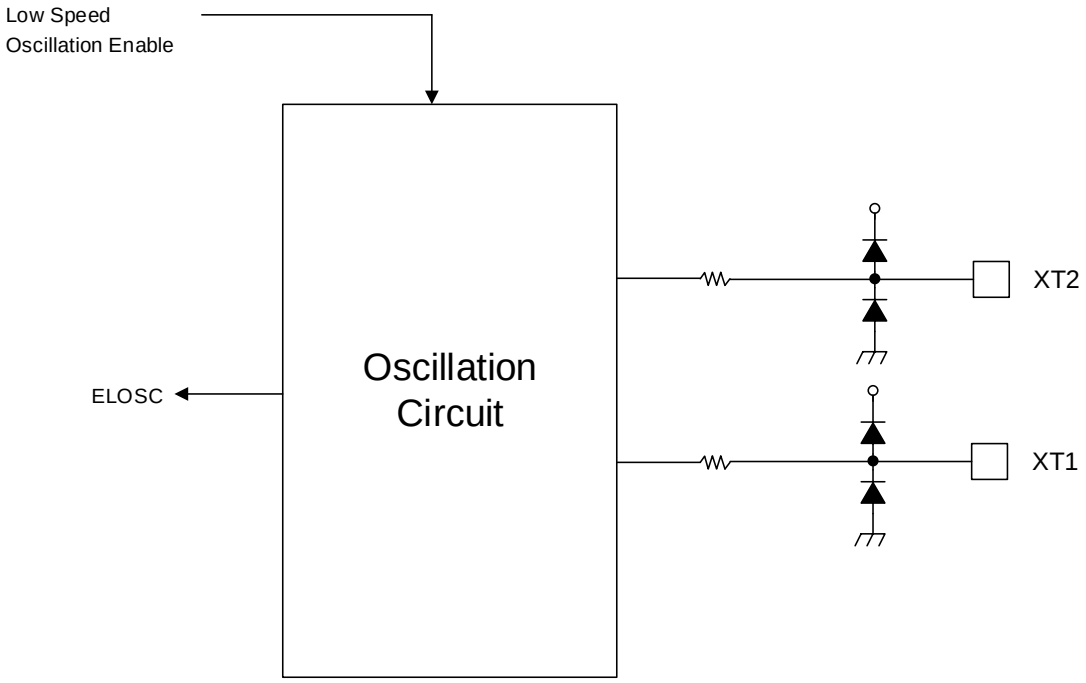
AVDD5 **AVSS**	

Note: SW: ON/OFF Switch Circuit

6.3. Control Pin

MODE	 Note: MODE pin must be connected to GND.
RESET_N	

6.4. Clock control

X1, X2	
XT1, XT2	

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD5A DVDD5B	-0.3 to 6.0	V
		AVDD5	-0.3 to DVDD5 (Note 2)	
Capacitor pin voltage for voltage maintenance		REGOUT2	-0.3 to 3.9	
Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 3, PA6、PA7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, PW0, MODE, RESET_N, BOOT_N	V_{IN1} V_{IN2}	-0.3 to DVDD5+0.3 (≤6.0V) (Note 2)	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0、PG1	V_{IN3}	-0.3 to AVDD5+0.3 (≤6.0V) (Note 2)	
	PA4 to 5	V_{IN4}	-0.3 to 6.0	
Low level output current	Per Pin PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 3, PA6, PA7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1, PW0	I_{OL}	5	mA
	Per Pin PA4 to 5	I_{OL4}	25	
	Total	ΣI_{OL}	50	
High level output current	Per pin PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1, PW0	I_{OH}	-5	
	Total	ΣI_{OH}	-50	
Power consumption (Ta = 105°C)		PD	600	mW
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operating temperature		T_{OPR}	-40 to 105	°C

Note 1: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

Note 2: DVDD5 is a generic name for DVDD5A, DVDD5B. DVSS is a generic name for DVSSA, DVSSB. Apply the same voltage to DVDD5 and AVDD5.
And refer to following description for turning-on and turning-off a power.

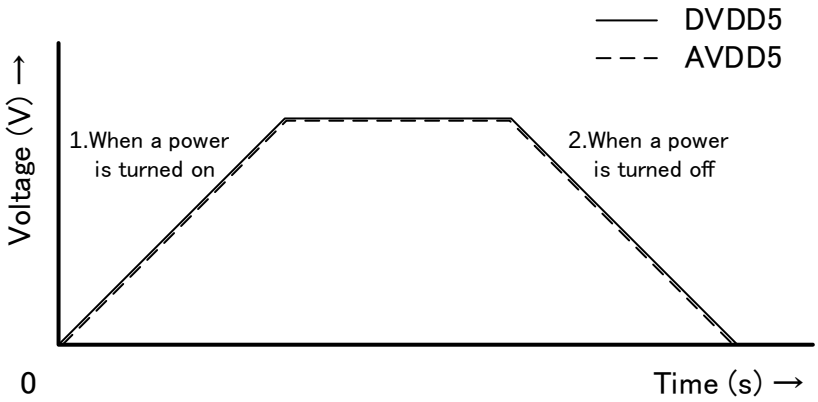


Figure 7.1 Notice When a Power is Turned On and Off

(1) When a power is turned on
Note the following:

1. Even if DVDD5 and AVDD5 are supplied a voltage from a same power supply, the voltage between DVDD5 and AVDD5 may have a difference by the capacity of the capacitors which are connected between DVDD5 and DVSS, and between AVSS5 and AVSS, and by the stray capacitances and inductance of PCB patterns.

(2) When a power is turned off
Note the following:

1. Because capacitors and PCB patterns still have a residual electric charge, the voltage between DVDD5 and AVDD5 may have a difference.

2. A power is re-turned on in above situation.

7.2. DC Electrical Characteristics (1/2)

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A, DVDD5B, AVDD5	VDD	f_{OSC} = 6 to 12MHz fsys = 1 to 120MHz fs = 30 to 34kHz	4.5	-	5.5	V
Low level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N	V_{IL1}	-	-0.3	-	DVDD5×0.25	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, PW0, BOOT_N	V_{IL2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	V_{IL3}				AVDD5×0.25	
	PA4, PA5	V_{IL4}				DVDD5×0.3	
High level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IH1}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, PW0, BOOT_N	V_{IH2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	V_{IH3}		AVDD5×0.75		AVDD5+0.3	
	PA4, PA5	V_{IH4}		DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5, PW0	V_{OL1} V_{OL2}	DVDD5 = 4.5V IOL = 1.6mA	-	-	0.4	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	V_{OL3}	AVDD5 = 4.5V IOL = 1.6mA	-	-	0.4	
	PA4, PA5	V_{OL4}	DVDD5 = 4.5V IOL = 8mA	-	-	1.0	
High level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5, PW0	V_{OH1} V_{OH2}	DVDD5 = 4.5V IOH = -1.6mA	DVDD5-0.4	-	-	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	V_{OH3}	AVDD5 = 4.5V IOH = -1.6mA	AVDD5-0.4	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.
Note 3: Apply the same voltage to DVDD5 and AVDD5.

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Output leak current		I_{LO}	0.2 ≤VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤ AVDD5-0.2	-10	±0.05	10	
Schmitt trigger Input width		VTH	DVDD5 = AVDD5 = 5V	-	1	-	V
Reset pull-up resistor		R_{RST}	-	25	50	100	kΩ
Programmable pull-up/-down resistor		P_{KH}	Pull-up	25	50	100	kΩ
			Pull-down	25	50	100	
Pin capacity (except power supply pin)		C_{IO}	fc = 1MHz	-	-	10	pF
Low level output current	Per pin except below ports	I_{OL}	DVDD5 = 5V AVDD5 = 5V	-	-	2 (Note 4)	mA
	Per pin PA4 to 5	I_{OL4}	DVDD5 = 5V	-	-	12 (Note 4)	
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7	$\sum I_{OL1}$	DVDD5 = 5V	-	-	35 (Note 5)	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, PW0	$\sum I_{OL2}$	DVDD5 = 5V	-	-	35 (Note 5)	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	$\sum I_{OL3}$	AVDD5 = 5V	-	-	20 (Note 5)	
High level output current	Per pin	I_{OH}	DVDD5 = 5V AVDD5 = 5V	-2 (Note 4)	-	-	mA
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7	$\sum I_{OH1}$	DVDD5 = 5V	-35 (Note 5)	-	-	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, PW0	$\sum I_{OH2}$	DVDD5 = 5V	-35 (Note 5)	-	-	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	$\sum I_{OH3}$	AVDD5 = 5V	-20 (Note 5)	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Note 4: The current sum total of a terminal should not exceed the sum total of each group current.

Note 5: The sum total of each group current should not exceed the absolute maximum rating.

2.7V ≤ DVDD5 = AVDD5 < 4.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A, DVDD5B, AVDD5	VDD	fOSC = 6 to 12MHz fsys = 1 to 120MHz fs = 30 to 34kHz	2.7	-	4.5	V
Low level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IL1}	-	-0.3	-	DVDD5×0.25	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, PW0, BOOT_N	V_{IL2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	V_{IL3}				AVDD5×0.25	
	PA4, PA5	V_{IL4}				DVDD5×0.3	
High level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N	V_{IH1}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, PW0, BOOT_N	V_{IH2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	V_{IH3}	-	AVDD5×0.75		AVDD5+0.3	
	PA4, PA5	V_{IH4}	-	DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5, PW0	V_{OL1} V_{OL2}	DVDD5 = 2.7V IOL = 0.8mA	-	-	0.4	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	V_{OL3}	AVDD5 = 2.7V IOL = 0.8mA	-	-	0.4	
	PA4, PA5	V_{OL4}	DVDD5 = 2.7V IOL = 4mA	-	-	1.0	
High level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5, PW0	V_{OH1} V_{OH2}	DVDD5 = 2.7V IOH = -0.8mA	DVDD5-0.4	-	-	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	V_{OH3}	AVDD5 = 2.7V IOH = -0.8mA	AVDD5-0.4	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

2.7V ≤ DVDD5 = AVDD5 < 4.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Output leak current		I_{LO}	0.2 ≤ VIN ≤ DVDD5-0.2 0.2 ≤ VIN ≤ AVDD5-0.2	-10	±0.05	10	
Schmitt trigger Input width		VTH	DVD D5 = AVDD5 = 3V	-	0.5	-	V
Reset pull-up resistor		R_{RST}	-	25	100	200	kΩ
Programmable pull-up/-down resistor		P_{KH}	Pull-up	25	100	200	
			Pull-down	25	100	200	
Pin capacity (except power supply pin)		C_{IO}	fc = 1MHz	-	-	10	pF
Low level output current	Per pin (except PA4 and PA5)	I_{OL}	DVDD5 = 3V AVDD5 = 3V	-	-	1 (Note 4)	mA
	Per pin PA4, PA5	I_{OL4}	DVDD5 = 3V	-	-	6 (Note 4)	
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7	$\sum I_{OL1}$	DVDD5 = 3V	-	-	18 (Note 5)	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, PW0	$\sum I_{OL2}$	DVDD5 = 3V	-	-	18 (Note 5)	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	$\sum I_{OL3}$	AVDD5 = 3V	-	-	10 (Note 5)	
High level output current	Per pin	I_{OH}	DVDD5 = 3V AVDD5 = 3V	-1 (Note 4)	-	-	mA
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7	$\sum I_{OH1}$	DVDD5 = 3V	-18 (Note 5)	-	-	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, PW0	$\sum I_{OH2}$	DVDD5 = 3V	-18 (Note 5)	-	-	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0, PG1	$\sum I_{OH3}$	AVDD5 = 3V	-10 (Note 5)	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.
Note 3: Apply the same voltage to DVDD5 and AVDD5.
Note 4: The current sum total of a terminal should not exceed the sum total of each group current.
Note 5: The sum total of each group current should not exceed the absolute maximum rating.

7.3. DC Electrical Characteristics (2/2) (Current consumption)

Ta = -40 to 105°C

Parameter	Symbol	Conditions					Min	Typ. (Note 2)	Max	Unit
		Supply voltage	High-speed oscillator	Low-speed oscillator	Operating condition	fsys				
Normal	I_{DD}	DVDD5 = AVDD5 = 5.5V	Refer to Table 7.2 and Table 7.3 for detail.			80MHz	-	15	26	mA
						120MHz	-	20	32	
IDLE			Oscillation	Oscillation	Refer to Table 7.2 and Table 7.3 for detail.	80MHz	-	4.6	14.5	
						120MHz	-	5	15	
STOP1			Stop	Oscillation		-	-	2700	12000	µA
STOP2							-	4	300	
				Stop			-	3	300	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Note 4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1	STOP2	
				ELOSC run		ELOSC stop
Pin setting	DVDD5 = AVDD5	5.0V (Typ.), 5.5V (max)				
	X1, X2	Oscillator connected (10MHz)				
	XT1, XT2	Oscillator connected (32.768kHz)				
	Input pins	Fixed				
	Output pins	Open				
Operating condition (Oscillation Circuit)	System clock (fsys)	80MHz, 120MHz		Stop		
	External High speed frequency oscillator (EHOSC)	Oscillation		Stop		
	Internal High speed frequency oscillator (IHOSC1)	Stop				
	PLL	run (8 or 12 times)		Stop		
	External Low speed oscillator (ELOSC)	Oscillation				Stop

Table 7.3 IDD measurement condition (CPU, Peripheral)

Peripheral	unit number	NORMAL	IDLE	STOP1	STOP2
				LOSC oscillation	LOSC stop
CPU	1	Run (Dhrystone Ver.2.1)	Stop		
DMAC	1	(Request from UARTch0 Transmission, destination: RAM)	Stop		
ADC	1	Run (1.5µs, Repeated conversion)	Stop		
DAC	2	Run	Stop		
T32A	6	All ch: Run	Stop		
A-PMD	1	Run	Stop		
A-ENC	1	Run	Stop		
RTC	1	Run			
SIWDT	1	Run	Stop		
UART	8	All ch: Transmission (2.5Mbps)	Stop		
I2C/EI2C	4/4	Stop			
TSPI	5	Ch0, ch1: Transmission, 20MHz	Stop		
RMC	1	Run	Stop		
DLCD	1	Stop			
LVD	1	Stop			
OFD	1	Stop			
Input Output Port	-	Run	Stop		

7.4. 12-bit AD Converter Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH (AVDD5)		-	AVDD5	-	V
Analog input voltage	VAIN		AVSS (VREFL)	-	AVDD5 (VREFH)	V
Integral nonlinearity error (INL)	-	2.7V ≤ AVDD5 ≤ 5.5V AIN load resistor = 600Ω AIN load capacity ≥ 0.1μF Conversion time = 1.0 to 16.65μs	-5.0	-	+5.0	LSB
Differential nonlinearity error (DNL)			-2.0	-	+4.0	
Zero-scale error			-5.0	-	+3.0	
Full-scale error			-4.5	-	+3.0	
Total errors			-7.0	-	+6.0	
Stable time	t_{sta}	After ***[ADMOD0]***<DACON> is set to "1".	3	-	-	μs
Conversion time	t_{conv}	4.5V ≤ AVDD5 ≤ 5.5V SCLK = 30MHz (Note 3)	1.0	-	10.87	
		4.5V ≤ AVDD5 ≤ 5.5V SCLK = 20MHz (Note 3)	1.5	-	16.3	
		2.7V ≤ AVDD5 < 4.5V SCLK = 20MHz (Note 3)	2.05	-	16.65	

Note 1: 1LSB = (AVDD5 (VREFH) - AVSS (VREFL)) / 4096[V]

Note 2: The characteristic when a single unit AD converter operates only.

Note 3: For detail of setting, refer to the reference manual "Analog to Digital Converter".

7.5. 8-bit DA Converter Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH (AVDD5)		-	AVDD5	-	V
Integral nonlinearity error (INL)	-	4.5V ≤ AVDD5 ≤ 5.5V Rload = 10MΩ	-1	-	+1	LSB
Differential nonlinearity error (DNL)			-1	-	+1	
Total errors			-1	-	+1	
Integral nonlinearity error (INL)	-	2.7V ≤ AVDD5 < 4.5V Rload = 10MΩ	-2	-	+2	LSB
Differential nonlinearity error (DNL)			-1	-	+1	
Total errors			-2	-	+2	
Stable time	t_{sta}	Cload = 20pF	4.7	-	-	μs

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V or Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note 3: 1LSB = (AVDD5 (VREFH) - AVSS (VREFL)) / 256 [V]

Note 4: This is the characteristic in case only DA converter is operating.

Note 5: When using DAC0 as the reference voltage of Comparator, DAC0 pin should be open.

7.6. Comparator Characteristics

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
AIN Input voltage Range	VINC	-	VREFC - 1.5	-	VREFC + 1.5	V
Reference Voltage Range (Note 1)	VREFC		0.2	-	AVDD5-0.5	V
Response time (Note 2)	-		-	-	0.5	μs
Comparator Start-up time	T_{sta}		-	-	5	μs

Note 1: Output of On-chip 8-bit DA converter (DAC0)

Note 2: In case of the VINC change from VREFC - 100mV to VREFC + 100mV, or from VREFC + 100mV to VREFC - 100mV.

Note 3: This is the characteristic in case only Comparator is operation.

7.7. Characteristics of Internal processing at RESET

DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal initialization time	t_{IINIT}	Power-on	-	-	1.91	ms
Internal processing time for Reset	t_{IRST}	STOP2 released by RESET with RESET_N or LVD.	-	-	1.61	
		STOP2 released by Interrupt	-	-	1.02	
		Reset operation except STOP2 releasing	0.15	-	1.13	
Waiting time till CPU running (Note)	t_{CPUWT}	Power-on Reset operation by LVD in STOP1 or STOP2 mode Reset operation by RESET_N pin in STOP1 or STOP2 mode	12	-	15	µs
		Reset operation by LVD in NORMAL or IDLE mode Reset operation by RESET_N pin in NORMAL or IDLE mode Reset operation by WDT, OFD, LOCKUP, or SYSRESET in NORMAL or IDLE mode	138	-	143	
Power gradient	V_{PON}	Rising slope	0.3	-	100	mV/µs
	V_{POFF}	Falling slope	-	-	10	

Note: Except reset operation by WDT, OFD, LOCKUP, or SYSRESET, when reset factor continues, t_{CPUWT} (Waiting time till CPU running) starts measuring elapse time after releasing this factor.

7.8. Characteristics of Power On Reset

DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power-up	2.22	2.33	2.44	V
	V_{PDET}	Power-down	2.17	2.28	2.39	
Detection pulse width	T_{PDET}	-	200	-	-	µs

7.9. Characteristics of PORF

DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PORFL}	Power-up	2.57	2.64	2.71	V
	V_{PORFD}	Power-down	2.52	2.59	2.66	
Detection pulse width	T_{PDET}	-	200	-	-	µs

7.10. Characteristics of Voltage Detection Circuit

DVDD5 = AVDD5 = 2.7 to 5.5V
DVSS = AVSS = 0V
Ta = -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{LVL0}	Power-up (releasing)	2.63	2.70	2.77	V
		Power-down (detecting)	2.58	2.65	2.72	
	V_{LVL1}	Power-up (releasing)	2.68	2.75	2.82	V
		Power-down (detecting)	2.63	2.70	2.77	
	V_{LVL2}	Power-up (releasing)	2.78	2.85	2.92	V
		Power-down (detecting)	2.73	2.80	2.87	
	V_{LVL3}	Power-up (releasing)	2.88	2.95	3.02	V
		Power-down (detecting)	2.83	2.90	2.97	
	V_{LVL4}	Power-up (releasing)	3.96	4.05	4.14	V
		Power-down (detecting)	3.91	4.00	4.09	
	V_{LVL5}	Power-up (releasing)	4.16	4.25	4.34	V
		Power-down (detecting)	4.11	4.20	4.29	
	V_{LVL6}	Power-up (releasing)	4.36	4.45	4.54	V
		Power-down (detecting)	4.31	4.40	4.49	
	V_{LVL7}	Power-up (releasing)	4.56	4.65	4.74	V
		Power-down (detecting)	4.51	4.60	4.69	
Detection response time	t_{VDDT1}	Power-down	-	-	100	µs
Detection release time	t_{VDDT2}	Power-up	-	-	100	
Setup time	t_{LVDEN}		-	-	100	
Detection minimum pulse width	t_{LVDPW}		200	-	-	

7.11. AC Electrical Characteristics

7.11.1. Serial Peripheral Interface (TSPI)

7.11.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of k1 is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of k2 is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>.

<RXDLY> is added setting value of ***[TSPIxCR2]***<RXDLY[2:0]> with 1.

- <RXDLY> = 1 when ***[TSPIxCR2]***<RXDLY[2:0]> = 000
- <RXDLY> = 2 when ***[TSPIxCR2]***<RXDLY[2:0]> = 001
- <RXDLY> = 3 when ***[TSPIxCR2]***<RXDLY[2:0]> = 010

(1) Master in SPI mode (TSPI1/2/3/4)

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz k1 = k2 = 1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-13	-	12	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-13	-	12	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC}×k1)-20	(t_{CYC}×k1)+9	30	59	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	(t_{CYC}×(k2+0.5))-20	-	55	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35-<RXDLY>×T	-	10	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	<RXDLY>×T-10.5	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC}×(k1-0.5))-25	(t_{CYC}×(k1-0.5))+9	0	34	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Equation		fsys = 80MHz k1 = k2 = 1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-16	-	9	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-16	-	9	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC}×k1)-20	(t_{CYC}×k1)+11	30	61	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	(t_{CYC}×(k2+0.5))-22.5	-	52.5	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45-<RXDLY>×T	-	20	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	<RXDLY>×T-10.5	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC}×(k1-0.5))-25	(t_{CYC}×(k1-0.5))+13	0	38	

(2) Master in SPI mode (TSPI0)

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz k1 = k2 = 1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	5.88	-	5.88	MHz
TSPIxSCK output cycle	t_{CYC}	170	-	170	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-13	-	72	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-13	-	72	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC}×k1)-140	(t_{CYC}×k1)+9	30	179	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	(t_{CYC}×(k2+0.5))-20	-	235	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35-<RXDLY>×T	-	10	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	<RXDLY>×T-10.5	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC}×(k1-0.5))-145	(t_{CYC}×(k1-0.5))+9	-60	94	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Equation		fsys = 80MHz k1 = k2 = 1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	4.34	-	4.34	MHz
TSPIxSCK output cycle	t_{CYC}	230	-	230	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-16	-	99	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-16	-	99	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC}×k1)-200	(t_{CYC}×k1)+9	30	239	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	(t_{CYC}×(k2+0.5))-20	-	325	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45-<RXDLY>×T	-	20	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	<RXDLY>×T-10.5	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC}×(k1-0.5))-211	(t_{CYC}×(k1-0.5))+13	-96	128	

(3) Slave in SPI mode (TSPI0/1/2/3/4)

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level input pulse width	t_{WH}	37	-	37	-	
TSPIxCSIN input (1st edge) ← TSPIxSCK rise/fall time	t_{CSU1}	170	-	170	-	
TSPIxCSIN input (2nd edge) ← TSPIxSCK rise/fall time	t_{CSU2}	80	-	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (1st edge)	t_{CHD}	80	-	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (2nd edge)		7	-	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	49	-	49	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	55	-	55	
TSPIxCSIN high level input pulse width (1st edge)	t_{WDIS}	T×5+20	-	82.5	-	
TSPIxCSIN high level input pulse width (2nd edge)		T×2+20	-	45	-	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level input pulse width	t_{WH}	37	-	37	-	
TSPIxCSIN input (1st edge) ← TSPIxSCK rise/fall time	t_{CSU1}	170	-	170	-	
TSPIxCSIN input (2nd edge) ← TSPIxSCK rise/fall time	t_{CSU2}	80	-	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (1st edge)	t_{CHD}	80	-	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time (2nd edge)		7	-	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	55	-	55	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	55	-	55	
TSPIxCSIN high level input pulse width (1st edge)	t_{WDIS}	T×5+20	-	82.5	-	
TSPIxCSIN high level input pulse width (2nd edge)		T×2+20	-	45	-	

(4) Master in SIO Mode (TSPI0/1/2/3/4)

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-13	-	12	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-13	-	12	-	
TSPIxRXD input ← TSPIxSCK rise/fall time	t_{DSU}	35-<RXDLY>×T	-	10	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	<RXDLY>×T-10.5	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-16	-	9	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-16	-	9	-	
TSPIxRXD input ← TSPIxSCK rise/fall time	t_{DSU}	45-<RXDLY>×T	-	20	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	<RXDLY>×T-10.5	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

(5) Slave in SIO mode (TSPI0/1/2/3/4)

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level input pulse width	t_{WH}	37	-	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	49	-	49	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level input pulse width	t_{WH}	37	-	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	55	-	55	

(1) 1st clock edge sampling (Master)

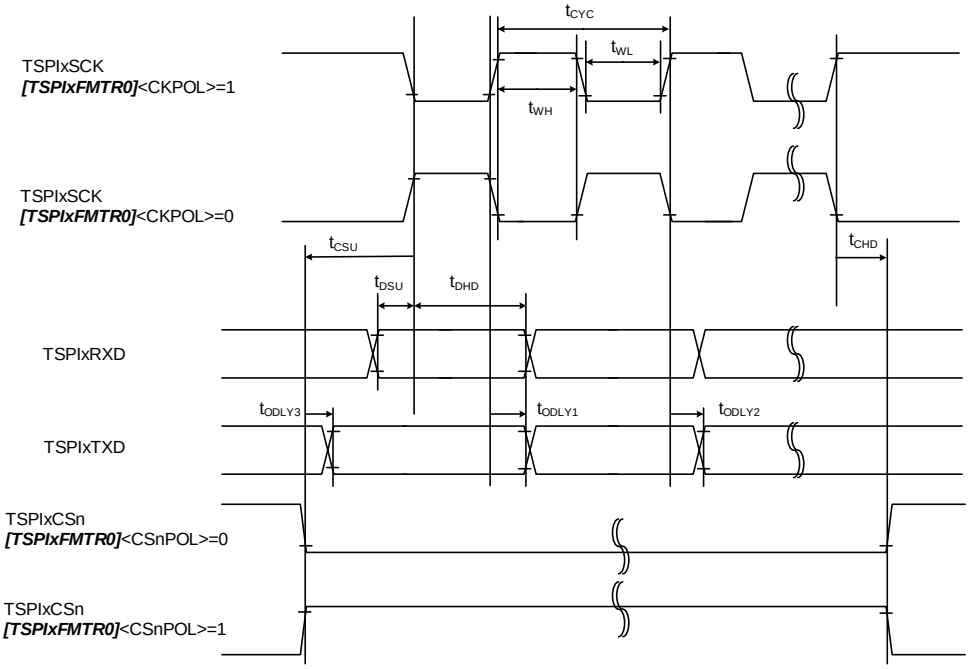


Figure 7.2 1st clock edge sampling (Master)

(2) 2nd clock edge sampling (Master)

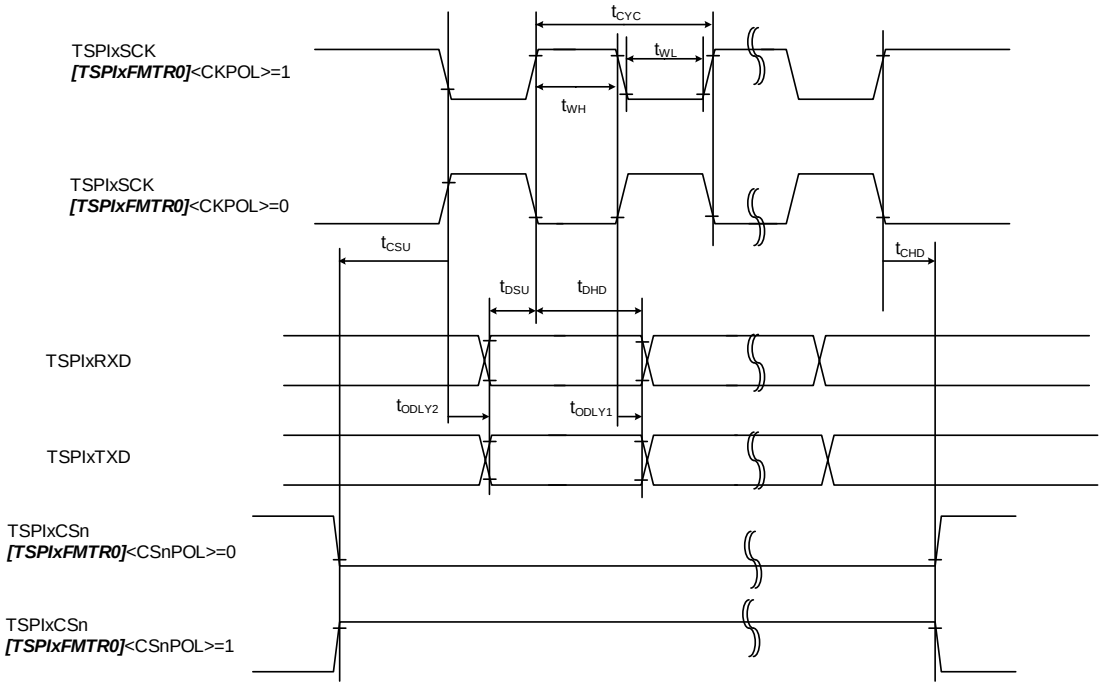


Figure 7.3 2nd clock edge sampling (Master)

(3) 1st clock edge sampling (Slave)

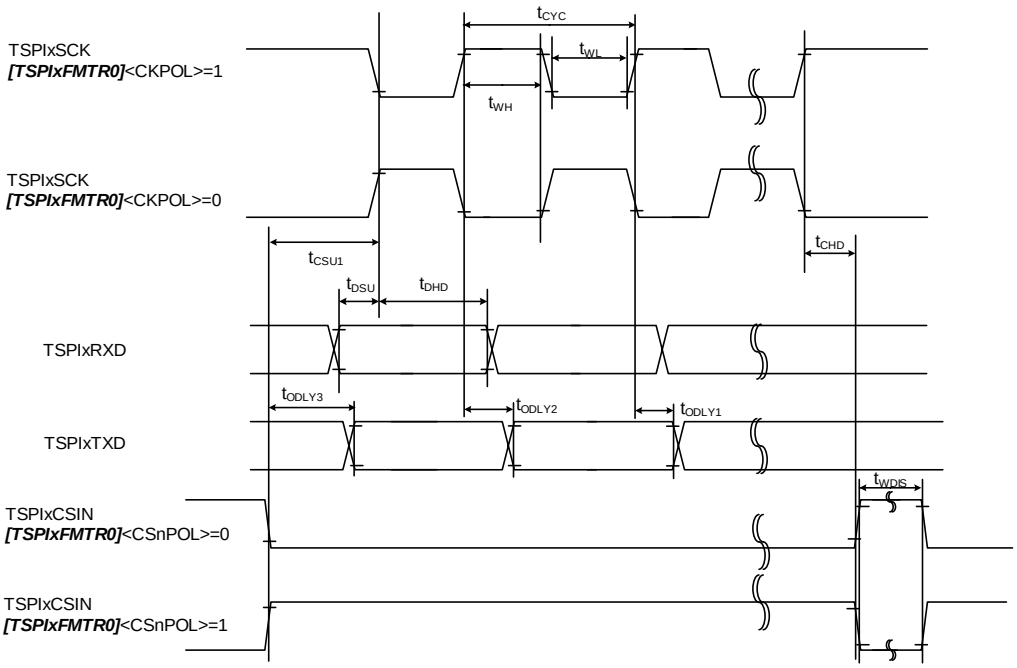


Figure 7.4 1st clock edge sampling (Slave)

(4) 2nd clock edge sampling (Slave)

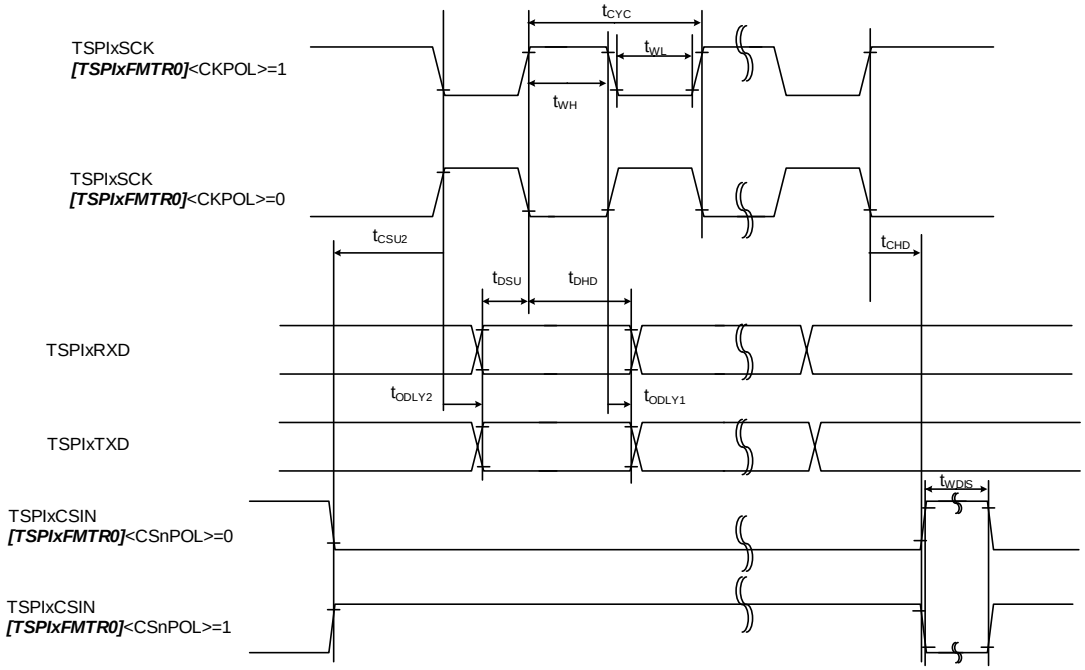


Figure 7.5 2nd clock edge sampling (Slave)

7.11.2. I²C Interface (I2C)

7.11.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF
- External pull-up resistor R_p = 2.2kΩ

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.2.2. AC Electrical Characteristics

Parameter		Symbol	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
SCL clock frequency		f_{SCL}	0	100	0	400	kHz
Start condition hold time		$t_{HD;STA}$	4.0	-	0.6	-	µs
SCL clock Low width (Input) (Note 1)		t_{LOW}	4.7	-	1.3	-	
SCL clock High width (Input) (Note 1)		t_{HIGH}	4.0	-	0.6	-	
Re-start condition setup time	<SREN> = 0	$t_{SU;STA}$	4.7 (Note 3)	-	0.6 (Note 3)	-	
	<SREN> = 1		4.7 (Note 3)	-	0.6	-	
Data hold time (Input) (Note 2)		$t_{HD;DAT}$	0	-	0	-	
Data setup time		$t_{SU;DAT}$	250	-	100	-	ns
Stop condition setup time		$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus free time between stop condition and start condition (Note 3)		t_{BUF}	4.7	-	1.3	-	
Pulse width of spikes that must be suppressed by the input filter		t_{SP}	-	-	0	50	ns
Rise time of both SDA and SCL signals		t_r	-	1000	20	300	
Fall time of both SDA and SCL signals		t_f	-	300	20 × (VDD/5.5V)	300	

Note 1: On I2C bus standard, the maximum speed of standard mode/fast mode is 100kHz/400kHz, respectively. For the frequency setting of the internal SCL clock, refer to the calculation formula in 3.3.2. of reference manual "I2C Interface".

Note 2: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/tf on the SCL/SDA should be included in the data hold time.

Note 3: To keep the time by software.

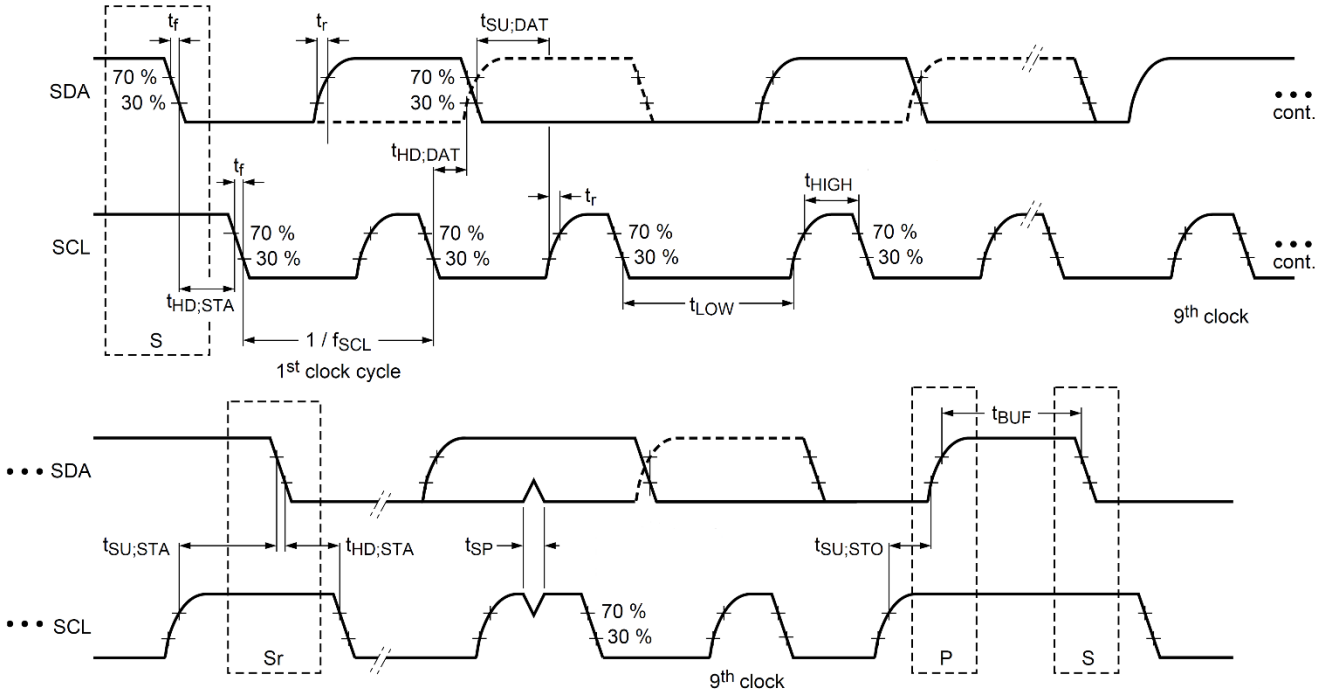


Figure 7.6 AC timing of I2C

7.11.3. I²C Interface version A (EI2C)

7.11.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF
- External pull-up resistor: R_p = 2.2kΩ

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.3.2. AC Electrical Characteristics

Parameter	Symbol	Standard mode		Fast mode		Fast mode plus		Unit
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Start condition hold time	$t_{HD;STA}$	4.0	-	0.6	-	0.26	-	µs
SCL clock Low width (Input) (Note 1)	t_{LOW}	4.7	-	1.3	-	0.5	-	
SCL clock High width (Input) (Note 1)	t_{HIGH}	4.0	-	0.6	-	0.26	-	
Re-start condition setup time	$t_{SU;STA}$	4.7	-	0.6	-	0.26	-	
Data hold time (Input) (Note 2)	$t_{HD;DAT}$	0	-	0	-	0	-	
Data setup time	$t_{SU;DAT}$	250	-	100	-	50	-	ns
Stop condition setup time	$t_{SU;STO}$	4.0	-	0.6	-	0.26	-	µs
Bus free time between stop condition and start condition (Note 3)	t_{BUF}	4.7	-	1.3	-	0.5	-	
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	-	-	0	50	0	50	ns
Rise time of both SDA and SCL signals	t_r	-	1000	20	300	-	120	
Fall time of both SDA and SCL signals	t_f	-	300	20 × (VDD/5.5V)	300	20 × (VDD/5.5V)	120	

Note 1: On I²C bus standard, the maximum speed of standard mode/fast mode/fast mode plus is 100kHz/ 400kHz/1000kHz, respectively. For the frequency setting of the internal SCL clock, refer to the calculation formula in 3.3.1. of reference manual "I²C Interface Version A".

Note 2: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/tf on the SCL/SDA should be included in the data hold time.

Note 3: To keep the time by software.

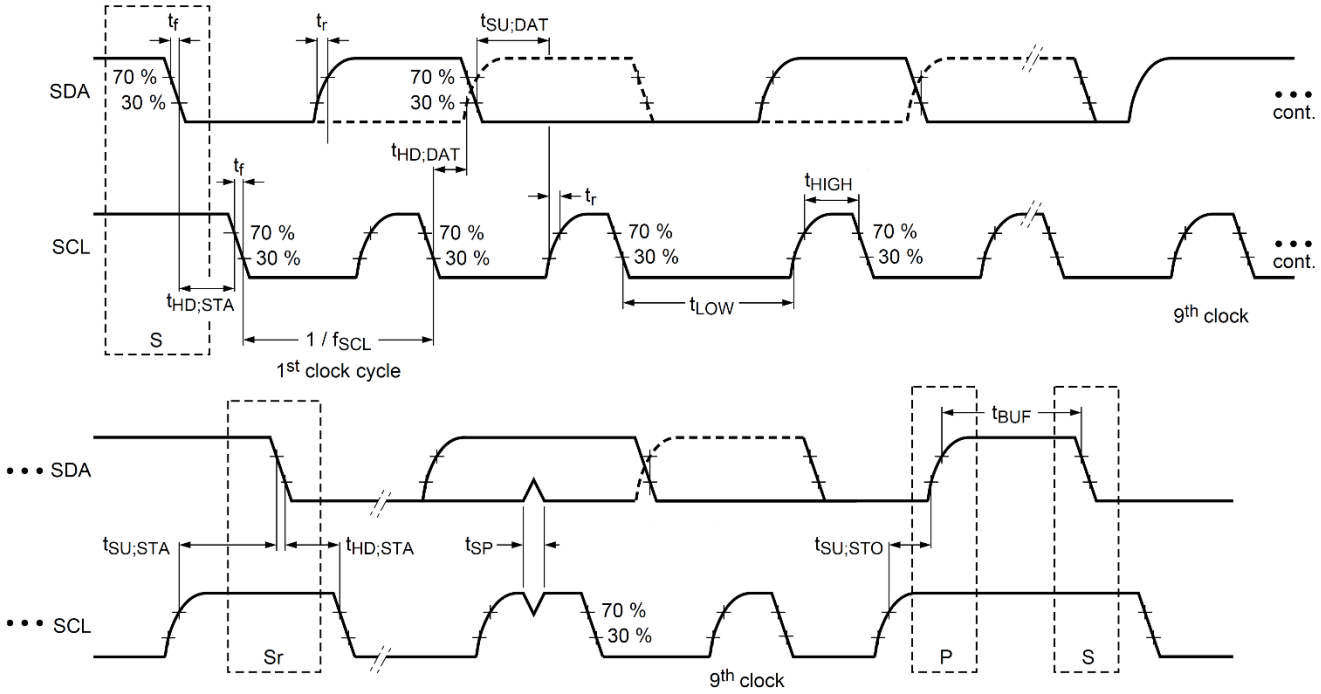


Figure 7.7 AC timing of EI2C

7.11.4. 32-bit Timer Event Counter (T32A)

This section describes the AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.11.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.4.2. AC Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0 clock. This cycle depends on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Equation		ΦT0 = 80MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	45	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	45	-	

(2) At the pulse count

Parameter	Symbol	Equation		ΦT0 = 80MHz NF = 4		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	
Input setup	t_{ABS}	(NF+1)×T+20	-	82.5	-	
Input hold	t_{ABH}	(NF+1)×T+20	-	82.5	-	

NF Value depends on the ***[T32AxPLSCR]***<NF[1:0]> setting as follows.

***[T32AxPLSCR]*<NF[1:0]>**	**NF Value of Formula**
00	0
01	2
10	4
11	8

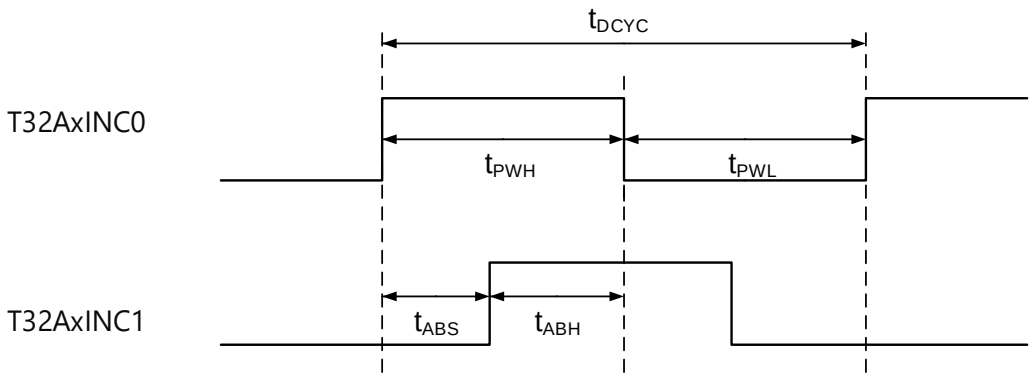


Figure 7.8 Count Pulse input

7.11.5. External Interrupt

7.11.5.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.5.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock fsys.

(1) NORMAL, IDLE mode

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTAL1}	T + 100	-	112.5	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	112.5	-	

(2) STOP1, STOP2 mode

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTCL2}	125	-	125	-	ns
High level pulse width	t_{INTCH2}	125	-	125	-	

7.11.6. Trigger Input (TRGINx)

7.11.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.6.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock fsys.

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{ADL}	2T + 20	-	45	-	ns
High level pulse width	t_{ADH}	2T + 20	-	45	-	

7.11.7. Debug Communication

7.11.7.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.7.2. SWD Interface

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK high level width	t_{dckh}	50	-	ns
CLK low level width	t_{dckl}	50	-	
Output data hold time from the rising edge of CLK	t_{d1}	1	-	
Output data valid time from the rising edge of CLK	t_{d2}	-	35	
Rising edge of CLK time from the input data valid	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Min	Max	Unit
CLK high level width	t_{dckh}	50	-	ns
CLK low level width	t_{dckl}	50	-	
Output data hold time from the rising edge of CLK	t_{d1}	1	-	
Output data valid time from the rising edge of CLK	t_{d2}	-	45	
Rising edge of CLK time from the input data valid	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

7.11.7.3. JTAG Interface

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK high level width	t_{dckh}	50	-	ns
CLK low level width	t_{dckl}	50	-	
Output data hold time from the falling edge of CLK	t_{d3}	0	-	
Output data valid time from the falling edge of CLK	t_{d4}	-	35	
Rising edge of CLK time from the input data valid	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Min	Max	Unit
CLK high level width	t_{dckh}	50	-	ns
CLK low level width	t_{dckl}	50	-	
Output data hold time from the falling edge of CLK	t_{d3}	0	-	
Output data valid time from the falling edge of CLK	t_{d4}	-	45	
Rising edge of CLK time from the input data valid	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

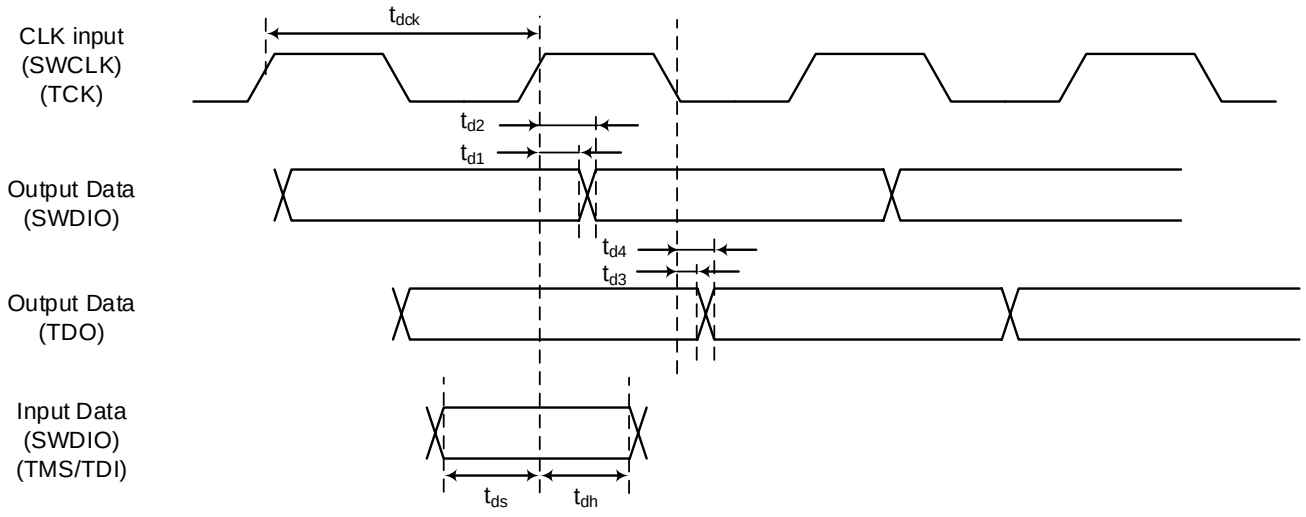


Figure 7.9 JTAG/SWD waveform

7.11.7.4. ETM Trace

4.5V ≤ DVDD5 = AVDD5 ≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	50	-	ns
Rising edge of TRACECLK time from the TRACEDATA valid	t_{setupr}	2	-	
TRACEDATA hold time from the rising edge of TRACECLK	t_{holdr}	1	-	
Falling edge of TRACECLK time from the TRACEDATA valid	t_{setupf}	2	-	
TRACEDATA hold time from the falling edge of TRACECLK	t_{holdf}	1	-	

2.7V ≤ DVDD5 = AVDD5 < 4.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	100	-	ns
Rising edge of TRACECLK time from the TRACEDATA valid	t_{setupr}	2	-	
TRACEDATA hold time from the rising edge of TRACECLK	t_{holdr}	1	-	
Falling edge of TRACECLK time from the TRACEDATA valid	t_{setupf}	2	-	
TRACEDATA hold time from the falling edge of TRACECLK	t_{holdf}	1	-	

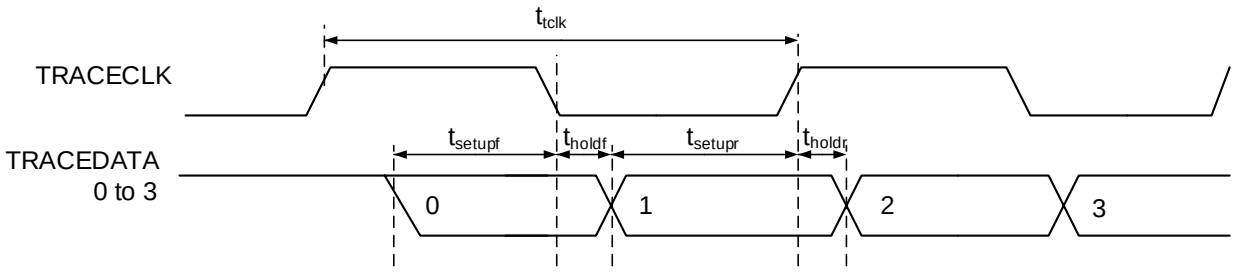


Figure 7.10 Trace signal waveform

7.11.8. SCOUT Pin

7.11.8.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.8.2. AC Electrical Characteristics

"T" in the table indicates the cycle of the SCOUT output waveform.

Parameter	Symbol	Equation		SCOUT = 20MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{SCL}	0.5T- 10	-	15	-	ns
High level pulse width	t_{SCH}	0.5T- 10	-	15	-	

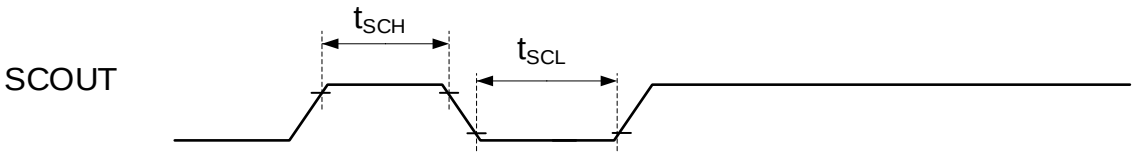


Figure 7.11 SCOUT wave output

7.11.9. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	-	15	30	60	ns

7.11.10. External Clock Input

7.11.10.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7 to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.11.10.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency ($1/t_{ehcin}$)	$f_{EHCLKIN}$	6	-	20	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

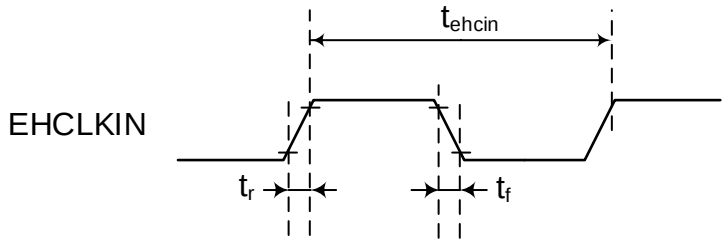


Figure 7.12 External clock input waveform

7.12. Flash Memory Characteristics

7.12.1. Code Flash

DVDD5 = 2.7V to 5.5V
Ta = -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	100,000	cycles
Programming time	Word Program time	-	22.6	-	μs
Erase time	Page Erase time	1.1	-	4.2	ms
	Block Erase time	8.4	-	33.6	
	Area Erase time (Note 2)	-	9.1	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note 2: When Erase command executes, no block with effective protection.

7.12.2. Data Flash

DVDD5 = 2.7V to 5.5V
Ta = -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	100,000	cycles
Programing time	-	-	78	-	μs
Erase time	Page Erase time	1.1	-	4.2	ms
	Block Erase time	16.2	-	64.6	
	Area Erase time (Note 2)	-	9.1	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note 2: When Erase command executes, no block with effective protection.

7.12.3. Chip Erase

DVDD5 = 2.7V to 5.5V
Ta = -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Chip Erase time	Code flash Data flash Protect Bits (Code) Protect Bits (Data) User Information Area Security Bits	21.3	-	30.6	ms

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note 2: When Chip Erase command executes, no block with effective protection.

7.13. Regulator

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT2 capacitor	DVDD5 = 2.7 to 5.5V Ta = -40 to 105°C	0.8	4.7	5.64	μF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.14. Oscillation Circuit

7.14.1. Internal Oscillator

DVDD5 = 2.7 to 5.5V
Ta = -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	-	9.9	10	10.1	MHz
	f_{IHOSC2}	-	-	10	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Please execute IHOSC1 oscillator adjustment by the trimming register, if it is required.
IHOSC2 oscillator cannot be adjusted.

7.14.2. External Oscillator

DVDD5 = 2.7 to 5.5V
Ta = -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}	-	6	-	12	MHz
	f_{ELOSC}	-	30	-	34	kHz

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

7.14.3. Oscillation Circuit Sample

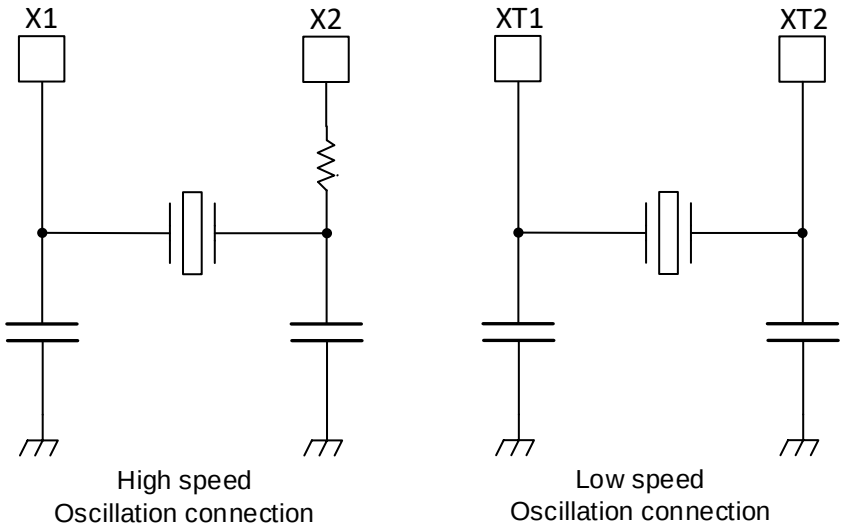


Figure 7.13 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer to this information when selecting external parts.

7.14.4. Ceramic Resonator

This product has been evaluated by the ceramic resonator by Murata Manufacturing Co., Ltd.

Please refer to the Murata Website for details.

7.14.5. Crystal Unit

This product has been evaluated by the crystal unit by KYOCERA Corporation.

Please refer to the KYOCERA Website for details.

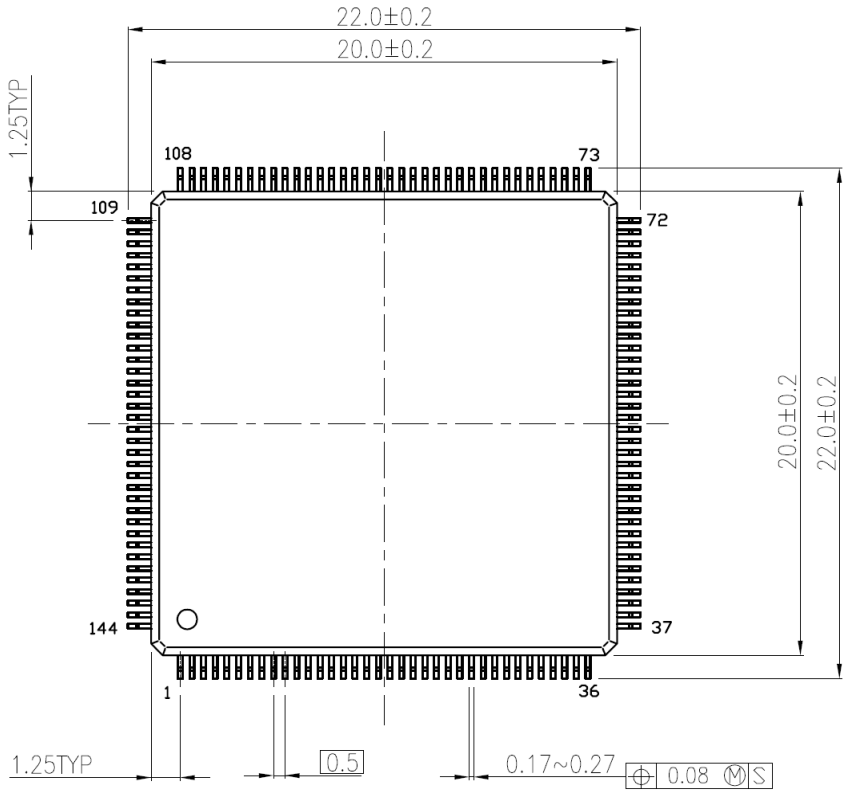
7.14.6. Precautions for designing printed circuit board

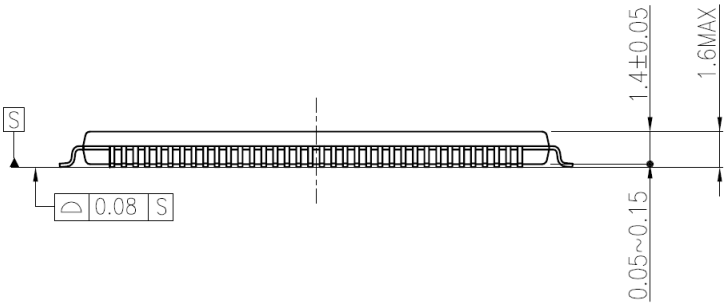
Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

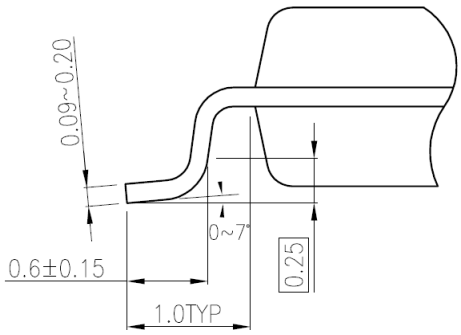
8. Package Dimensions

8.1. P-LQFP144-2020-0.50-002

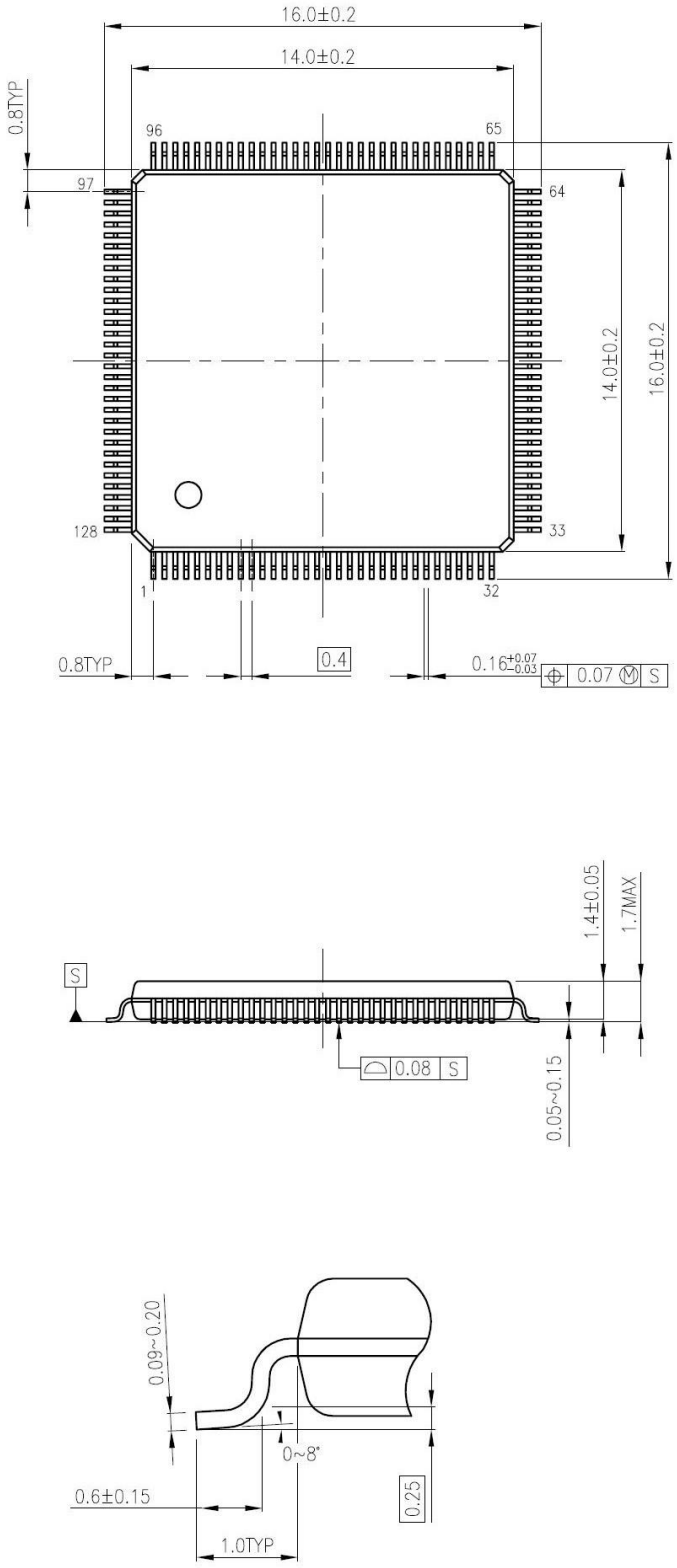
Unit: mm







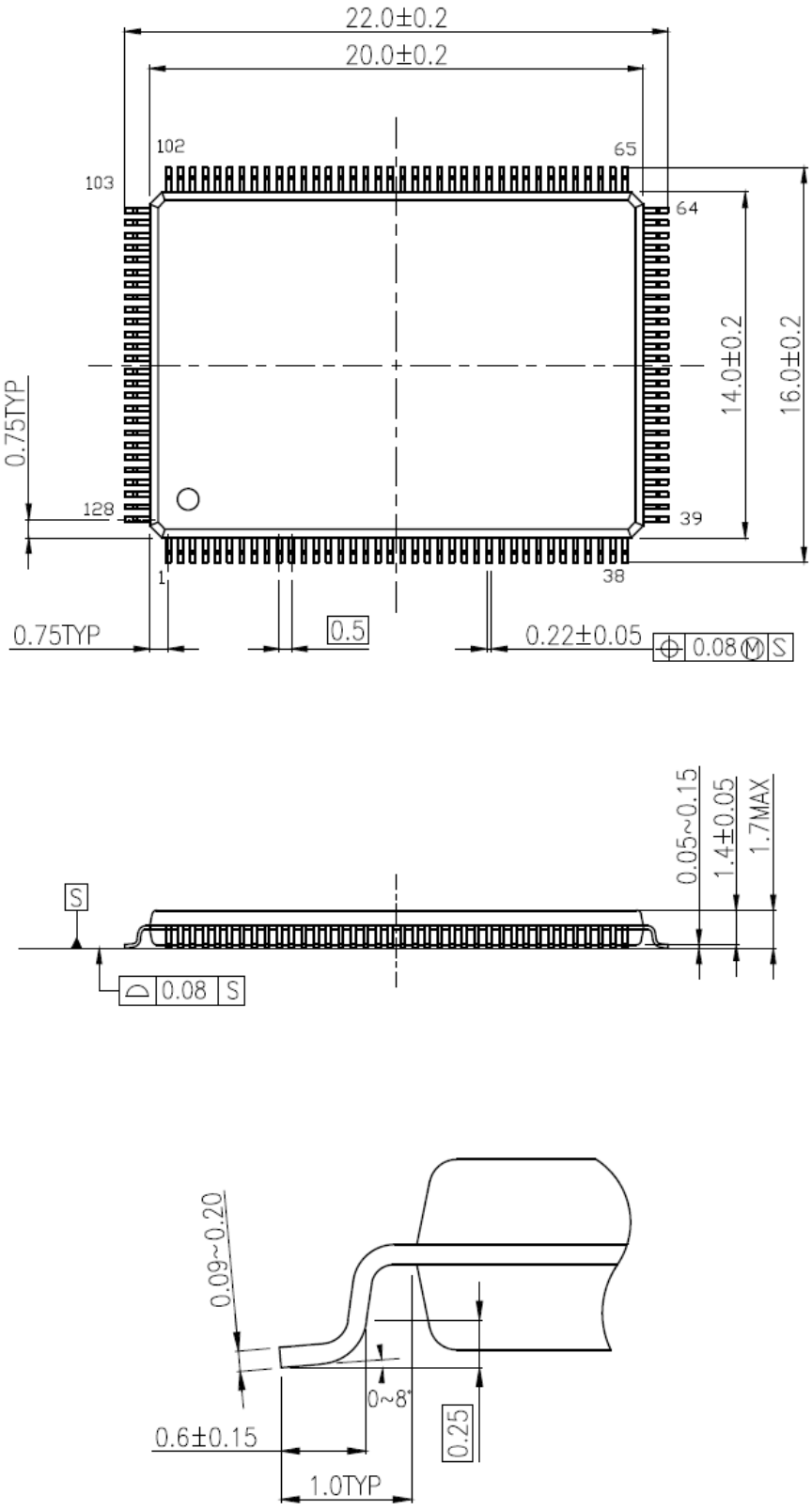
8.2. P-LQFP128-1414-0.40-001



Unit: mm

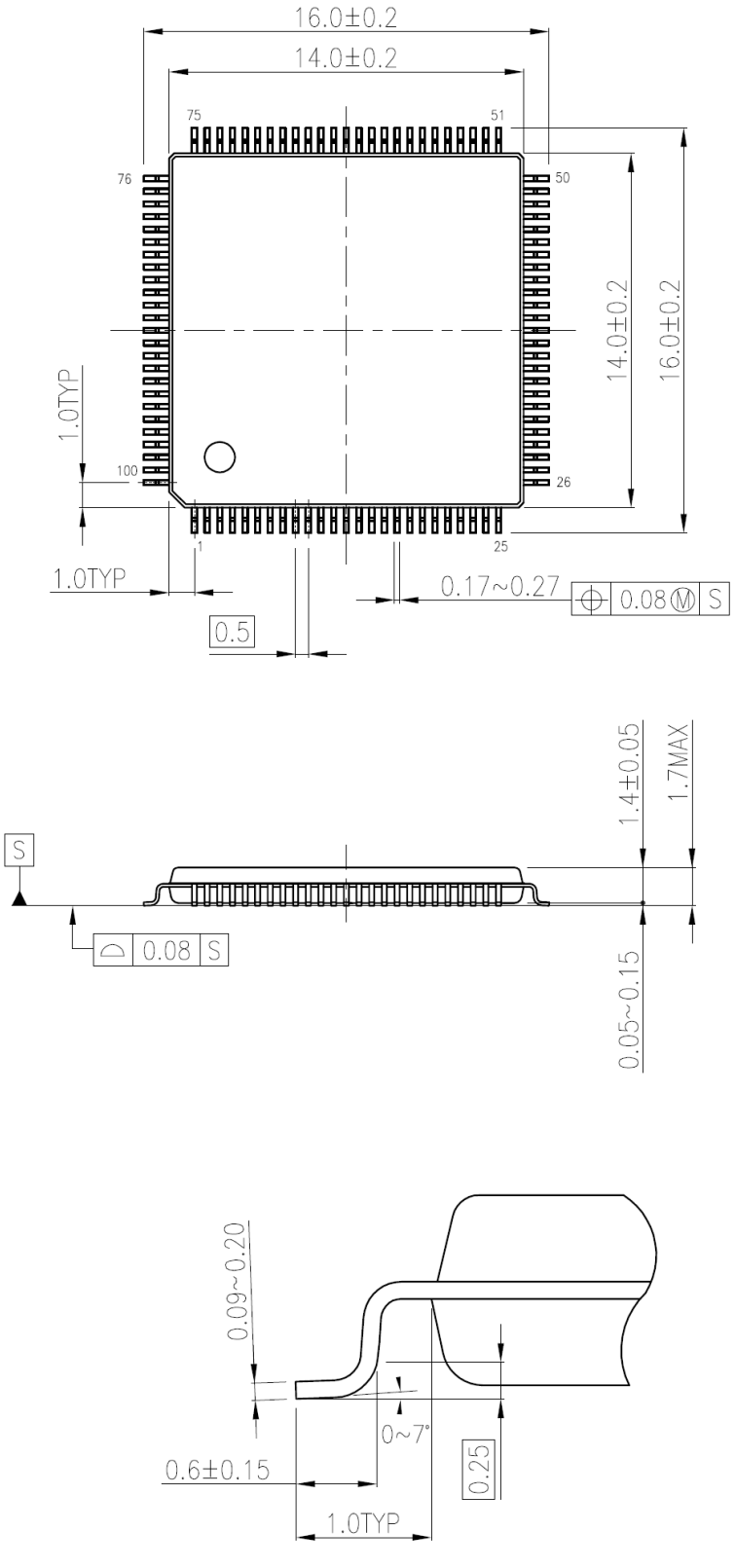
8.3. P-LQFP128-1420-0.50-001

Unit: mm



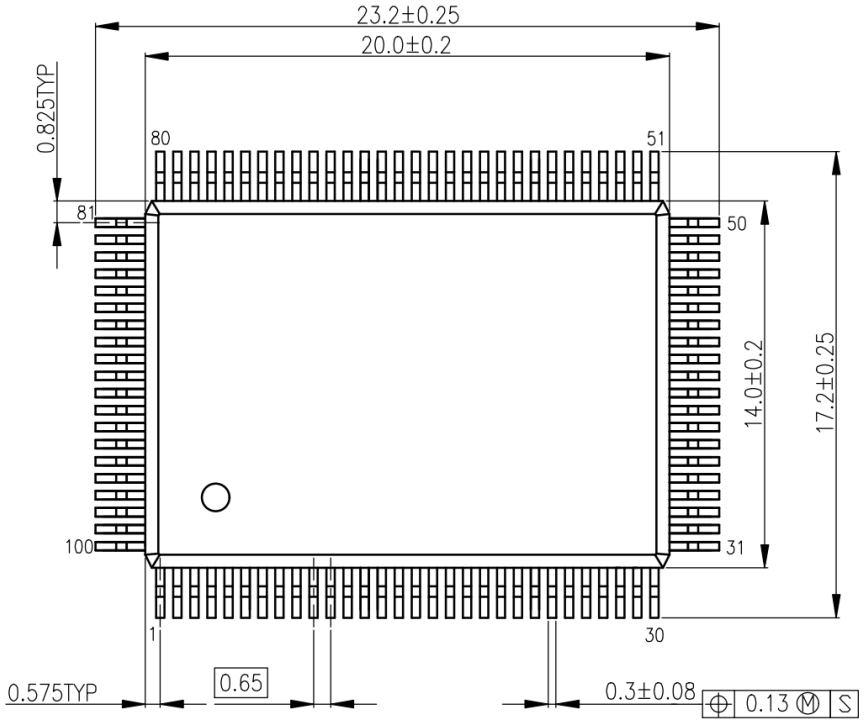
8.4. P-LQFP100-1414-0.50-002

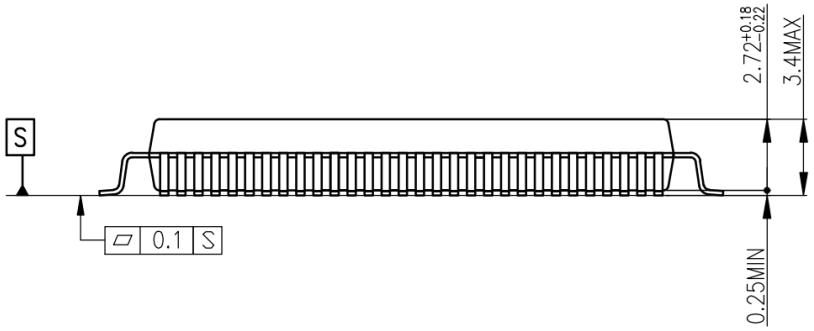
Unit: mm

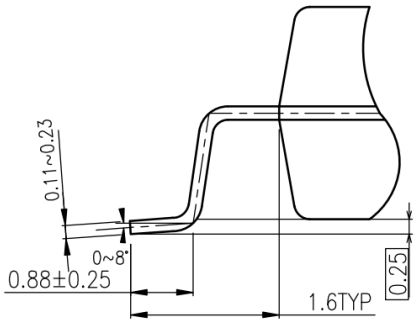


8.5. P-QFP100-1420-0.65-003

Unit: mm

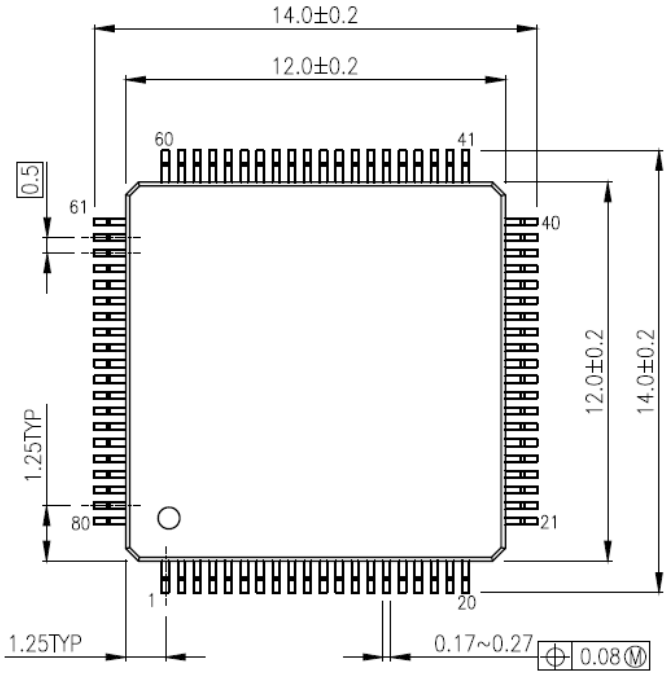


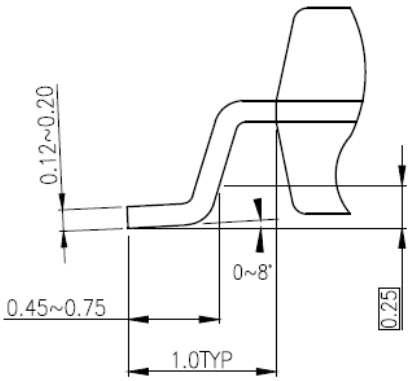




8.6. P-LQFP80-1212-0.50-003

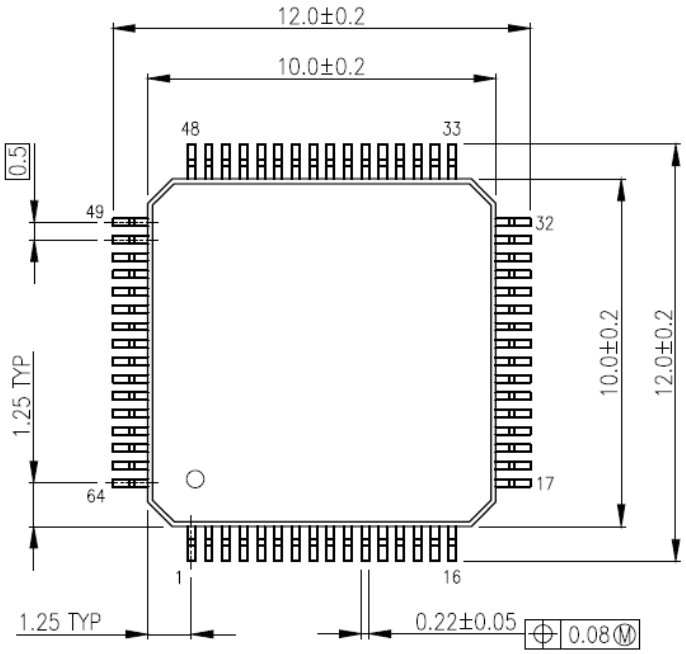
Unit: mm

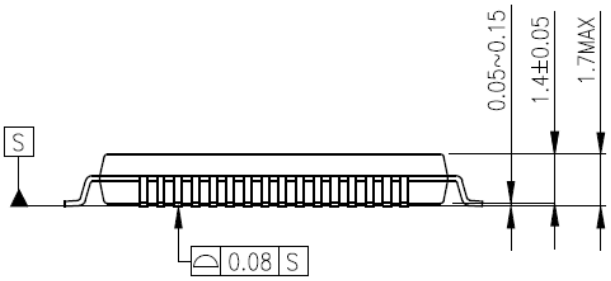


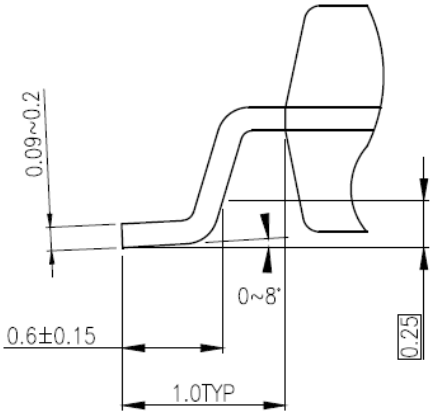


8.7. P-LQFP64-1010-0.50-003

Unit: mm







9. Precautions

This Page explains general precautions on the use of Toshiba MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of the document has higher priority.

(1) The MCUs' operation at power-on

At power-on, the internal state of the MCUs is unstable. Therefore, the state of the pins is undefined until the reset operation is started and valid.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is started and valid.

Also, when a reset is performed by the internal power-on reset, pins of the MCUs that use the internal power-on reset are undefined until power supply voltage reaches the voltage at which power- on reset is started and valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the destination clock is stable.

10. Revision History

Table 10.1 Revision History

Revision	Date	Description
2.0	2022-03-31	First release
2.1	2022-06-06	- 4.1.4. Power Supply Pins Changed Note 4. - 4.1.5. Capacitors between power supply pins Changed Note 3.
2.2	2023-02-10	- 7.4. 12-bit AD Converter Characteristics Deleted “Reference power supply” (ch27
2.3	2023-07-07	- 8.5 P-QFP100-1420-0.65-003 Package name and figure are changed.

Appendix

List of All pins

Combination Function A to B: These are the functions which become effective without setting up port function registers.

Combination Function 1 to 6: These are the functions which become effective with setting up port function registers.

List of All pins (1)

M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/Output	Pull-up/ Pull-down	5V_T	SMT/ CMOS	Under Reset	After Reset
1	1	4	1	3	PE1	AINA05								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
2	2	5	2	4	PE0	AINA04								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
3	3	6	3	5	PD3	AINA03								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
4	4	7	4	6	PD2	AINA02								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
5	5	8	5	7	PD1	AINA01								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
6	6	9	6	8	PD0	AINA00								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
7	7	10	7	9	AVDD5									-	-	-	-	-	-
8	8	11	8	10	AVSS									-	-	-	-	-	-
9	9	12	9	11	PG0	DAC0								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
10	10	13	10	12	PG1	DAC1								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
11	-	-	-	-	PU5									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
12	-	-	-	-	PU4									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
13	-	-	-	-	PU3									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
14	-	-	-	-	PU2									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
15	11	14	-	-	PG2		INT27	UT3RXD	UT3TXDA	T32A07OUTA	T32A07OUTC			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
16	12	15	-	-	PG3		INT28	UT3TXDA	UT3RXD	T32A07INA0	T32A07INC0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
17	13	16	-	-	PG4			UT3TXDB		T32A07INA1	T32A07INC1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
18	14	17	-	-	PG5					T32A07OUTB				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
19	15	18	-	-	PG6					T32A07INB0				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
20	16	19	-	-	PG7					T32A07INB1				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
21	17	20	11	13	PA7		INT11	UT3TXDA	UT3RXD					Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
22	18	21	12	14	PA6		INT07	UT3RXD	UT3TXDA					Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
23	19	22	13	15	PA5			I2C1SDA	EI2C1SDA		T32A00INB1			Input/Output	PU/PD	T	SMT	Hi-Z	Hi-Z
24	20	23	14	16	PA4			I2C1SCL	EI2C1SCL	TSPI0CS1	T32A00INB0			Input/Output	PU/PD	T	SMT	Hi-Z	Hi-Z
25	21	24	15	17	PA3				TSPI0CSIN	TSPI0CS0	T32A00OUTB		TRGIN1	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
26	22	25	16	18	PA2			UT0RXD	UT0TXDA	TSPI0RXD	T32A00INA1	T32A00INC1	ENC0Z	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
27	23	26	17	19	PA1			UT0TXDA	UT0RXD	TSPI0TXD	T32A00INA0	T32A00INC0	ENC0B	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
28	24	27	18	20	PA0			UT0TXDB		TSPI0SCK	T32A00OUTA	T32A00OUTC	ENC0A	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
29	25	28	-	-	PM7									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
30	26	29	19	21	PM6		INT15							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
31	27	30	20	22	PM5						T32A00INB1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
32	28	31	21	23	PM4			UT0RTS_N	UT0CTS_N	TSPI0CS1	T32A00INB0		TRACEDATA3	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
33	29	32	22	24	PM3			UT0CTS_N	UT0RTS_N	TSPI0CS0	T32A00OUTB	TSPI0CSIN	TRACEDATA2	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
34	30	33	23	25	PM2		INT09	UT0RXD	UT0TXDA	TSPI0RXD	T32A00INA1	T32A00INC1	TRACEDATA1	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
35	31	34	24	26	PM1			UT0TXDA	UT0RXD	TSPI0TXD	T32A00INA0	T32A00INC0	TRACEDATA0	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
36	32	35	25	27	PM0			UT0TXDB		TSPI0SCK	T32A00OUTA	T32A00OUTC	TRACECLK	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
37	33	36	26	28	PB0	BOOT_N					T32A01OUTA	T32A01OUTC	SCOUT	Output	PU/PD	N/A	SMT	Hi-Z (Note1)	Hi-Z
38	34	37	27	29	PB1		INT03	RXIN0			T32A01INA0	T32A01INC0	TRGIN0	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
39	35	38	28	30	PB2			UT2TXDA	UT2RXD	TSPI1SCK	T32A01INA1	T32A01INC1		Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
40	36	39	29	31	PB3			UT2RXD	UT2TXDA	TSPI1TXD	T32A01OUTB			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
41	37	40	30	32	PB4			UT2CTS_N	UT2RTS_N	TSPI1RXD	T32A01INB0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
42	38	41	31	33	PB5			UT2RTS_N	UT2CTS_N	TSPI1CS0	T32A01INB1	TSPI1CSIN		Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
43	39	42	32	34	PB6					TSPI1CS1				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
44	40	43	33	35	PB7		INT16							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
45	-	-	-	-	PU0		INT30							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
46	-	-	-	-	PU1		INT31							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
47	41	44	34	36	PL0			UT2TXDA	UT2RXD	I2C2SCL	EI2C2SCL	TRST_N		Input/Output	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
48	42	45	35	37	PL1			UT2RXD	UT2TXDA	I2C2SDA	EI2C2SDA	TDI		Input/Output	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
49	43	46	36	38	PL2			UT2CTS_N	UT2RTS_N	T32A06OUTB		TDO/SWV		Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
50	44	47	37	39	PL3		INT08	UT2RTS_N	UT2CTS_N	T32A06INB0		TCK/SWCLK		Input/Output	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
51	45	48	38	40	PL4		INT12			T32A06INB1		TMS/SWDIO		Input/Output	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
52	46	49	39	41	PL5					T32A06OUTA	T32A06OUTC			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
53	47	50	40	42	PL6					T32A06INA0	T32A06INC0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
54	48	51	-	-	PL7					T32A06INA1	T32A06INC1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
55	-	-	-	-	PT7		INT29			T32A06INA1	T32A06INC1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
56	-	-	-	-	PT6					T32A06INA0	T32A06INC0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
57	-	-	-	-	PT5					T32A06OUTA	T32A06OUTC			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
58	-	-	-	-	PT4			TSPI2RXD		T32A06INB1				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
59	49	52	-	-	PT3		INT26	TSPI2TXD		T32A06INB0				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
60	50	53	-	-	PT2		INT25	TSPI2SCK		T32A06OUTB				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
61	51	54	-	-	PT1		INT24	I2C3SCL	TSPI2CS0	TSPI2CSIN	EI2C3SCL			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
62	52	55	-	-	PT0		INT23	I2C3SDA	TSPI2CS1		EI2C3SDA			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
63	53	56	41	43	PP0				TSPI2SCK	T32A01OUTA	T32A01OUTC			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
64	54	57	42	44	PP1				TSPI2TXD	T32A01INA0	T32A01INC0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
65	55	58	43	45	PP2				TSPI2RXD	T32A01INA1	T32A01INC1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
66	56	59	44	46	DVDD5A									-	-	-	-	-	-
67	57	60	45	47	REGOUT2									-	-	-	-	-	-
68	58	61	46	48	PW0									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
69	59	62	47	49	DVSSA									-	-	-	-	-	-
70	60	63	48	50	PH0	X1	EHCLKIN							Input	PD	N/A	SMT	Hi-Z	Hi-Z
71	61	64	49	51	PH1	X2								Input	PD	N/A	SMT	Hi-Z	Hi-Z
72	62	65	50	52	RESET_N									-	PU	-	SMT	-	-
73	63	66	51	53	PH2	XT1								Input	PD	N/A	SMT	Hi-Z	Hi-Z
74	64	67	52	54	PH3	XT2	INT06							Input	PD	N/A	SMT	Hi-Z	Hi-Z
75	65	68	53	55	MODE									-	PD	-	SMT	-	-
76	66	69	-	-	PH4		INT19	TSPI4SCK						Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
77	67	70	-	-	PH5		INT20	TSPI4TXD						Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
78	68	71	-	-	PH6		INT21	TSPI4RXD						Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
79	69	72	-	-	PH7		INT22							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
80	-	-	-	-	PV5			UT4TXDB						Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
81	-	-	-	-	PV6			UT4TXDA	UT4RXD					Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
82	-	-	-	-	PV7			UT4RXD	UT4TXDA					Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
83	70	73	54	56	PC0		INT00	I2C0SCL	EI2C0SCL	T32A02OUTA	T32A02OUTC		DCOM3	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
84	71	74	55	57	PC1		INT01	I2C0SDA	EI2C0SDA	T32A02INA0	T32A02INC0		DCOM2	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
85	72	75	56	58	PC2		INT02	UT4TXDB		T32A02INA1	T32A02INC1	RTCOUT	DCOM1	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
86	73	76	57	59	PC3			UT4TXDA	UT4RXD	T32A02OUTB			DCOM0	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
87	74	77	58	60	PC4			UT4RXD	UT4TXDA	T32A02INB0			SEG39	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
88	75	78	59	61	PC5			UT4CTS_N	UT4RTS_N	T32A02INB1			SEG38	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
89	76	79	60	62	PC6			UT4RTS_N	UT4CTS_N				SEG37	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
90	77	80	61	63	PR0			UT7RXD	UT7TXDA	T32A02OUTA	T32A02OUTC		SEG36	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
91	78	81	62	64	PR1			UT7TXDA	UT7RXD	T32A02INA0	T32A02INC0		SEG35	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
92	79	82	63	65	PR2			UT7TXDB		T32A02INA1	T32A02INC1		SEG34	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
93	80	83	64	66	PR3								SEG33	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
94	81	84	-	-	PR4								SEG32	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
95	82	85	-	-	PR5								SEG31	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
96	83	86	-	-	PR6								SEG30	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
97	84	87	-	-	PR7								SEG29	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
98	85	88	65	67	PN5					T32A05INB1			SEG28	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
99	86	89	66	68	PN4			UT5TXDB		T32A05INB0			SEG27	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
100	87	90	67	69	PN3		INT10	UT5TXDA	UT5RXD	T32A05OUTB		TRGIN2	SEG26	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
101	88	91	68	70	PN2			UT5RXD	UT5TXDA	T32A05INA1	T32A05INC1		SEG25	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
102	89	92	69	71	PN1			UT5CTS_N	UT5RTS_N	T32A05INA0	T32A05INC0		SEG24	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
103	90	93	70	72	PN0			UT5RTS_N	UT5CTS_N	T32A05OUTA	T32A05OUTC		SEG23	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z

Note 1: When the RESET_N pin is "Low", a built-in pull-up resistor becomes effective.

Note 2: The Initial value of built-in Pull-up/Pull-down resistor is effective.

List of All pins (2)

M3HQ (LQFP144)	M3HP (LQFP128-1414)	M3HP (LQFP128-1420)	M3HN (LQFP100)	M3HN (QFP100)	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/Output	Pull-up/ Pull-down	5V_T	SMT/ CMOS	Under Reset	After Reset
104	91	94	71	73	PJ0			UT1TXDB		T32A03OUTA	T32A03OUTC	UO0	SEG22	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
105	92	95	72	74	PJ1			UT1TXDA	UT1RXD	T32A03INA0	T32A03INC0	XO0	SEG21	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
106	93	96	73	75	PJ2			UT1RXD	UT1TXDA	T32A03INA1	T32A03INC1	VO0	SEG20	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
107	94	97	74	76	PJ3			UT1CTS_N	UT1RTS_N	T32A03OUTB		YO0	SEG19	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
108	95	98	75	77	PJ4		INT04	UT1RTS_N	UT1CTS_N	T32A03INB0		WO0	SEG18	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
109	96	99	76	78	PJ5					T32A03INB1		ZO0	SEG17	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
110	97	100	77	79	PK0			UT1TXDB				EMG0	SEG16	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
111	98	101	78	80	PK1		INT05	UT1TXDA	UT1RXD			OVV0	SEG15	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
112	99	102	79	81	PK2			UT1RXD	UT1TXDA	T32A04OUTA	T32A04OUTC		SEG14	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
113	100	103	80	82	PK3			UT1CTS_N	UT1RTS_N	T32A04INA0	T32A04INC0		SEG13	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
114	101	104	81	83	PK4			UT1RTS_N	UT1CTS_N	T32A04INA1	T32A04INC1		SEG12	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
115	102	105	82	84	PK5			UT6RXD	UT6TXDA	T32A04OUTB			SEG11	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
116	103	106	83	85	PK6			UT6TXDA	UT6RXD	T32A04INB0			SEG10	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
117	104	107	84	86	PK7		INT13	UT6TXDB		T32A04INB1			SEG09	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
118	105	108	85	87	PP3		INT14	TSPI3RXD					SEG08	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
119	106	109	86	88	PP4			TSPI3TXD					SEG07	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
120	107	110	87	89	PP5			TSPI3SCK					SEG06	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
121	108	111	88	90	PP6			TSPI3CS0	TSPI3CSIN	PMD0DBG			SEG05	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
122	109	112	89	91	PP7			TSPI3CS1					SEG04	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
123	110	113	-	-	PV0								SEG03	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
124	111	114	-	-	PV1								SEG02	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
125	112	115	-	-	PV2		INT17						SEG01	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
126	113	116	-	-	PV3		INT18						SEG00	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
127	-	-	-	-	PV4									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
128	114	117	-	-	DVDD5B									-	-	-	-	-	-
129	115	118	-	-	DVSSB									-	-	-	-	-	-
130	-	-	-	-	PD5	AINA20								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
131	-	-	-	-	PD4	AINA19								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
132	116	119	-	-	PF7	AINA18								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
133	117	120	-	-	PF6	AINA17								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
134	118	121	90	92	PF5	AINA16								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
135	119	122	91	93	PF4	AINA15								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
136	120	123	92	94	PF3	AINA14	INT32							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
137	121	124	93	95	PF2	AINA13	INT33							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
138	122	125	94	96	PF1	AINA12								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
139	123	126	95	97	PF0	AINA11								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
140	124	127	96	98	PE6	AINA10								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
141	125	128	97	99	PE5	AINA09								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
142	126	1	98	100	PE4	AINA08								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
143	127	2	99	1	PE3	AINA07								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
144	128	3	100	2	PE2	AINA06								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z

List of All pins (3)

M3HM (LQFP80)	M3HL (LQFP64)	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/Output	Pull-up/ Pull-down	5V_T	SMT/ CMOS	Under Reset	After Reset
1	1	PE1	AINA05								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
2	2	PE0	AINA04								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PD3	AINA03								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
3	3	PD2	AINA02								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
4	4	PD1	AINA01								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
5	5	PD0	AINA00								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
6	6	AVDD5									-	-	-	-	-	-
7	7	AVSS									-	-	-	-	-	-
8	8	PG0	DAC0								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
9	9	PG1	DAC1								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PU5									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PU4									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PU3									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PU2									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PG2		INT27	UT3RXD	UT3TXDA	T32A07OUTA	T32A07OUTC			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PG3		INT28	UT3TXDA	UT3RXD	T32A07INA0	T32A07INC0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PG4			UT3TXDB		T32A07INA1	T32A07INC1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PG5					T32A07OUTB				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PG6					T32A07INB0				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PG7					T32A07INB1				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
10	10	PA7		INT11	UT3TXDA	UT3RXD					Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
11	11	PA6		INT07	UT3RXD	UT3TXDA					Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
12	-	PA5			I2C1SDA	EI2C1SDA		T32A00INB1			Input/Output	PU/PD	T	SMT	Hi-Z	Hi-Z
13	-	PA4			I2C1SCL	EI2C1SCL	TSPI0CS1	T32A00INB0			Input/Output	PU/PD	T	SMT	Hi-Z	Hi-Z
14	12	PA3				TSPI0CSIN	TSPI0CS0	T32A00OUTB		TRGIN1	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
15	13	PA2			UT0RXD	UT0TXDA	TSPI0RXD	T32A00INA1	T32A00INC1	ENC0Z	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
16	14	PA1			UT0TXDA	UT0RXD	TSPI0TXD	T32A00INA0	T32A00INC0	ENC0B	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
17	15	PA0			UT0TXDB		TSPI0SCK	T32A00OUTA	T32A00OUTC	ENC0A	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PM7									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PM6		INT15							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PM5						T32A00INB1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PM4			UT0RTS_N	UT0CTS_N	TSPI0CS1	T32A00INB0		TRACEDATA3	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PM3			UT0CTS_N	UT0RTS_N	TSPI0CS0	T32A00OUTB	TSPI0CSIN	TRACEDATA2	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
18	-	PM2		INT09	UT0RXD	UT0TXDA	TSPI0RXD	T32A00INA1	T32A00INC1	TRACEDATA1	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
19	-	PM1			UT0TXDA	UT0RXD	TSPI0TXD	T32A00INA0	T32A00INC0	TRACEDATA0	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
20	16	PM0			UT0TXDB		TSPI0SCK	T32A00OUTA	T32A00OUTC	TRACECLK	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
21	17	PB0	BOOT_N					T32A01OUTA	T32A01OUTC	SCOUT	Output	PU/PD	N/A	SMT	Hi-Z (Note1)	Hi-Z
22	18	PB1		INT03	RXIN0			T32A01INA0	T32A01INC0	TRGIN0	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
23	19	PB2			UT2TXDA	UT2RXD	TSPI1SCK	T32A01INA1	T32A01INC1		Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
24	20	PB3			UT2RXD	UT2TXDA	TSPI1TXD	T32A01OUTB			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
25	-	PB4			UT2CTS_N	UT2RTS_N	TSPI1RXD	T32A01INB0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PB5			UT2RTS_N	UT2CTS_N	TSPI1CS0	T32A01INB1	TSPI1CSIN		Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PB6					TSPI1CS1				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PB7		INT16							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PU0		INT30							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PU1		INT31							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
26	21	PL0			UT2TXDA	UT2RXD	I2C2SCL	EI2C2SCL	TRST_N		Input/Output	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
27	22	PL1			UT2RXD	UT2TXDA	I2C2SDA	EI2C2SDA	TDI		Input/Output	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
28	23	PL2			UT2CTS_N	UT2RTS_N	T32A06OUTB		TDO/SWV		Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
29	24	PL3		INT08	UT2RTS_N	UT2CTS_N	T32A06INB0		TCK/SWCLK		Input/Output	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
30	25	PL4		INT12			T32A06INB1		TMS/SWDIO		Input/Output	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
-	-	PL5					T32A06OUTA	T32A06OUTC			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PL6					T32A06INA0	T32A06INC0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PL7					T32A06INA1	T32A06INC1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PT7		INT29			T32A06INA1	T32A06INC1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PT6					T32A06INA0	T32A06INC0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PT5					T32A06OUTA	T32A06OUTC			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PT4			TSPI2RXD		T32A06INB1				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PT3		INT26	TSPI2TXD		T32A06INB0				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PT2		INT25	TSPI2SCK		T32A06OUTB				Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PT1		INT24	I2C3SCL	TSPI2CS0	TSPI2CSIN	EI2C3SCL			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PT0		INT23	I2C3SDA	TSPI2CS1		EI2C3SDA			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
31	-	PP0				TSPI2SCK	T32A01OUTA	T32A01OUTC			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
32	-	PP1				TSPI2TXD	T32A01INA0	T32A01INC0			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
33	-	PP2				TSPI2RXD	T32A01INA1	T32A01INC1			Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
34	26	DVDD5A									-	-	-	-	-	-
35	27	REGOUT2									-	-	-	-	-	-
36	28	PW0									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
37	29	DVSSA									-	-	-	-	-	-
38	30	PH0	X1	EHCLKIN							Input	PD	N/A	SMT	Hi-Z	Hi-Z
39	31	PH1	X2								Input	PD	N/A	SMT	Hi-Z	Hi-Z
40	32	RESET_N									-	PU	-	SMT	-	-
41	33	PH2	XT1								Input	PD	N/A	SMT	Hi-Z	Hi-Z
42	34	PH3	XT2	INT06							Input	PD	N/A	SMT	Hi-Z	Hi-Z
43	35	MODE									-	PD	-	SMT	-	-
-	-	PH4		INT19	TSPI4SCK						Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PH5		INT20	TSPI4TXD						Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PH6		INT21	TSPI4RXD						Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PH7		INT22							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PV5			UT4TXDB						Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PV6			UT4TXDA	UT4RXD					Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PV7			UT4RXD	UT4TXDA					Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
44	36	PC0		INT00	I2C0SCL	EI2C0SCL	T32A02OUTA	T32A02OUTC		DCOM3	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
45	37	PC1		INT01	I2C0SDA	EI2C0SDA	T32A02INA0	T32A02INC0		DCOM2	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
46	-	PC2		INT02	UT4TXDB		T32A02INA1	T32A02INC1	RTCOUT	DCOM1	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
47	38	PC3			UT4TXDA	UT4RXD	T32A02OUTB			DCOM0	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
48	39	PC4			UT4RXD	UT4TXDA	T32A02INB0			SEG39	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
49	-	PC5			UT4CTS_N	UT4RTS_N	T32A02INB1			SEG38	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
50	-	PC6			UT4RTS_N	UT4CTS_N				SEG37	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PR0			UT7RXD	UT7TXDA	T32A02OUTA	T32A02OUTC		SEG36	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PR1			UT7TXDA	UT7RXD	T32A02INA0	T32A02INC0		SEG35	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PR2			UT7TXDB		T32A02INA1	T32A02INC1		SEG34	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PR3								SEG33	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PR4								SEG32	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PR5								SEG31	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PR6								SEG30	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PR7								SEG29	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PN5					T32A05INB1			SEG28	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
51	40	PN4			UT5TXDB		T32A05INB0			SEG27	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
52	41	PN3		INT10	UT5TXDA	UT5RXD	T32A05OUTB		TRGIN2	SEG26	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
53	42	PN2			UT5RXD	UT5TXDA	T32A05INA1	T32A05INC1		SEG25	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
54	43	PN1			UT5CTS_N	UT5RTS_N	T32A05INA0	T32A05INC0		SEG24	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
55	-	PN0			UT5RTS_N	UT5CTS_N	T32A05OUTA	T32A05OUTC		SEG23	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z

Note 1: When the RESET_N pin is "Low", a built-in pull-up resistor becomes effective.

Note 2: The Initial value of built-in Pull-up/Pull-down resistor is effective.

List of All Pins (4)

M3HM (LQFP80)	M3HL (LQFP64)	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/Output	Pull-up/ Pull-down	5V_T	SMT/ CMOS	Under Reset	After Reset
56	44	PJ0			UT1TXDB		T32A03OUTA	T32A03OUTC	UO0	SEG22	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
57	45	PJ1			UT1TXDA	UT1RXD	T32A03INA0	T32A03INC0	XO0	SEG21	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
58	46	PJ2			UT1RXD	UT1TXDA	T32A03INA1	T32A03INC1	VO0	SEG20	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
59	47	PJ3			UT1CTS_N	UT1RTS_N	T32A03OUTB		YO0	SEG19	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
60	48	PJ4		INT04	UT1RTS_N	UT1CTS_N	T32A03INB0		WO0	SEG18	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
61	49	PJ5					T32A03INB1		ZO0	SEG17	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
62	50	PK0			UT1TXDB				EMG0	SEG16	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
63	51	PK1		INT05	UT1TXDA	UT1RXD			OVV0	SEG15	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
64	52	PK2			UT1RXD	UT1TXDA	T32A04OUTA	T32A04OUTC		SEG14	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
65	53	PK3			UT1CTS_N	UT1RTS_N	T32A04INA0	T32A04INC0		SEG13	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
66	54	PK4			UT1RTS_N	UT1CTS_N	T32A04INA1	T32A04INC1		SEG12	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
67	55	PK5			UT6RXD	UT6TXDA	T32A04OUTB			SEG11	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
68	56	PK6			UT6TXDA	UT6RXD	T32A04INB0			SEG10	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
69	-	PK7		INT13	UT6TXDB		T32A04INB1			SEG09	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
70	57	PP3		INT14	TSPI3RXD					SEG08	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
71	-	PP4			TSPI3TXD					SEG07	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
72	-	PP5			TSPI3SCK					SEG06	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
73	-	PP6			TSPI3CS0	TSPI3CSIN	PMD0DBG			SEG05	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PP7			TSPI3CS1					SEG04	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PV0								SEG03	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PV1								SEG02	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PV2		INT17						SEG01	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PV3		INT18						SEG00	Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PV4									Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	DVDD5B									-	-	-	-	-	-
-	-	DVSSB									-	-	-	-	-	-
-	-	PD5	AINA20								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PD4	AINA19								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PF7	AINA18								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PF6	AINA17								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PF5	AINA16								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PF4	AINA15								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PF3	AINA14	INT32							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
-	-	PF2	AINA13	INT33							Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
74	58	PF1	AINA12								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
75	59	PF0	AINA11								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
76	60	PE6	AINA10								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
77	61	PE5	AINA09								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
78	62	PE4	AINA08								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
79	63	PE3	AINA07								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z
80	64	PE2	AINA06								Input/Output	PU/PD	N/A	SMT	Hi-Z	Hi-Z

Part Naming Conventions

TMP M3 H Q F D x FG

The identification of Toshiba microcontrollers

Revision

Package

Symbol	Description
QG	Plastic-shrink quad outline non-leaded package, dry-packed
UG, DUG, FG,DFG	Plastic quad flat package, dry-packed
MG,DMG	Plastic small outline package, dry-packed
XBG	Plastic ball grid array, dry-packed

Core

Symbol	Description
M4	Arm Cortex-M4 with FPU
M3	Arm Cortex-M3
M0	Arm Cortex-M0

Product Group

Family	Group	Main application
TXZ/ TXZ+	H	For General-purpose/Consumer electronics equipment
	K	For Motor/Inverter control/Industrial equipment (Analog combo)
	M	For Motor/Inverter control/Industrial equipment (Analog combo), built-in CAN
	G	For OA/Digital equipment/Industrial equipment
	N	For Industrial network/IoT information management device/Ethernet, built-in USB/CAN
	E	For Precision instrument
	L	For One motor/Inverter control/Industrial equipment
	V	For General-purpose/Consumer electronics equipment (Entry Series)

ROM size

Symbol	Size [KB]
M	32
P	48
S	64
U	96
W	128
Y	256
Z	384
D	512
E	768
10	1,024
15	1,536
20	2,048

Pin Count

Symbol		Pin count	Symbol		Pin count
0	G	32pin 以下	7	P	101pin to 128pin
1	H	33pin to 44pin	8	Q	129pin to 144pin
2	J	45pin to 48pin	9	R	145pin to 176pin
3	K	49pin to 52pin	A	S	177pin to 200pin
4	L	53pin to 64pin	B	T	201pin to 224pin
5	M	65pin to 80pin	C	U	225pin to 250pin
6	N	81pin to 100pin	D	V	251pin to 300pin

ROM type

Symbol	Type
F	Flash

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