Photorelays
~Points for photorelays in high frequency circuit applications 2~

Description

Photorelays (MOSFET output photocouplers) have a variety of advantages, and replacement from mechanical relays is progressing. However, there are some points that must be taken into consideration in comparison with mechanical relays when they are used in high-frequency circuits such as semiconductor testers and measuring instrument applications.

This application note mainly describes precautions when controlling high-frequency signals with photorelays.

Here, signals with a frequency ranging from several hundred MHz to several ten GHz are positioned as high-frequency signals. In addition, assume that a 1-Form-A photorelay (a photorelay in which the output-side MOSFET is turned on when the input-side LED signal is on) is used as a precondition.

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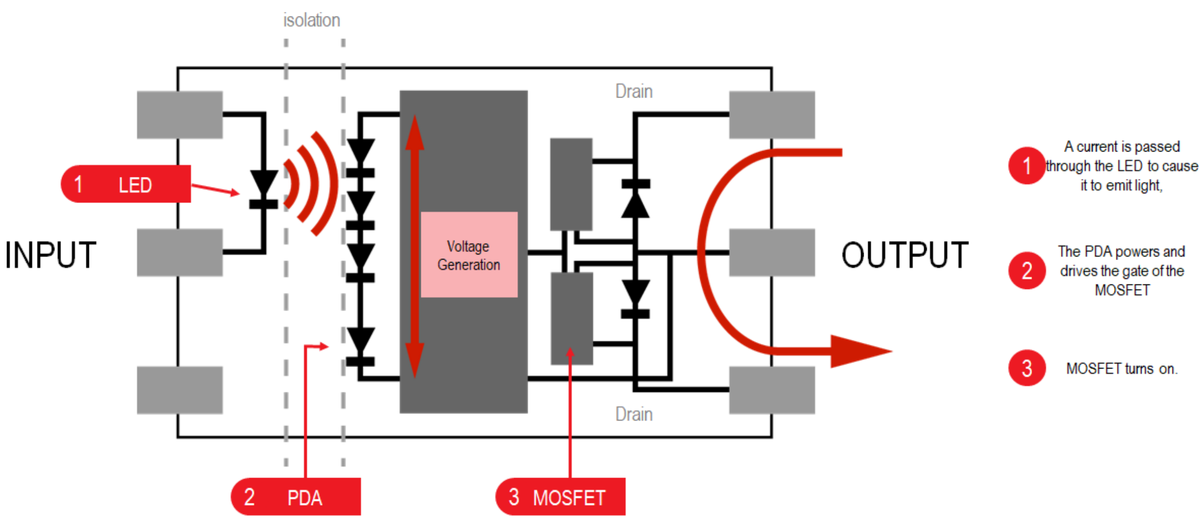
1. Introduction

A photorelay is a semiconductor relay with MOSFETs at the output stage (Fig. 1). Table 1 shows feature comparison between photorelays and mechanical relays.

Recently, reliability has become important and packages of photorelays have become smaller, ther replacement from mechanical relays is progresssing in terms of space saving. However, there is a resistance component (on-resistance R_{ON}) when a photorelay is on compared with a mechanical relay, and a capacitance component (output capacitance C_{OFF}) mainly from the PN junction capacitance of the parasitic diode on the output side MOSFETs when the photorelay is off (Fig. 2). As the frequency increases, the inductance (L) component can also be seen (Fig. 3). Consideration should be given to relpacing mechanical relays with photorelays in circuits that transmit high-frequency signals.

This application note describes additional precautions for photorelays when controlling high-frequency signals, which continues from “Points for photorelays in high frequency circuit applications (released in October, 2020)”.



(1) When current is applied to the LED on the input side, the LED emits light and an optical signal is generated.

(2) The optical signal is converted into an electrical signal by the output-side PDA and MOSFETs. Input the electrical signal to the control terminal (gate).

(3) When the electric signal is input to the gate, MOSFETs are turned on, and the contact is connected.

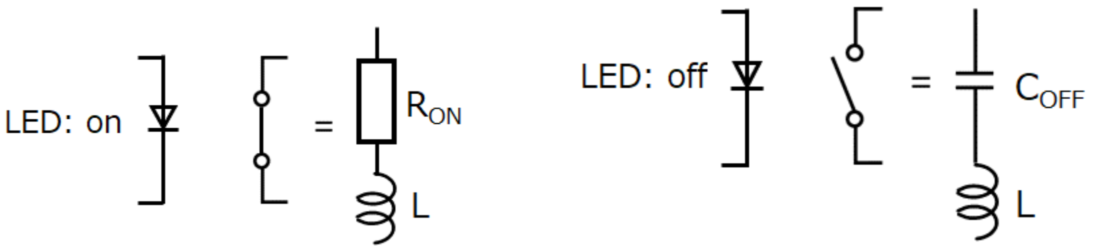
Fig. 1 Principles of operation of photorelay (1-Form-A contact)

Table 1 Comparison between photorelays and mechanical relays

	Mechanical relay (Signal relay)	Photorelay	Remarks (Feature of Photorelay)
Lifetime	△ (With contact limit)	◎ (No contact limit)	Long life
Contact Capacity	◎(2A) ※Ta 85℃/AC・DC applicable	〇 (~5A) ※Ta 25℃/VOFF=60V basis	
Contact Resistance (ON Resistance)	About 0.1Ω (Degraded by On/Off)	About 0.02~25Ω (Stable)	High reliability
Contact Voltage (OFF Voltage)	◎ (ex：AC 250V, DC 30V)	〇 (ex：line up with 20V～600V)	
Isolation Voltage	〇 (ex：1KVrms)	◎ (max 5KVrms)	
Operation / Release Time	△ About 5ms	〇 About 0.1ms	High speed
Operation Sound	△(exist)	◎(No sound)	No noise
Miniaturization	〇 (ex: 60mm²)	◎ (S-VSON: 2.9mm² - 1.45 × 2.0 mm)	Smaller size
Input Power Consumption	× (coil) 100mW～	◎ (LED) (ex: 0.5mW～)	Less power consumption
Contact Form	1c、2c	1a、1b、2a、1a1b	
Leakage Current	◎(not exist)	〇(20pA～)	

(a) LED: on (Contact: on)　　(b) LED: off (Contact: off)

Fig. 2 R_{ON} and C_{OFF} of the photorelay output part



(a) LED: on (Contact: on)　　(b) LED: off (Contact: off)

Fig. 3 Inductance (L) components also appear in a high frequency

2. Photorelay behavior for high frequency signals

As described above, the photorelay has an on-resistor (R_{ON}) and a pin-to-pin capacitance (C_{OFF}). This is a major difference from mechanical relays.

When the specified current and voltage are applied to the photorelay input, the photorelay turns on. At this time, the photorelay output (MOSFETs) behaves as a resistance component when the applied current frequency ranges from DC to low frequency. However, as the frequency increases, an inductance component appears in addition to the resistance component. On the other hand, if no biasing is applied to the photorelay input, the output MOSFETs are turned off. At this time, MOSFETs are equivalent to the capacitance component when the applied signal frequency ranges from DC to low frequency, but an LC resonance occurs because the inductance component appears in addition to the capacitance component as the frequency increases. Note this when controlling high frequency signals whth a photorelay. In other words, the signal after passing through the photorelay is distorted with respect to the expected output signal. A common parameter for expressing this distortion is the S-parameters (Scattering parameters).

3. Points when using photorelays in high-frequency circuits

A problem when operating photorelay is the transmission characteristics when the output is turned on.

When the frequency increases, the output waveform rise time (t_{rout}) after passing through the photorelay changes from the input waveform rise time (t_{rin}) due to effects of inductance components of the photorelay. This change is expressed as the Equivalent Rise Time (ERT). The ERT is defined by the equation shown in Fig. 4, where the smaller the value, the less signal changes and the better characteristic. The pass-through characteristic can also be expressed using the S-parameters.

$$ERT = \sqrt{{t_{rout}}^2 - {t_{rin}}^2}$$

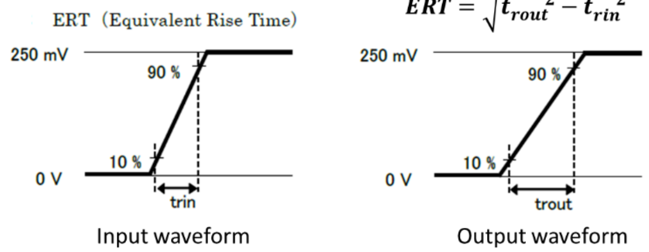


Fig. 4 Pass-through characteristics

A leakage current is also a problem when the output (contact) of the photorelay is turned off. When a steep rising voltage is applied to the contact when the photorelay is turned off, a leakage current is generated (Fig. 5). Approximately, $I_L = C_{OFF} \times dV/dt_r$ flows. An impedenace, the total opposition to alternating current by an electrical circuit, which corresponds to the resistance in a DC circuit. This impedance at C_{OFF} decreases as the frequency increases, then the leakage current increases. In such cases, it is recommended to use a photorelay with smaller C_{OFF}.

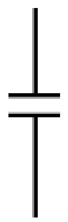
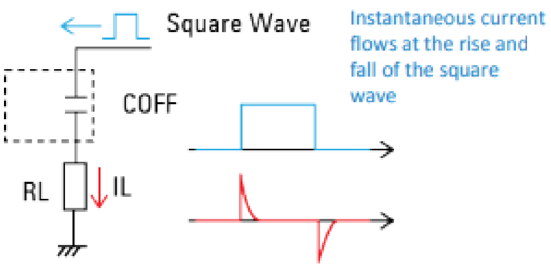
Mode	Equivalent Circuit	Operation Example
LED : OFF	Capacitor 	

Fig. 5 Leakage current when the contact is turned off

4. Lumped- and distributed-element circuits (general explanation)

A lumped-element circuit is a circuit consisting of electronic components (resistance: R, capacitance: C, inductance: L, conductance: G), and wiring impedances between components is negligibly small compared to the signal wavelength λ to be transmitted (Fig. 6). Photorelays can generally control DC or AC loads. In case of DC load controls, a lumped-element circuit can be adopted.

A distributed-element circuit is a circuit in which several lumped-element circuits are connected and distributed continuously throughout the circuit (Fig. 7). When controling an AC load, a distributed-element circuit can be adopted though it depends on the control signal frequency. In this case, the transmission line is thought as a circuit having a characteristic impedance Z_0.

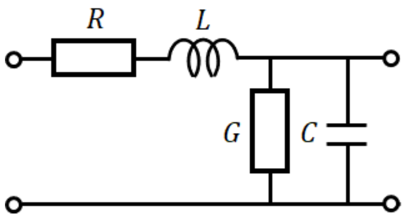


Fig. 6 A lumped-element circuit

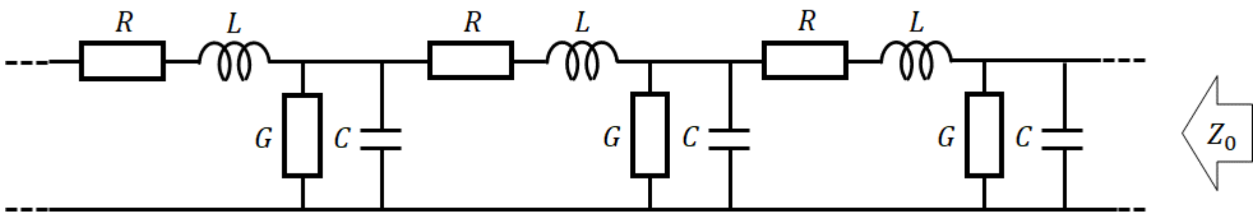


Fig. 7 Transmission lines expressed by distributed-element circuit

4.1 When a photorelay is inserted into a transmission line represented by a distributed-element circuit

Fig. 8 shows a simplified equivalent circuit in which a photorelay is inserted into a transmission line represented by a distributed-element circuit.

When the photorelay is on, MOSFET on-resistance, as well as the inductance component caused by bonding wires and the lead frame in the photorelay, and the capacitance component between the ground and the package are expressed. On the other hand, when the photorelay is off, MOSFET off-state capacitance component, as well as the inductance component caused by bonding wires and the lead frame in the photorelay, and the capacitance component between the ground and the package are expressed.

1. Signal loss when a photorelay is on = Insertion loss
2. Signal loss when a photorelay is off = Isolation

Thus, photorelays with a smaller R_{ON} and/or a smaller C_{OFF} is required for high frequency signal control.

Toshiba photorelay examples) Low R_{ON} type: TLP3475 / TLP3475S

Low C_{OFF} type: TLP3440 / TLP3440S

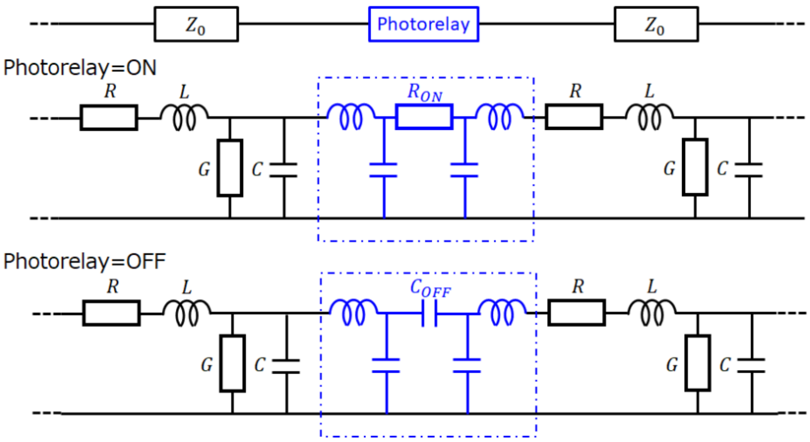


Fig. 8 Simplified equivalent circuit when a photorelay is inserted

4.2 Photorelay application examples for high-frequency signal control

As an example of the behavior of photorelays on a distributed-element circuit, here shows an application of a photorelay in semiconductor testers (Fig. 9). In semiconductor testers, there is a circuit block called pin electronics (PE) for measuring DUT. This block consists of two parts: (1) the FC test section, which inputs a desired signal (usually a pulse signal) to the DUT and checks whether is behaves as desired, and (2) the DC test section, which checks DC characteristics. In FC and DC tests, photorelays are often used to control signal lines, and it is necessary to pay attention to the behavior when those are in on or off state.

During the FC test, the signal from the pulse driver is transmitted to the DUT. Before sending the signal, the photorelay between the DUT and the pulse driver is turned on, and the two photorelays on the DC test section should be in the off state. As described in Chapter 2, the MOSFET in the photorelay output is equivalent to capacitance components when they are off. Thus, if C_{OFF} of the photorelay for the DC test is large, some of the pulse signals that should be input to the DUT will be split to the DC unit section through those photorelays (as leakage current). This leakage induces lower FC test accuracy.

During the DC test, the two photorelays connected to the DC unit are turned on, while the photorelay on the FC test section is also turnes off. Those FC test photorelay has C_{OFF}, but this is not affect during the DC test.

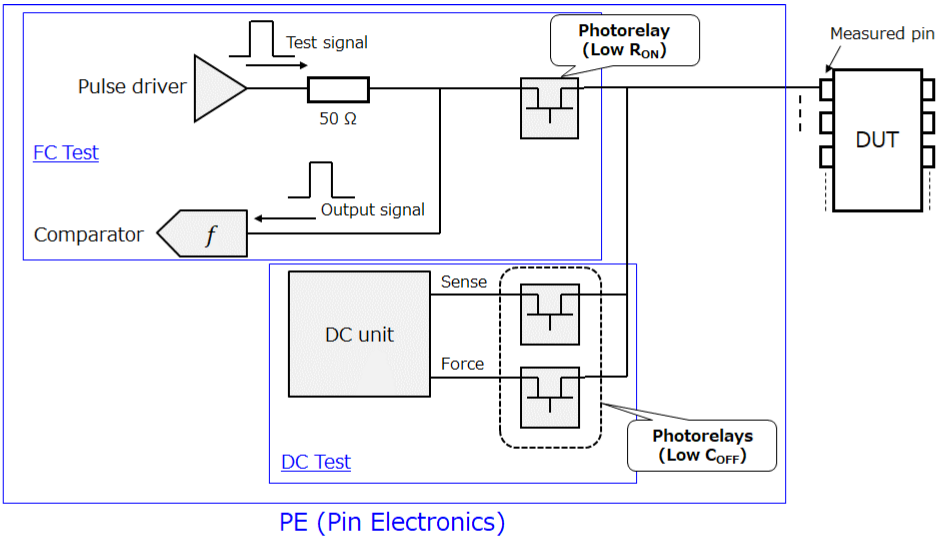


Fig. 9 An application example of photorelays in semiconductor testers

Toshiba can provide S-parameter of photorelays to see the behavior of the components on such distributed-element circuits. For more information, refer to "Points for photorelays in high frequency circuit applications (released in October, 2020)".

5. Microstrip line (general explanation)

A microstrip line is electromagnetic waves transmission line using a pattern on the surface layer (conductive film) and ground plane as a pair to convey microwave-frequency signals (Fig. 10).

The microwave-frequency signals propagate through a medium such as a pattern on a PCB or a coaxial cable from the signal source to the load. The signal propagates as an electromagnetic wave in the media, and its speed is urually slower than the speed of light in vacuum. The characeristic impedance Z_0 of a microstrip line is determined by the substrate (insulation layer) thickness H, the relative dielectric constance ε_r, and the conductive layer width W and thickness T of the transmission line.

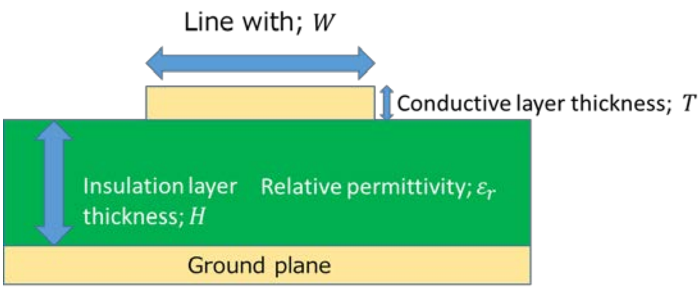
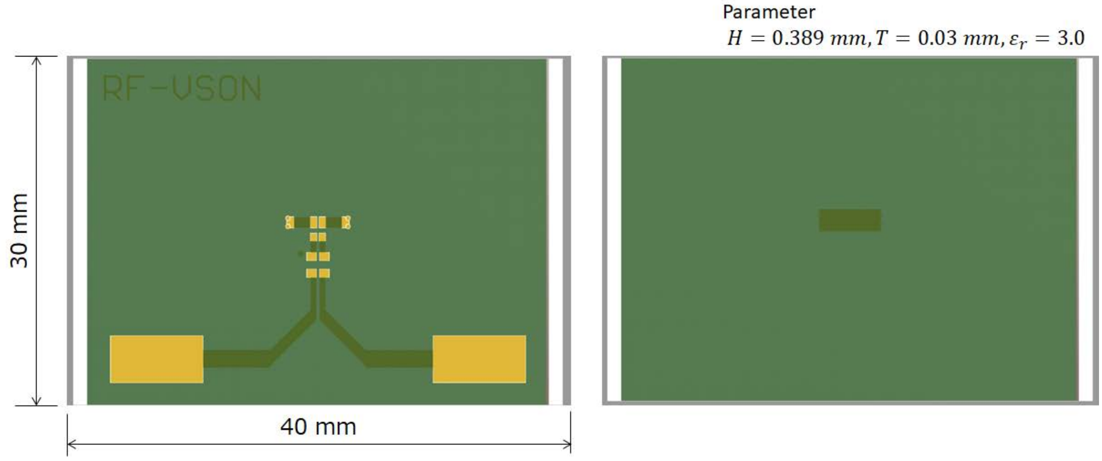


Fig. 10 Microstripline (transmission lines configured on a PCB)

5.1 Microstrip line for photorelay evaluation

Fig. 11 shows an example of microstrip line used for high-frequency characterization of our photorelays.

Toshiba is developing photorelays and expanding and product lineups suitable for GHz-band signal control applications (e.g. semiconductor testers), and we are using this substrate for thse product evaluations. In the following sections realization of substrates with better high-frequency performances are discussed.



(a)Top view (b) Bottom view

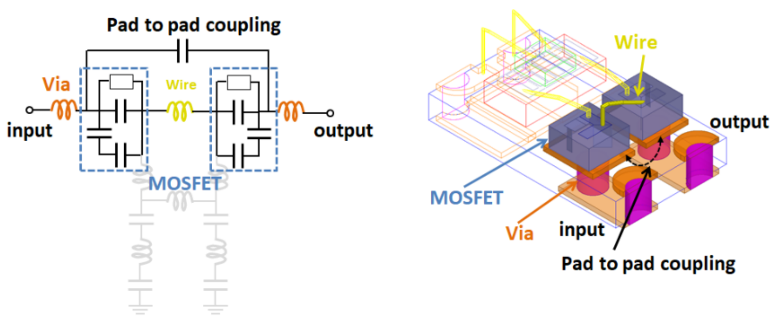
Fig. 11 Microstrip line (example)

6. PCB design for photorelays

This section describes points to be noted when mounting a photorelay on a PCB.

Here, mounting a VSON package (Very-thin Small Outline Non-leaded package) with COC (Chip-On-Chip) structure shown in Fig. 12 is studied as an example. As shown is this figure, resistances, capacitances and inductances are formed into the photorelay. If the package and its internal structure are different, these parameters will be different.

In the previous section, a microstrip line for photorelay evaluation are shown. However, high frequency performances (e.g. S-parameters) may differ depending on the PCB insulation layer thickness, transmission line width, photorelay mount position, and other factors. Is also said for practical PCB where photorelays are used. This chapter explains some examples of changes in insertion loss (S21) on microstrip lines due to differences in PCB designs and mounting conditions.



A resonant circuit is formed by inductors connected in series between input and output, and capacitors caused by pad-pad coupling.

Fig. 12 A VSON package photorelay internal construction (example)

6.1 PCB design

Based on the PCB shown in Fig. 11, we study a high-frequency performance improvement. First, the S-parameter measurement path is defigned as shown in Fig. 13. Here, through characteristics (no photorelay mounted) under several wiring width (W) and insulation layer thickness (H) condition of the PCB are performed. Fig. 14 shows simulation results.

<<Simulation results>>
(1) Insertion loss varies by signal frequency band.
(2) Narrower wiring width and thinner insulation layer thickness have better insertion loss characteristics.

Though above simulation results may differ depends on the PCB design, it can be seen that when handling above 10 GHz, it is necessary to carefully design the wiring width and insulation layer thickness of the PCB.

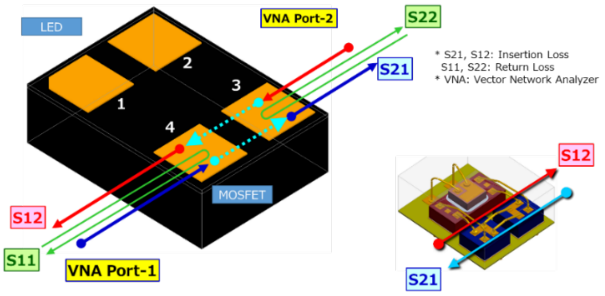


Fig. 13 S-parameter measurement and signal paths

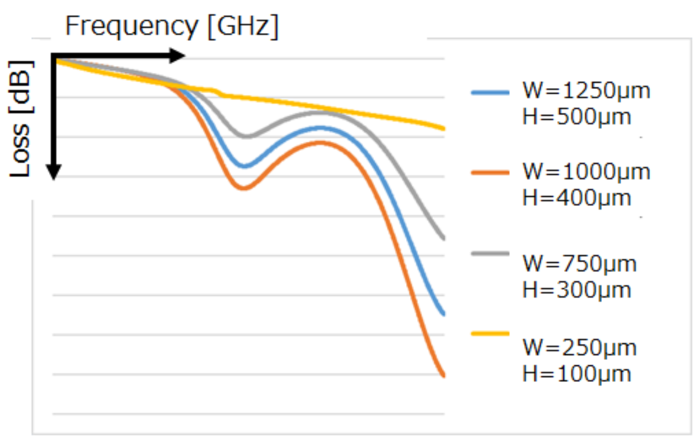
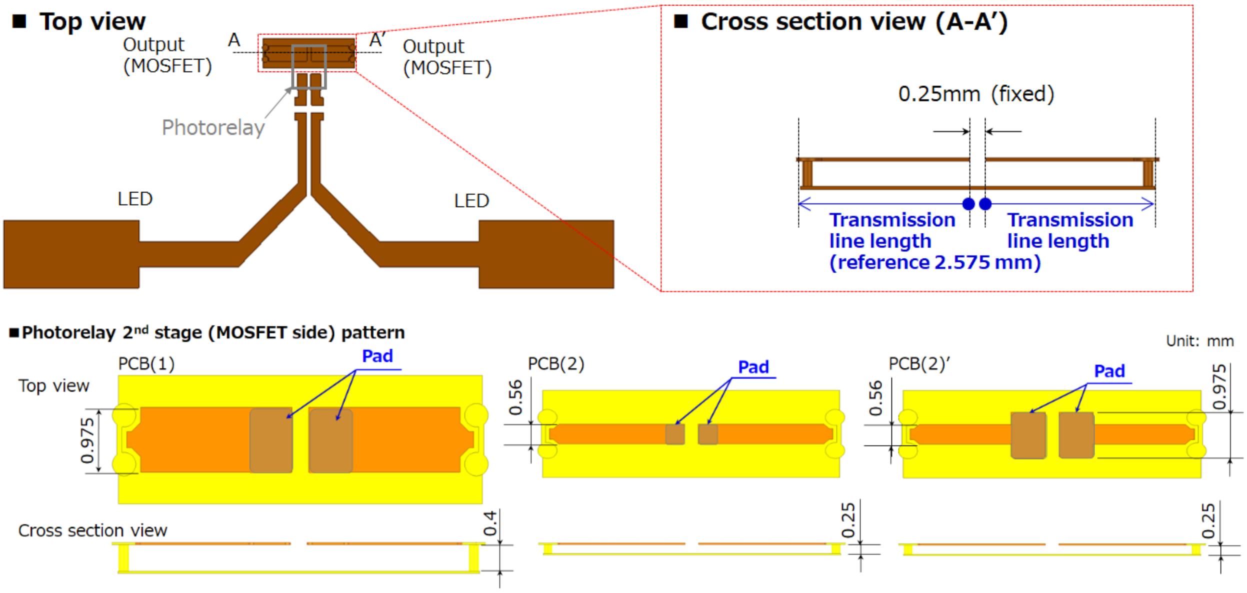


Fig. 14 Simulation results of insertion loss for different line width (W) and PCB thickness (H)

6.2 Improvement of high-frequency characteristics of substrates

Based on the simulation results in the previous section, three types of boards shown in Fig. 15 are considered. Then, the through characteristics of these PCBs and the insertion loss (S21) when a photorelay is mounted on those PCBs. Here, the transmission line length of the secondary side of photorelay (MOSFET side) is set to 2.575 mm as a reference.



PCB (1): Line width = 975 µm, insulation layer thickness = 400 µm

PCB (2): Line width = 560 µm, insulation layer thickness = 250 µm

PCB (2)': Line width = 560 µm, insulation layer thickness = 250 µm (pad width = 975 µm)

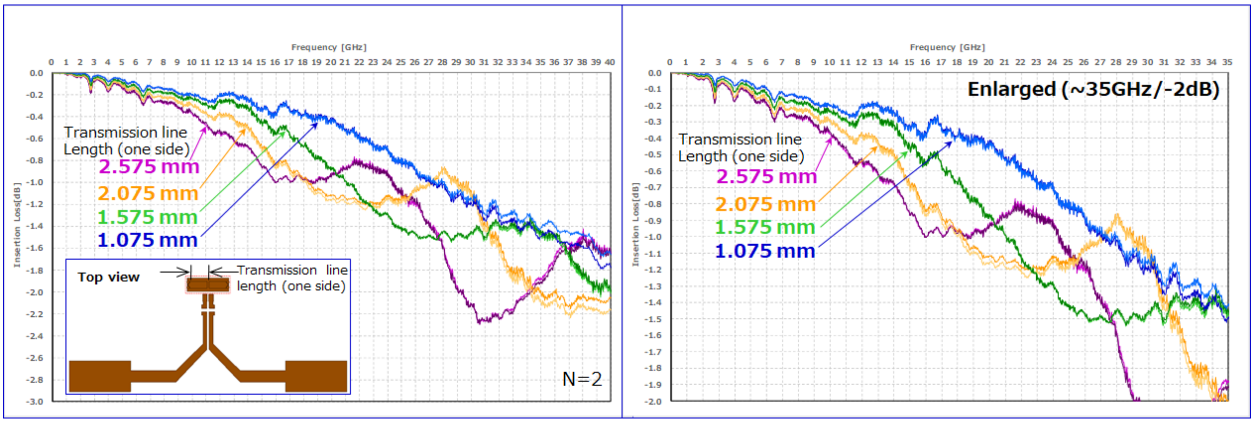
Fig. 15 Designing three types of substrates

In addition, for the three types of PCBs shown in Fig. 15, PCBs with shorter line length compared to the reference values are made. The position of center gap is 0.25 mm (distance between photorelay MOSFET drain pads) which is fixed, and below different transmission line length are made;

A) 2.575 mm (reference)
B) 2.075 mm (0.5 mm shortened)
C) 1.575 mm (1.0 mm shortened)
D) 1.075 mm (1.5 mm shortened)

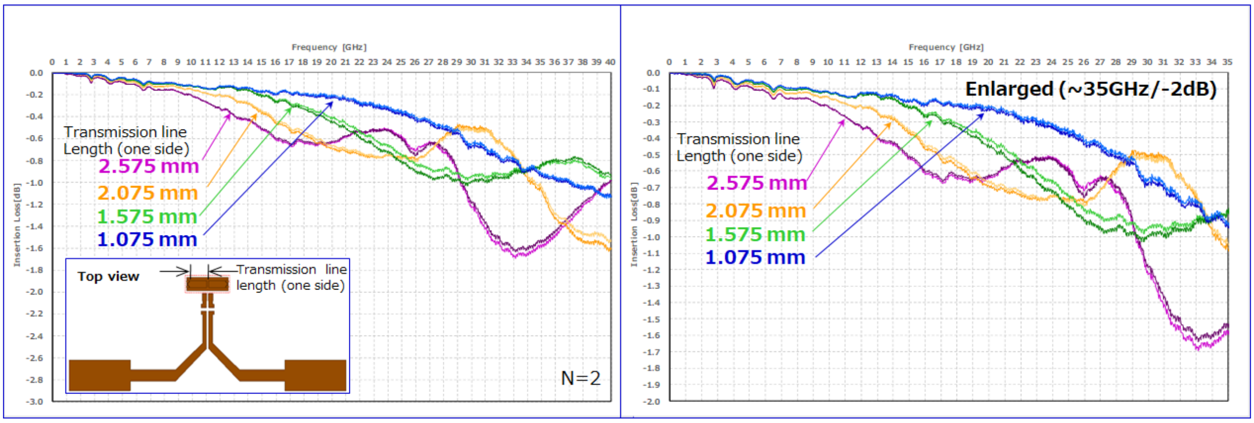
Fig. 16 to Fig. 18 shows the measurement result of the insertion loss (S21 ; no photorelay mounted). This result indicates that shorter transmission line lengths result in less insertion loss and suppression of ripple.

Fig. 18 shows the difference in pad size. When the pad size is increased in relation to the transmission line length, the loss becomes larger below 27 GHz, while the loss becomes smaller above it. This is because when the pad is large, the part that overhangs from the transmission line width become as stubs.



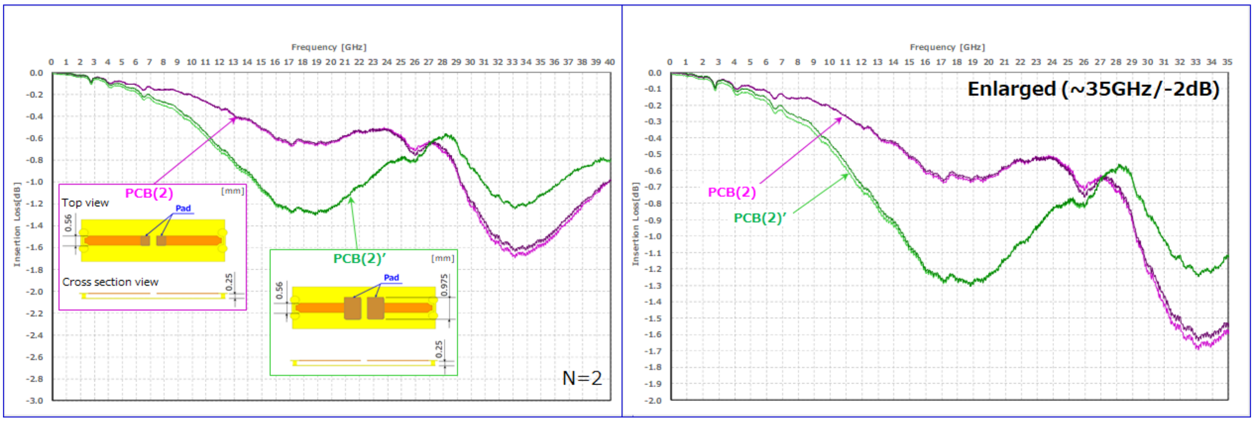
PCB(1) Wiring width =975 μm, insulation layer thickness =400 μm

Fig. 16 Insertion loss characteristics of the PCB with different transmission line length (through characteristics; no photorelay mounted)



PCB(2) Wiring width =560 μm, insulation layer thickness =250 μm

Fig. 17 Insertion loss characteristics of the PCB with different transmission line length (through characteristics; no photorelay mounted)



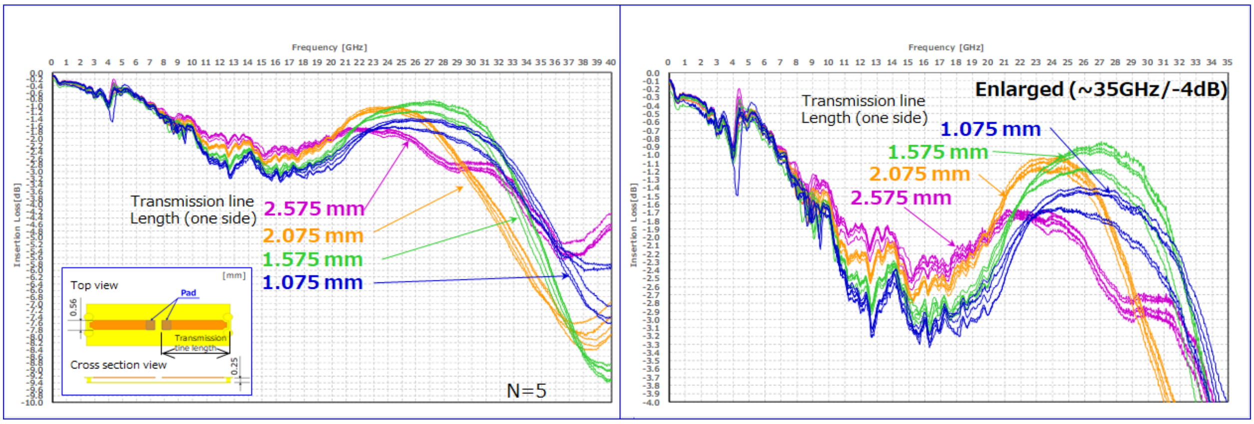
PCB(2) Wiring width =560 μm, insulation layer thickness =250 μm

PCB(2)' Wiring width = 560 μm, insulation layer thickness = 250 μm (pad width = 975 μm)

Fig. 18 Insertion loss characteristics of the PCB with different pad sizes (through characteristics; no photorelay mounted)

Next, as an example of the insertion loss when a photorelay is placed, results under the condition of PCB(2) are shown (Fig. 19). When the pad size is increased in relation to the transmisssion line length, the loss becomes largers below 27 GHz and smaller above 27 GHz resion.

When the transmission line length was shortened, the loss increased at below 20 GHz region and fluctuated sharply at 20 GHz or above. This is because an interference between measurement probes and the photorelay. On the other hand, since there is no interference in case of the through characteristic (no device is placed), the result is as simulated. In particular, it is believed that bonding wires between the PDA (photodiode array, which generates MOSFET gate drive voltage) and MOSFETs inside the photorelay is affected to the insertion loss performance.



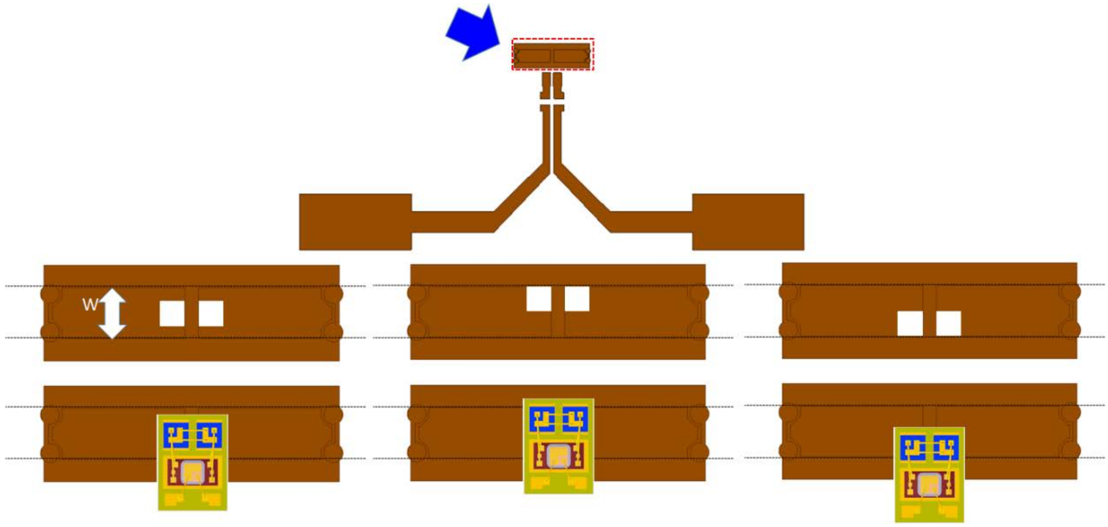
PCB(2) Wiring width = 560 μm, insulation layer thickness = 250 μm

Fig. 19 Insertion loss characteristics when a photorelay exists

6.3 Insertion characteristic differences by photorelay mounting position

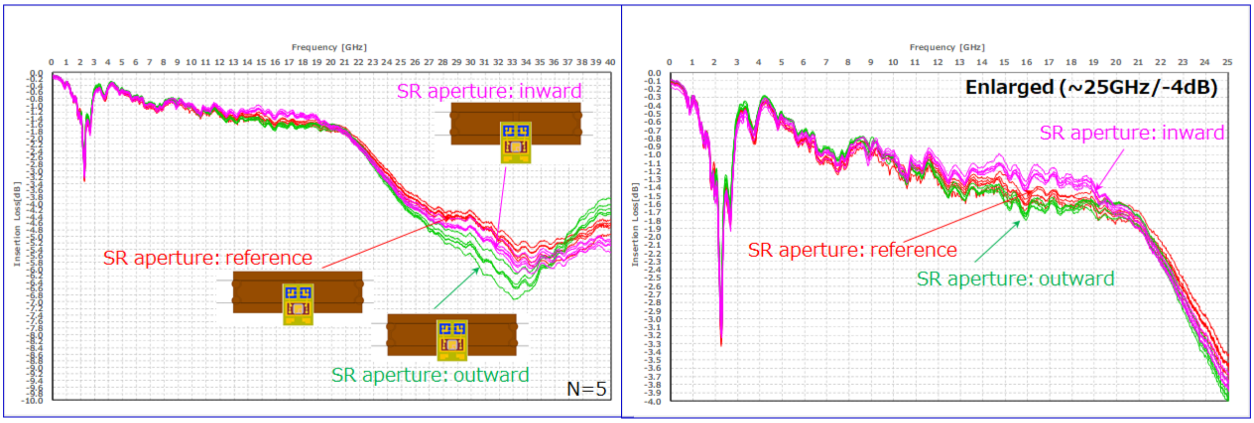
Next, insertion loss characterization according to photorelay mounting position difference is performed (SR aperture; soluder resist aperture, is placed in the center, offset outward and inward as shown in Fig. 20). Fig. 21 shows an example of the results., the insertion characteristic at 16 GHz region is better when the SR is placed offset inward, and at 20 to 36 GHz region is bettern when the SR is center. The characterisic at >36 GHz region is better when the SR is placed offset outward, although it is generally disadvantageous. It is presumed that this is due to the amount of overlap between the PDA part in the photorelay and the transmission line, as there is parasitic capacitance between the PDA part, which consists of the PDA die itself and the lead frame on which it is mounted, and the transmission line. By reducing the amount of overlap, insertion loss at 36 GHz can be reduced.

In the section 6.2, through characteristics vary depending on PCB design parameters (PCB thickness, transmission line length, etc.), and this section shows the insertion loss characteristics when a photorelay is mounted. Thus, those loss characteristics change depending on whether a photorelay is mounted or not.



(a) Center (b) Offset outward (c) Offset inward

Fig. 20 SR aperture conditions



PCB(2) Wiring width = 560 μm, insulation layer thickness = 250 μm

Fig. 21 Insertion loss characteristic differences by photorelay mounting position

7. Influence of the LED side transmission lines

In the previons evaluation result of insertion loss when a photorelay is mounted (Fig. 21), you may have noticed that the loss is larger at 2 to 3 GHz. This is due to the fact that the structure of photorelay is affected by the LED side wiring since the LED is mounted on the primary side. In other words, the wiring on the LED side (L: wiring length) functions as a stub (open or short stub), which causes the effect (frequency range that the loss occurs and magnitude of the loss may vary depending on the product). To suppress this, insert an inductor such as a ferrite bead into the wiring on the LED side (Fig. 22).

This characteristic depends on the open stub = wire length ($=\lambda/4$). The effect of the PCB insulation layer thickness and the wiring width on the PCB is considered to be extremely low.

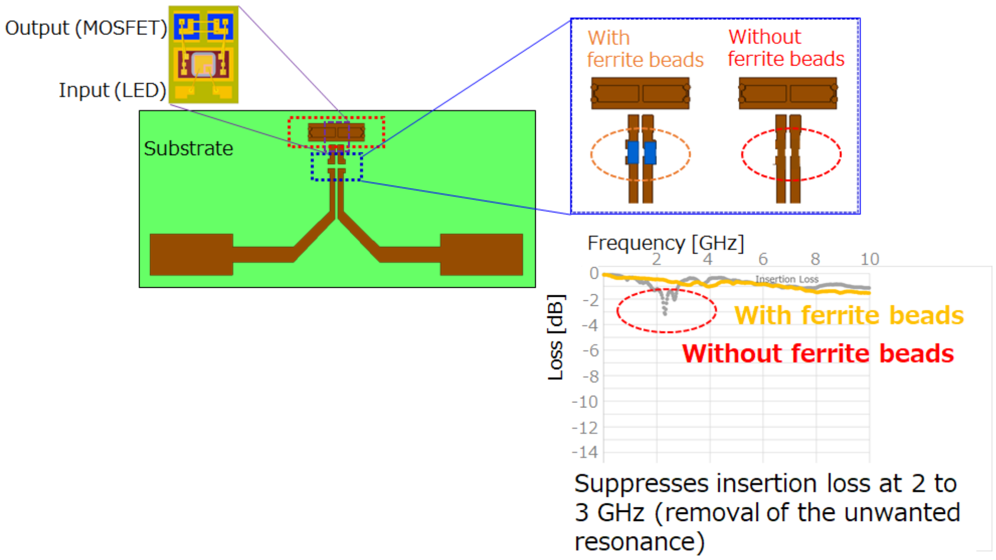
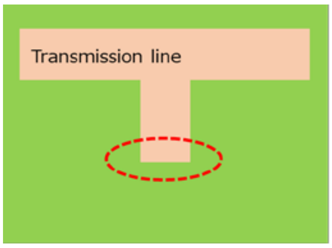


Fig. 22 Improves wiring effect on the LED side by inserting an inductor (ferrite beads)

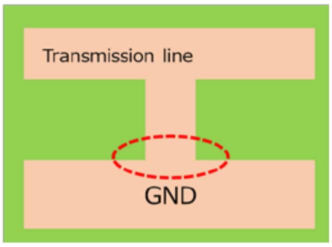
(Reference) Open stub and short stub

A distributed-element circuit connected by branching to a transmission line of a high-frequency circuit is called a stub. Since stubs behave like an element in high-frequency circuits, they are actively used as impedance matching and filters. A stub which has open-ended is called an open stub, and a stub which connects to GND is called a short stub.

On the other hand, unexpected stub formation may cause problems. For example, a signal coming from the left (signal source) in Fig. 23 is divided into a stub. At this time, the signal that enters the stub is reflected at the end and returns to the division point. At the division point, a signal from the source and the signal reflected by the stub are combined and transmitted to the transmission line after the stub. Therefore, depending on the conditions of the stub, the synthesized wave collapses from the intended signal wave and the expected signal transmission cannot be performed. For example, an open stub at 1/4 wavelength will eliminate the field of energy at the open end, and will behave like a voltage reflecting off at the same polarity as the line voltage. Then, at the branch point (1/4 wavelength from the open end point), the voltage is zero (Fig. 24). As a result, an open stub with 1/4 wavelengh works as short-circuit at this wavelength (or frequency).



(a) Open stub



(b) Short stub

Fig. 23 Open stub and short stub

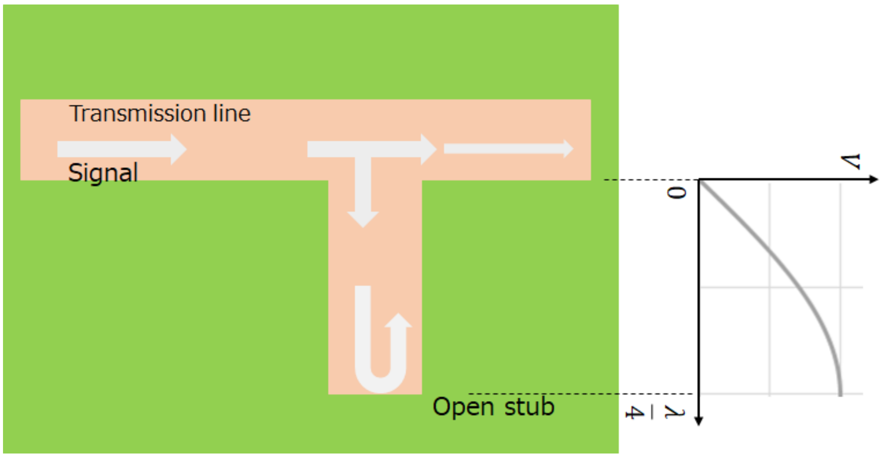
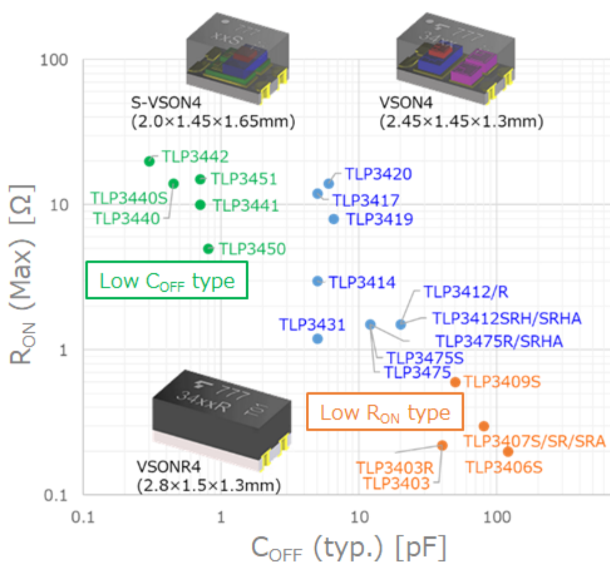


Fig. 24 Signal flow when a stub is connected and voltage standing wave in case of a 1/4 λ-length open stub

8. Product Information

We offer a wide lineup of small package photorelays (VSON package series) suitable for use in semiconductor testers. Table 2 shows the products.

Table 2 VSON package photorelays



P/N	Package (Toshiba)	IFT max. (mA)	VFON max. (V)	VOFF max. (V)	COFF typ. (pF)	RON max. (Ω)	ION max. (A)	ton max. (ms)	toff max. (ms)
TLP3403	VSON4	3		20	40.00	0.22	1.00	2.0	1.0
TLP3403R	VSONR4		3	20	40.00	0.22	1.00	2.0	1.0
TLP3406S	S-VSON4	3		30	120.00	0.20	1.50	2.0	1.0
TLP3406SRH	S-VSON4T		3	30	120.00	0.20	1.50	2.0	1.0
TLP3406SRL	S-VSON4T		1.6	30	120.00	0.20	1.50	2.0	1.0
TLP3407S	S-VSON4	3		60	80.00	0.30	1.00	2.0	1.0
TLP3407SR	S-VSON4T		3	60	80.00	0.30	1.00	20	1.0
TLP3407SRA	S-VSON4T		3	60	80.00	0.30	1.00	20	1.0
TLP3407SRH	S-VSON4T		3	60	80.00	0.30	1.00	2.0	1.0
TLP3407SRL	S-VSON4T		1.6	60	80.00	0.30	1.00	2.0	1.0
TLP3409S	S-VSON4	3		100	50.00	0.60	0.65	2.0	1.0
TLP3412	VSON4	3		60	20.00	1.50	0.40	0.5	0.5
TLP3412R	VSONR4		3	60	20.00	1.50	0.40	0.5	0.5
TLP3412SRH	S-VSON4T		3	60	20.00	1.50	0.40	0.5	0.2
TLP3412SRHA	S-VSON4T		3	60	20.00	1.50	0.40	0.5	0.2
TLP3414	VSON4	3		40	5.00	3.00	0.25	0.5	0.5
TLP3417	VSON4	3		80	5.00	12.00	0.12	0.5	0.2
TLP3419	VSON4	3		80	6.50	8.00	0.20	0.4	0.4
TLP3420	VSON4	3		100	6.00	14.00	0.10	0.3	0.3
TLP3431	VSON4	3		20	5.00	1.20	0.45	0.5	0.5
TLP3440	VSON4	3		40	0.45	14.00	0.12	0.2	0.3
TLP3440S	S-VSON4T	3		40	0.45	14.00	0.12	0.2	0.3
TLP3441	VSON4	3		40	0.70	10.00	0.14	0.2	0.2
TLP3442	VSON4	3		40	0.30	20.00	0.10	0.2	0.2
TLP3450	VSON4	3		20	0.80	5.00	0.20	0.2	0.2
TLP3451	VSON4	3		60	0.70	15.00	0.12	0.2	0.2
TLP3475	VSON4	3		50	12.00	1.50	0.30	0.5	0.4
TLP3475R	VSONR4		3	50	12.00	1.50	0.30	0.5	0.4
TLP3475S	S-VSON4	3		60	12.00	1.50	0.40	0.5	0.25
TLP3475SRHA	S-VSON4T		3	60	12.00	1.50	0.40	0.5	0.2

9. Conclusion

In this document, insertion loss - frequency characteristics for a photorelay mounted on a PCB varies depending on the transmission line width, PCB thickness, photorelay mount position, and transmission line length on the PCB. Please note those performances when selecting photorelay and designing PCB.

We will continue to develop products for improving the performance and miniaturization of photorelays, and expand our lineup of products that can control signals in a higher frequency ranges and can be mounted in a smaller space. Please consider using photorelays for semiconductor testers and various measuring instruments.

When designing a new product, please check the latest product information on our website.

Revision history

Revision	Date	Page	Description
Rev. 1.0	2021-11-30	-	1st edition

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