

HIGH SPEED QUAD CHANNEL DIGITAL ISOLATORS

DCL540x01,DCL541x01

DCL540C01/DCL540D01/DCL540L01/DCL540H01/DCL541A01/DCL541B01

1. Applications

- Industrial automation systems
- Motor control
- Inverter
- Switching power supply

2. Description

DCL540C01/DCL540D01/DCL540L01/DCL540H01/DCL541A01/DCL541B01 are high-speed quad-channel digital isolators. Outstanding performance characteristics are achieved by Toshiba CMOS technology and the magnetic coupling structure. In addition, they comply with UL 1577 and has a 5000Vrms rating as an isolation voltage. These products can operate with a temperature range of -40 to 110 °C and a wide supply voltage of 2.25 to 5.5 V.

3. Features

Data rate	: Up to 150 Mbps
Supply voltage	: 2.25 V to 5.5 V
Temperature Range	: -40 °C to 110 °C
Propagation Delay	: 10.9 ns Typical (5.0 V operation)
Default Output	: High and Low Options
CMTI (min)	: 100 kV/μs
Withstand Voltage	: 5 kVrms
Package	: 16pin SOIC Wide body

Safety-Related Certification :

UL : UL1577, File No. E519997

cUL : CSA Component Acceptance Service Notice No. 5A, File No. E519997

VDE : DIN EN IEC 60747-17 (VDE V 0884-17) Certificate No.40055132

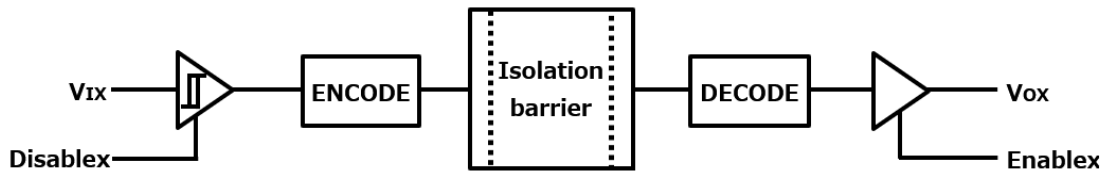
CQC : GB 4943.1-2022 Certificate No. CQC22001345018

Start of commercial production
2023-05

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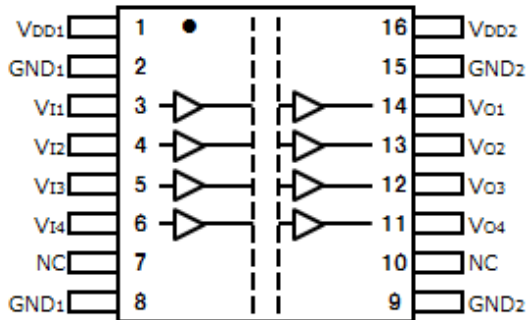
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4. Internal Circuit (Simplified Schematic)

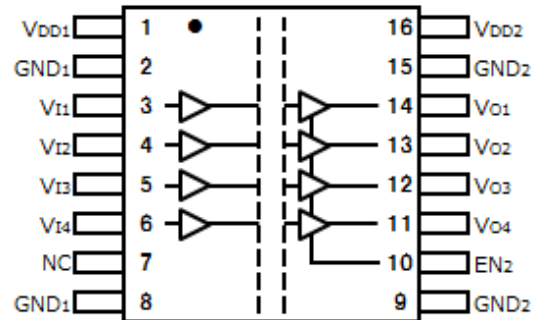


5. Pin configuration and Functions

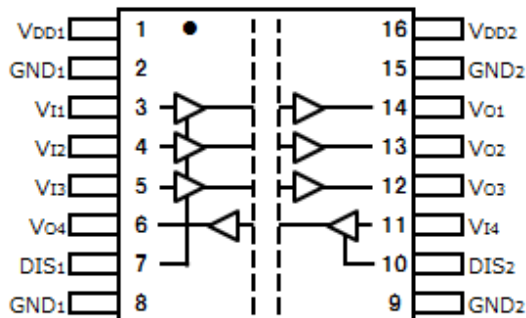
DCL540C01 / DCL540D01



DCL540L01 / DCL540H01



DCL541A01 / DCL541B01



5.1. Pin Functions

NAME	PIN			I/O	DESCRIPTION
	DCL540 C01 / D01	DCL540 L01 / H01	DCL541 A01 / B01		
VDD ₁	1	1	1	-	Power Supply, side 1
GND ₁	2	2	2	-	GND connection for VDD ₁ , side 1
V _{I1}	3	3	3	I	Input, Channel1
V _{I2}	4	4	4	I	Input, Channel2
V _{I3}	5	5	5	I	Input, Channel3
V _{I4}	6	6	11	I	Input, Channel4
NC	7	7	-	-	Non connected
DIS ₁	-	-	7	I	Input disable 1. Input pins on side 1 are disabled when DIS ₁ is high, and in enabled state when DIS ₁ is low or open.
GND ₁	8	8	8	-	GND connection for VDD ₁ , side 1
GND ₂	9	9	9	-	GND connection for VDD ₂ , side 2
DIS ₂	-	-	10	I	Input disable 2. Input pins on side 2 are disabled when DIS ₂ is high, and in enabled state when DIS ₂ is low or open.
EN ₂	-	10	-	I	Input enable 2. Input pins on side 2 are enabled when EN ₂ is high or open, and in high impedance state when EN ₂ is low.
NC	10	-	-	-	Non connected
V _{O4}	11	11	6	O	Output, Channel4
V _{O3}	12	12	12	O	Output, Channel3
V _{O2}	13	13	13	O	Output, Channel2
V _{O1}	14	14	14	O	Output, Channel1
GND ₂	15	15	15	-	GND connection for VDD ₂ , side 2
VDD ₂	16	16	16	-	Power Supply, side 2

6. Functional Description

(1) DCL540C01/ DCL540D01

VDD ₁	VDD ₂	INPUT (V _{ix})	OUTPUT (V _{ox})	COMMENTS
PU	PU	L	L	Normal Operation
		H	H	
PD		OPEN	Default	Default mode DCL540C01=L , DCL540D01=H
	L or OPEN			
PU	PD	X	Undetermined	When VDD ₂ is unpowered, a channel output is undetermined.
PD		L or OPEN		
PD	X	H	-	Don't use, since a certain voltage will be output through the internal ESD circuit.

PU= Powered up (VDD≥2.25 V), PD= Powered down (VDD≤1.7 V), H= High level, L= Low level, X= Don't care

(2) DCL540L01/ DCL540H01

VDD ₁	VDD ₂	OUTPUT ENABLE (EN ₂)	INPUT (V _{ix})	OUTPUT (V _{ox})	COMMENTS
PU	PU	H or OPEN	L	L	Normal Operation
			H	H	
			OPEN	Default	Default mode DCL540L01=L , DCL540H01=H
		L	X	Z	Output Disable mode
PD	PU	H or OPEN	L or OPEN	Default	Default mode DCL540L01=L , DCL540H01=H
		L		Z	Output Disable mode
	X	X	H	-	Don't use, since a certain voltage will be output through the internal ESD circuit.
PU	PD	L or OPEN	X	Undetermined	When VDD ₂ is unpowered, a channel output is undetermined.
PD			L or OPEN		
X			H	X	-

PU= Powered up (VDD≥2.25 V), PD= Powered down (VDD≤1.7 V), H= High level, L= Low level, X= Don't care

(3) DCL541A01/ DCL541B01

V _{DD1}	V _{DD2}	INPUT DISABLE (DIS _x)	INPUT (V _{ix})	OUTPUT (V _{ox})	COMMENTS
PU	PU	L or OPEN	L	L	Normal Operation
			H	H	
		OPEN	Default	Default mode DCL541A01=L, DCL541B01=H	
	H	Input Disable mode DCL541A01=L, DCL541B01=H			
	PD	X	X	Undetermined	When V _{DD2} is unpowered, a channel output is undetermined.
PD	X	H	X	Don't use	Don't use, since a certain voltage will be output through the internal ESD circuit.
		X	H		
	PU	L or OPEN	L or OPEN	Default	Default mode DCL541A01=L, DCL541B01=H
	PD			Undetermined	When V _{DD2} is unpowered, a channel output is undetermined.

V_{DD1}: Input V_{DDx}, V_{DD0}: Output V_{DDx}, PU= Powered up (VDD≥2.25 V), PD=Powered down (VDD≤1.7 V),
H=High Level, L=Low Level, X= Don't care

7. Absolute Maximum Ratings (T_a = 25 °C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V _{DD1} , V _{DD2}	-0.5	6.0	V
Input Voltage	V _I	-0.5	V _{DDX} +0.5 ⁽¹⁾	V
Output Voltage	V _O	-0.5	V _{DDX} +0.5 ⁽¹⁾	V
Output Current	I _O	-15	15	mA
Storage Temperature	T _{stg}	-65	150	°C
Operating Temperature	T _{opr}	-40	110	°C
Soldering Temperature (10 s)	T _{sol}	-	260	°C
Maximum Withstanding Isolation Voltage (1 min.)	BV _S	-	5000	V _{rms}

Note(1): Maximum voltage must not exceed 6 V. X = 1 or 2.

8. Recommended Operating Conditions (Note)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V _{DD1} , V _{DD2}	2.25	5.5	V
Junction Temperature	T _J	-40	150	°C
Ambient Temperature	T _a	-40	110	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 1 (V_{DD1}) and pin 2 (GND₁) for VDD1 and between pin 16 (V_{DD2}) and pin 15 (GND₂) for VDD2, and should be the layout on the IC as close as possible (less than 10 mm).

Otherwise, the IC may not switch properly.

9. Electrical Characteristics

9.1. Electrical Characteristics – 5 V Supply

All typical specifications are at $T_a=25\text{ }^\circ\text{C}$, $V_{DD1}=V_{DD2}=5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $4.5\text{ V}\leq V_{DD1}\leq 5.5\text{ V}$, $4.5\text{ V}\leq V_{DD2}\leq 5.5\text{ V}$, and $-40\text{ }^\circ\text{C}\leq T_a\leq 110\text{ }^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12.1	V_{DDxUV+}	-	2.1	2.25	V
	Threshold when supply voltage is falling		V_{DDxUV-}	1.7	1.9	-	
	Supply voltage hysteresis		V_{DDxUVH}	0.1	0.2	-	
Output Voltage Logic High	$V_{ix}=H, I_{OH}=-20\text{ }\mu\text{A}$	12.2	V_{OH}	$V_{DDO}^{(1)}-0.1$	$V_{DDO}^{(1)}$	-	V
	$V_{ix}=H, I_{OH}=-4\text{ mA}$			$V_{DDO}^{(1)}-0.4$	$V_{DDO}^{(1)}-0.2$	-	
Output Voltage Logic Low	$V_{ix}=L, I_{OL}=20\text{ }\mu\text{A}$	12.2	V_{OL}	-	0.0	0.1	V
	$V_{ix}=L, I_{OL}=4\text{ mA}$			-	0.2	0.4	
Output impedance	-	12.2	Z_o	-	50	-	Ω
High-level input voltage	-	12.3	V_{IH}	$0.7*V_{DDI}^{(1)}$	-	-	V
Low-level input voltage	-	12.3	V_{IL}	-	-	$0.3*V_{DDI}^{(1)}$	V
Input Voltage Hysteresis	-	12.3	V_{HYS}	-	0.37	-	V
Input Current	$V_i=V_{DDI}^{(1)}$ or 0 V	-	I_i	-	-	± 10	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	150	Mbps
Pulse Width	-	-	PW	6.6	-	-	ns
Propagation Delay	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}, C_L=15\text{ pF}$	12.4	t_{PHL}, t_{PLH}	-	10.9	18.3	ns
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	12.4	PWD	-	0.8	2.8	ns
Propagation Delay Skew (Between any two units)	Note (2)	-	t_{PSK}	-	-	10	ns
Channel Matching	Same Direction	12.4	t_{skCD}	-	-	3.2	ns
	Opposing Direction	12.4	t_{skOD}	-	-	3.6	
Output Rise Time	10 % - 90 %	12.4	t_r	-	0.9	-	ns
Output Fall Time	90 % - 10 %	12.4	t_f	-	0.9	-	ns
Enable 3-state output enable time	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}, C_L=15\text{ pF}$	12.5	t_{pZL}, t_{pZH}	-	-	15.0	ns
Enable 3-state output disable time	Note (3)	12.5	t_{pLZ}, t_{pHZ}	-	-	18.0	ns
Disable output enable time	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}, C_L=15\text{ pF}$	12.6	t_{p_EN}	-	-	23.0	ns
Disable output disable time		12.6	t_{p_DIS}	-	-	23.0	ns
Common mode transient immunity	$V_i=V_{DDI}$ or 0 V, $V_{CM}=1500\text{ V}, T_a=25\text{ }^\circ\text{C}$	12.7	$ CMTI $	100	-	-	kV/ μs

Note (1) V_{DDI} =Input-side V_{DDx} , V_{DDO} =Output-side V_{DDx}

Note (2) Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.)

Note (3) When EN_2 signal is changed from Low to High or OPEN, the output signal(V_{Ox}) is valid after the output enable time. The output signal(V_{Ox}) within the output enable time is undefined.

9.2. Electrical Characteristics – 3.3 V Supply

All typical specifications are at $T_a=25\text{ }^\circ\text{C}$, $V_{DD1}=V_{DD2}=3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $3.0\text{ V}\leq V_{DD1}\leq 3.6\text{ V}$, $3.0\text{ V}\leq V_{DD2}\leq 3.6\text{ V}$, and $-40\text{ }^\circ\text{C}\leq T_a\leq 110\text{ }^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12.1	V_{DDxUV+}	-	2.1	2.25	V
	Threshold when supply voltage is falling		V_{DDxUV-}	1.7	1.9	-	
	Supply voltage hysteresis		V_{DDxUVH}	0.1	0.2	-	
Output Voltage Logic High	$V_{ix}=H$, $I_{OH}=-20\text{ }\mu\text{A}$	12.2	V_{OH}	$V_{DDO^{(1)}}-0.1$	$V_{DDO^{(1)}}$	-	V
	$V_{ix}=H$, $I_{OH}=-4\text{ mA}$			$V_{DDO^{(1)}}-0.4$	$V_{DDO^{(1)}}-0.2$	-	
Output Voltage Logic Low	$V_{ix}=L$, $I_{OL}=20\text{ }\mu\text{A}$	12.2	V_{OL}	-	0.0	0.1	V
	$V_{ix}=L$, $I_{OL}=4\text{ mA}$			-	0.2	0.4	
Output impedance	-	12.2	Z_O	-	50	-	Ω
High-level input voltage	-	12.3	V_{IH}	$0.7*V_{DDI^{(1)}}$	-	-	V
Low-level input voltage	-	12.3	V_{IL}	-	-	$0.3*V_{DDI^{(1)}}$	V
Input Voltage Hysteresis	-	12.3	V_{HYS}	-	0.32	-	V
Input Current	$V_I=V_{DDI^{(1)}}$ or 0 V	-	I_I	-	-	± 10	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	150	Mbps
Pulse Width	-	-	PW	6.6	-	-	ns
Propagation Delay	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}$, $C_L=15\text{ pF}$	12.4	t_{PHL} , t_{PLH}	-	11.6	19.1	ns
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	12.4	PWD	-	0.8	2.8	ns
Propagation Delay Skew (Between any two units)	Note (2)	-	t_{PSK}	-	-	10	ns
Channel Matching	Same Direction	12.4	t_{skCD}	-	-	3.3	ns
	Opposing Direction	12.4	t_{skOD}	-	-	3.7	
Output Rise Time	10 % - 90 %	12.4	t_r	-	0.8	-	ns
Output Fall Time	90 % - 10 %	12.4	t_f	-	0.8	-	ns
Enable 3-state output enable time	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}$, $C_L=15\text{ pF}$	12.5	t_{pZL} , t_{pZH}	-	-	15.0	ns
Enable 3-state output disable time	Note (3)	12.5	t_{pLZ} , t_{pHZ}	-	-	18.0	ns
Disable output enable time	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}$, $C_L=15\text{ pF}$	12.6	t_{p_EN}	-	-	23.0	ns
Disable output disable time		12.6	t_{p_DIS}	-	-	23.0	ns
Common mode transient immunity	$V_I=V_{DDI}$ or 0 V , $V_{CM}=1500\text{ V}$, $T_a=25\text{ }^\circ\text{C}$	12.7	$ CMTI $	100	-	-	kV/ μs

Note (1) V_{DDI} =Input-side V_{DDx} , V_{DDO} =Output-side V_{DDx}

Note (2) Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.).

Note (3) When EN_2 signal is changed from Low to High or OPEN, the output signal (V_{Ox}) is valid after the output enable time. The output signal (V_{Ox}) within the output enable time is undefined)

9.3. Electrical Characteristics – 2.5 V Supply

All typical specifications are at $T_a=25\text{ }^\circ\text{C}$, $V_{DD1}=V_{DD2}=2.5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $2.25\text{ V}\leq V_{DD1}\leq 2.75\text{ V}$, $2.25\text{ V}\leq V_{DD2}\leq 2.75\text{ V}$, and $-40\text{ }^\circ\text{C}\leq T_a\leq 110\text{ }^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12.1	V_{DDxUV+}	-	2.1	2.25	V
	Threshold when supply voltage is falling		V_{DDxUV-}	1.7	1.9	-	
	Supply voltage hysteresis		V_{DDxUVH}	0.1	0.2	-	
Output Voltage Logic High	$V_{ix}=H$, $I_{OH}=-20\text{ }\mu\text{A}$	12.2	V_{OH}	$V_{DDO^{(1)}}-0.1$	$V_{DDO^{(1)}}$	-	V
	$V_{ix}=H$, $I_{OH}=-4\text{ mA}$			$V_{DDO^{(1)}}-0.4$	$V_{DDO^{(1)}}-0.2$	-	
Output Voltage Logic Low	$V_{ix}=L$, $I_{OL}=20\text{ }\mu\text{A}$	12.2	V_{OL}	-	0.0	0.1	V
	$V_{ix}=L$, $I_{OL}=4\text{ mA}$			-	0.2	0.4	
Output impedance	-	12.2	Z_O	-	50	-	Ω
High-level input voltage	-	12.3	V_{IH}	$0.7*V_{DDI^{(1)}}$	-	-	V
Low-level input voltage	-	12.3	V_{IL}	-	-	$0.3*V_{DDI^{(1)}}$	V
Input Voltage Hysteresis	-	12.3	V_{HYS}	-	0.32	-	V
Input Current	$V_I=V_{DDI^{(1)}}$ or 0 V	-	I_I	-	-	± 10	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	150	Mbps
Pulse Width	-	-	PW	6.6	-	-	ns
Propagation Delay	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}$, $C_L=15\text{ pF}$	12.4	t_{PHL} , t_{PLH}	-	12.6	21.0	ns
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	12.4	PWD	-	1.0	3.0	ns
Propagation Delay Skew (Between any two units)	Note (2)	-	t_{PSK}	-	-	10	ns
Channel Matching	Same Direction	12.4	t_{skCD}	-	-	3.5	ns
	Opposing Direction	12.4	t_{skOD}	-	-	3.9	
Output Rise Time	10 % - 90 %	12.4	t_r	-	0.8	-	ns
Output Fall Time	90 % - 10 %	12.4	t_f	-	0.8	-	ns
Enable 3-state output enable time	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}$, $C_L=15\text{ pF}$ Note (3)	12.5	t_{pZL} , t_{pZH}	-	-	15.0	ns
Enable 3-state output disable time		12.5	t_{pLZ} , t_{pHZ}	-	-	18.0	ns
Disable output enable time	50 kHz, Duty=50 %, $t_r=t_f=2\text{ ns}$, $C_L=15\text{ pF}$	12.6	t_{p_EN}	-	-	23.0	ns
Disable output disable time		12.6	t_{p_DIS}	-	-	23.0	ns
Common mode transient immunity	$V_I=V_{DDI}$ or 0 V , $V_{CM}=1500\text{ V}$, $T_a=25\text{ }^\circ\text{C}$	12.7	$ CMTI $	100	-	-	kV/ μs

Note (1) V_{DDI} =Input-side V_{DDx} , V_{DDO} =Output-side V_{DDx}

Note (2) Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.).

Note (3) When EN_2 signal is changed from Low to High or OPEN, the output signal (V_{Ox}) is valid after the output enable time. The output signal (V_{Ox}) within the output enable time is undefined)

9.4. Supply Current Characteristics – 5 V Supply

All typical specifications are at $T_a=25\text{ }^\circ\text{C}$, $V_{DD1}=V_{DD2}=5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $4.5\text{ V}\leq V_{DD1}\leq 5.5\text{ V}$, $4.5\text{ V}\leq V_{DD2}\leq 5.5\text{ V}$, and $-40\text{ }^\circ\text{C}\leq T_a\leq 110\text{ }^\circ\text{C}$, unless otherwise noted.

(1) DCL540x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	$V_I=0$ (DCL540C01 , DCL540L01) , $V_I=1$ (DCL540D01 , DCL540H01)	$I_{DD1(Q)}$	-	2.1	3.0	mA
		$I_{DD2(Q)}$	-	5.0	7.3	mA
	$V_I=0$ (DCL540D01 , DCL540H01) , $V_I=1$ (DCL540C01 , DCL540L01)	$I_{DD1(Q)}$	-	19.6	28.1	mA
		$I_{DD2(Q)}$	-	5.3	7.6	mA
1 Mbps	$f_{CLK}=500\text{ kHz}$, duty=50 % cycle square wave. $C_L=15\text{ pF}$	$I_{DD1(1)}$	-	11.2	17.5	mA
		$I_{DD2(1)}$	-	5.4	8.3	mA
25 Mbps	$f_{CLK}=12.5\text{ MHz}$, duty=50 % cycle square wave. $C_L=15\text{ pF}$	$I_{DD1(25)}$	-	11.0	17.1	mA
		$I_{DD2(25)}$	-	9.8	14.7	mA
100 Mbps	$f_{CLK}=50\text{ MHz}$, duty=50 % cycle square wave. $C_L=15\text{ pF}$	$I_{DD1(100)}$	-	12.4	18.4	mA
		$I_{DD2(100)}$	-	25.2	37.1	mA

(2) DCL541x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	$V_I=0$ (DCL541A01) , $V_I=1$ (DCL541B01)	$I_{DD1(Q)}$	-	3.0	4.3	mA
		$I_{DD2(Q)}$	-	4.5	6.6	mA
	$V_I=0$ (DCL541B01) , $V_I=1$ (DCL541A01)	$I_{DD1(Q)}$	-	16.6	22.5	mA
		$I_{DD2(Q)}$	-	10.2	14.1	mA
1 Mbps	$f_{CLK}=500\text{ kHz}$, duty=50 % cycle square wave. $C_L=15\text{ pF}$	$I_{DD1(1)}$	-	10.0	15.5	mA
		$I_{DD2(1)}$	-	7.6	10.2	mA
25 Mbps	$f_{CLK}=12.5\text{ MHz}$, duty=50 % cycle square wave. $C_L=15\text{ pF}$	$I_{DD1(25)}$	-	12.1	18.2	mA
		$I_{DD2(25)}$	-	10.6	15.4	mA
100 Mbps	$f_{CLK}=50\text{ MHz}$, duty=50 % cycle square wave. $C_L=15\text{ pF}$	$I_{DD1(100)}$	-	17.4	24.5	mA
		$I_{DD2(100)}$	-	22.5	35.2	mA

9.5. Supply Current Characteristics – 3.3 V Supply

All typical specifications are at $T_a=25\text{ }^\circ\text{C}$, $V_{DD1}=V_{DD2}=3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $3.0\text{ V}\leq V_{DD1}\leq 3.6\text{ V}$, $3.0\text{ V}\leq V_{DD2}\leq 3.6\text{ V}$, and $-40\text{ }^\circ\text{C}\leq T_a\leq 110\text{ }^\circ\text{C}$, unless otherwise noted.

(1) DCL540x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL540C01 , DCL540L01) , VI=1(DCL540D01 , DCL540H01)	I _{DD1(Q)}	-	2.0	2.9	mA
		I _{DD2(Q)}	-	4.9	7.1	mA
	VI=0(DCL540D01 , DCL540H01) , VI=1(DCL540C01 , DCL540L01)	I _{DD1(Q)}	-	19.4	27.7	mA
		I _{DD2(Q)}	-	5.2	7.4	mA
1 Mbps	f _{CLK} =500 kHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(1)}	-	11.0	16.7	mA
		I _{DD2(1)}	-	5.2	7.8	mA
25 Mbps	f _{CLK} =12.5 MHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(25)}	-	10.6	16.0	mA
		I _{DD2(25)}	-	8.2	12.4	mA
100 Mbps	f _{CLK} =50 MHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(100)}	-	11.6	16.6	mA
		I _{DD2(100)}	-	16.5	29.3	mA

(2) DCL541x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL541A01) , VI=1(DCL541B01)	I _{DD1(Q)}	-	2.9	4.1	mA
		I _{DD2(Q)}	-	4.4	6.5	mA
	VI=0(DCL541B01) , VI=1(DCL541A01)	I _{DD1(Q)}	-	16.5	22.3	mA
		I _{DD2(Q)}	-	10.1	14.0	mA
1 Mbps	f _{CLK} =500 kHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(1)}	-	9.9	14.9	mA
		I _{DD2(1)}	-	7.5	9.5	mA
25 Mbps	f _{CLK} =12.5 MHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(25)}	-	10.8	16.6	mA
		I _{DD2(25)}	-	9.7	12.8	mA
100 Mbps	f _{CLK} =50 MHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(100)}	-	14.5	19.9	mA
		I _{DD2(100)}	-	16.6	26.0	mA

9.6. Supply Current Characteristics – 2.5 V Supply

All typical specifications are at $T_a=25\text{ }^\circ\text{C}$, $V_{DD1}=V_{DD2}=2.5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $2.25\text{ V}\leq V_{DD1}\leq 2.75\text{ V}$, $2.25\text{ V}\leq V_{DD2}\leq 2.75\text{ V}$, and $-40\text{ }^\circ\text{C}\leq T_a\leq 110\text{ }^\circ\text{C}$, unless otherwise noted

(1) DCL540x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL541A01) , VI=1(DCL541B01)	I _{DD1(Q)}	-	1.9	2.8	mA
		I _{DD2(Q)}	-	4.9	7.0	mA
	VI=0(DCL541B01) , VI=1(DCL541A01)	I _{DD1(Q)}	-	19.3	27.6	mA
		I _{DD2(Q)}	-	5.2	7.3	mA
1 Mbps	f _{CLK} =50 MHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(1)}	-	11.0	16.6	mA
		I _{DD2(1)}	-	5.2	7.7	mA
25 Mbps	f _{CLK} =500 kHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(25)}	-	10.4	15.8	mA
		I _{DD2(25)}	-	7.5	11.6	mA
100 Mbps	f _{CLK} =12.5 MHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(100)}	-	11.5	16.3	mA
		I _{DD2(100)}	-	13.6	25.8	mA

(2) DCL541x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	VI=0(DCL541A01) , VI=1(DCL541B01)	I _{DD1(Q)}	-	2.9	4.1	mA
		I _{DD2(Q)}	-	4.5	6.4	mA
	VI=0(DCL541B01) , VI=1(DCL541A01)	I _{DD1(Q)}	-	16.4	22.2	mA
		I _{DD2(Q)}	-	10.0	13.9	mA
1 Mbps	f _{CLK} =500 kHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(1)}	-	9.8	14.8	mA
		I _{DD2(1)}	-	7.4	9.5	mA
25 Mbps	f _{CLK} =12.5 MHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(25)}	-	10.4	16.1	mA
		I _{DD2(25)}	-	9.2	12.2	mA
100 Mbps	f _{CLK} =50 MHz, duty=50 % cycle square wave. C _L =15 pF	I _{DD1(100)}	-	13.1	18.2	mA
		I _{DD2(100)}	-	14.3	24.1	mA

10. Insulation Specifications

PARAMETER	Symbol	TEST CONDITIONS	VALUE	UNIT
Minimum External Clearance	CLR	Shortest terminal-to-terminal distance through air	8	mm
Minimum External Creepage	CPG	Shortest terminal-to-terminal distance across the package surface	8	mm
Distance Through The Insulation	DTI	Minimum internal gap	17	μm
Comparative Tracking Index	CTI		600	V
Material Group	-	According to IEC 60664-1	I	-
Overvoltage Category Per IEC 60664-1	-	Related Mains Voltage ≤ 300 V _{rms}	I-IV	-
	-	Related Mains Voltage ≤ 600 V _{rms}	I-IV	-
	-	Related Mains Voltage ≤ 1000 V _{rms}	I-III	-
DIN EN IEC 60747-17; (VDE 0884-17)				
Maximum Repetitive Peak Isolation Voltage	V _{IORM}	AC voltage (bipolar)	1414	V _{PK}
Maximum Transient Isolation Voltage	V _{IOTM}	V _{TEST} = V _{IOTM} , t = 60 s (qualification) , V _{TEST} = 1.2 x V _{IOTM} , t = 1 s (100 % production)	8000	V _{PK}
Maximum Impulse Voltage	V _{IMP}	IEC 61000-4-5 1.2/50 μs waveform	8000	V _{PK}
Maximum surge isolation voltage	V _{IOSM}	Test method per IEC 61000-4-5, 1.2/50 μs waveform, V _{IOSM} ≥ 1.3 x V _{IMP} (qualification)	12800	V _{PK}
Apparent charge measuring voltage	V _{pd(m)}	Method A, After Input/Output safety test subgroup 2&3, V _{ini,a} =V _{IOTM} , V _{pd(m)} =1.2 x V _{IORM} t _{ini} = 60 s, t _m = 10 s, partial discharge < 5 pC	1697	V _{PK}
		Method A, After environmental tests subgroup 1, V _{ini,a} =V _{IOTM} , V _{pd(m)} =1.6 x V _{IORM} t _{ini} = 60 s, t _m = 10 s, partial discharge < 5 pC	2263	
		Method B1; At routine test (100 % production) and preconditioning (type test) V _{ini,b} ≥ 1.2 x V _{IOTM} , V _{pd(m)} =1.875 x V _{IORM} t _{ini,b} = 1 s, t _m = 1 s partial discharge < 5 pC	2652	
Barrier capacitance, input to output	C _{IO}	f = 1 MHz	1.5	pF
Input Capacitance	C _I	V _{IX}	1.8	pF
Isolation Resistance	R _{IO}	V _{IO} = 500 V, T _A = 25 °C	>10 ¹²	Ω
		V _{IO} = 500 V, 100 °C ≤ T _A ≤ 110 °C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150 °C	>10 ⁹	
Pollution Degree	-	-	2	-
Climatic Category	-	-	40/110/21	-
UL 1577				
Maximum Withstanding Isolation Voltage	V _{ISO}	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 x V _{ISO} , t = 1 s (100 % production)	5000	V _{rms}

11. Safety Limiting Values

PARAMETER	Symbol	TEST CONDITIONS	Value	Unit
Safety Input, Output Or Supply Current	I_S	$V_{DD1}=V_{DD2}=5.5\text{ V}$, $T_j=150\text{ }^\circ\text{C}$, $T_a=25\text{ }^\circ\text{C}$	284	mA
		$V_{DD1}=V_{DD2}=3.6\text{ V}$, $T_j=150\text{ }^\circ\text{C}$, $T_a=25\text{ }^\circ\text{C}$	434	mA
		$V_{DD1}=V_{DD2}=2.75\text{ V}$, $T_j=150\text{ }^\circ\text{C}$, $T_a=25\text{ }^\circ\text{C}$	568	mA
Safety Input, Output Or Total Power	P_S	$T_j=150\text{ }^\circ\text{C}$, $T_a=25\text{ }^\circ\text{C}$	1562	mW
Maximum Safety Temperature	T_S	-	150	$^\circ\text{C}$

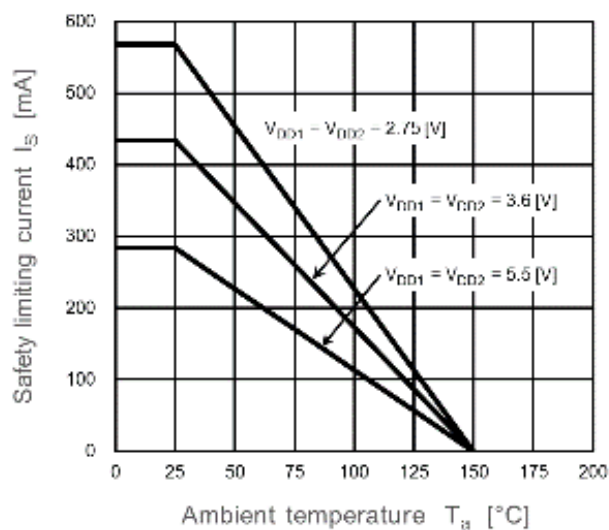
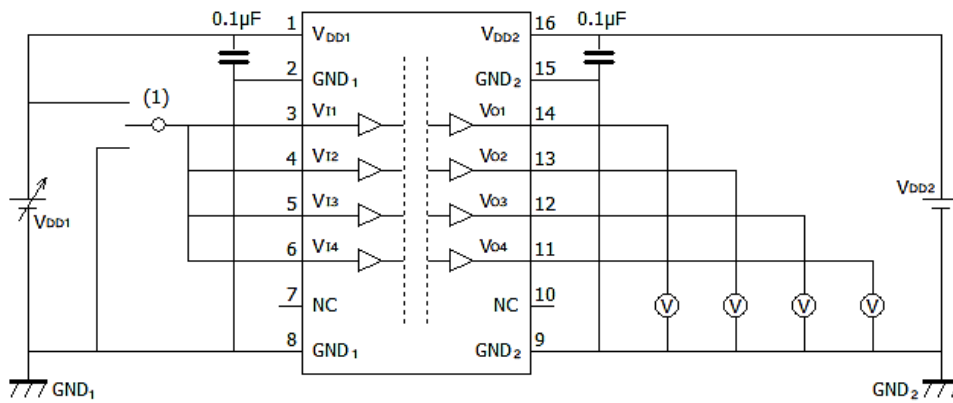


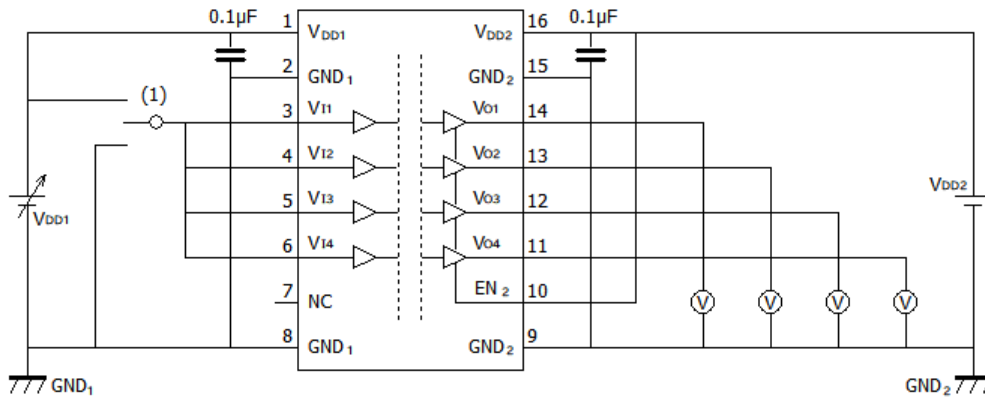
Fig. 11.1. Thermal Derating Curve for Safety Limiting Current— T_a

12. Test Circuit



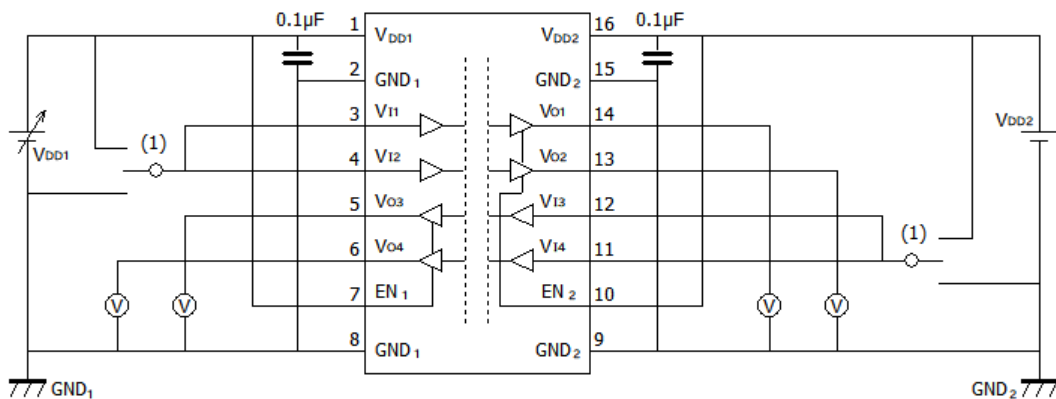
1: Default=L : V_{DD1} , Default=H : GND₁

Fig.12.1.1. DCL540C01/DCL540D01 V_{DD1UV+}/ V_{DD1UV-} Test Circuit



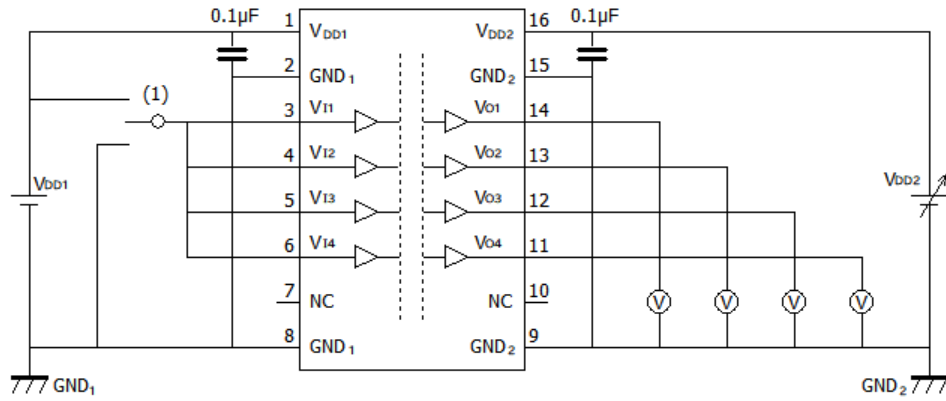
1: Default=L : V_{DD1} , Default=H : GND₁

Fig.12.1.2. DCL540L01/DCL540H01 V_{DD1UV+}/ V_{DD1UV-} Test Circuit



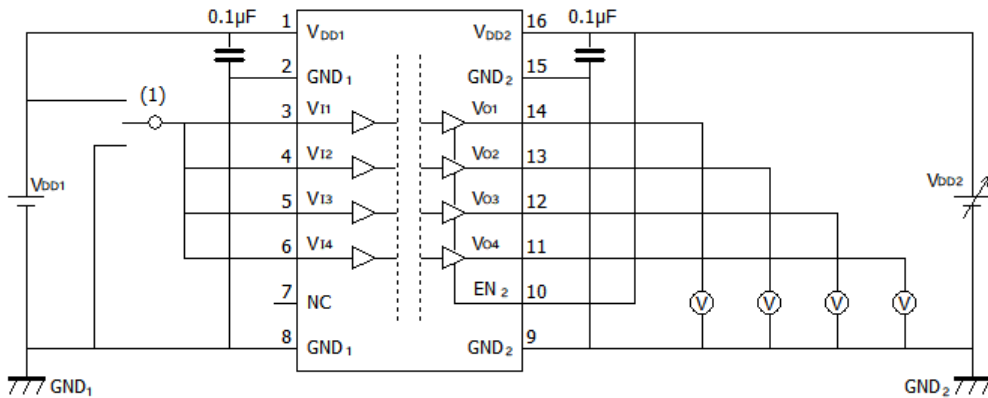
1: Default=L : V_{DDx} , Default=H : GND_x

Fig.12.1.3. DCL541A01/DCL541B01 V_{DD1UV+}/ V_{DD1UV-} Test Circuit



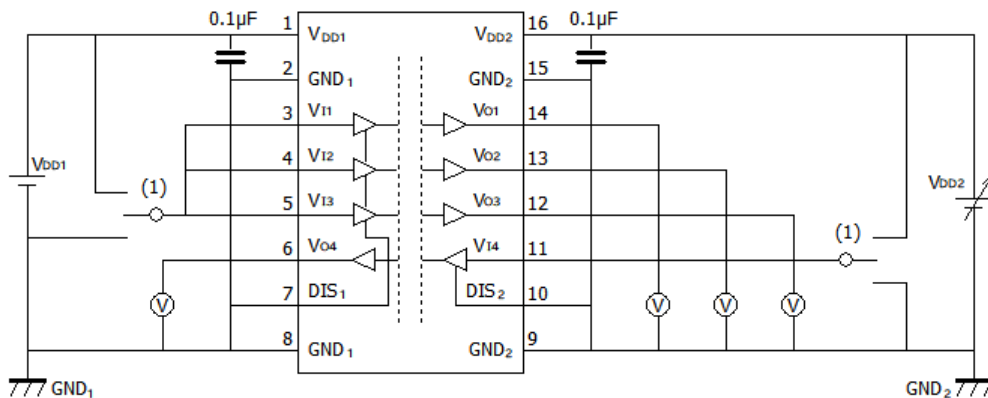
1: Default=L : V_{DD1} , Default=H : GND₁

Fig.12.1.4. DCL540C01/DCL540D01 V_{DD2UV+}/ V_{DD2UV-} Test Circuit



1: Default=L : V_{DD1} , Default=H : GND₁

Fig.12.1.5. DCL540L01/DCL540H01 V_{DD2UV+}/ V_{DD2UV-} Test Circuit



1: Default=L : V_{DDx} , Default=H : GND_x

Fig.12.1.6. DCL541A01/DCL541B01 V_{DD2UV+}/ V_{DD2UV-} Test Circuit

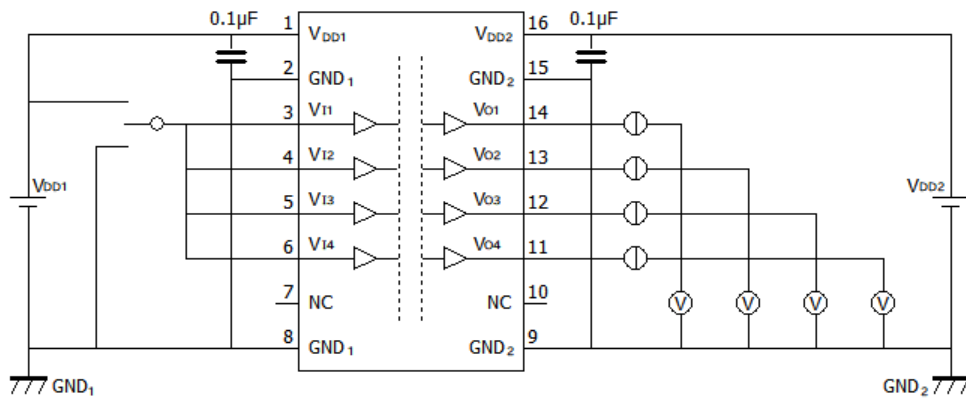


Fig.12.2.1. DCL540C01/DCL540D01 V_{OH}/V_{OL} Test Circuit

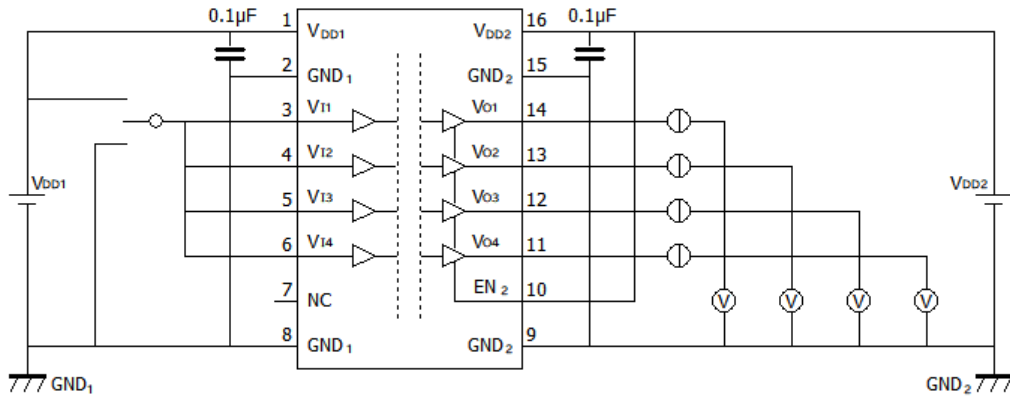


Fig.12.2.2. DCL540L01/DCL540H01 V_{OH}/V_{OL} Test Circuit

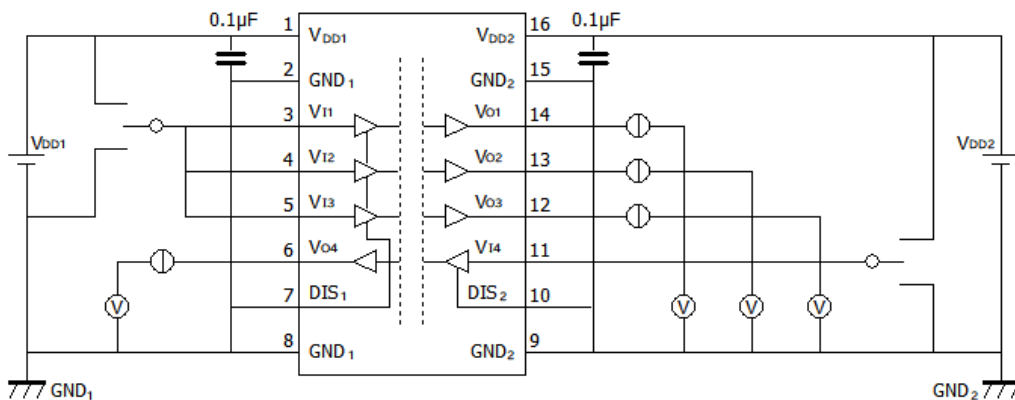


Fig.12.2.3. DCL541A01/DCL541B01 V_{OH}/V_{OL} Test Circuit

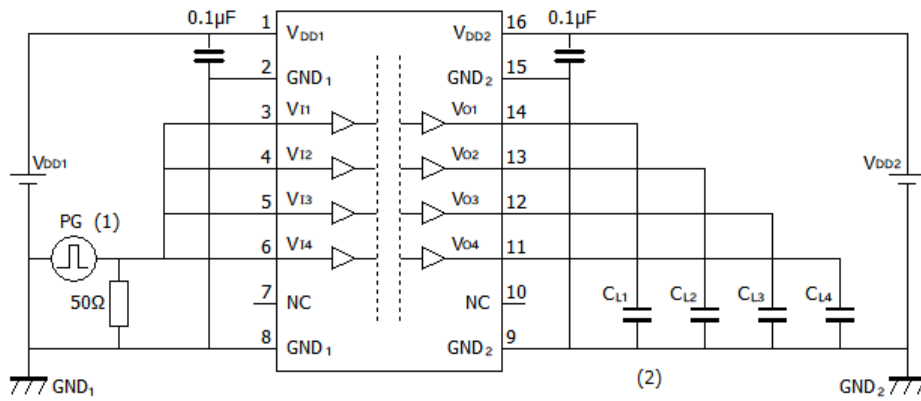


Fig.12.3.1. DCL540C01/DCL540D01 V_{IH}/V_{IL} Test Circuit

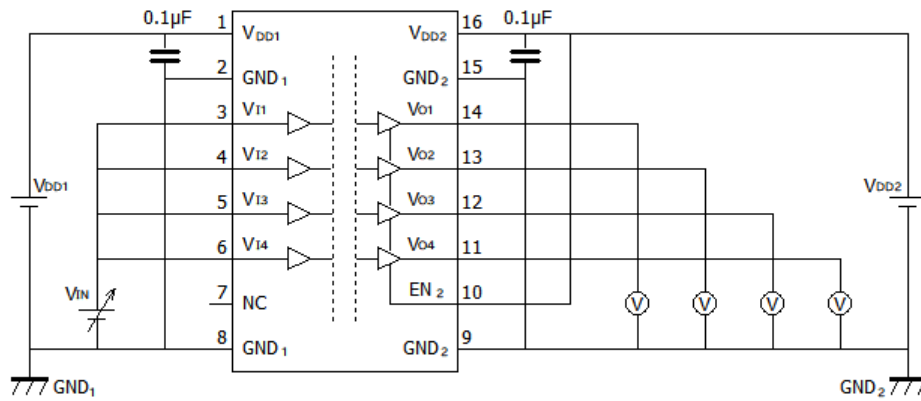


Fig.12.3.2. DCL540L01/DCL540H01 V_{IH}/V_{IL} Test Circuit

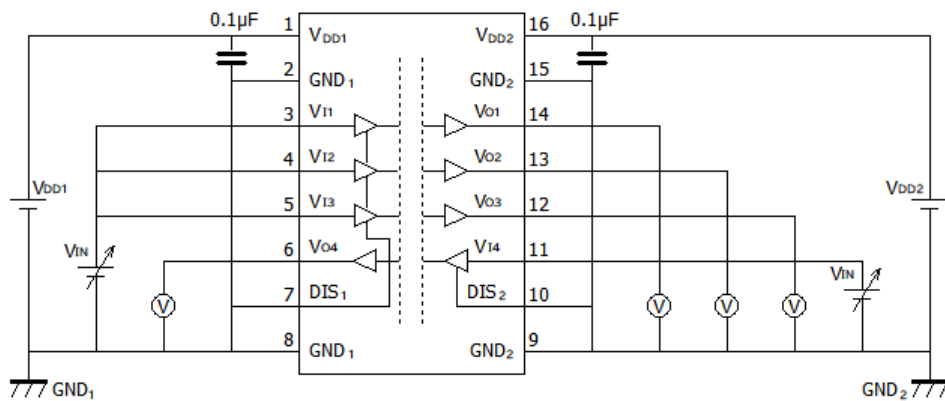
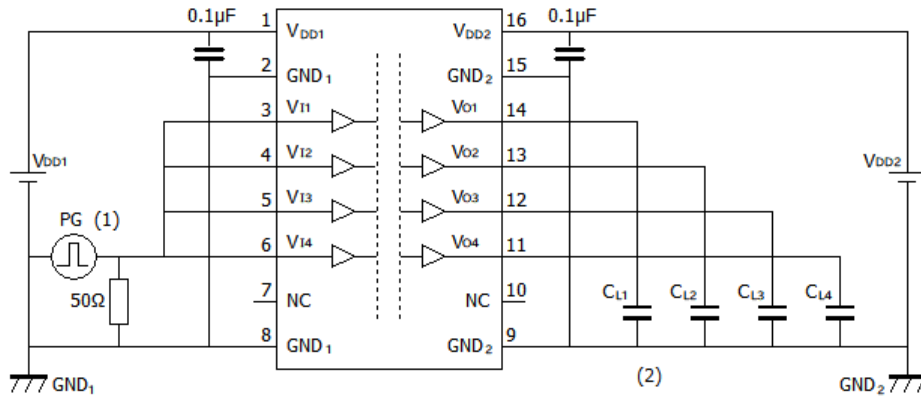


Fig.12.3.3. DCL541A01/DCL541B01 V_{IH}/V_{IL} Test Circuit



- 1: The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50 % duty cycle, $t_r \leq 2$ ns, $t_f \leq 2$ ns, $Z_0 = 50 \Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is needed not in actual application.
- 2: $C_{LX} = 15$ pF includes instrumentation and fixture capacitance.

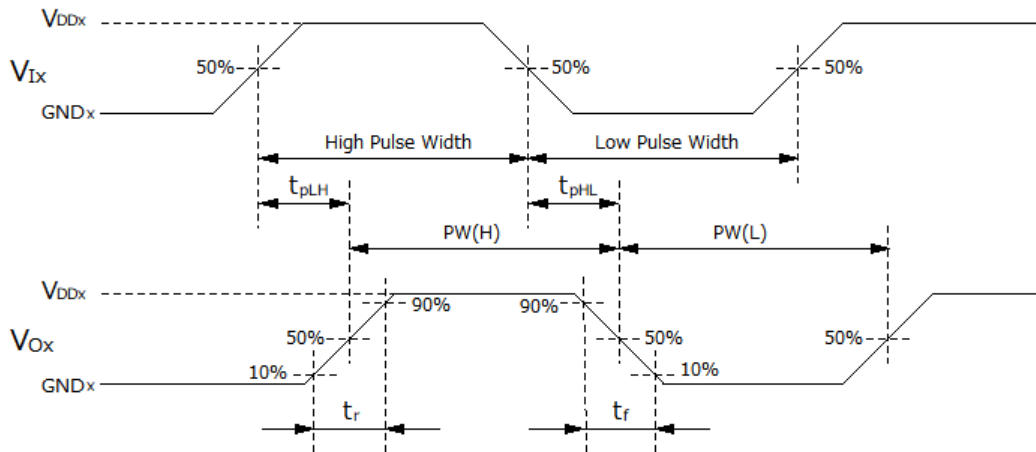
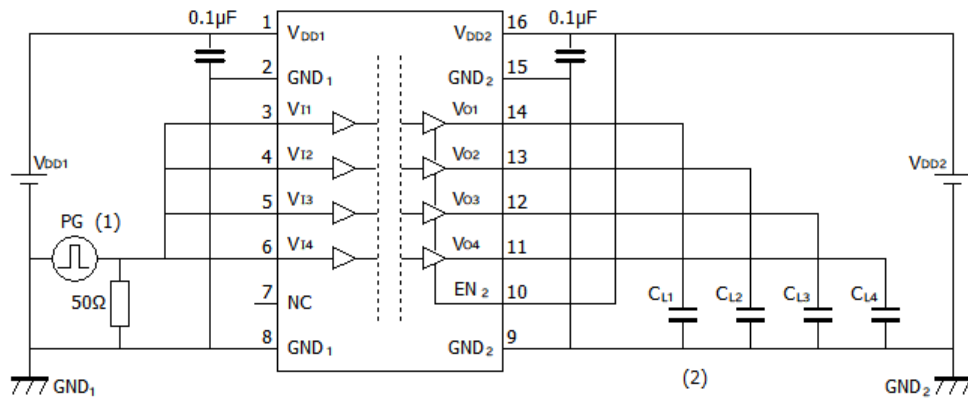


Fig.12.4.1. DCL540C01/DCL540D01 Switching Test Circuit and Voltage Waveforms



- 1: The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50 % duty cycle, $t_r \leq 2$ ns, $t_f \leq 2$ ns, $Z_0 = 50 \Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is needed not in actual application.
- 2: $C_{LX} = 15$ pF includes instrumentation and fixture capacitance.

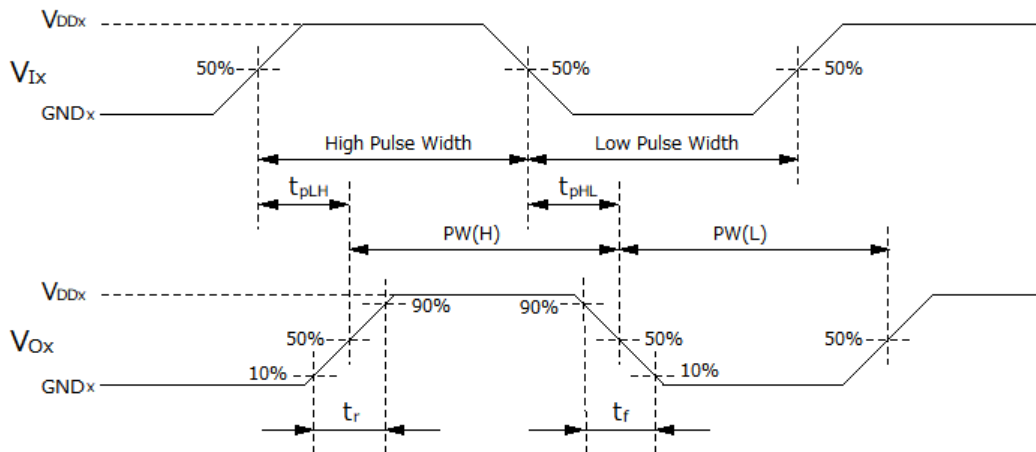
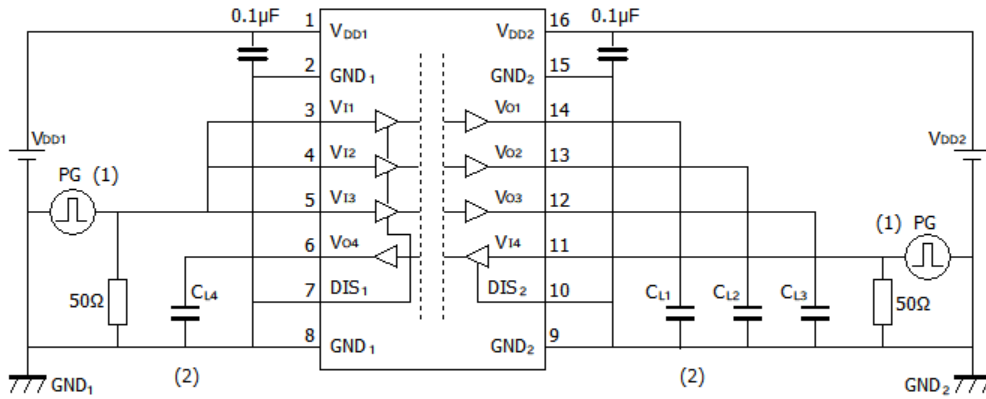


Fig.12.4.2. DCL540L01/DCL540H01 Switching Test Circuit and Voltage Waveforms



- 1: The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50 % duty cycle, $t_r \leq 2$ ns, $t_f \leq 2$ ns, $Z_0 = 50 \Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is needed not in actual application.
- 2: $C_{Lx} = 15$ pF includes instrumentation and fixture capacitance.

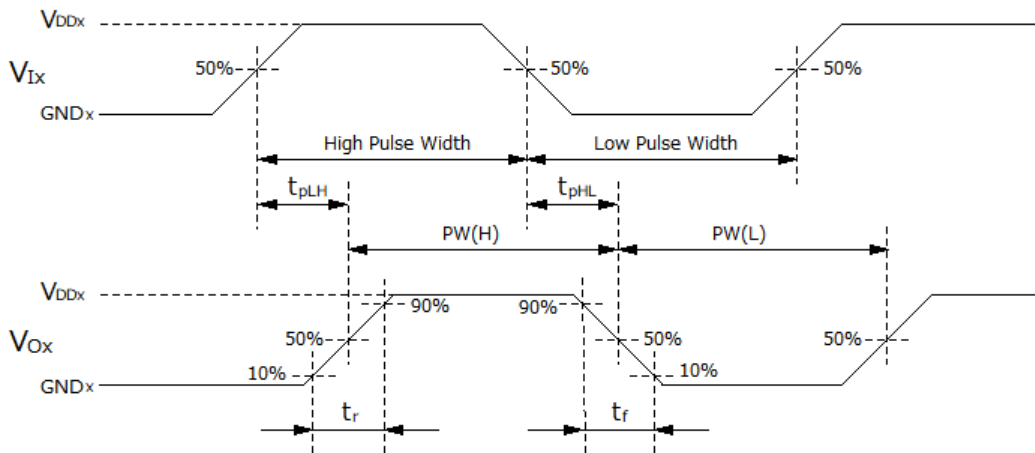
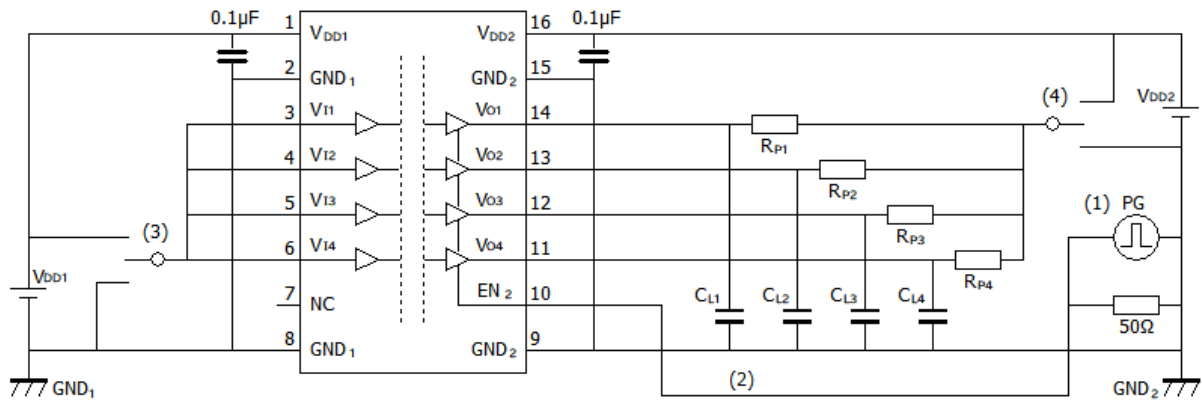


Fig.12.4.3. DCL541A01/DCL541B01 Switching Test Circuit and Voltage Waveforms



- 1: The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50 % duty cycle, $t_r \leq 2$ ns, $t_f \leq 2$ ns, $Z_0 = 50 \Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is needed not in actual application.
- 2: $C_{Lx} = 15$ pF includes instrumentation and fixture capacitance.
- 3: GND for t_{pZL} , t_{pLZ} , V_{DD} for t_{pZH} , t_{pHZ}
- 4: V_{DD} for t_{pZL} , t_{pLZ} , GND for t_{pZH} , t_{pHZ} .

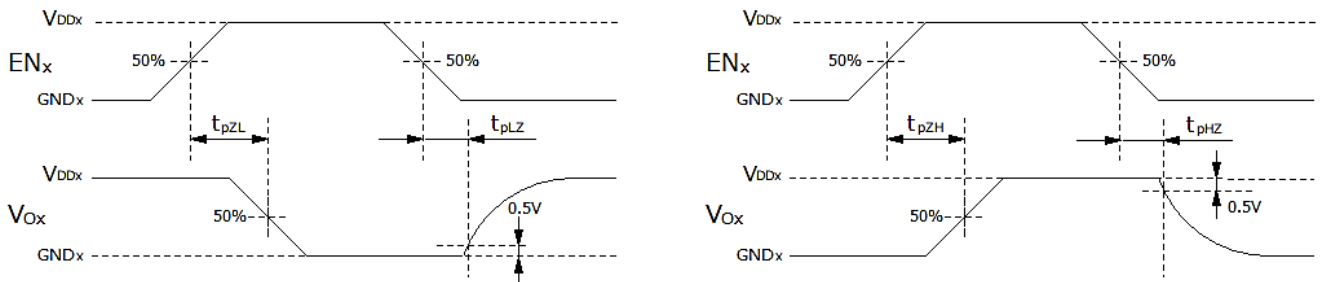
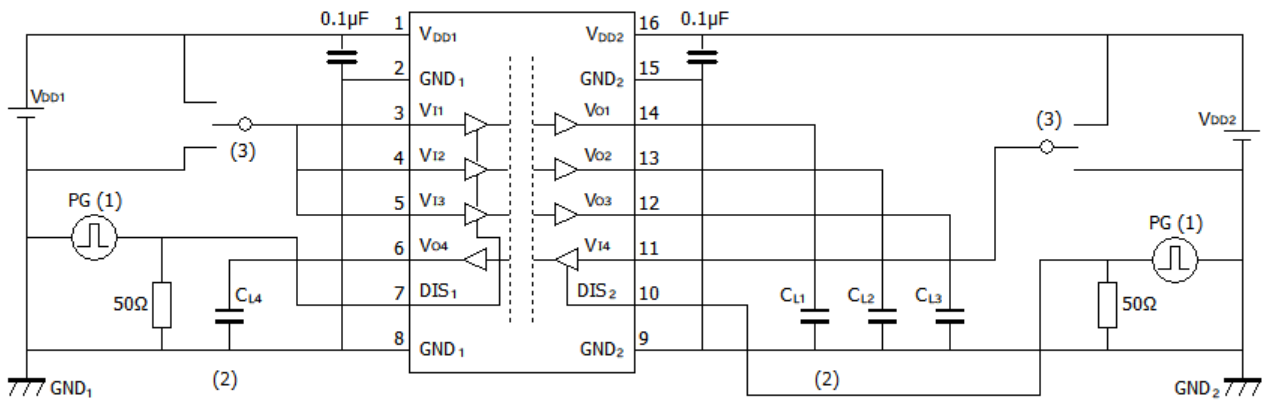


Fig.12.5. DCL540L01/ DCL540H01 Enable Propagation Delay Time Test Circuit and Waveforms



- 1: The input pulse is supplied by a generator having the following characteristics: PRR≤50 kHz, 50 % duty cycle, $t_r \leq 2$ ns, $t_f \leq 2$ ns, $Z_o = 50 \Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is needed not in actual application.
- 2: $C_{Lx} = 15$ pF includes instrumentation and fixture capacitance.
- 3: GND for DCL541B01, V_{DD} for DCL541A01

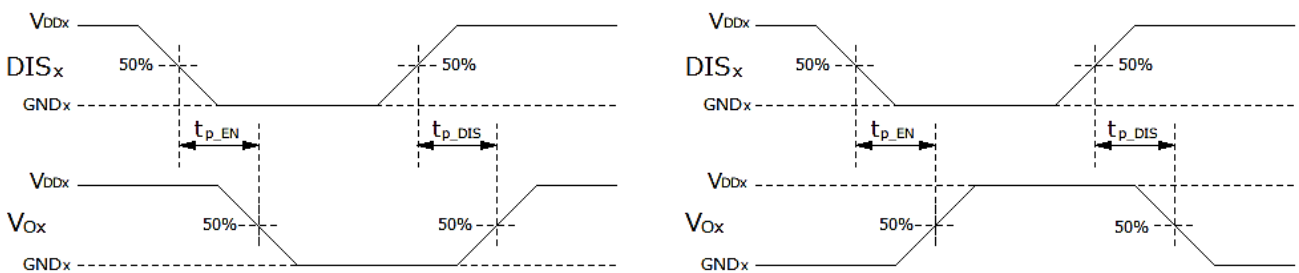
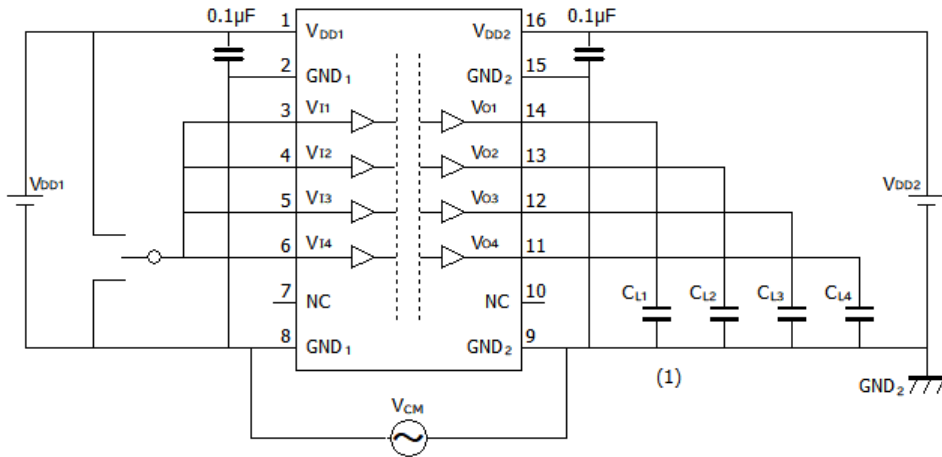
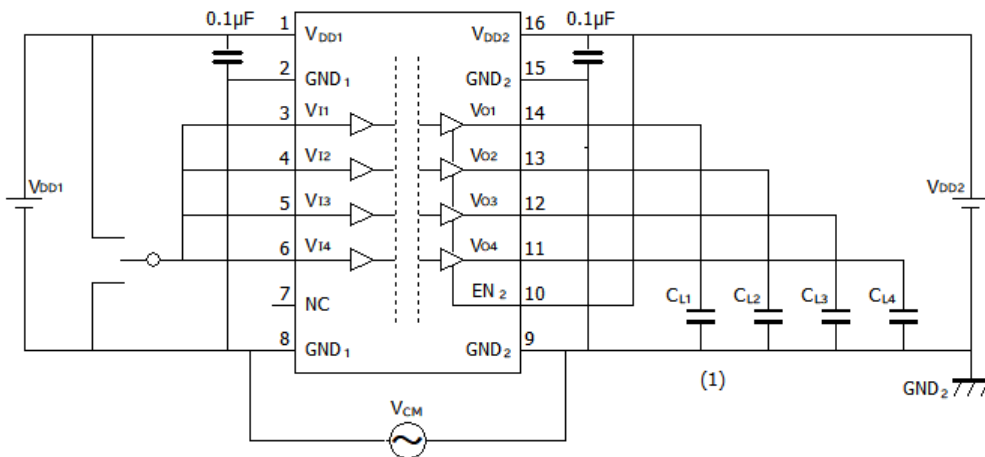


Fig.12.6. DCL541A01/DCL541B01 Disable Propagation Delay Time Test Circuit and Waveforms



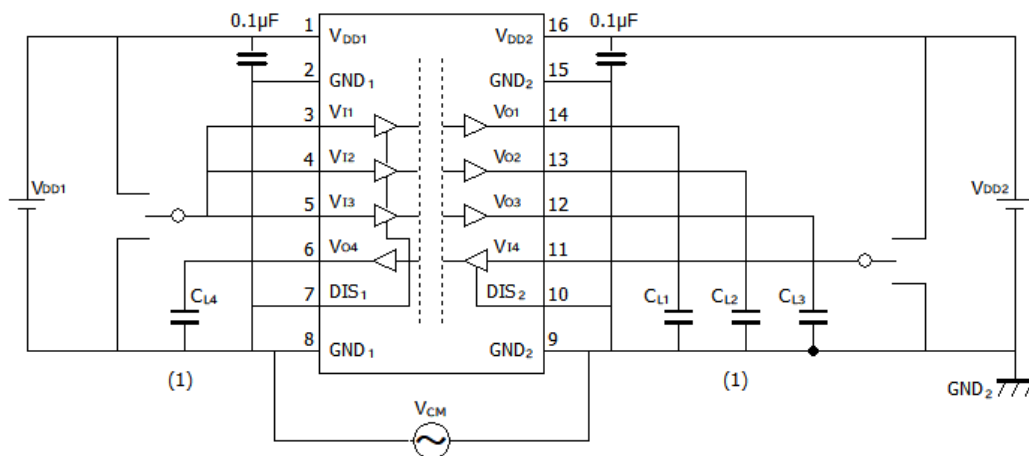
- 1: $C_{LX}=15$ pF includes instrumentation and fixture capacitance.
- 2: Apply V_{CM} with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured, V_{CM} may be applied with reference to GND₁ or with reference to GND₂.

Fig.12.7.1. DCL540C01/DCL540D01 Common-Mode Transient Immunity Test Circuit



- 1: $C_{LX}=15$ pF includes instrumentation and fixture capacitance.
- 2: Apply V_{CM} with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured, V_{CM} may be applied with reference to GND₁ or with reference to GND₂.

Fig.12.7.2. DCL540L01/DCL540H01 Common-Mode Transient Immunity Test Circuit



- 1: $C_{LX}=15\text{ pF}$ includes instrumentation and fixture capacitance.
- 2: Apply V_{CM} with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured, V_{CM} may be applied with reference to GND₁ or with reference to GND₂.

Fig.12.7.3. DCL541A01/DCL541B01 Common-Mode Transient Immunity Test Circuit

13. Characteristics Curves (Note)

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

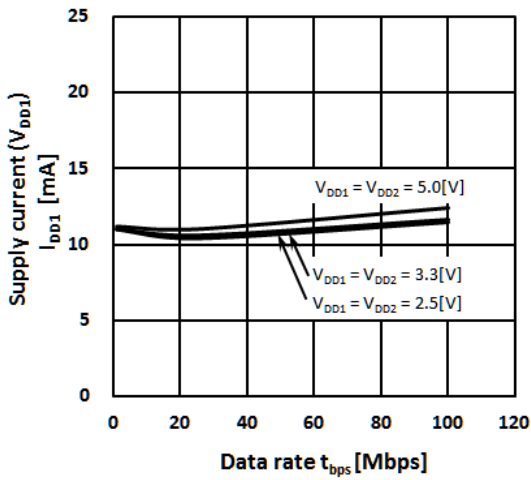


Fig.13.1. DCL540xx01 I_{DD1} Supply Current - Data rate

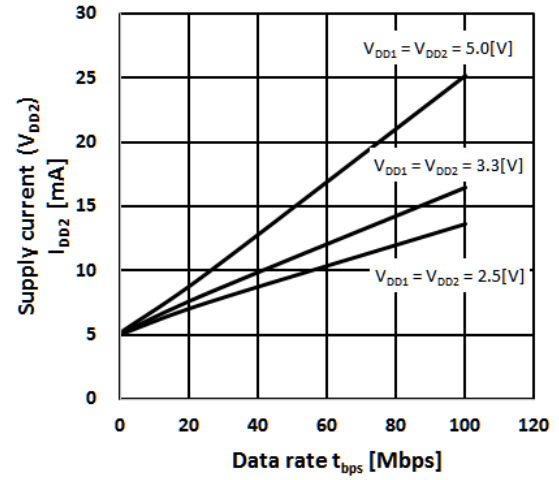


Fig.13.2. DCL540xx01 I_{DD2} Supply Current - Data rate

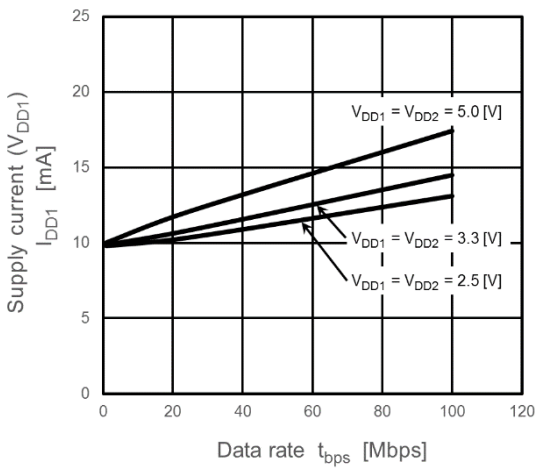


Fig.13.3. DCL541xx01 I_{DD1} Supply Current - Data rate

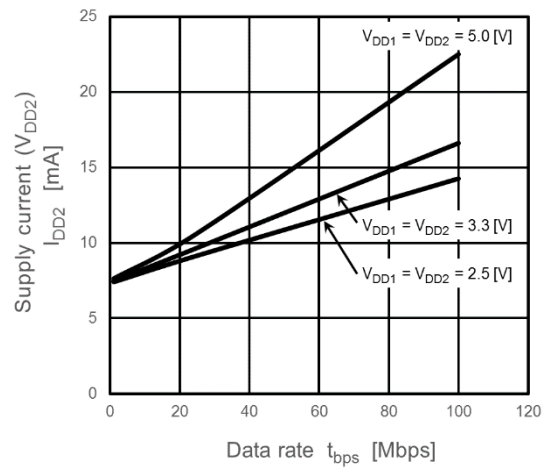


Fig.13.4. DCL541xx01 I_{DD2} Supply Current - Data rate

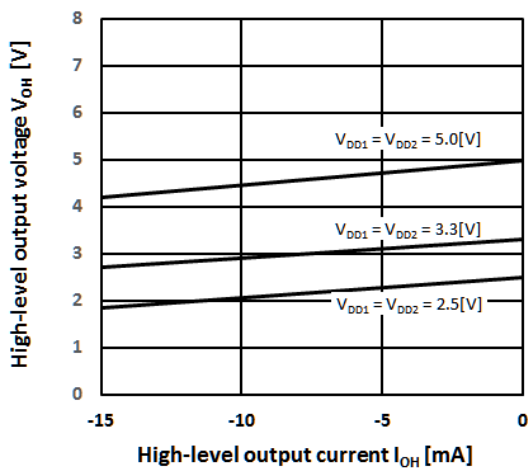


Fig.13.5. V_{OH} - I_{OH}

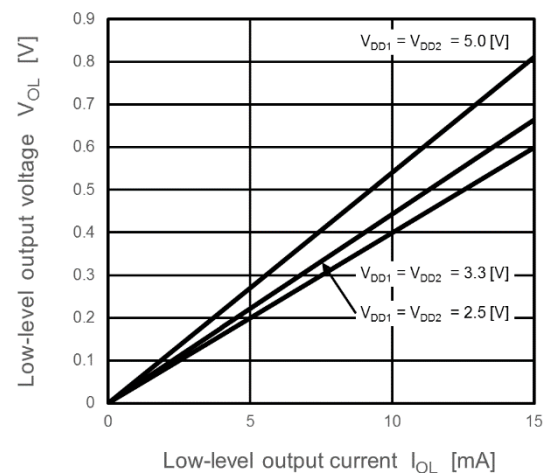


Fig.13.6. V_{OL} - I_{OL}

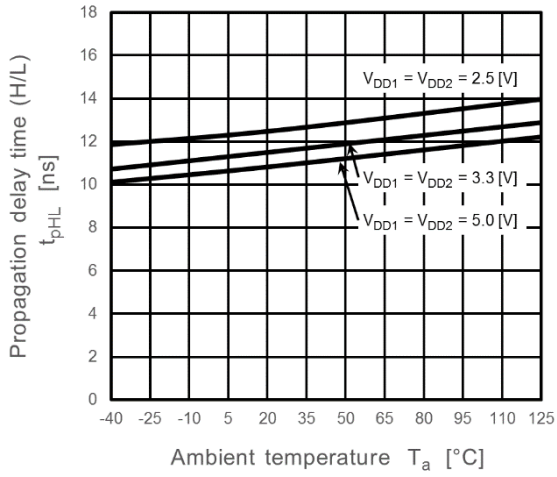


Fig.13.7. Propagation Delay Time t_{pHL} - T_a

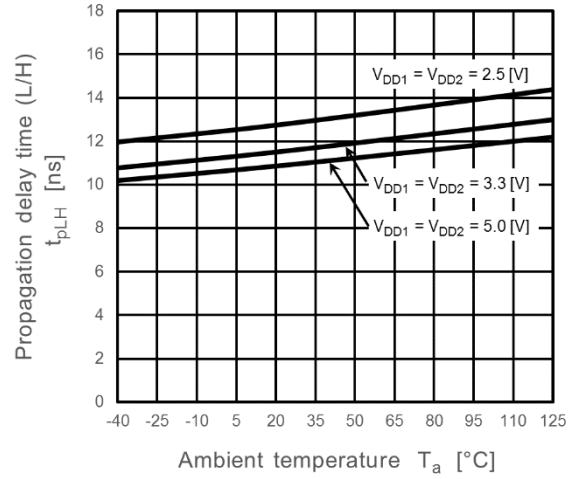


Fig.13.8. Propagation Delay Time t_{pLH} - T_a

14. Application Note

14.1. Eye diagram

The following figure shows typical eye diagrams of DCL541xx01 at the maximum data rate of 150Mbps with pseudorandom bit sequences (PRBS), supply voltage 3.3 V for reference only.

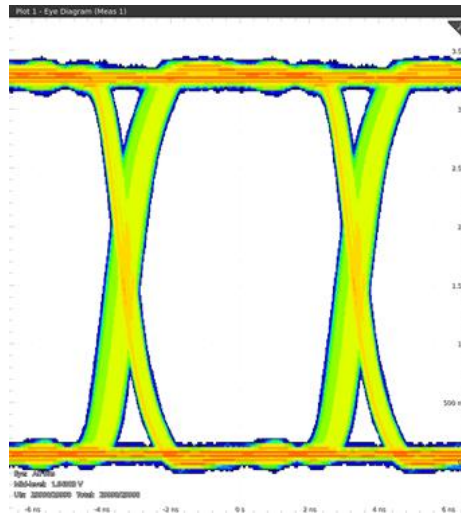


Fig.14.1 DCL541A01 Eye diagram at 150Mbps

14.2. PCB layout

A ceramic capacitor (0.1 μF) should be connected between pin 1 (V_{DD1}) and pin 2 (GND_1) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND_2) for V_{DD2} , and it should be the layout on the IC as close as possible (less than 10mm). Otherwise, the IC may not operate properly.

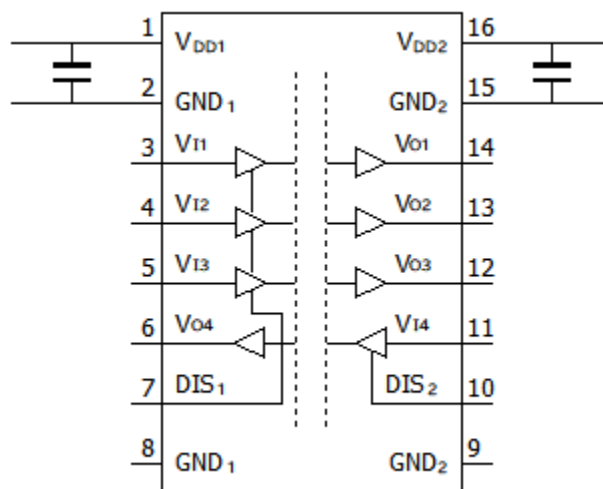
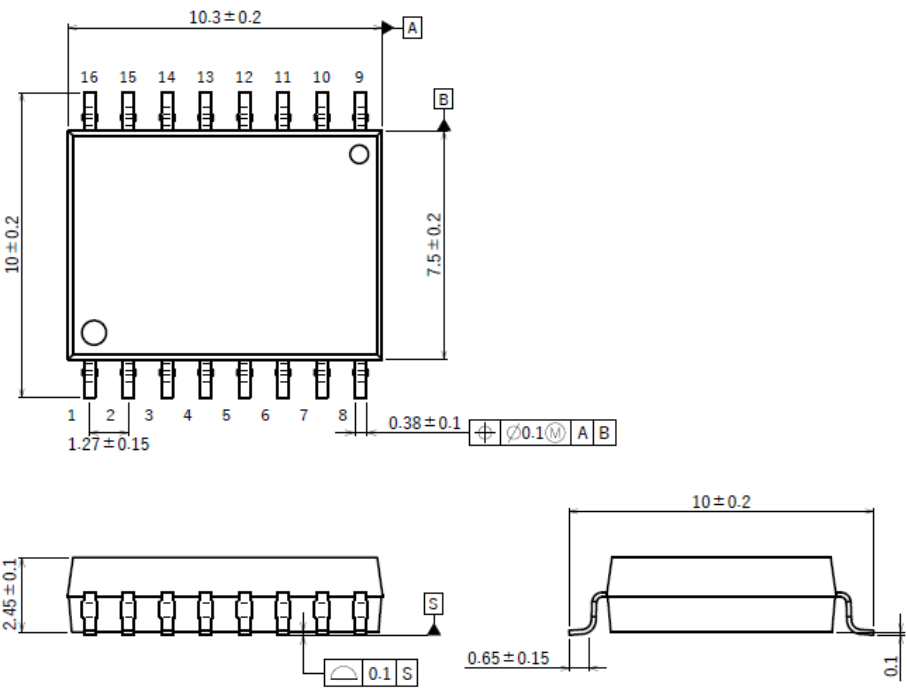
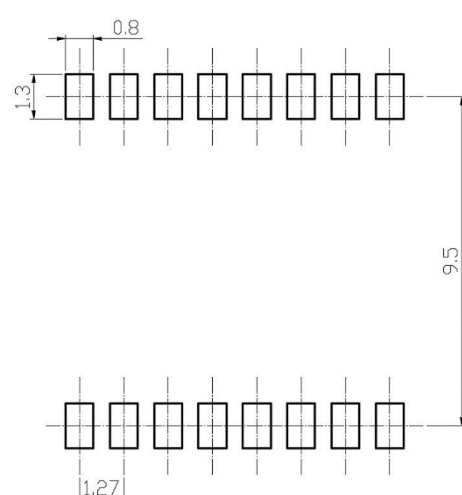


Fig.14.2 Recommended Printed Circuit Board Layout

15. Package Information

Implementation category	Surface Mount
Pin Number	16
Weight (g)	0.426 (Typical)
Package Dimension Width × Length × Height (mm)	10.3 × 10.0 × 2.45 (Typical)
Package Dimension(mm) / Land Pattern Example (mm)	<p>Package Dimension</p>  <p>Land Pattern Dimensions (for reference only)</p> 

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