Digital Isolator
EMC Application Notes

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1. Introduction

In equipment used in the Factory automation market, two systems that operate at high voltage and low voltage are mixed. High voltage and large current may applied to the low voltage part depending on the environment in which it is used. Therefore, a high voltage applied to the low voltage circuit and it may damage the circuit or cause an electric shock to the person who operates the equipment. In addition, the GND loop that occurs inside the device may cause an unexpected current and noise. As a countermeasure against these issues, it is necessary to insulate between high voltage block and low voltage block and suppress the current between the two blocks. In general, devices that require insulation are required from equipment in factory automation market, automotive market and consumer market.

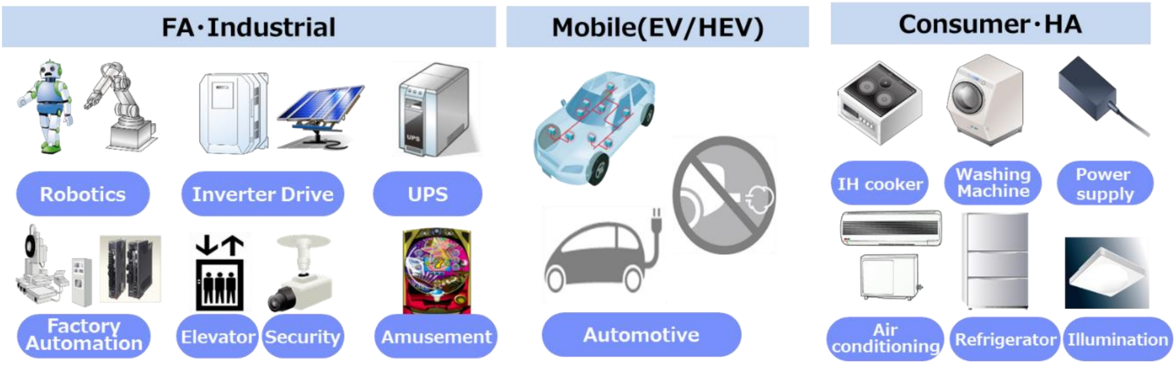


Figure 1-1 Application Examples

For many years, photocoupler used to insulate, but the digital isolator developed in response to the demand for higher-speed digital signal transmission, for smaller systems, and for longer product life. Currently, two types of products are developed, magnetic type and capacitive type.

2. Isolation Products

As mentioned above, there are three types of isolation products according to the transmission method.

2.1. Photocoupler

Photocouplers can insulate between two points by using optical signals.

An electrical signal is converted into an optical signal at the primary side, and an optical signal received by a phototransistor at the secondary side is converted into an electrical signal again.

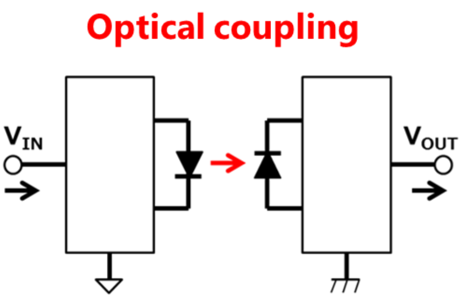


Figure 2-1 Photocoupler

2.2. Magnetic coupling digital isolator

Magnetic coupling digital isolator can insulate between two points by using magnetic energy generated by the coil current. An electrical signal is converted into a magnetic energy at the primary side, and a magnetic energy received at the secondary side is converted into an electrical signal again.

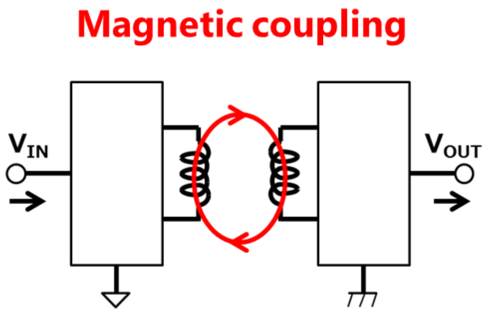


Figure 2-2 Digital isolator of magnetic coupling type

2.3. Capacitive coupling digital isolators

Capacitive coupling digital isolator can insulate between two points by using the charge and discharge of capacitor. An electrical signal is converted into the charge and discharge of capacitor at the secondary side and it is converted into an electrical signal again.

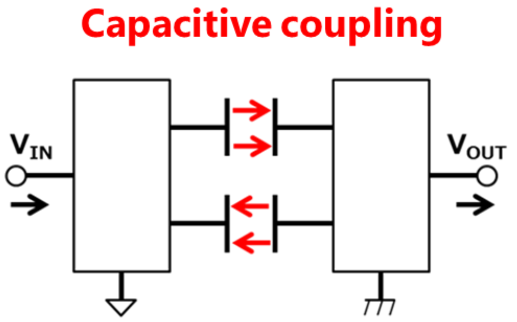


Figure 2-3 Digital isolator of capacitive coupling type

2.4. Photocoupler and digital isolator

A comparison table of the photocoupler and the digital isolator is shown below.

Digital isolator has advantages that are long isolation barrier life, high-speed communication, high common-mode noise robustness and low current consumption. Furthermore, it is easy to compose multichannel structure, so it is possible to reduce the number of parts. On the other hand, Photocouplers have many product lineups based on the abundant market performance over many years and have good characteristics of EMC.

Table 2-1 Product comparison table21

	Photocoupler	Digital isolator
Product life	△	○
Transmission speed	×	○
Power consumption	△	○
CMTI*	△	○
EMC	○	△
Multi-channel	×	○
Analog transmission	○	×
Number of product lineups	○	×

*CMTI: Common Mode Transient Immunity

3. Digital isolator

3.1. Product classification of digital isolators

Digital isolator products are divided mainly into three parts, depending on the purpose of the signal to be Transmitted.

- High speed communication IC
  Transmitting high-speed digital signals through an isolation barrier.

- Gate driver
  Driver IC that converts the control signal from the external controller IC to the control signal of the power device (MOSFET, IGBT, SiC, GaN).

- Isolation amplifier
  Amplifier that converts the input analog signal to a digital signal on the transmitting side and outputs analog signal or digital signal according to the output specifications.

3.2. How to Select Digital Isolator Products

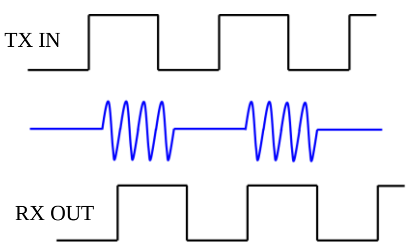
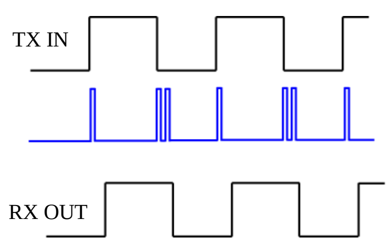
Many digital isolators are designed for use in specific applications. Therefore, it is necessary to confirm whether the selected product is suitable for the required specifications of the application.

The criteria for this are the electrical specifications and the signal transmission method. They are summarized in Table 3-1 and Table 3-1.

Table 3-1 Electrical Characteristics31

Parameter	Description	Check point
Insulation guarantee	Insulation voltage between input and output	Package size
Maximum input current consumption	Maximum current consumption at input side	System Power Consumption
Maximum output current	Maximum supply current to the load	Load Specifications
Input voltage	Amplitude of the input signal	System side I/O voltage
Output voltage	Amplitude of output signal	Load supply voltage
Minimum pulse width	Minimum pulse width of input waveform	Switching frequency
Drive frequency	Drive frequency of the load	Switching frequency
Propagation delay time	Propagation delay time between input and output	Load control timing
CMTI	Robustness of Common Mode Noise	Noise immunity

Table 3-2 Signal transmission methods32

	On-Off Keying (OOK)	Edge-Detection
Outline	Converts the H / L of the input digital signal to the amplitude of the carrier wave.	Detects the rising / falling edges of the input digital signal and converts it into a pulse signal.
Pros	・Simple control ・Low propagation delay	・High noise immunity ・Low current consumption
Cons	・Susceptible to noise ・Excessive current consumption	・Complicated control ・Refresh pulse required ・Large propagation delay
Sample Waveform		

3.3. Example of adoption of digital isolator products

The adoption of digital isolators is shown below. High-speed communication ICs are mainly used for communication signals between the controller and peripheral blocks. Gate drivers are used to control the gates of power devices. In addition, the isolation amplifier monitors each voltage and current and transmits them to the controller.

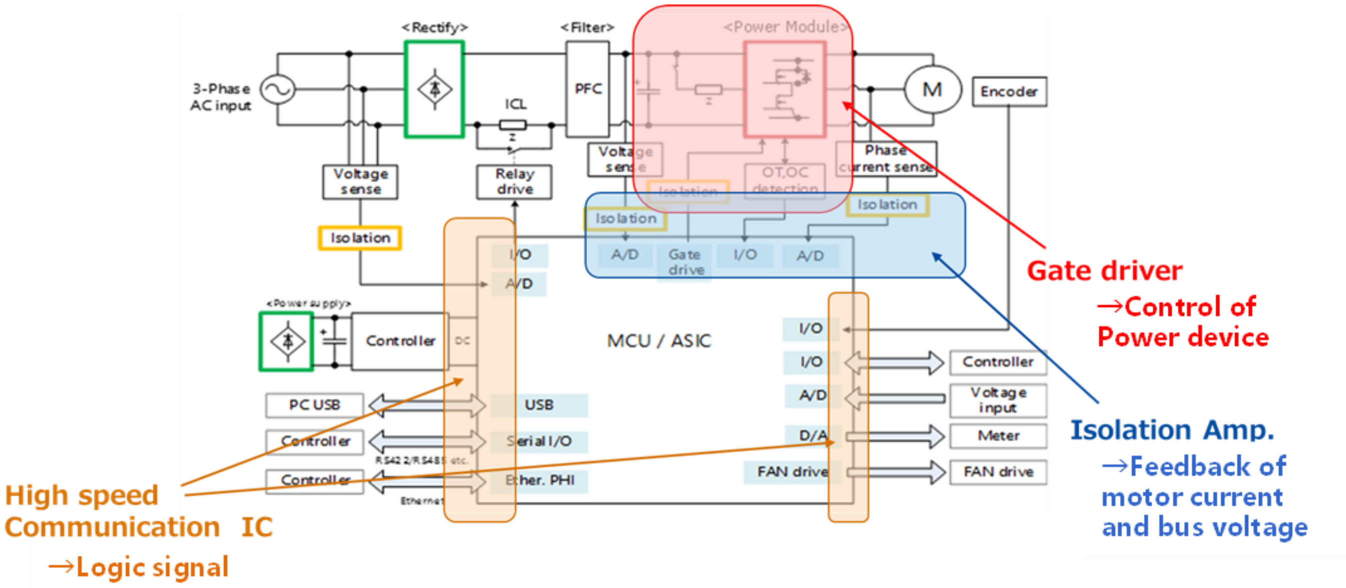


Figure 3-1 Application Examples

4. PCB Design Guide

To keep the robust EMC characteristics, it is important to start the EMC oriented design from early design stage. For this purpose, this section provides a PCB (Printed Circuit Board) design guide when considering EMC performance as a priority.

* This PCB design guide helps designer to reduce EMC risk and does not mean that it will compliant with EMC requirement at the System level testing. It is also recommended to give priority to high-speed signal lines, high-current power lines, and other wiring with high EMC risk when designing.

4.1. Layer stack-up

Table 4.1 shows an example of the layer stack-up of the PCB. Various layer stack-ups are conceivable depending on the target application. The basic concept is minimum four-layer PCB. It is assumed that a digital isolator IC will be placed in the L1 layer.

Table 4-1 Example of layer stack-up.41

L1	Signal (main), GND
L2	GND
L3	Power supply, GND
L4	Signal (secondary), GND

(1) Routing the signal line on L1. Especially, it is desirable to route the important signals such as clock signal, bus signal, and communication line on the L1 side. The free space other than the signal line of L1 is filled with the GND plane and must be connected with the solid GND of L2 with the VIAs.
(2) L2 shall be a solid GND plane.
(3) L3 shall be a power line and GND plane. Prioritize the power supply with a large current and route at the shortest distance. The free space other than the power supply is with the GND wiring, and must be connected with the solid GND of L2 with the VIAs. (See Section 4.2.)
(4) Routing the signal line (less critical wiring) on L4 that cannot be L1. The adjacent L3 has slits multiple power supplies and GNDs, but it is desirable that the signal line on L4 should not cross these slits not to have the detour of the return path. (See Section 4.2. also)

4.2. GND design

(1) No slit on the reference Planes under the signal line.
The high-frequency return current will flow through the GND directly below the signal line, but if there is a slit on the reference plane in the middle, the high-frequency return current will turn farther along the slit back. Such slits should be avoided, since this slit will increase the loop path of the current and increase the EMI noise.

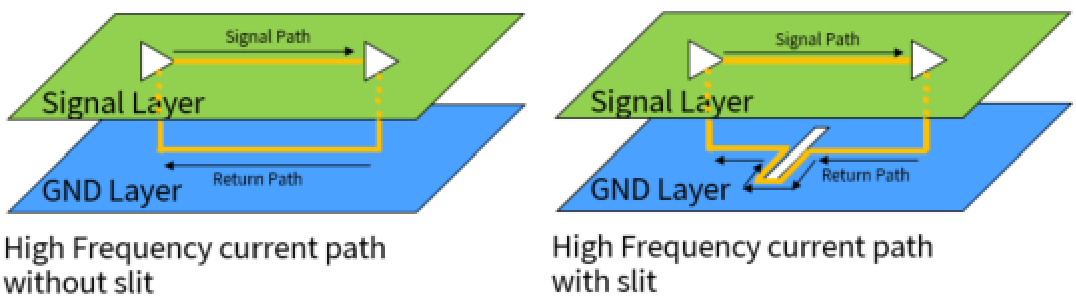


Figure 4-1 Differences in return paths with and without slits

(2) GND VIAs should be placed every 5mm as minimum

One wavelength of a 1GHz signal is about 300mm, but the wavelength is shortened due to the influence of the dielectric on the board, and it is about half, 150mm. Therefore, if there is an elongated GND pattern of 150 mm or more on the board, a potential difference of one wavelength will occur on that pattern, and the potential will become unstable. This unstable potential tends to generate EMI, so to avoid this, place GND VIAs every 5 mm or less on the entire board.

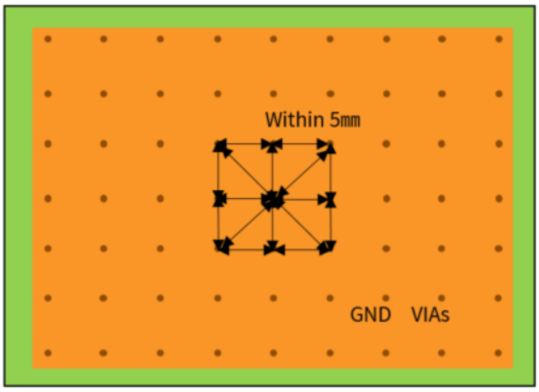


Figure 4-2 Sample Spacing of GND VIAs

(3) Avoid the Elongated GND patterns and stub-shaped GND patterns

Due to the relationship between the wiring length and frequency described in (2), the slender GND pattern and the stub-shaped GND pattern acts as the antenna and are likely to generate EMI. Therefore, the unnecessary GND stub pattern should be avoided. If the pattern becomes too narrow, make corrections such as placing the GND VIAs densely or making the pattern width thicker.

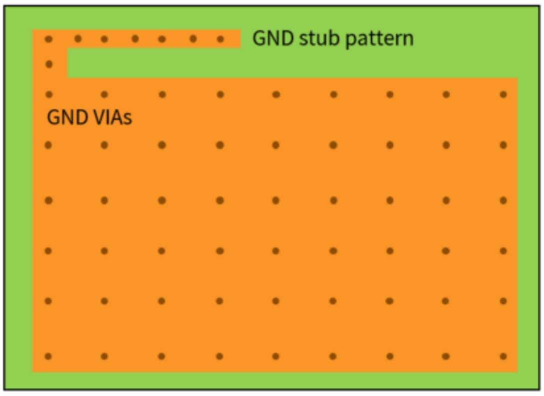


Figure 4-3 Example of an elongated stub-shaped GND pattern

(4) Avoid the placing continuous VIAs without gaps
Ideally, L2 should be a solid GND plane as described in 4.1, but a solid GND will be drilled in the signal VIAs between L1 and L4 and the power VIAs between L1 and L3, L3and L4. If there are one or two VIAs are adjacent, there is no problem. However, if multiple VIAs are continuously adjacent as shown in Fig. 4.4, VIAs anti-pad will be combined to form a slit, which may break the return path and cause EMI deterioration. Especially four or more consecutive VIAs should be avoided.

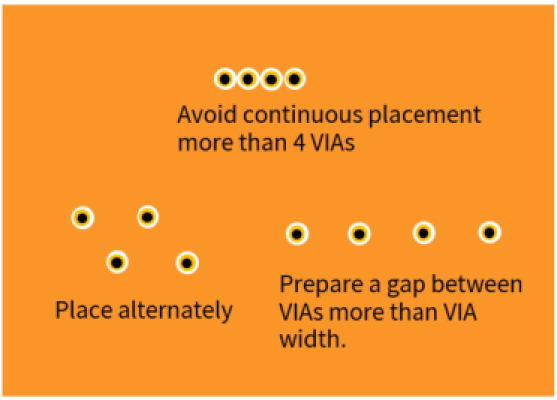


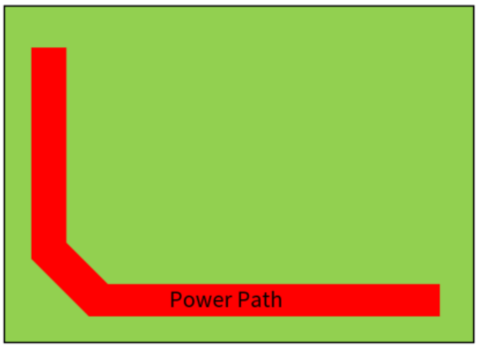
Figure 4.4 VIAs placement

4.3. Power supply design

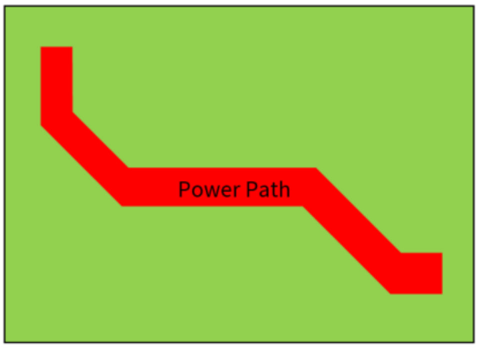
Guidelines for power supply design include:

(1) It is recommended to wire the power supply wiring thickly on the power supply layer (L3). When drawing power with wires, consider that the wiring width should be at least 1mm for the consumed current 1A.

(2) It is recommended that the power supply wiring be drawn at the shortest distance. However, it is important to note that the shortest distance may not be optimum, because interference with the upper and lower signal lines and power supply lines is also important.



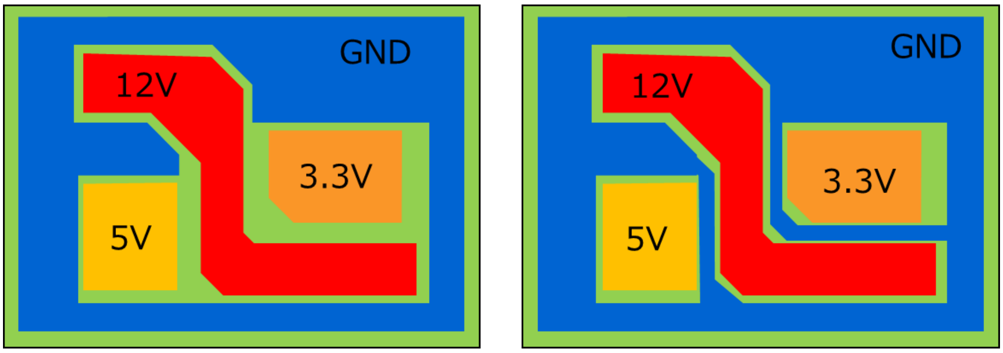
(a) NG example



(b) OK Example

Figure 4-5 Routing of power supply lines

(3) When there are multiple domains of power supply wiring, a guard GND is provided between the power supply domains for suppressing noise interference between them. It is recommended that the wiring width of the guard GND is 1mm or more. It is also recommended to place VIAs every 5 mm or less for guard GND. Avoid placing close to each other without guard GND between power supplies as shown in Fig. 4.6 (a), and place guard GND between power supplies as shown in (b).

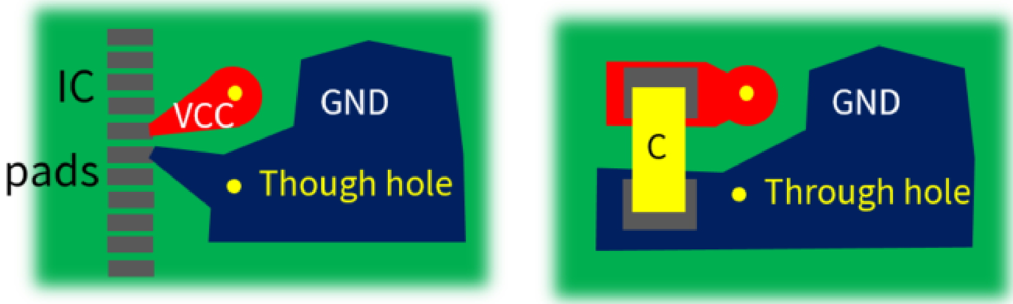


(a) NG example **(b) OK Example**

Figure 4-6. Example of Interference Reduction Method between Power Supplies

(4) When power plane resonance occurs, the risk of deterioration of EMC characteristics at that resonant frequency increases. To avoid this, it is recommended to perform power plane resonance analysis after the power layout design. Place an appropriate capacitor at the resonance point and take measures to suppress power fluctuations.

(5) Arrange the capacitance so that the current loop (IC power supply terminal, capacitor and IC GND terminal) is minimized. If the capacitor placed on the opposite side of the digital isolator implementation side, layout as shown in Figure 4.7. For L1, placing the through hole near the power supply and GND terminals, for L4, it is desirable to place the capacitor in the vicinity of the through hole.



(a) L1 (b) L4

Figure 4-7 Layout recommendation of the bypath capacitor

4.4. Clock routing design

Clock routing is the most EMI prone wiring, and special design care is required. The clock signal is defined as the single-ended wiring at a relatively high speed (several tens of MHz or higher). The following matters are equivalent precautions even in differential communication line design, and it is recommended to apply them as many as possible.

(1) Wire with L1 in microstrip line.

(2) Avoid wiring with L4. If necessary, wire as short as possible.

(3) Place the guard GND on both sides of the signal line.

(4) When changing the wiring layer, prepare GND VIA(s) to the signal VIA as close as possible.

(5) Wire the return current path with care so that it is uninterrupted.

4.5. Data bus wiring design

It is recommended to apply the following design for the data bus wiring. Guard GND placement for each data line is difficult as the actual design, so it is recommended to provide guard GND every 4 bits.

(1) Wire with L1 in microstrip line.

(2) Avoid wiring with L4. If necessary, wire as short as possible.

(3) Place the guard GND every 4 bits.

(4) When changing the wiring layer, prepare GND VIA(s) to the signal(s) VIA as close as possible.

(5) Wire the return current path with care so that it is uninterrupted.

4.6. General signal wiring design

In addition, it is recommended to perform the following design in the same way for signal routing design.

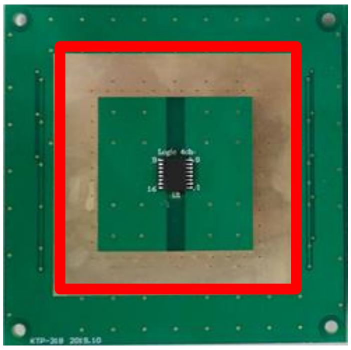
(1) Wire with L1 in microstrip line.

(2) The wiring at L4 should be as short as possible.

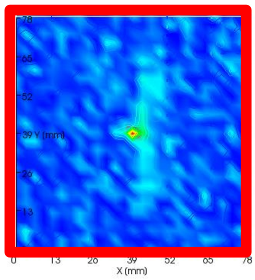
(3) Prevent the return current path not be interrupted.

4.7. Effect of the insulation of the digital isolator

The digital isolator evaluation board must have a structure in which the primary and secondary sides of the signal and power supply are separated, and there must be a slit structure on the board. Such an elongated shape becomes a slit antenna depending on the frequency, which may deteriorate EMI. Figure 4-8 shows the current distribution around the digital isolator IC and the slit at the carrier frequency. At the carrier frequency, the current is concentrated around the IC and is not affected by the slit. However, a slit of about 5cm may become a slit antenna in a higher frequency band, and a strong current may flow around the slit portion and radiate into the space as electromagnetic waves.



Measurement area in red frame



Current distribution at the carrier frequency

Figure 4-8 Current distribution on the board

5. Noise and EMC

5.1. What is noise?

When an electronic device operates, voltage, current, signals, etc. contain unnecessary components due to various factors. Many of them may be the cause of malfunction or performance degradation, unlike the ideal that designers expect.

There are two types of noise: natural noise such as lightning strikes and static electricity, and artificial noise such as motors and fluorescent lamps. Some of them intentionally emit electromagnetic waves, such as communications equipment and broadcasting towers.

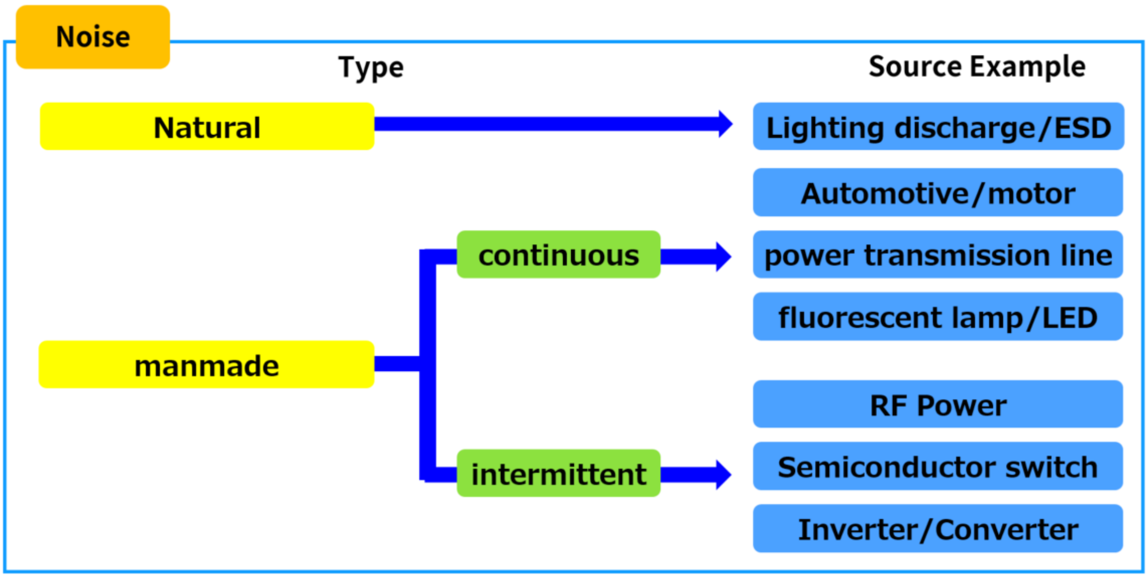


Figure 5-1 Noise Types

In addition, the types of noise caused by noise propagation paths are classified into the following:
Conducted noise in which noise travels through wires or board patterns;
Induction noise generated by electromagnetic induction or electrostatic induction when power lines or signal lines of peripheral devices come close to lines (wires or patterns) in which noise currents flow;
Radiation noise generated by input/output lines serving as antennas and radiated to peripheral devices.

5.2. What is EMC?

As system designs become increasingly sophisticated and compact in recent years, the semiconductor itself used in systems is becoming increasingly multifunctional, higher currents, lower voltages, and faster operating speeds. It makes demands for the best noise characteristics of electronic equipment.

In order to prevent the system from malfunctioning even in severe noise-disturbing environments, immunity (EMS: Electromagnetic Susceptibility) characteristics on Semiconductor device is increasingly required to prevent the system from malfunctioning even if the system is subject to electromagnetic interference (EMI: Electromagnetic Interference), which does not cause electromagnetic interference to others or to themselves. EMC (Electromagnetic Compatibility) is defined as the ability to have the both EMI and EMS characteristics by the system requirement to have the proper function.

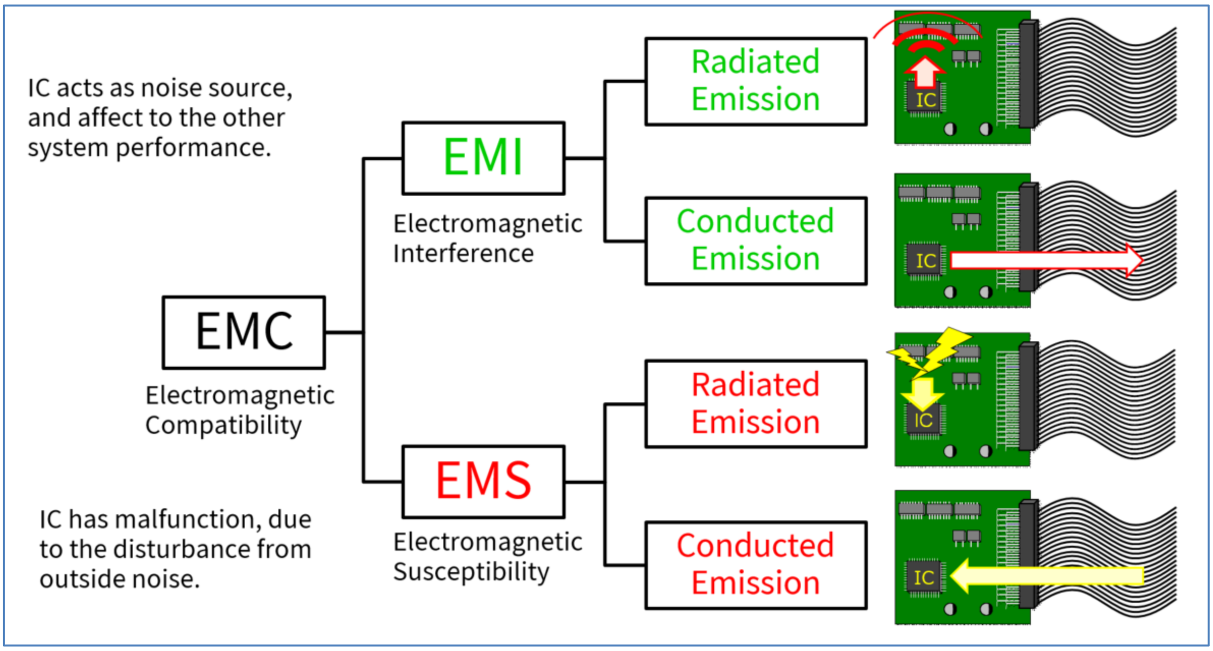


Figure 5-2 EMC Definition

5.3. EMC standards and standardization organization

In order to guarantee EMC performance, many countries and regions have been enacting the EMC regulations. In order to sell products in these countries and regions, these EMC regulations must be satisfied and certified. In the EMC regulations, international standards are referenced as test methods to measure EMC performance.

International Standards are assumed to be standardized to measure EMC performance with accuracy and repeatability, and to be used as a common guideline by following it.

EMC international standards for electrical and electronic systems are deliberated and standardized by the following international standardization organizations. To test following these standards, the EMC measurement results can be accepted by many countries and regions. In addition, these standards define the test condition and setup, it can be recognized which test methods have been applied.

IECs (International Electrotechnical Commission)
CISPR (Comite International Special des Peturbations Radio-electiques)
ISO (International Organization for Standardization)

In addition, IEC has established the following classification for the preparation of EMC standards.

Basic Standards Terminology, Electromagnetic Environment Classification, General Requirements for Emission and Immunity, Common Measurements, testing methods, etc. are specified.
Common Standards Emission and immunity test levels, values etc. for all products in a particular environment is specified.
Specific product Standards EMC test methods and level values for specific product groups, such as information equipment, home appliances, etc. are specified.
Product Standards EMC test methods and level values for specific products. EMC test methods and level values for specific product are specified.

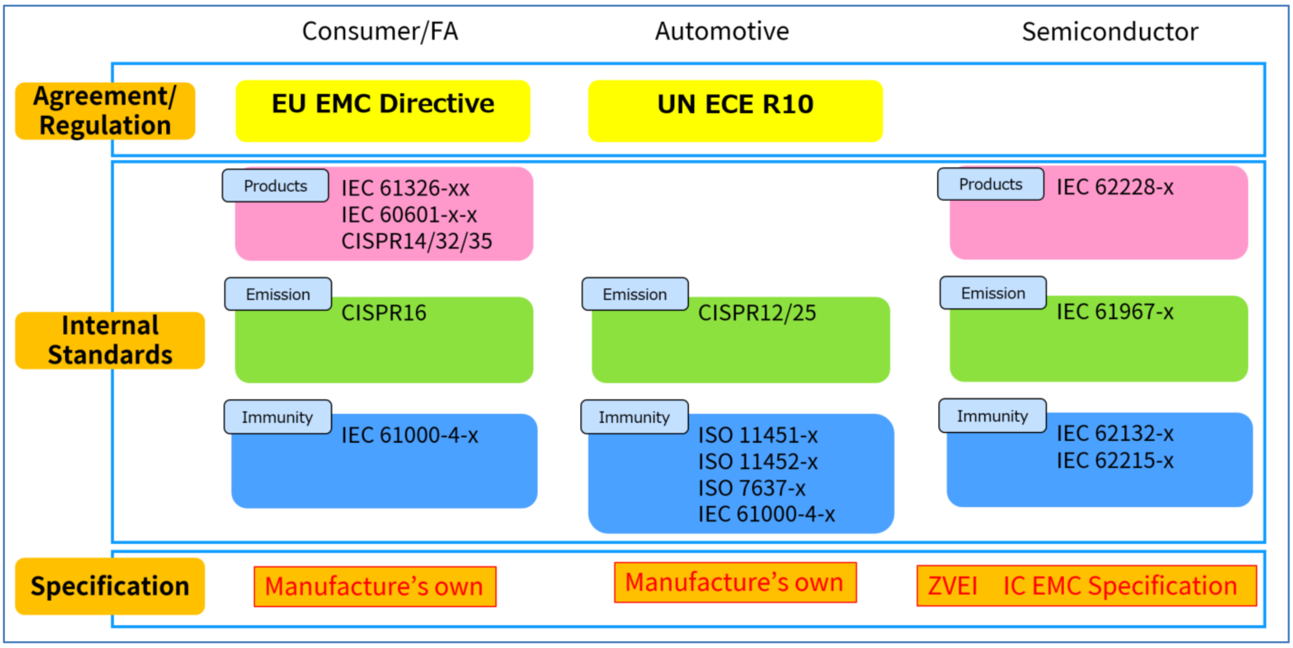


Figure 5-3 EMC standards

5.4. EMC International Standard for Product Lineup

For example, EMC requirements for electrical equipment for measurement, control, and laboratory use (such as factory automation equipment) are specified by IEC 61326-1 in terms of scope of application, test items, test levels, performance evaluation standards, etc. In this standard, the basic standards for measuring methods of immunity are referenced.

Emission requirements, measurement methods and limits are also standardized by CISPR32 are specified.

The following test methods are referenced in this standard:

Table 5-1 EMC-testing standards referred in IEC 61326

Part	Type	Name
IEC 61000-3-2 :2018	Limit	Limits for harmonic current emissions (equipment input current ≤16 A per phase)
IEC 61000-3-3 :2013	Limit	Limitation of voltage changes, voltage fluctuations and flicker in low-voltage supply systems, for equipment with rated current ≤16 A per phase and not subject to conditional connection
IEC 61000-3-11 : 2017	Limit	Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems, -Equipment with rated current ≤75 A and subject to conditional connection
IEC 61000-3-12 : 2011	Limit	Limits for harmonic currents produced by equipment connected to public low-voltage systems with input current > 16 A and ≤75 A per phase
IEC 61000-4-2 :2008	ESD	Testing and measurement techniques –Electrostatic discharge immunity test
IEC 61000-4-3 :2006	Radiated	Testing and measurement techniques –Radiated, radio-frequency, electromagnetic field immunity test
IEC 61000-4-4 :2012	Conducted	Testing and measurement techniques Electrical fast transient/burst immunity test
IEC 61000-4-5 :2014	Conducted	Testing and measurement techniques –Surge immunity test
IEC 61000-4-6 :2013	Conducted	Testing and measurement techniques –Surge immunity test
IEC 61000-4-8 :2009	Conducted	Testing and measurement techniques – Power frequency magnetic field immunity test
IEC 61000-4-11 :2020	Conducted	Testing and measurement techniques – Voltage dips, short interrupt and voltage variations immunity tests for equipment with input current up to 16 A per phase
CISPR11:2015	Limit	Industrial, scientific and medical equipment –Radio-frequency disturbance characteristics – Limits and methods of measurement

5.5. EMC standards for semiconductors

As EMC countermeasures for electronic equipment become difficult year by year, semiconductors become noise sources and malfunction factors, EMC measurement methods for semiconductors themselves are being standardized in response to the need to quantify and compare the performance of individual semiconductors.

EMC standards for semiconductors do not specify limits for testing, and no requirement by the regulations. The purposes of these standards are to define conditions and measurement methods for ensuring reproducibility of EMC measurements on a single semiconductor, and assume a role as an object to compare the performance of multiple semiconductors.

On the other hand, EMC testing with application level by the user, evaluate to meet with the local regulation and/or internal standard. If the violation or problem happened at this evaluation, it may cause of the delay of mass production or product launch. Since it requires the root cause analysis, countermeasure planning and PCB re-design.

Even though, customer knows the EMC characteristics of semiconductor EMC at the early design stage of the application, it is utilized to use this result for the PCB design with the EMC countermeasure. It may be possible to reduce the EMC risk a lot during the Application design, using the semiconductor which has known EMC characteristics.

And it is noted that semiconductor EMC evaluation results with the different condition (i.e. evaluation board, methods) from the application level, EMC results with application level are determined by the combination of the noise propagation path and EMC characteristics of application level and/or semiconductor which is Noise source or Noise recipients.

- Emission measuring method (IEC 61967 series. (Table 5-2))
- Immunity measuring method (IEC 62132 series. (Table 5-3))
- Impulse immunity measuring method (IEC 62215 series. (Table 5-4))

Table 5-2 IEC 61967 Series Integrated Circuit Immunity Measurements

Part	Type	Name	Status
1	General	General conditions and definitions	IS, Ed2.0, 2018
1－1	General	General conditions and definitions -Near-field scan data exchange format	TR, Ed2.0, 2015
2	Radiated	TEM cell and wideband TEM cell method（150kHz to 1GHz)	IS, Ed1.0, 2005
3	Radiated	Surface scan method	TS, Ed2.0, 2014
4	Conducted	1Ω/150Ω direct coupling method	IS, Ed2.0, 2021
4－1	General	1Ω/150Ω direct coupling method (150kHz to 1GHz) - Application guidance to IEC 61967-4	TR, Ed1.0, 2005
5	Conducted	Workbench Faraday Cage method（150kHz to 1GHz）	IS, Ed1.0, 2003
6	Conducted	Magnetic probe method（150kHz to 1GHz）	IS, Ed1.1, 2008
8	Radiated	IC stripline method	IS, Ed1.0, 2011

As of Jan/2023

Table 5-3 IEC 62132 Series Integrated Circuit Emission Measurements

Part	Type	Name	Status
1	General	General conditions and definitions	IS, Ed2.0, 2015
2	Radiated	TEM cell and wideband TEM cell method	IS, Ed1.0, 2010
4	Conducted	DPI (Direct RF Power injection) method（150kHz to 1GHz）	IS, Ed1.0, 2006
5	Conducted	Workbench Faraday Cage method（150kHz to 1GHz）	IS, Ed1.0, 2005
8	Radiated	IC stripline method	IS, Ed1.0, 2012
9	Radiated	Surface scan method	TS, Ed1.0, 2014

As of Jan/2023

Table 5-4 IEC 62215 Series Integrated Circuit Impulse Immunity Measurements

Part	Type	Name	Status
2	Conducted Pulse	Synchronous transient injection method	TS, Ed1.0, 2007
3	Conducted Pulse	Non-synchronous transient injection method	IS, Ed1.0, 2013

As of Jan/2023

IS: International Standard
TS: Technical Specification

Some integrated circuit emission measurement methods are described below.

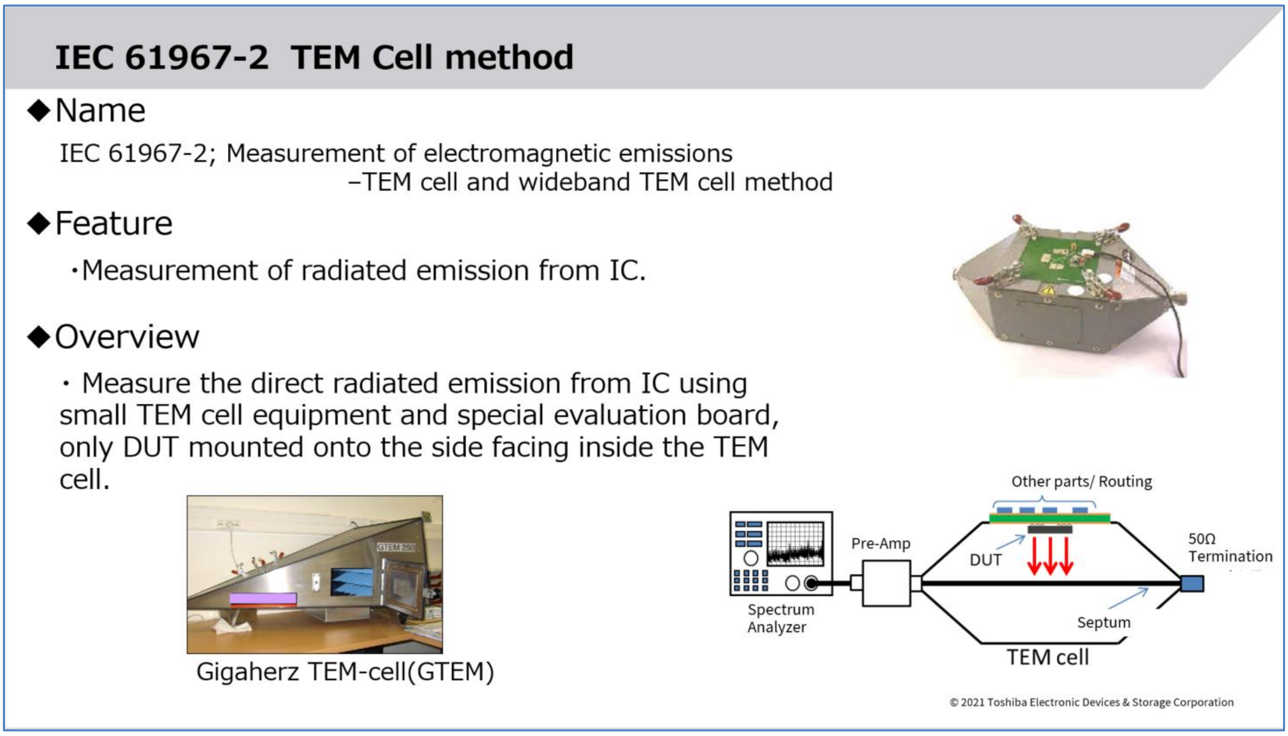


Figure 5-4 Radiated Emission TEM Cell Method

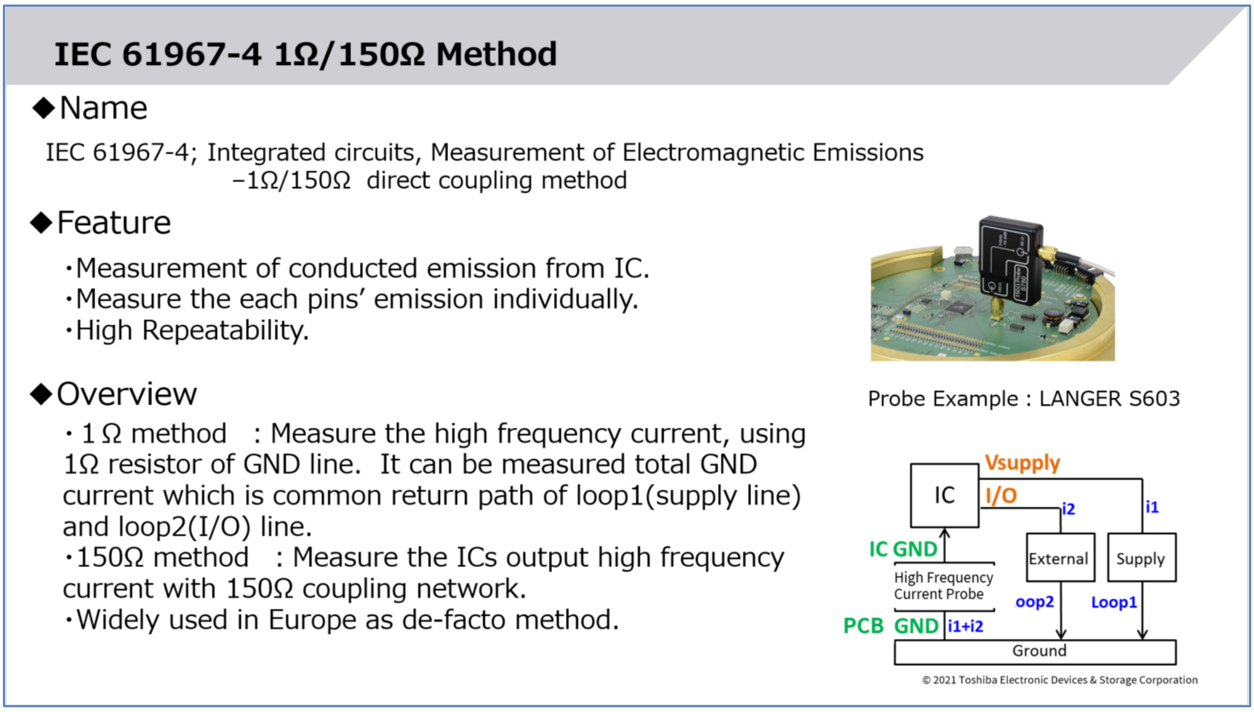


Figure. 5-5 Conducted emission 1 Ω/150 Ω method

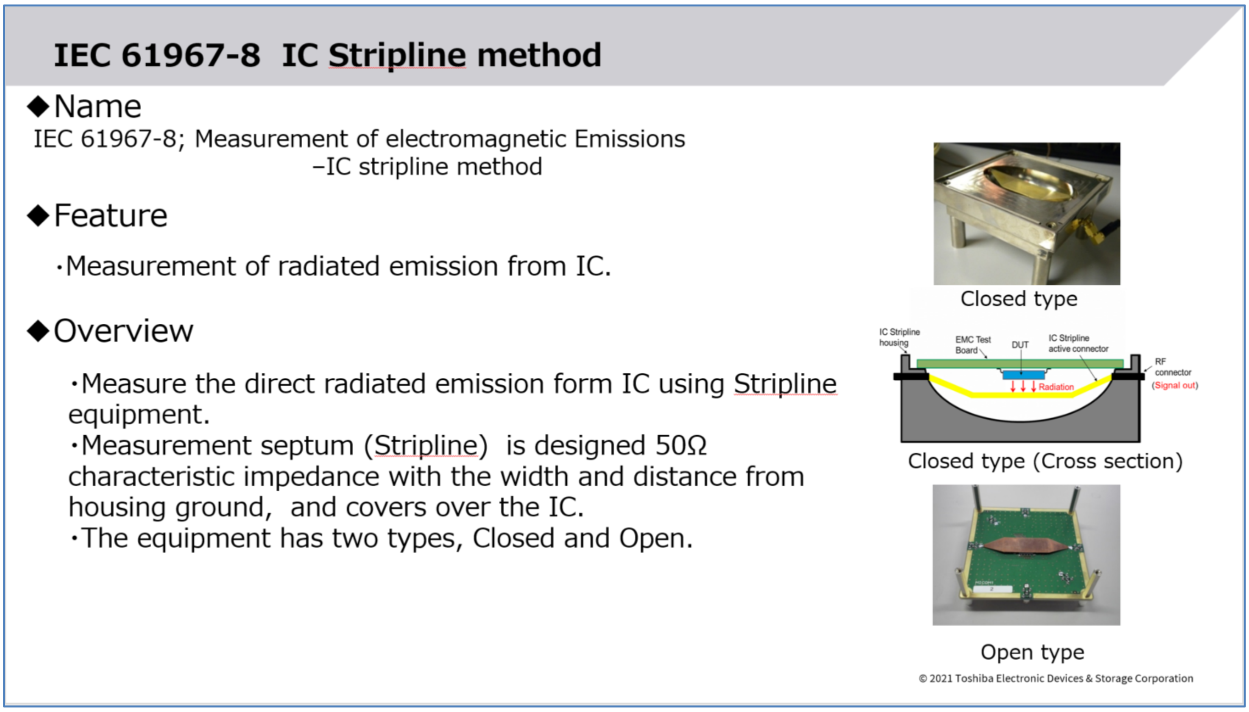


Figure 5-6 Radiated Emission IC Stripline Method

Some integrated circuit electromagnetic immunity measurement methods are described below.

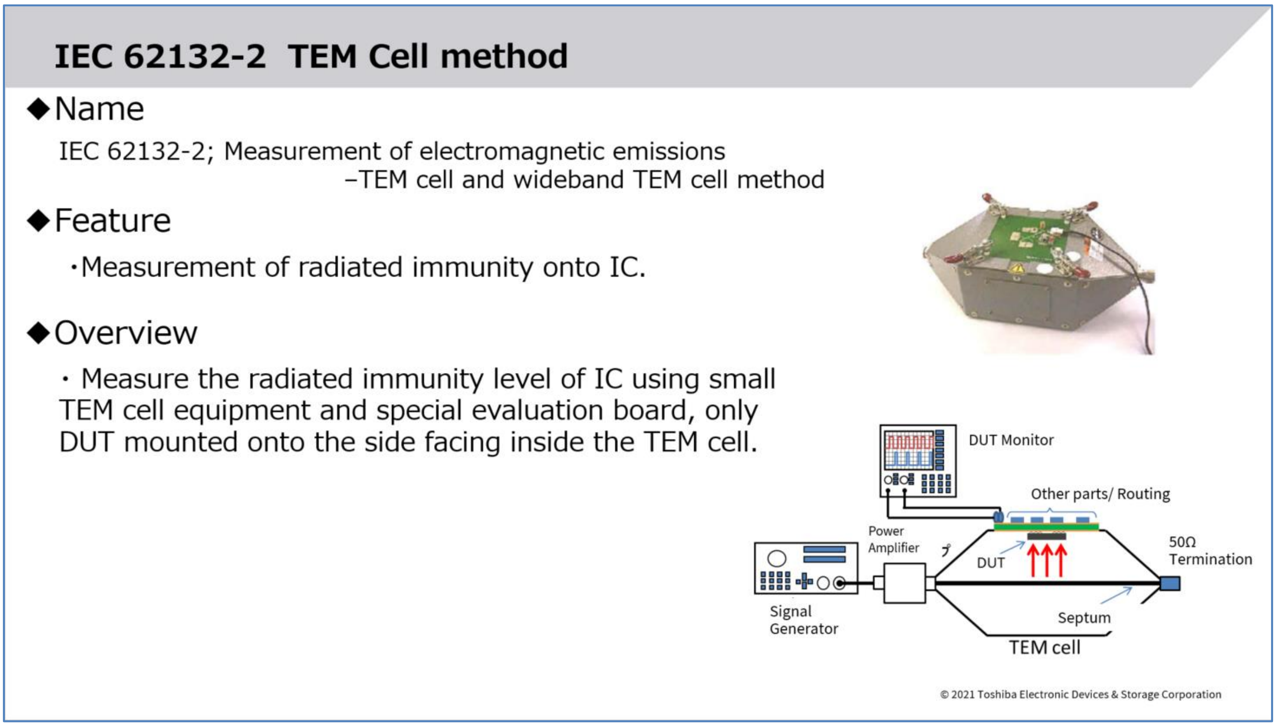


Figure 5-7 Radiated Immunity TEM Cell Method

IEC 62132-4 DPI Method

◆Name

IEC 62132-4; Measurement of electromagnetic Immunity
–Direct Power Injection (DPI) method

◆Feature

・Evaluate the IC malfunction level, applying the disturbance using the capacitive coupling.
・Measure the each pins' immunity level individually.
・High Repeatability.

◆Overview

・Widely used in Europe as de-facto method.
・Direct apply the continuous wave and modulated wave into the each pin, and check the level when the malfunction occurs.

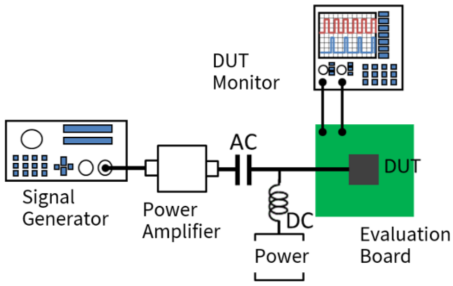


Figure 5-8 Conducted Immunity DPI Method

IEC 62132-8 IC Stripline method

◆Name

IEC 62132-8; Measurement of electromagnetic Emissions
–IC stripline method

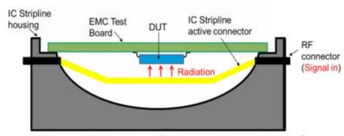
◆Feature

・Measurement of radiated immunity into IC.

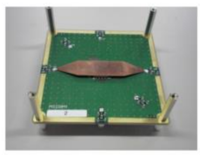
◆Overview

・Measure the immunity level using Stripline equipment.
・Measurement septum (Stripline) is designed 50Ω characteristic impedance with the width and distance from housing ground, and covers over the IC.
・The equipment has two types, Closed and Open.

Closed type



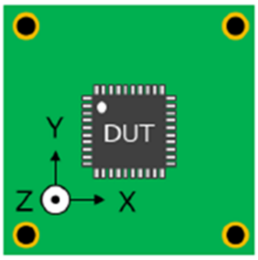
Closed type (Cross section)



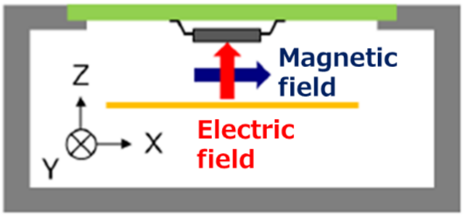
Open type

Figure 5-9 Radiated Immunity IC Stripline Method

With the Radiated immunity, IC stripline method（IEC 62132-8）, the electric field as disturbance is injected along the Z-direction.　In addition, it should be assumed that the magnetic field as disturbance is injected from the power rail or harness, which are placed nearby, considering the real design. So on top of IC stripline method, the evaluation of immunity to magnetic field should be considered.



(a) EMC Evaluation board



(b) Direction of electric field during IEC62132-8 test

Figure 5-10 Distribution of Electric and Magnetic fields during test (IEC 62132-8)

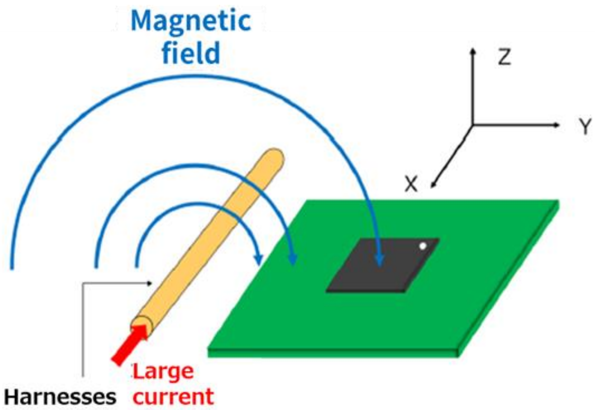


Figure 5-11 Layout example Magnetic field disturbance injection along Z direction

For magnetic field immunity test, IEC 61000-4-8 (Testing and Measurement Techniques – Power Frequency Magnetic Field Immunity Test) is available. Since this method will apply onto whole equipment, the loop antenna coil is too large versus IC package. Therefore, this method is not proper way to apply semiconductor itself. To improve the EMC robustness, it will be required to establish the test methodology of magnetic field immunity test only for the IC itself.

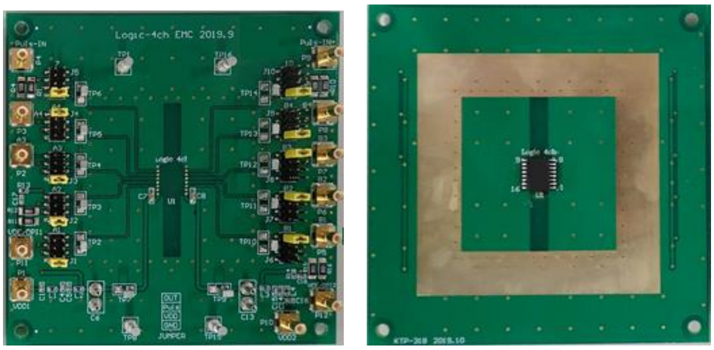
6. EMC measurement results

6.1. EMC measurement boards

Figure6-1 is the example of EMC measurement boards. The other components except the IC being evaluated and wiring are placed the side, to measure the radiated emission and immunity only IC itself. This follows the measurement board definition by IEC 61967-1 and IEC 62132-1. As described on clause 4.7, for the evaluation board of the Digital Isolator IC, no component and pattern are placed underneath of the IC to have the insulation. Therefore, these measurement boards have the slit under the IC. This slit may act as the radiation antenna in some frequency range, so the evaluation with these boards are harder condition.

On the other hand, the evaluation board for CISPR32 does not follow the IEC standards, since this evaluation is for the application level.

<IEC 62132-8 IC Stripline immunity Evaluation Board>



<CISPR32 emission Evaluating Board>

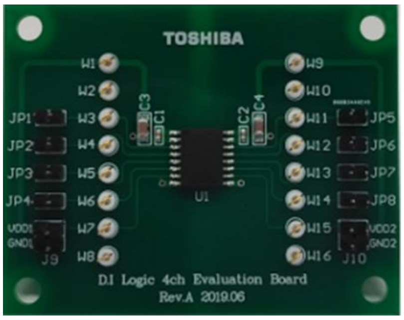


Figure 6-1 Measurement boards

6.2. Immunity measurement

The result of IEC 62132-8 IC Stripline method (radiated immunity) is shown in Fig. 6-2. Immunity results shows the maximum disturbance level not to occur the malfunction at the each frequency. It means that upper plots mean the good immunity characteristics.

DCL54xxxx has no malfunction up to 800 V/m noise injection between 150kHz and 1GHz, which is compliant with class 3 of BISS specification.*

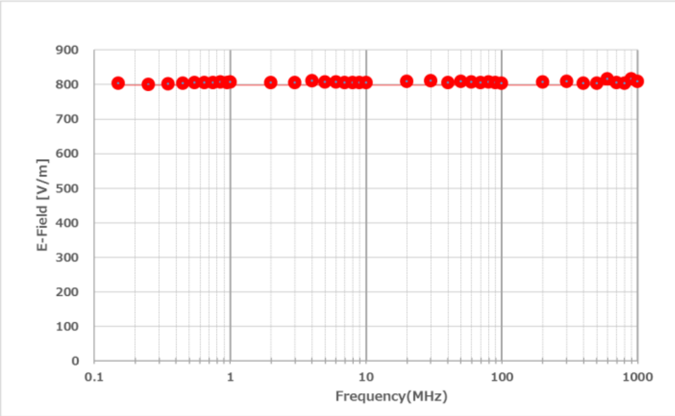


Figure 6-2 Measurement results of Radiated Immunity IC Stripline Method

※The most stringent classification for automotive semiconductor by the specifications for IC EMC testing formulated by Bosch, Infineon and Siemens (now Continental)

6.3. Emission measurement (near field)

The result of IEC 61967-8 IC Stripline (Radiation Emission) method is shown in Fig. 6-3.

DCL54xx01 has the emission level between 150kHz and 1GHz, which is compliant with class 1 of BISS specification.

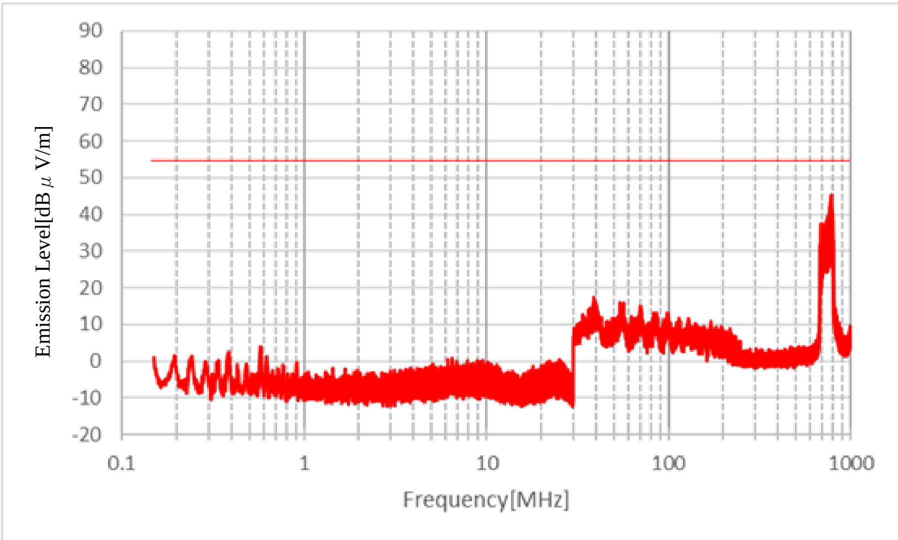
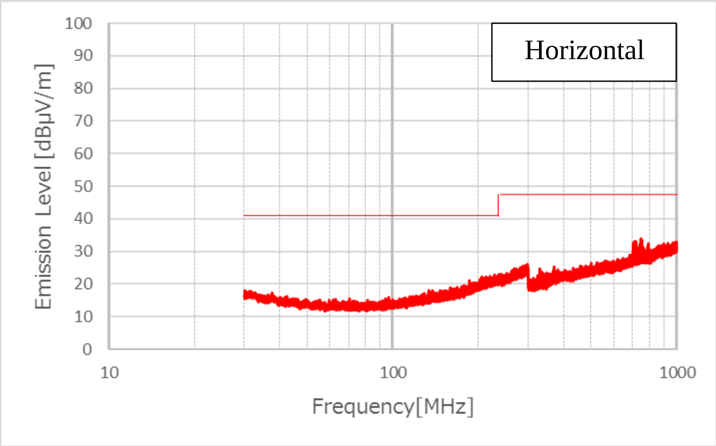


Figure 6-3 Measurement results of Radiated Emission IC Stripline Method

※The classification for automotive semiconductor by the specifications for IC EMC testing formulated by Bosch, Infineon and Siemens (now Continental)

6.4. Emission measurement (far field)

The result of CISPR32 is shown in Fig. 6-4.　DLC54xx01 has a margin of 10dB or more between 30MHz to 1GHz, is ensured for Class B*.



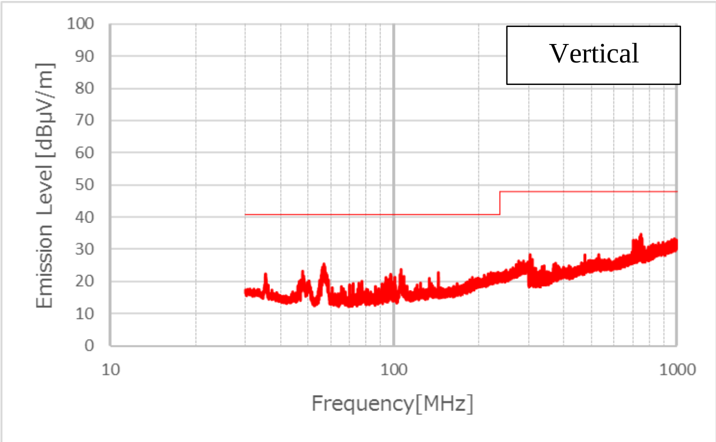


Figure 6-4 Measurement results of Radiated Emission 3m Method

※The more stringent classification for the equipment that are marketed for use in home.

Reference international standard

IEC 61326-1: 2020, Electrical equipment for measurement, control and laboratory use – EMC requirements –Part1: General Requirements

IEC 60050 (all parts),International Electrotechnical Vocabulary

IEC 61000-3-2: 2005, Electromagnetic compatibility (EMC)-Part 3-2: Limits−Limits for harmonic current emissions (equipment input current ≤ 16 A per phase), Amendment 1:2008 and Amendment 2:2009

IEC 61000-4-2:2008,Electromagnetic compatibility (EMC)−Part 4-2: Testing and measurement techniques−Electrostatic discharge immunity test

IEC 61000-4-3: 2006, Electromagnetic compatibility (EMC)-Part 4-3: Testing and measurement techniques−Radiated, radio-frequency, electromagnetic field immunity test,Amendment 1:2007 and Amendment 2:2010

IEC 61000-4-4: 2004, Electromagnetic compatibility (EMC)-Part 4-4: Testing and measurement techniques−Electrical fast transient/burst immunity test and Amendment 1:2010

IEC 61000-4-5:2005,Electromagnetic compatibility (EMC)−Part 4-5: Testing and measurement techniques−Surge immunity test

IEC 61000-4-6:2008,Electromagnetic compatibility (EMC)−Part 4-6: Testing and measurement techniques−Immunity to conducted disturbances, induced by radio-frequency fields

IEC 61000-4-8:2009,Electromagnetic compatibility (EMC)−Part 4-8: Testing and measurement techniques−Power frequency magnetic field immunity test

IEC 61000-4-11:2004,Electromagnetic compatibility (EMC)−Part 4-11: Testing and measurement techniques−Voltage dips, short interruptions and voltage variations immunity tests

CISPR 11: 2009, Industrial, scientific and medical equipment−Radio-frequency disturbance characteristics−Limits and methods of measurement and Amendment 1:2010

IEC 61967-1:2018, Integrated circuits - Measurement of electromagnetic emissions – Part1: General conditions and definitions

IEC/TR 61967-1-1:2015, Integrated circuits - Measurement of electromagnetic emissions - Part: General conditions and definitions –Near field scan data exchange format

IEC 61967-2:2005, Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 2: Measurement of radiated emissions - TEM cell and wideband TEM cell method

IEC 61967-3:2014, Integrated circuits - Measurement of electromagnetic emissions – Part3: Measurement of radiated emissions – Surface scan method

IEC 61967-4:2021, Integrated circuits - Measurement of electromagnetic emissions – Part4: Measurement of conducted emissions – 1ohm/150ohm direct coupling method

IEC/TR 61967-4-1:2005, Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part4-1: Measurement of conducted emissions -1ohm/150ohm direct coupling method –Application guidance to IEC 61967-4

IEC 61967-5:2003, Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part5: Measurement of conducted emissions – Workbench Faraday Cage method

IEC 61967-6:2008, Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part6: Measurement of conducted emissions – Magnetic probe method

IEC 61967-8:2011, Integrated circuits - Measurement of electromagnetic emissions – Part8: Measurement of radiated emissions – IC stripline method

IEC 62132-1:2015, Integrated circuits - Measurement of electromagnetic immunity – Part1: General conditions and definitions

IEC 62132-2:2010, Integrated circuits - Measurement of electromagnetic immunity - Part 2: Measurement of radiated immunity - TEM cell and wideband TEM cell method

IEC 62132-4:2006, Integrated circuits - Measurement of electromagnetic immunity – Part4: Measurement of conducted immunity – Direct RF power injection method

IEC 62132-5:2005, Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1 GHz – Part5: Measurement of conducted immunity – Workbench Faraday Cage method

IEC 62132-8:2012, Integrated circuits - Measurement of electromagnetic immunity – Part8: Measurement of radiated immunity – IC stripline method

IEC 62132-9:2014, Integrated circuits - Measurement of electromagnetic immunity – Part9: Measurement of conducted emissions – Surface scan method

IEC/TS 62215-2:2007, Integrated circuits - Measurement of impulse immunity – Part2: Synchronous transient injection method

IEC 62215-3:2013, Integrated circuits - Measurement of impulse immunity – Part3: Non-synchronous transient injection method

Changelog

Version	Date	Content of change
Rev. 1.0	28th Jan. 2022	First edition
Rev. 2.0	24th Mar. 2023	5-5 EMC standards for semiconductors Added about magnetic field immunity 6-1 EMC measurement boards Added description of evaluation board

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