

TC74AC166F

1. Functional Description

- 8-Bit Shift Register (P-IN, S-OUT)

2. General

The TC74AC166F is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

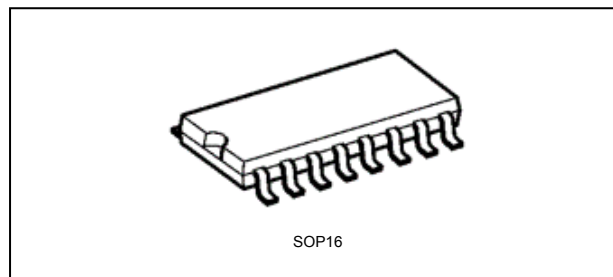
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/LOAD input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

- (1) High speed: $f_{MAX} = 150 \text{ MHz (typ.)}$ at $V_{CC} = 5.0 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$
- (2) Low power dissipation: $I_{CC} = 8.0 \mu\text{A (max)}$ at $T_a = 25 \text{ }^\circ\text{C}$
- (3) High noise immunity: $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (min)}$
- (4) Output current: $|I_{OH}|/I_{OL} = 24 \text{ mA (min)}$ ($V_{CC} = 4.5 \text{ V}$)
- (5) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- (6) Wide operating voltage range: $V_{CC(opr)} = 2.0 \text{ V to } 5.5 \text{ V}$
- (7) Pin and function compatible with 74F166

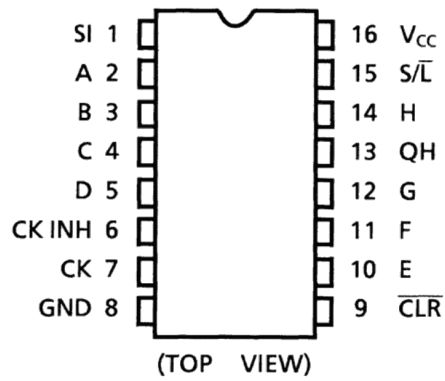
4. Packaging



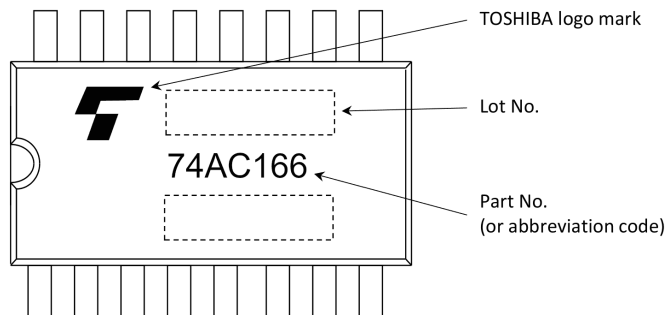
Start of commercial production

1988-10

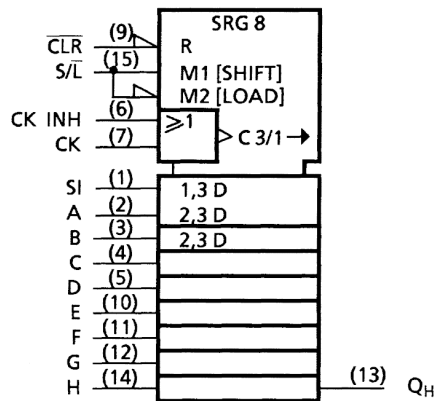
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



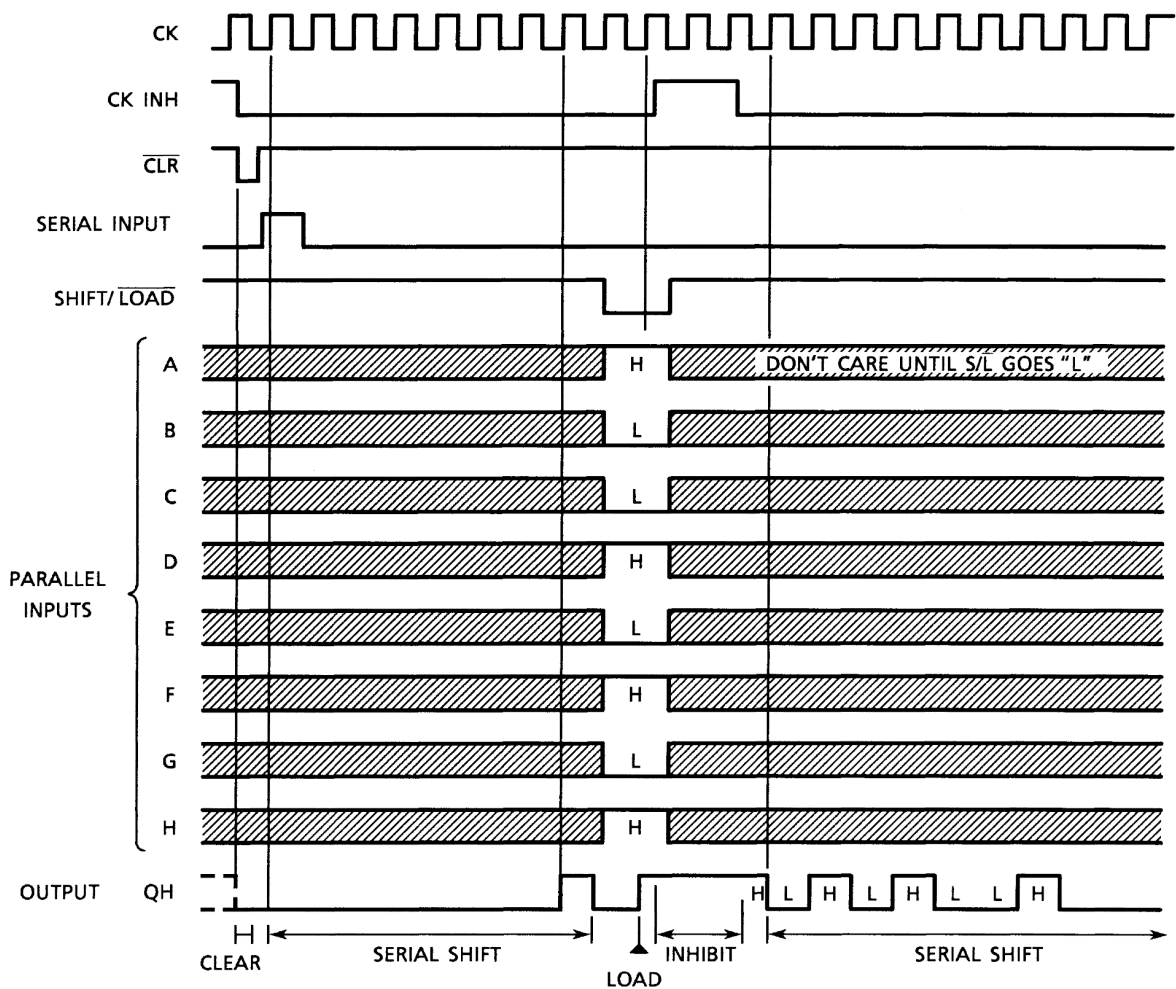
8. Truth Table

Inputs						Internal Output		Output
CLR	SHIFT/LOAD	CK INH.	CK	SERIAL IN	PARALLEL A.....H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	X		X	X	No Change		
H	L	L		X	a.....h	a	b	h
H	H	L		H	X	H QAn		QGn
H	H	L		L	X	L QAn		QGn
H	X	H	X	X	X	No Change		

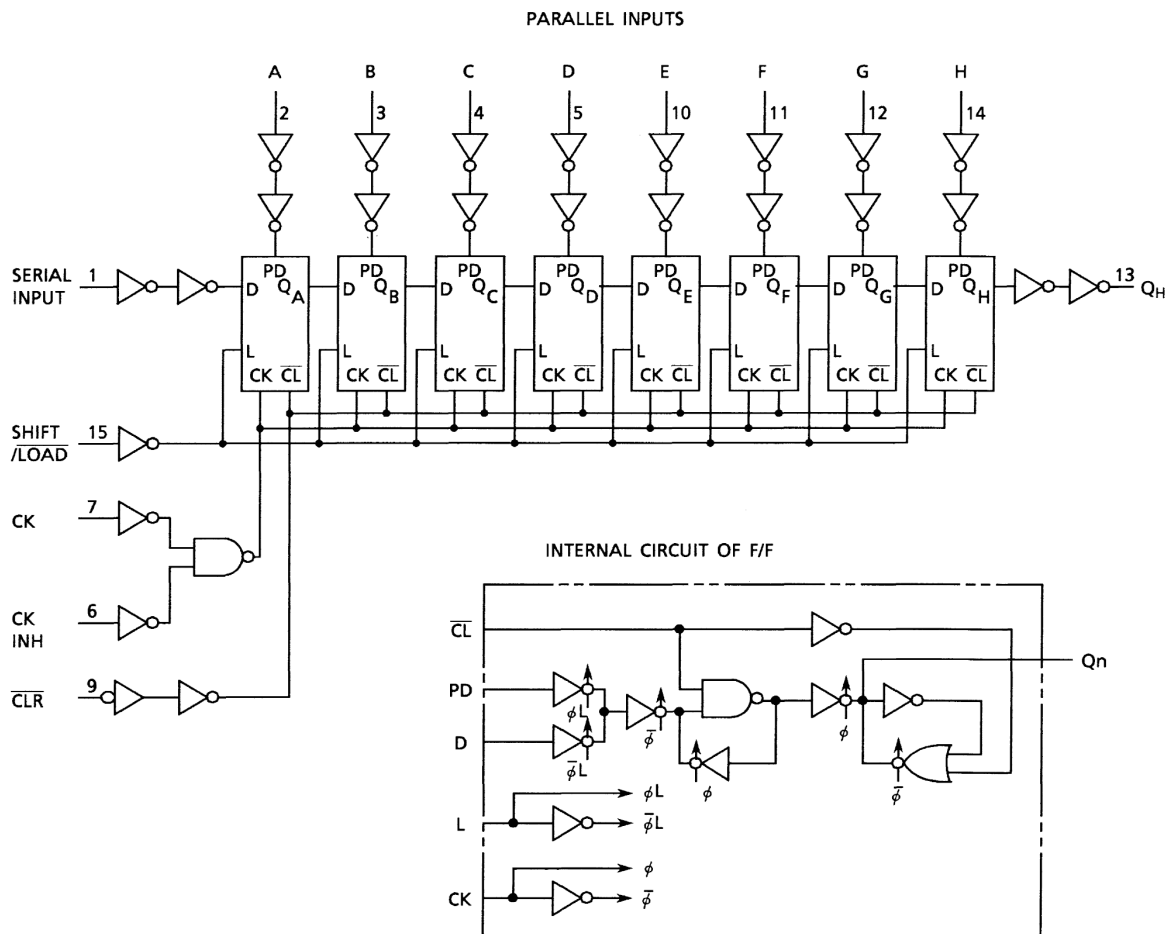
X :Don't care

a . . . h: The level of steady state input voltage at inputs A through H respectively.

9. Timing Diagrams



10. System Diagram



11. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±50	mA
Output current	I_{OUT}	±50	mA
V_{CC} /ground current	I_{CC}	±100	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

12. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}	—	2.0 to 5.5	V
Input voltage	V_{IN}	—	0 to V_{CC}	V
Output voltage	V_{OUT}	—	0 to V_{CC}	V
Operating temperature	T_{opr}	—	-40 to 85	°C
Input rise and fall times	dt/dv	$V_{CC} = 3.3 \pm 0.3$ V	0 to 100	ns/V
		$V_{CC} = 5.0 \pm 0.5$ V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

13. Electrical Characteristics

13.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit	
High-level input voltage	V_{IH}	—	2.0	1.50	—	—	V	
			3.0	2.10	—	—		
			5.5	3.85	—	—		
Low-level input voltage	V_{IL}	—	2.0	—	—	0.50	V	
			3.0	—	—	0.90		
			5.5	—	—	1.65		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
			$I_{OH} = -4\text{ mA}$	4.5	4.4	4.5	—	
				$I_{OH} = -24\text{ mA}$	3.0	2.58	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 12\text{ mA}$	3.0	—	—	0.36	
				$I_{OL} = 24\text{ mA}$	4.5	—	—	
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	μA	

13.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Note	V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				3.0	2.10	—	
				5.5	3.85	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				3.0	—	0.90	
				5.5	—	1.65	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
			$I_{OH} = -4\text{ mA}$	4.5	4.4	—	
				$I_{OH} = -24\text{ mA}$	3.0	2.48	
			$I_{OH} = -75\text{ mA}$ (Note 1)	4.5	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 12\text{ mA}$	3.0	—	0.44	
				$I_{OL} = 24\text{ mA}$	4.5	—	
			$I_{OL} = 75\text{ mA}$ (Note 1)	5.5	—	1.65	
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND		5.5	—	± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	80.0	μA

Note 1: This spec indicates the capability of driving $50\text{ }\Omega$ transmission lines.
One output should be tested within a 10 ms maximum duration.

13.3. Timing Requirements

(Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	3.3 ± 0.3	7.0	ns
		5.0 ± 0.5	5.0	
Minimum pulse width (CLR)	$t_{w(L)}$	3.3 ± 0.3	8.0	ns
		5.0 ± 0.5	5.0	
Minimum setup time (SI, PI)	t_s	3.3 ± 0.3	8.0	ns
		5.0 ± 0.5	4.0	
Minimum setup time (S/\bar{L})	t_s	3.3 ± 0.3	7.0	ns
		5.0 ± 0.5	4.0	
Minimum hold time (SI, PI)	t_h	3.3 ± 0.3	0.5	ns
		5.0 ± 0.5	0.5	
Minimum hold time (S/\bar{L})	t_h	3.3 ± 0.3	1.0	ns
		5.0 ± 0.5	1.0	
Minimum removal time (CLR)	t_{rem}	3.3 ± 0.3	4.0	ns
		5.0 ± 0.5	1.5	

13.4. Timing Requirements

(Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	3.3 ± 0.3	7.0	ns
		5.0 ± 0.5	5.0	
Minimum pulse width (CLR)	$t_{w(L)}$	3.3 ± 0.3	8.0	ns
		5.0 ± 0.5	5.0	
Minimum setup time (SI, PI)	t_s	3.3 ± 0.3	8.0	ns
		5.0 ± 0.5	4.0	
Minimum setup time (S/\bar{L})	t_s	3.3 ± 0.3	7.0	ns
		5.0 ± 0.5	4.0	
Minimum hold time (SI, PI)	t_h	3.3 ± 0.3	0.5	ns
		5.0 ± 0.5	0.5	
Minimum hold time (S/\bar{L})	t_h	3.3 ± 0.3	1.0	ns
		5.0 ± 0.5	1.0	
Minimum removal time (CLR)	t_{rem}	3.3 ± 0.3	4.0	ns
		5.0 ± 0.5	1.5	

13.5. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Propagation delay time (CK-QH)	t_{PLH}, t_{PHL}		$C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$	3.3 ± 0.3	—	9.4	16.1	ns
				5.0 ± 0.5	—	6.6	10.0	
Propagation delay time (CLR-QH)	t_{PHL}		$C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$	3.3 ± 0.3	—	9.2	15.2	ns
				5.0 ± 0.5	—	6.4	9.6	
Maximum clock frequency	f_{MAX}		$C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$	3.3 ± 0.3	55	105	—	MHz
				5.0 ± 0.5	90	150	—	
Input capacitance	C_{IN}		—	—	5	10	pF	
Power dissipation capacitance	C_{PD}	(Note 1)	—	—	67	—	pF	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

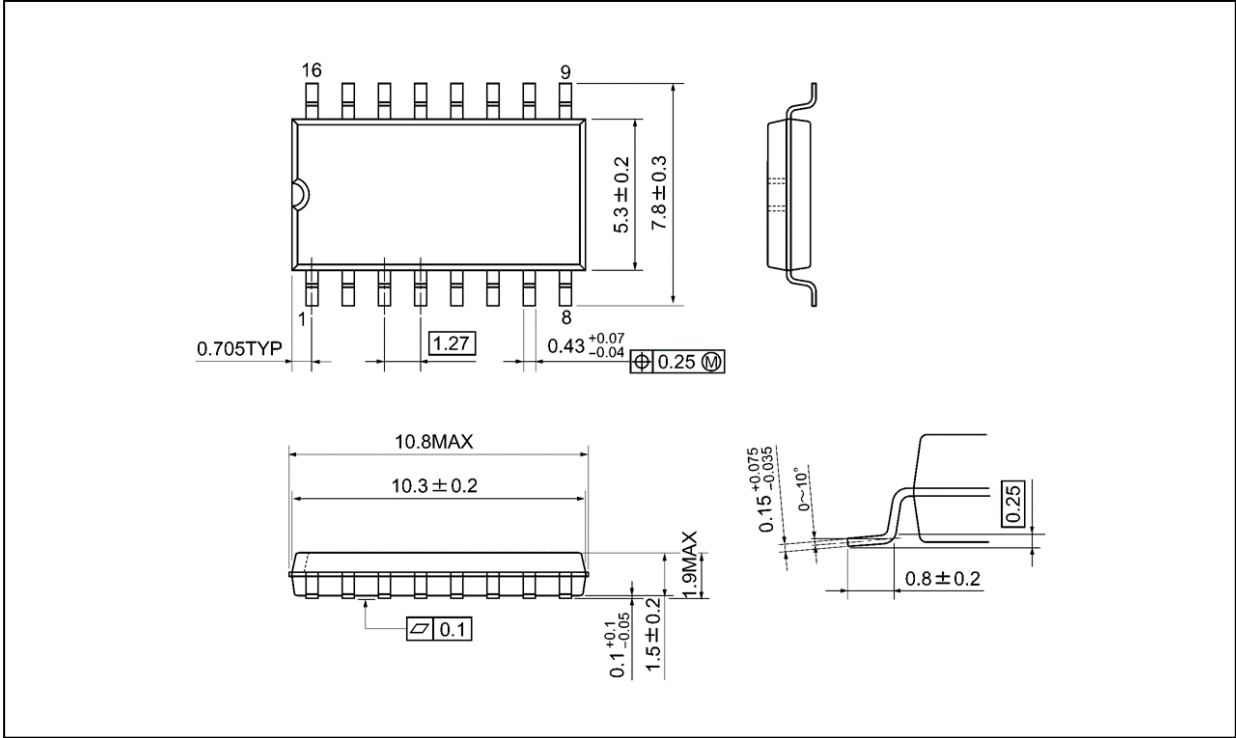
$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$

13.6. AC Characteristics (Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (CK-Q)	t_{PLH}, t_{PHL}	$C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$	3.3 ± 0.3	1.0	18.3	ns
			5.0 ± 0.5	1.0	11.4	
Propagation delay time (CLR-Q)	t_{PHL}	$C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$	3.3 ± 0.3	1.0	17.4	ns
			5.0 ± 0.5	1.0	10.9	
Maximum clock frequency	f_{MAX}	$C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$	3.3 ± 0.3	55	—	MHz
			5.0 ± 0.5	90	—	
Input capacitance	C_{IN}	—	—	—	10	pF

Package Dimensions

Unit: mm



Weight: 0.18 g (typ.)

Package Name(s)
Nickname: SOP16

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