Photocouplers Infrared LED & Photo IC

TLP5222

1. Applications

- Isolated gate drive for IGBT / Power MOSFET
- Industrial Inverters
- AC Servos
- Photovoltaic (PV) Inverters
- Uninterruptible Power Supply (UPS)

2. General

The TLP5222 is a highly integrated and multi-functional gate driver photocoupler with 2.5 A output current housed in a long creepage and clearance SO16L package.

The TLP5222, a smart gate driver photocoupler, includes functions of desaturation detection, isolated FAULT status feedback, soft gate turn-off, active Miller clamp, under voltage lockout (UVLO) and automatic FAULT status reset.

The TLP5222 consists of two infrared light-emitting diodes (LEDs) and two high-gain and high-speed photo-detector ICs. They realize high current, high-speed output control and FAULT status feedback with electrical isolation between a primary side and secondary side.

3. Features

(1)	Peak output current	: ± 2.5 A (max)
(2)	Operating temperature	: − 40 to 110 °C
(3)	Power supply voltage	: 15 to 30 V
(4)	Threshold input current	: 6 mA (max)
(5)	Supply current	: 5 mA (max)
(6)	Propagation delay time	: 250 ns (max)
(7)	DESAT leading edge blanking time	: 1.4 μs (typ.)
(8)	DESAT mute time	: 25.5 μs (typ.)
(9)	Common-mode transient immunity	: ± 25 kV/μs (min)
(10)	Isolation voltage	: 5000 Vrms (min)
(11)	Safety standards	

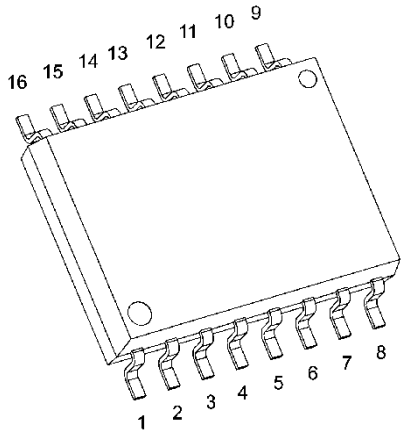
UL approved : UL1577, File No. E67349
cUL approved : CSA Component Acceptance Service No. 5A File No. E67349
VDE approved : EN 60747-5-5, EN 62368-1 (Note 1)
CQC approved : GB4943.1, GB8898 Japan Factory

仅适用于海拔 2000m 以下地区安全使用

Note 1: When a VDE approved type is needed, please designate the Option (D4).

Start of commercial production
2022-07

4. Packaging and Pin Assignment



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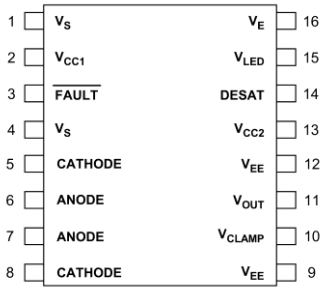
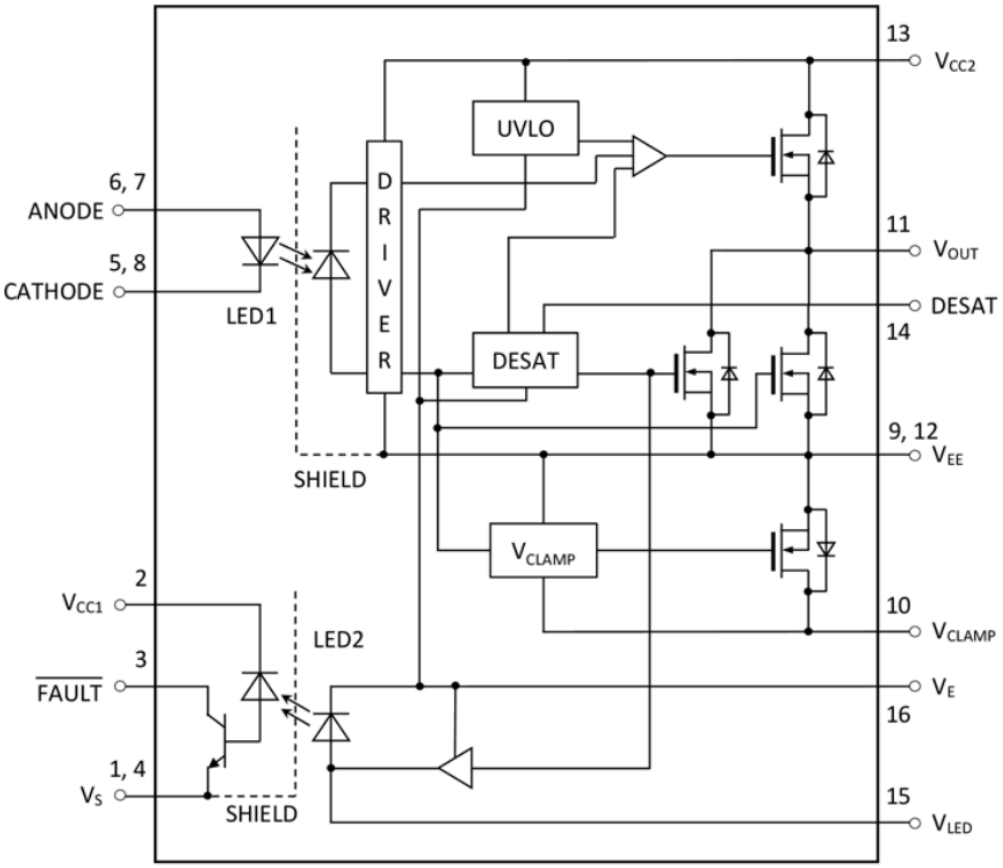


4.1. Pin Description

Pin No.	Symbol	Description
1	V_S	Input side Ground terminal
2	V_{CC1}	Input side Power Supply terminal
3	$\overline{FAULT}$	Fault Output terminal
4	V_S	Input side Ground terminal
5	CATHODE	LED Cathode terminal
6	ANODE	LED Anode terminal
7	ANODE	LED Anode terminal
8	CATHODE	LED Cathode terminal
9	V_{EE}	Output side Negative Power Supply terminal
10	V_{CLAMP}	Miller current Clamp terminal
11	V_{OUT}	Output terminal
12	V_{EE}	Output side Negative Power Supply terminal
13	V_{CC2}	Output side Positive Power Supply terminal
14	DESAT	Desaturation monitor terminal
15	V_{LED}	Not connect, for testing only
16	V_E	Common terminal

5. Internal Circuit (Note)



Note : Bypass capacitors (1 μF) must be connected between pin 13 (V_{CC2}) and 16 (V_E) to stabilize the operation of the high gain linear amplifier. When $V_E - V_{EE} > 0$ V (with negative gate drive), another bypass capacitor (1 μF) must be connected between pin 9 or 12 (V_{EE}) and 16 (V_E). Failure to provide the bypassing may impair the switching property. The total lead length between each capacitor and the coupler should not exceed 1 cm.

6. Principal of Operation

6.1 Truth table

Input Current (I_F)	Output side Positive Power Supply (V_{CC2} - V_E)	DESAT Monitor (Pin 14 input)	FAULT Output (Pin 3 output)	Output Voltage (Pin 11 output)
OFF	> V_{UVLO}^+	Not Active	High	Low
OFF	< V_{UVLO}^-	Not Active	High	Low
ON	> V_{UVLO}^+	Active (< V_{DESAT})	High	High
ON	> V_{UVLO}^+	Active (> V_{DESAT})	Low	Low
ON	< V_{UVLO}^-	Not Active	High	Low

6.2. Mechanical Parameters

Characteristics	Dimensions	Unit
Creepage distances	8.0 (min)	mm
Clearance distances		
Internal isolation thickness	0.4 (min)	

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 °C)

	Characteristics		Symbol	Note	Rating	Unit
LED & FAULT feedback IC (Controller side)	LED Input forward current		I_F		25	mA
	LED Input forward current derating (Ta ≥ 90 °C)		$\Delta I_F/\Delta Ta$		−0.65	mA/°C
	LED Peak transient input forward current		I_{FPT}	Note 1	1	A
	LED Reverse input voltage		V_R		5	V
	Input side supply voltage		V_{CC1}		−0.5 to 7	V
	FAULT feedback IC output current		$I_{\overline{FAULT}}$		8	mA
	FAULT feedback IC output voltage		$V_{\overline{FAULT}}$		−0.5 to V_{CC1}	V
	LED power dissipation		P_D	Note 3	60	mW
	LED power dissipation derating (Ta ≥ 90 °C)		$\Delta P_D/\Delta Ta$	Note 3	−1.9	mW/°C
Output IC (Gate side)	Peak high level output current	Ta = −40 to 110 °C	I_{OPH}	Note 2 Note 3	−2.5	A
	Peak low level output current		I_{OPL}		+2.5	A
	Output side total supply voltage		$(V_{CC2}-V_{EE})$		−0.5 to 35	V
	Output side negative supply voltage		(V_E-V_{EE})		−0.5 to 15	V
	Output side positive supply voltage		$(V_{CC2}-V_E)$		−0.5 to 35 − (V_E-V_{EE})	V
	Output voltage		V_{OUT}		V_{EE} to V_{CC2}	V
	Peak Miller clamp sinking current		I_{Clamp}		2.5	A
	Miller clamp terminal voltage		V_{Clamp}		V_{EE} to V_{CC2}	V
	DESAT terminal voltage		V_{DESAT}		V_E to V_E + 10	V
	Output IC power dissipation		P_O	Note 3	600	mW
	P_O derating (Ta ≥ 90 °C)		$\Delta P_O/\Delta Ta$	Note 3	−13.0	mW/°C
Common	Operating temperature		T_{opr}		−40 to 110	°C
	Storage temperature		T_{stg}		−55 to 125	°C
	Lead soldering temperature (10 s)		T_{sol}	Note 4	260	°C
	Isolation voltage (AC, 60 s, R.H. ≤ 60 %)		BV_S	Note 5	5000	Vrms

Note : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/”Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.)

Note 1: Pulse width ≤ 1 μs, 300 pps

Note 2: Exponential waveform. Pulse width ≤ 0.3 μs, f ≤ 25 kHz, V_{CC2} = 15 to 30 V

Note 3: Mounting on a substrate designated in accordance with JEDEC JESD51-7.

Note 4: For the effective lead soldering area.

Note 5: This device considered a two-terminal device: All pins on the LED & feedback IC side are shorted together, and all pins on the Output IC side are shorted together.

8. Recommended Operation Conditions (Note)

Characteristics	Symbol	Note	Min	Max	Unit
Output side total supply voltage	(V_{CC2} - V_{EE})	Note 1 Note 2	15	30	V
Output side negative supply voltage	(V_E - V_{EE})	Note 1 Note 3	0	15	V
Output side positive supply voltage	(V_{CC2} - V_E)	Note 1 Note 2	15	30 - (V_E - V_{EE})	V
Input side supply voltage	V_{CC1}		2.7	5.5	V
LED Input on-state current	$I_{F(ON)}$	Note 4	7.5	12	mA
LED Input off-state voltage	$V_{F(OFF)}$		0	0.8	V

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performances of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note 1: If the rising and falling slopes of V_{CC2} and V_{EE} are so steep, the internal circuit operation may not be stable. In that case, please design the slopes to be 0.5 V/μs or less.

Note 2: 15 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 12.5V.

Note 3: This supply is optional. Required only when negative gate drive is implemented.

Note 4: The rise and fall times of the input on-current should be less than 500 μs.

9. Electrical Characteristics (Note)

(Unless otherwise specified, Ta = - 40 to 110 °C, V_{CC2} - V_{EE} = 15 to 30 V, V_E - V_{EE} = 0 V)

Characteristics	Symbol	Note	Test Circuit	Test Conditions	Min	Typ.	Max	Unit
Input forward voltage	V_F			I_F = 10 mA, Ta = 25 °C	1.48	1.67	1.93	V
Input reverse current	I_R			V_R = 5 V, Ta = 25 °C	–	–	10	μA
Input capacitance (between Anode and Cathode)	C_t			V = 0 V, f = 1 MHz, Ta = 25 °C	–	20	–	pF
FAULT low level output voltage	$V_{\overline{FAULTL}}$			$I_{\overline{FAULT}}$ = 1.1 mA, V_{CC1} = 5.5 V	–	0.27	0.4	V
				$I_{\overline{FAULT}}$ = 1.1 mA, V_{CC1} = 2.7 V	–	0.27	0.4	
FAULT high level output current	$I_{\overline{FAULTH}}$			$V_{\overline{FAULT}}$ = V_{CC1} = 5.5 V, Ta = 25 °C	–	–	0.5	μA
				$V_{\overline{FAULT}}$ = V_{CC1} = 2.7 V, Ta = 25 °C	–	–	0.3	
Peak high level output current	I_{OPH}	Note 1	13.1.1	I_F = 10 mA, V_{OUT} = V_{CC2} - 4 V	–	−2.9	-2.0	A
Peak low level output current	I_{OPL}	Note 1	13.1.2	V_{OUT} = V_{EE} + 2.5 V	2.0	3.1	–	
Low level output current during fault condition	I_{OLF}		13.1.3	V_{OUT} - V_{EE} = 14 V	90	180	230	mA
High level output voltage	V_{OH}		13.1.4	I_{OUT} = - 650 μA	V_{CC2}− 2.9	V_{CC2}− 1.6	–	V
Low level output voltage	V_{OL}		13.1.5	I_{OUT} = 100 mA	–	0.12	0.5	
Clamp threshold voltage	V_{tClamp}			I_{CL} = 100 mA	–	2.3	–	
Clamp low level sinking current	I_{CL}		13.1.6	V_{Clamp} = V_{EE} + 2.5 V	0.35	2.2	–	A
High level supply current	I_{CC2H}		13.1.7	I_F = 10 mA	–	2.9	5	mA
Low level supply current	I_{CC2L}		13.1.8	I_F = 0 mA	–	2.2	5	
Blanking capacitor charging current	I_{CHG}		13.1.9	I_F = 10 mA, V_{DESAT} = 2 V	−0.33	−0.26	−0.13	
Blanking capacitor discharging current	I_{DSCHG}		13.1.10	V_{DESAT} = 7 V	10	27.7	–	
DESAT threshold voltage	V_{DESAT}		13.1.11	I_F = 10 mA, I_{DESAT} > 0	6.0	6.6	7.5	V
UVLO threshold voltage	V_{UVLO}^+		13.1.12	I_F = 10 mA, V_{OUT} > 5 V	10.5	11.4	12.5	
	V_{UVLO}^-		13.1.12	I_F = 10 mA, V_{OUT} < 5 V	9.2	10.0	11.1	
UVLO hysteresis	$UVLO_{HYS}$			V_{UVLO}^+ - V_{UVLO}^-	0.4	1.4	–	
Threshold input current (L/H)	I_{FLH}		13.1.13	V_{CC2} = 30 V, V_{OUT} > 5 V	–	1.1	6.0	mA
Threshold input voltage (H/L)	V_{FHL}			V_{CC2} = 30 V, V_{OUT} < 5 V	0.8	–	–	V

Note: All typical values are at V_{CC2} – V_E = 30 V, T_a = 25 °C, unless otherwise noted.

Note 1: I_O application time ≤ 10 μs, single pulse

10. Isolation Characteristics (Unless otherwise specified, Ta = 25 °C)

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	Note 1	V_S = 0 V, f = 1 MHz	–	1.0	–	pF
Isolation resistance	R_S	Note 1	V_S = 500 V, R.H. ≤ 60 %	10^{12}	10^{14}	–	Ω
Isolation voltage	BV_S	Note 1	AC, 60 s	5000	–	–	Vrms

Note 1: This device considered a two-terminal device: All pins on the LED & feedback IC side are shorted together, and all pin on the Output IC side are shorted together.

11. Switching Characteristics (Note)

(Unless otherwise specified, Ta = - 40 to 110 °C, V_{CC2} - V_{EE} = 15 to 30 V, V_E - V_{EE} = 0 V)

Characteristics		Symbol	Note	Test Circuit	Test Conditions		Min	Typ.	Max	Unit
Propagation delay time	L → H	t_{pLH}	Note 1	13.1.14	R_g = 10 Ω, C_g = 10 nF, f = 10 kHz, duty = 50 %	I_F = 0 → 10 mA	100	170	250	ns
	H → L	t_{pHL}				I_F = 10 → 0 mA	100	165	250	
Pulse width distortion		$\lvert t_{pHL}-t_{pLH} \rvert$				I_F = 0 ↔ 10 mA	–	5	50	
Propagation delay skew (device to device)		t_{psk}	Note 1 Note 2				-150	–	150	
Rise time		t_r	Note 1			I_F = 0 → 10 mA	–	58	–	
Fall time		t_f				I_F = 10 → 0 mA	–	57	–	
DESAT sense to 90% V_{OUT} delay		$t_{DESAT(90\%)}$		13.1.15	C_{DESAT} = 100 pF, R_g = 10 Ω, C_g = 10 nF		–	145	500	ns
DESAT sense to 10% V_{OUT} delay		$t_{DESAT(10\%)}$					–	2.1	3	µs
DESAT leading edge blanking time		$t_{DESAT(LEB)}$					–	1.4	–	
DESAT sense to 50% V_{DESAT} delay		$t_{DESAT(LOW)}$					–	167	–	ns
DESAT dense to low level FAULT signal delay		$t_{DESAT(FAULT)}$	Note 3		C_{DESAT} = 100 pF, R_g = 10 Ω, C_g = 10 nF, V_{CC1} = 5 V, R_F = 2.1 kΩ	C_F = Open	–	340	500	ns
						C_F = 1 nF	–	640	–	
DESAT input mute time		$t_{DESAT(MUTE)}$				–	15	25.5	40	µs
High level common-mode transient immunity		CM_H	Note 3 Note 4	13.1.16 13.1.17	Ta = 25 °C, V_{CM} = 1500 V_{P-P}, V_{CC2} = 30 V, R_F = 2.1 kΩ, R_g = 10 Ω, C_g = 10 nF	C_F = Open	±25	±40	–	kV/µs
						C_F = 1 nF	±50	±100	–	
Low level common-mode transient immunity		CM_L	Note 3 Note 5	13.1.18 13.1.19		C_F = Open	±25	±40	–	
						C_F = 1 nF	±50	±100	–	

Note: All typical values are at $V_{CC2} - V_E$ = 30 V, T_a = 25 °C, unless otherwise noted.

Note 1: Input signal: f = 10 kHz, duty = 50 %, tr = tf = 5 ns or less

Note 2: The propagation delay skew, t_{psk}, is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

Note 3: Even C_F is open, less than 15 pF of probe and stray wiring capacitance is included.

Note 4: High level common mode transient immunity is the maximum tolerable slew rate (dV_{CM}/dt) of the common mode pulse (V_{CM}) to assure that the output will remain in the high state (V_{OUT} > 23 V, $V_{\overline{FAULT}}$ > 3 V).

Note 5: Low level common mode transient immunity is the maximum tolerable slew rate (dV_{CM}/dt) of the common mode pulse (V_{CM}) to assure that the output will remain in a low state (V_{OUT} < 1 V, $V_{\overline{FAULT}}$ < 2 V).

12. Application Information

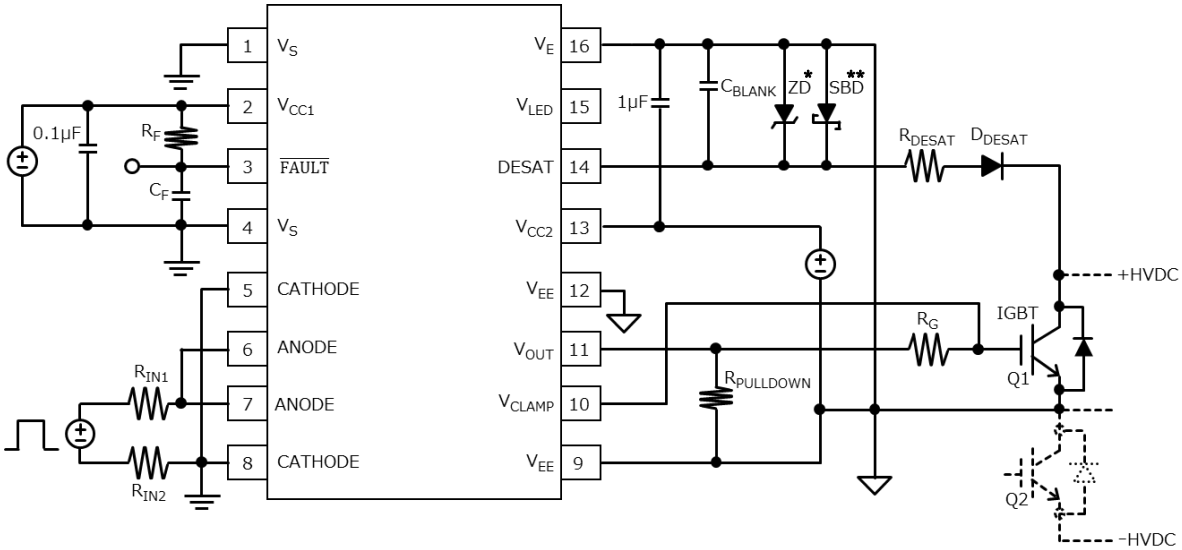


Fig 12.1 Recommended application circuit with positive gate drive, desaturation detection and active Miller clamp

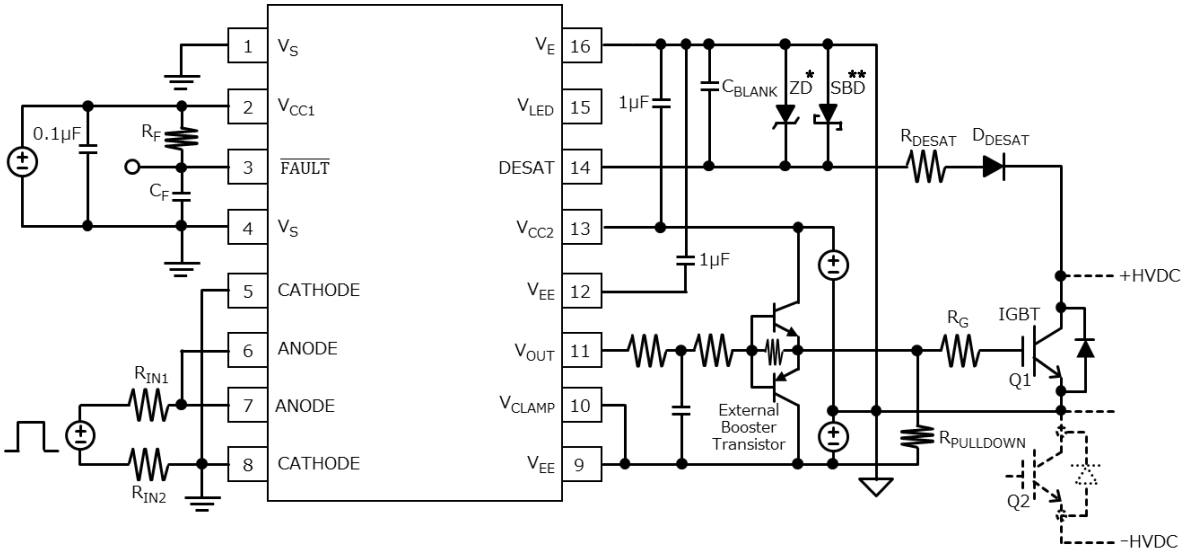


Fig 12.2 Recommended application circuit with negative gate drive, external booster transistors and desaturation detection

Note : Bypass capacitors (1 μF) must be connected between pin 13 (V_{CC2}) and 16 (V_E) to stabilize the operation of the high gain linear amplifier. When $V_E - V_{EE} > 0$ V (with negative gate drive), another bypass capacitor (1 μF) must be connected between pin 9 or 12 (V_{EE}) and 16 (V_E). Failure to provide the bypassing may impair the switching property. The total lead length between each capacitor and the coupler should not exceed 1 cm.

Refer to the connection of pin 14 and pin 16 for a desaturation detection function. The desaturation diode D_{DESAT} 600V / 1200V fast recovery type and capacitor C_{BLANK} are external components required for fault detection circuits. Also, select a resistance R_{DESAT} of 500 ohms or more for protection of DESAT pin 14. For details, refer to the application note "Smart Gate Driver Coupler Tips for Designing DESAT Detection Circuits".

＊ : Zener diode for DESAT pin protection. CUZ8V2 is recommended.

＊＊ : Schottky diode for DESAT false detection prevention. CUS05F30 is recommended.

13. Characteristics Figures

13.1. Test Circuits

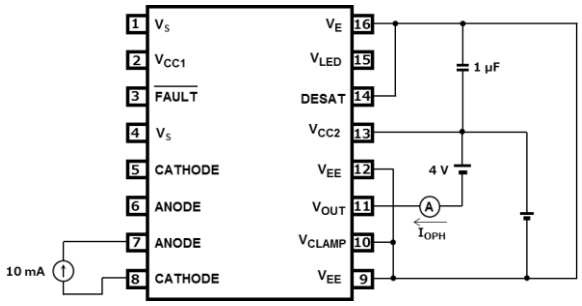


Fig. 13.1.1 I_{OPH} Test Circuit

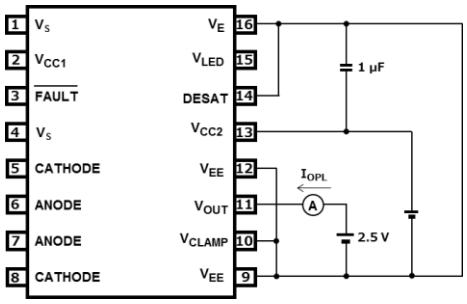


Fig. 13.1.2 I_{OPL} Test Circuit

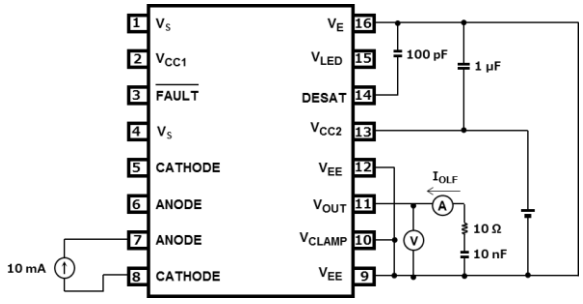


Fig. 13.1.3 I_{OLF} Test Circuit

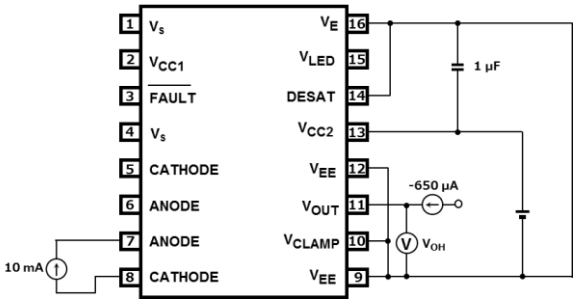


Fig. 13.1.4 V_{OH} Test Circuit

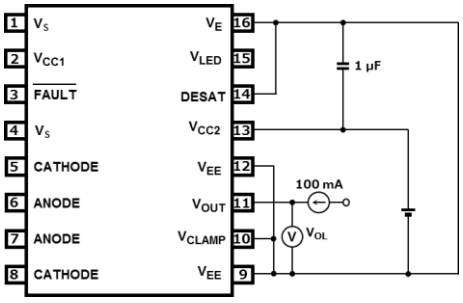


Fig. 13.1.5 V_{OL} Test Circuit

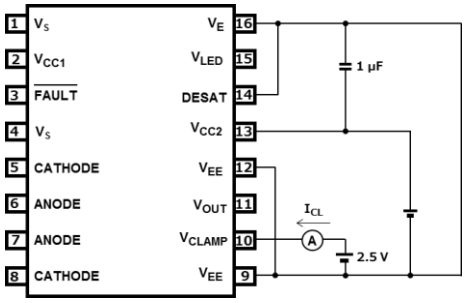


Fig. 13.1.6 I_{CL} Test Circuit

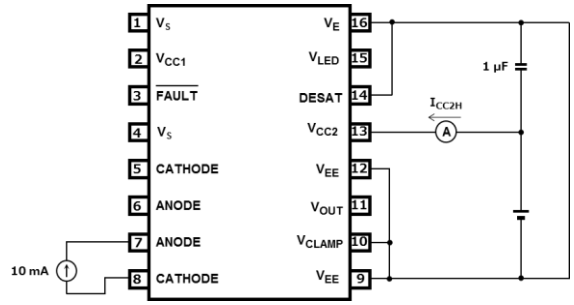


Fig. 13.1.7 I_{CC2H} Test Circuit

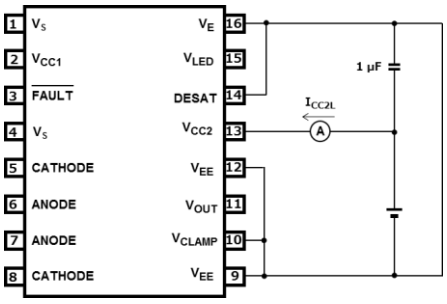


Fig. 13.1.8 I_{CC2L} Test Circuit

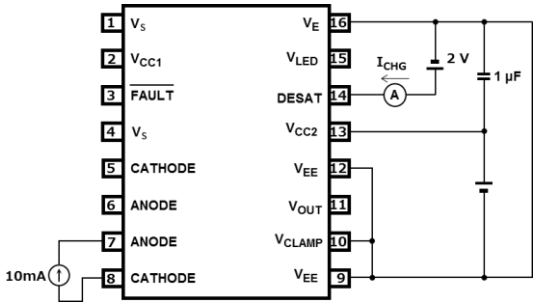


Fig. 13.1.9 I_{CHG} Test Circuit

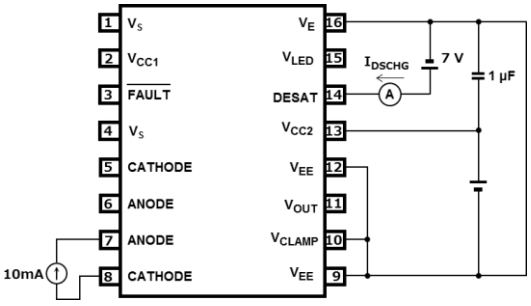


Fig. 13.1.10 I_{DSCHG} Test Circuit

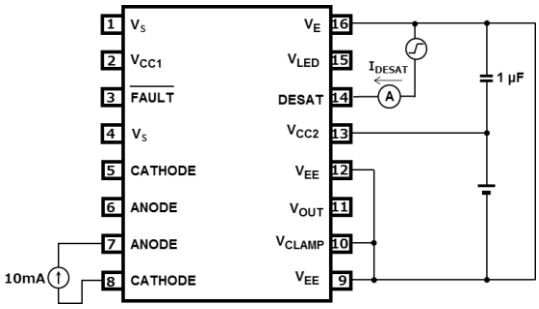


Fig. 13.1.11 V_{DESAT} Test Circuit

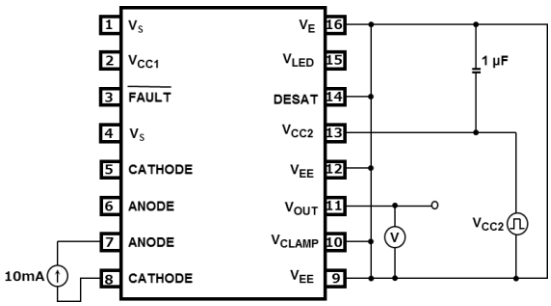


Fig. 13.1.12 V_{UVLO} Test Circuit

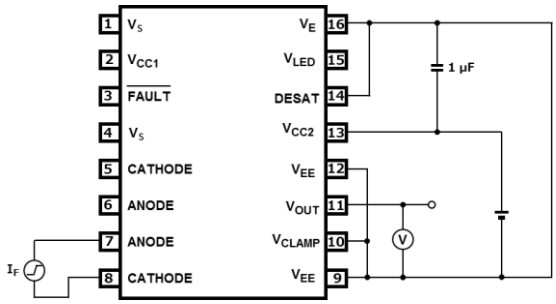
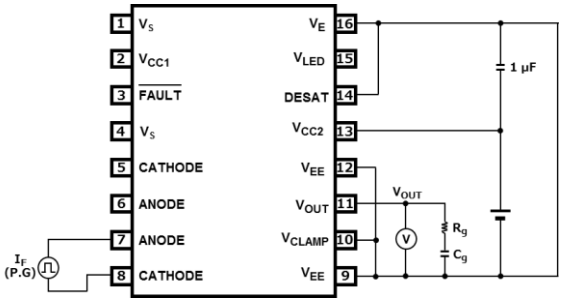


Fig. 13.1.13 I_{FLH} Test Circuit

I_F = 10 mA (P.G)
(f = 10 kHz, duty = 50 %, t_r = t_f = 5 ns or less)



P.G. : Pulse Generator

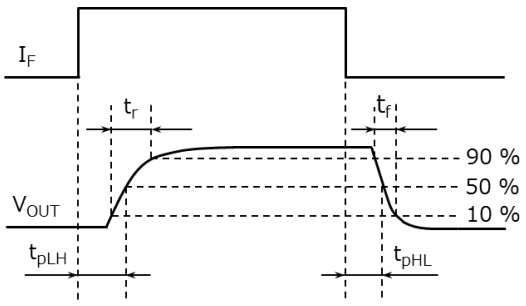


Fig. 13.1.14 t_{PLH}, t_{PHL}, t_r, t_f Test Circuit and Waveform

I_F = 10 mA (P.G)
(f = 10 kHz, duty = 50 %, t_r = t_f = 5 ns or less)

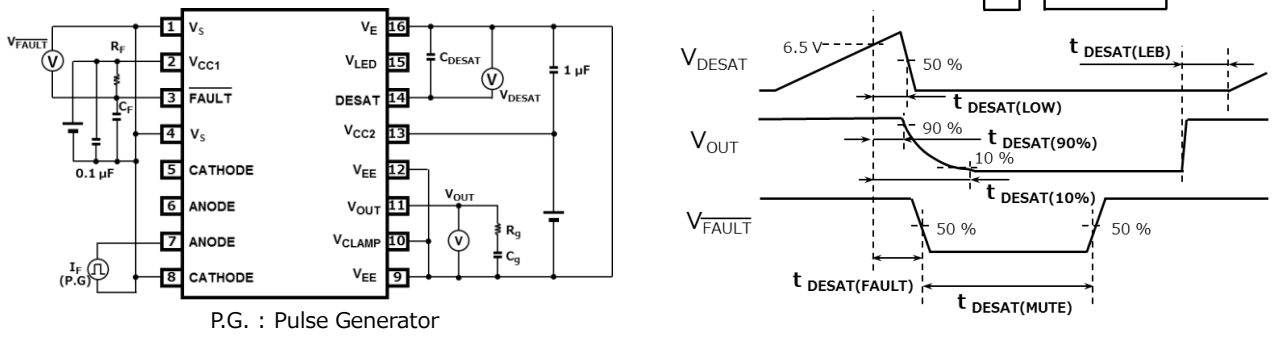


Fig. 13.1.15 $t_{DESAT(90\%)}$, $t_{DESAT(10\%)}$, $t_{DESAT(LEB)}$, $t_{DESAT(LOW)}$, $t_{DESAT(FAULT)}$, $t_{DESAT(MUTE)}$ Test Circuit and Waveform

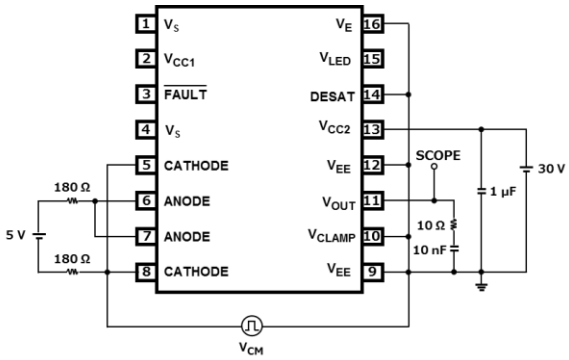


Fig. 13.1.16 CM_H refer to V_E Test Circuit

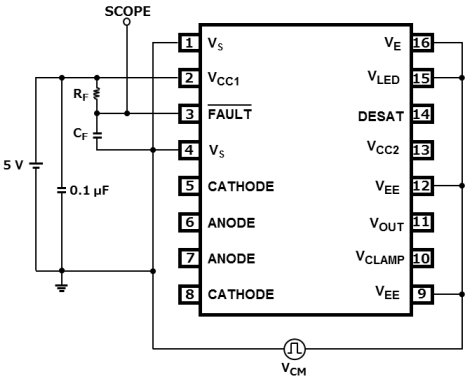


Fig. 13.1.17 CM_H refer to V_S Test Circuit

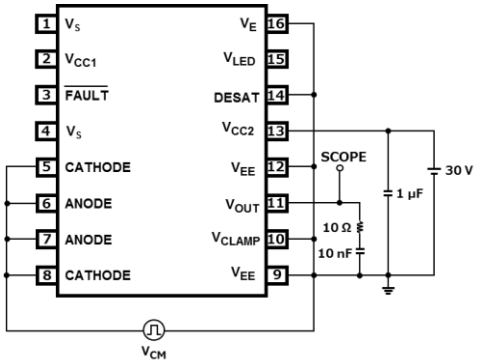


Fig. 13.1.18 CM_L refer to V_E Test Circuit

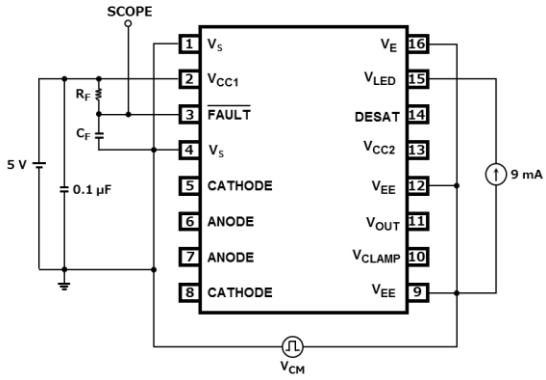
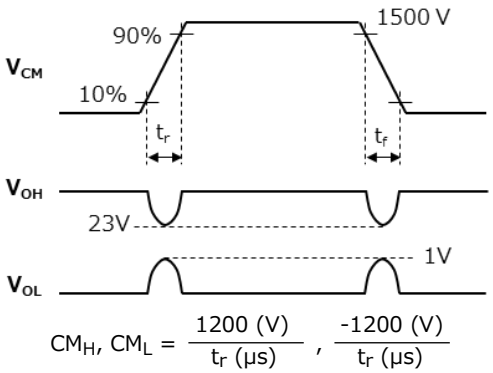
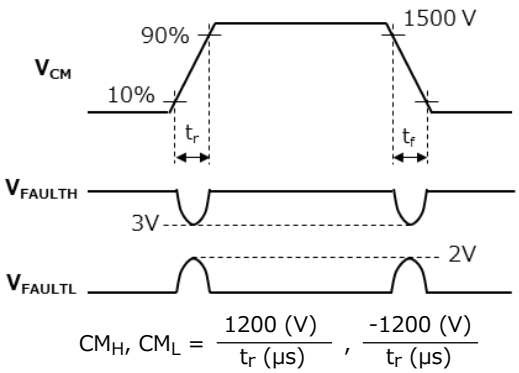


Fig. 13.1.19 CM_L refer to V_S Test Circuit



$$CM_H, CM_L = \frac{1200\ (V)}{t_r\ (\mu s)}, \frac{-1200\ (V)}{t_r\ (\mu s)}$$

Fig. 13.1.20 CM_H, CM_L refer to V_E Waveform



$$CM_H, CM_L = \frac{1200\ (V)}{t_r\ (\mu s)}, \frac{-1200\ (V)}{t_r\ (\mu s)}$$

Fig. 13.1.21 CM_H, CM_L refer to V_S Waveform

13.2 Timing Chart

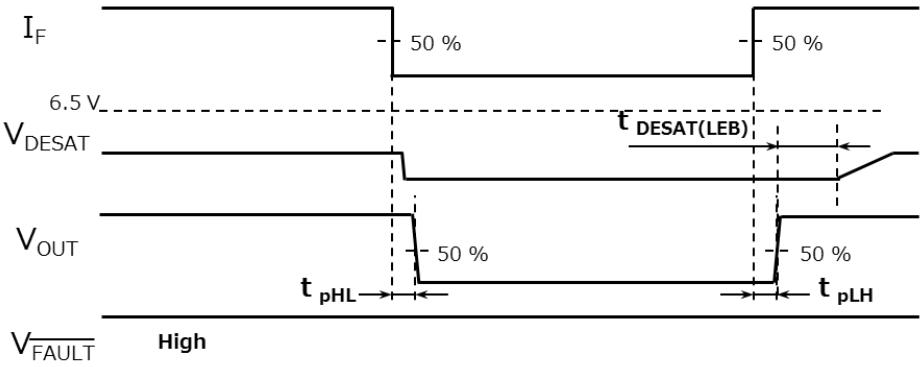


Fig 13.2.1 Normal state

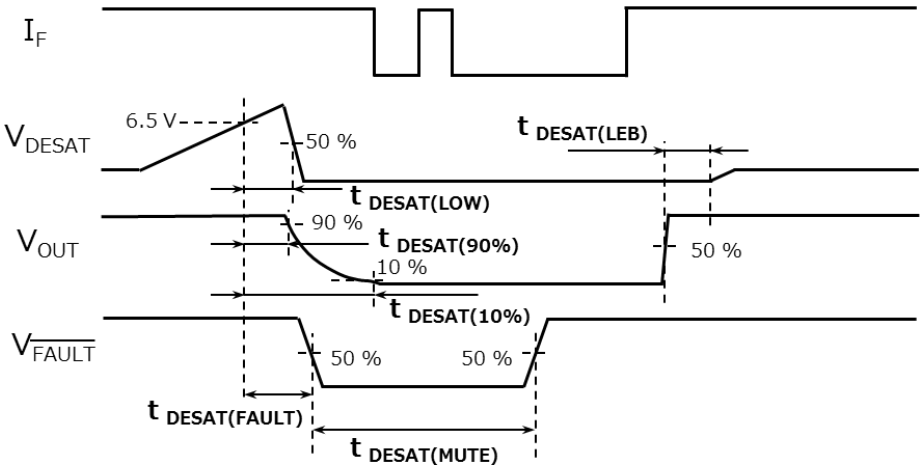


Fig 13.2.2 Protection state (when I_F turns off within the $t_{DESAT(MUTE)}$)

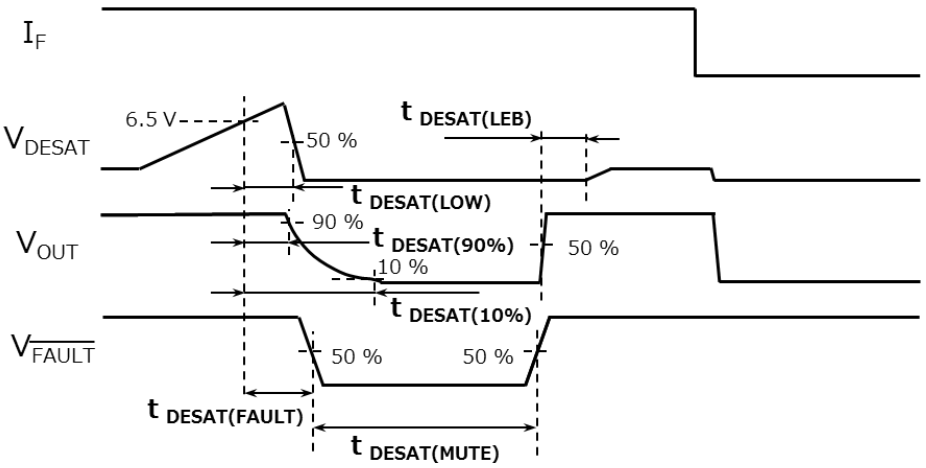


Fig 13.2.3 Protection state (when I_F turns off after the $t_{DESAT(MUTE)}$)

13.3 Characteristics Curves (Note)

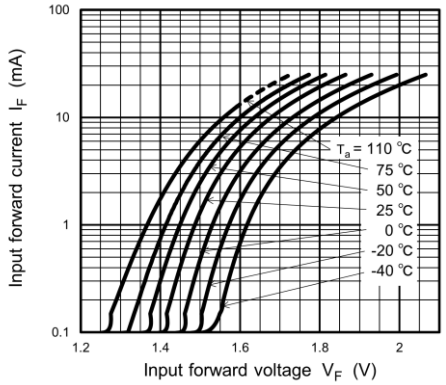


Fig 13.3.1 I_F - V_F

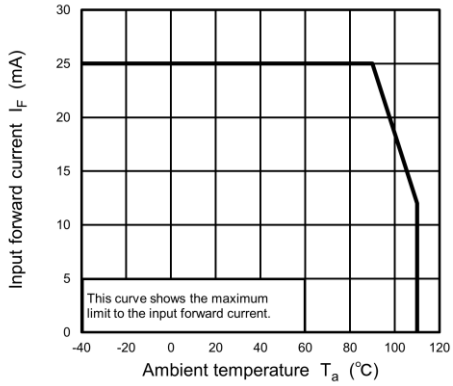


Fig 13.3.2 I_F - T_a

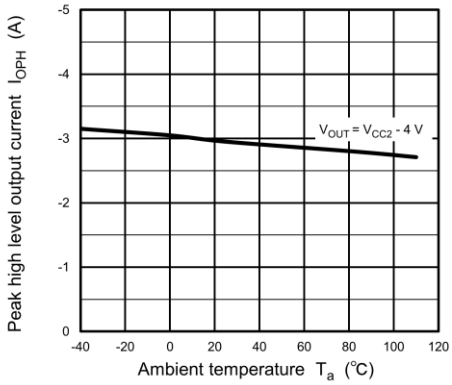


Fig 13.3.3 I_{OPH} - T_a

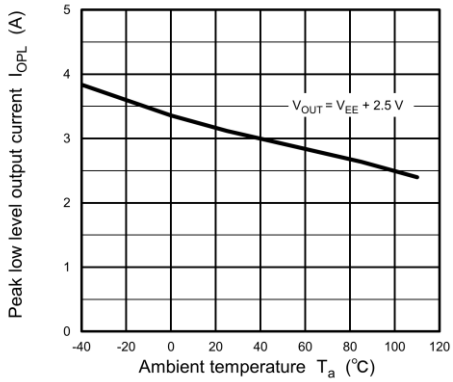


Fig 13.3.4 I_{OPL} - T_a

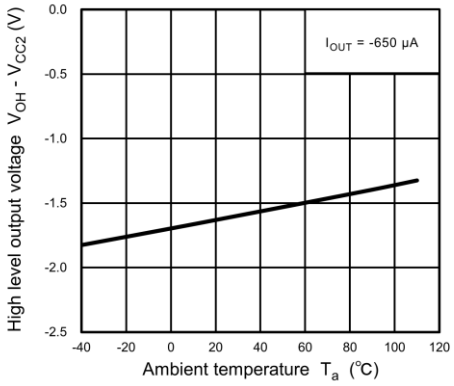


Fig 13.3.5 (V_{OH} - V_{CC2}) - T_a

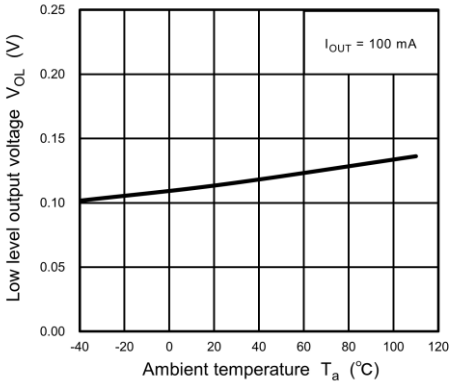


Fig 13.3.6 V_{OL} - T_a

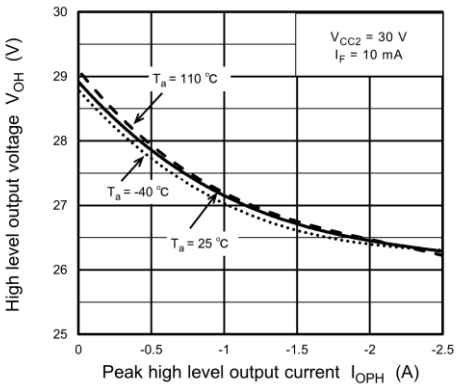


Fig 13.3.7 V_{OH} - I_{OPH}

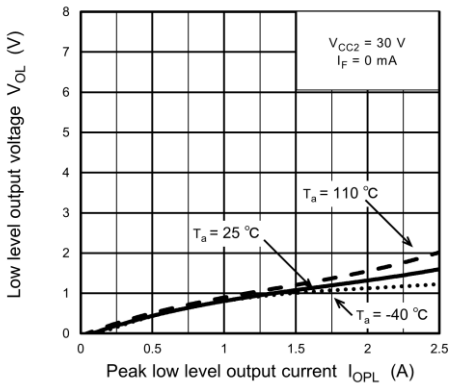


Fig 13.3.8 V_{OL} - I_{OPL}

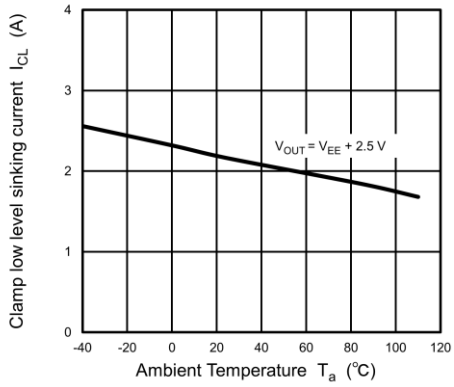


Fig 13.3.9 I_{CL} – T_a

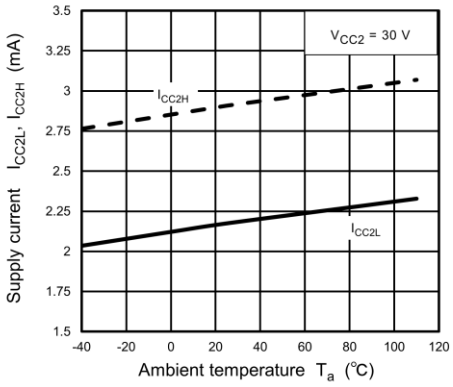


Fig 13.3.10 I_{CC2} – T_a

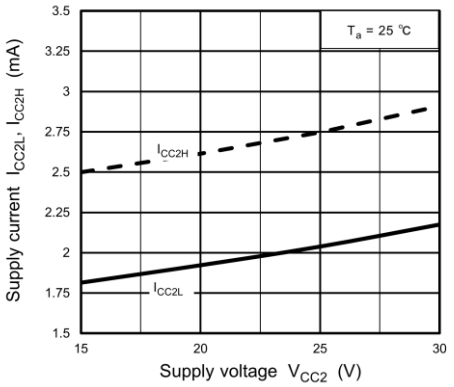


Fig 13.3.11 I_{CC2} - V_{CC2}

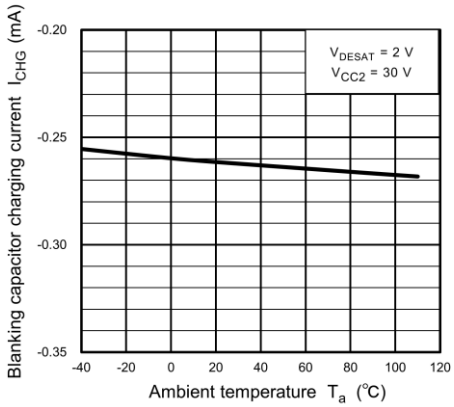


Fig 13.3.12 I_{CHG} - T_a

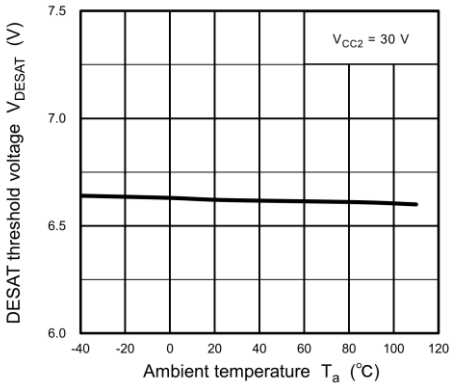


Fig 13.3.13 V_{DESAT} - T_a

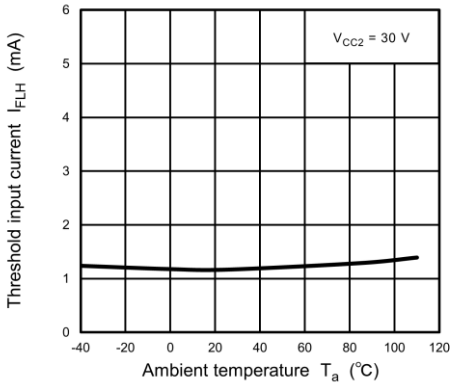


Fig 13.3.14 I_{FLH} - T_a

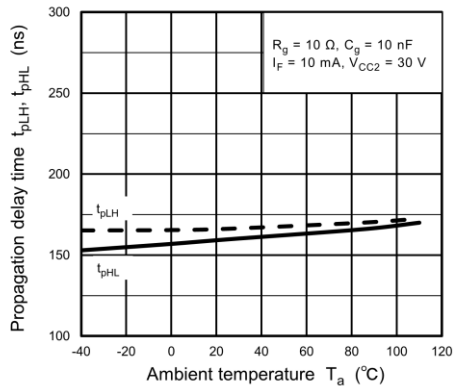


Fig 13.3.15 t_{pLH}, t_{pHL} - T_a

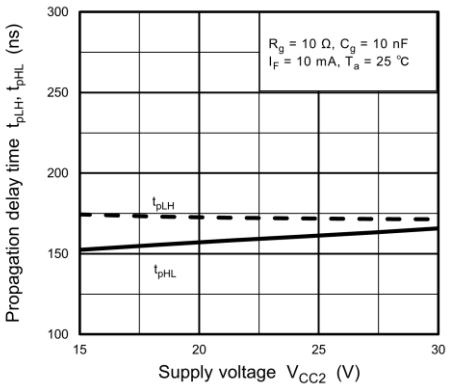


Fig 13.3.16 t_{pLH}, t_{pHL} - V_{CC2}

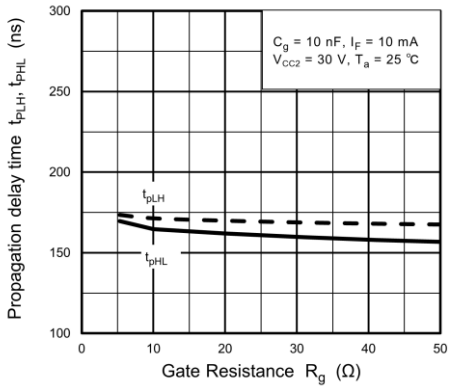


Fig 13.3.17 t_{pLH}, t_{pHL} - R_g

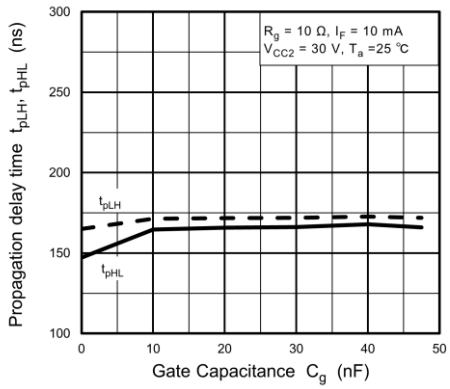


Fig 13.3.18 t_{pLH}, t_{pHL} - C_g

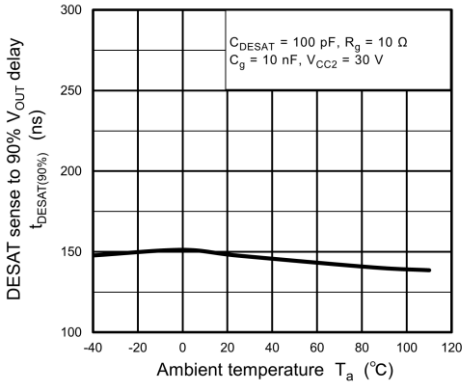


Fig 13.3.19 $t_{DESAT(90\%)}$ - T_a

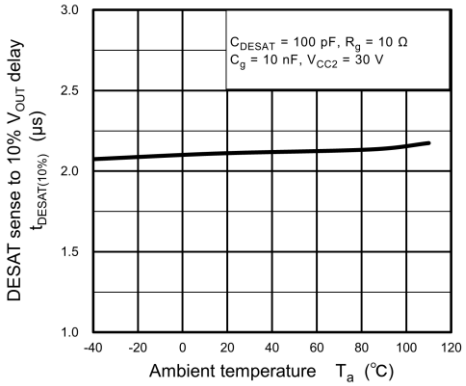


Fig 13.3.20 $t_{DESAT(10\%)}$ - T_a

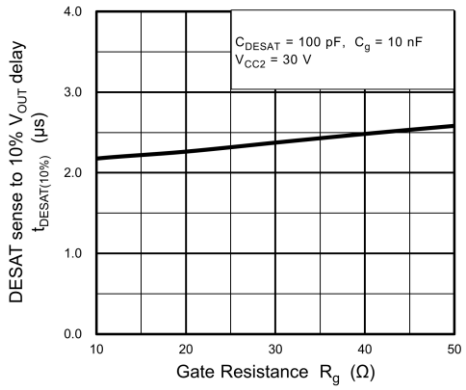


Fig 13.3.21 $t_{DESAT(10\%)}$ - R_g

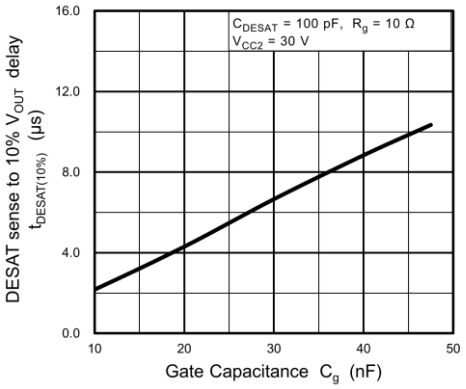


Fig 13.3.22 $t_{DESAT(10\%)}$ - C_g

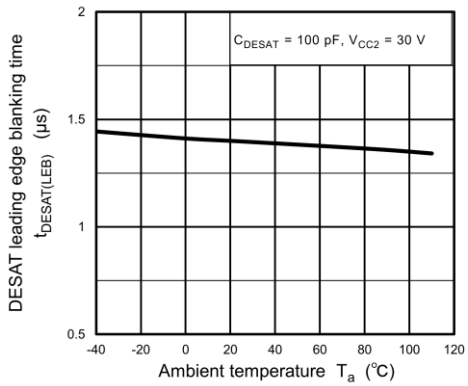


Fig 13.3.23 $t_{DESAT(LEB)}$ - T_a

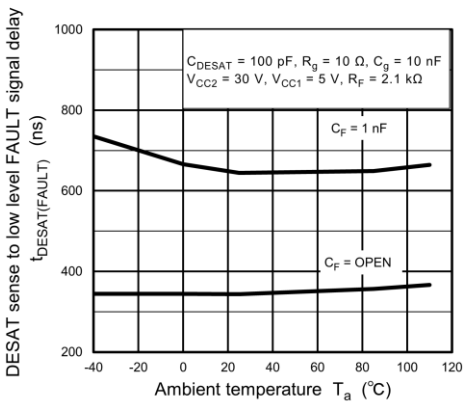


Fig 13.3.24 $t_{DESAT(FAULT)}$ - T_a

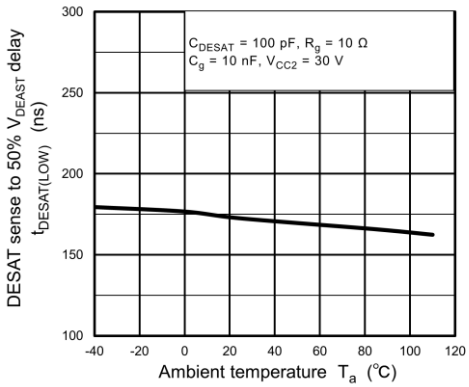


Fig 13.3.25 $t_{DESAT(LOW)}$ - T_a

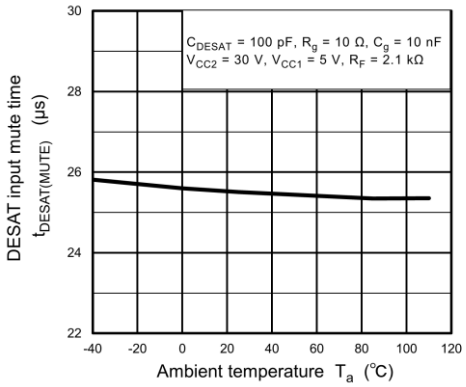


Fig 13.3.26 $t_{DESAT(MUTE)}$ - T_a

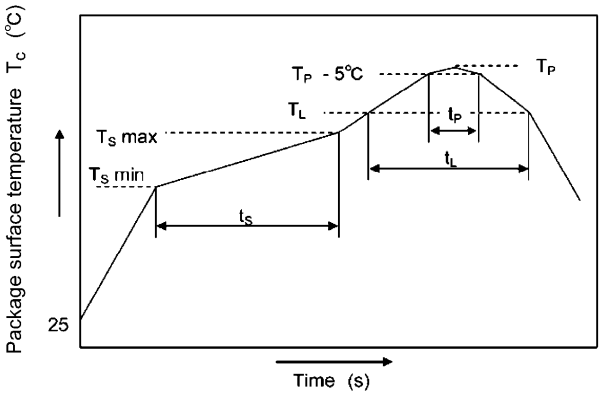
Note : The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

14. Soldering and Storage

14.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

· When using soldering reflow.
The soldering temperature profile is based on the package surface temperature.
(See the figure shown below, which is based on the package surface temperature.)
Reflow soldering must be performed once or twice.
The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



	Symbol	Min	Max	Unit
Preheat temperature	T_S	150	200	°C
Preheat time	t_S	60	120	s
Ramp-up rate (T_L to T_P)			3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	150	s
Peak temperature	T_P		260	°C
Time during which T_c is between (T_P – 5) and T_P	t_P		30	s
Ramp-down rate (T_P to T_L)			6	°C/s

An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used

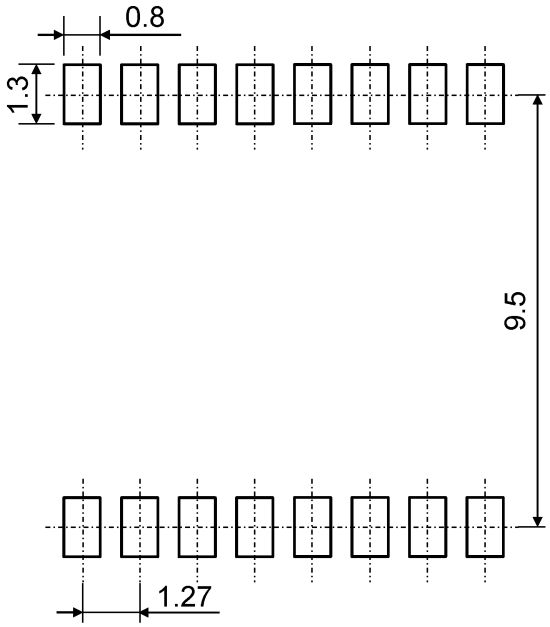
· When using soldering flow
Preheat the device at a temperature of 150℃ (package surface temperature) for 60 to 120 seconds.
Mounting condition of 260℃ within 10 seconds is recommended.
Flow soldering must be performed once.

· When using soldering Iron
Complete soldering within 10 seconds for lead temperature not exceeding 260℃ or within 3 seconds not exceeding 350℃.
Heating by soldering iron must be done only once per lead.

14.2. Precautions for General Storage

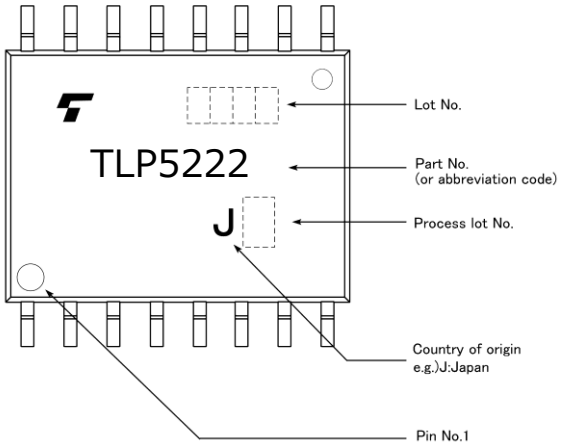
· Avoid storage locations where devices may be exposed to moisture or direct sunlight.
· Follow the precautions printed on the packing label of the device for transportation and storage.
· Keep the storage location temperature and humidity within a range of 5℃ to 35℃ and 45 % to 75 %, respectively.
· Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
· Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
· When restoring devices after removal from their packing, use anti-static containers.
· Do not allow loads to be applied directly to devices while they are in storage.
· If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

15. Land Pattern Dimensions (for reference only)



Unit: mm

16. Marking



17. EN 60747-5-5 Option (D4) Specification

- Part number: TLP5222 **(Note 1)**
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN 60747.

Example: TLP5222(D4-TP,E

D4: EN 60747 option
TP: Tape type
E: [[G]]/RoHS COMPATIBLE **(Note 2)**

Note 1: Use TOSHIBA standard type number for safety standard application.
e.g., TLP5222(D4-TP,E → TLP5222
Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Description	Symbol	Rating	Unit
Application classification for rated mains voltage ≤ 600 Vrms for rated mains voltage ≤ 1000 Vrms		 I-IV I-III	—
Climatic classification		40 / 110 / 21	—
Pollution degree		2	—
Maximum operating insulation voltage	V_{IORM}	1230	Vpeak
Input to output test voltage, Method A V_{pr} = 1.6 × V_{IORM}, type and sample test t_p = 10 s, partial discharge < 5 pC	V_{pr}	1970	Vpeak
Input to output test voltage, Method B V_{pr} = 1.875 × V_{IORM}, 100 % production test t_p = 1 s, partial discharge < 5 pC	V_{pr}	2310	Vpeak
Highest permissible overvoltage (transient overvoltage, t_{pr} = 60 s)	V_{TR}	8000	Vpeak
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I_F, P_{SO} = 0) power (output or total power dissipation) temperature	 I_{si} P_{SO} T_S	 400 1200 175	 mA mW °C
Insulation resistance V_{IO} = 500 V, T_a = 25 °C V_{IO} = 500 V, T_a = 100 °C V_{IO} = 500 V, T_a = T_S	R_{si}	≥ 10^{12} ≥ 10^{11} ≥ 10^{9}	Ω

Fig 17.1 EN 60747 Insulation Characteristics

Minimum creepage distance	Cr	8.0 mm
Minimum clearance	Cl	8.0 mm
Minimum insulation thickness	ti	0.4 mm
Comparative tracking index	CTI	500

Fig 17.2 Insulation Related Specifications (Note)

Note: This photocoupler is suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Fig 17.3 Marking on Packing for EN 60747

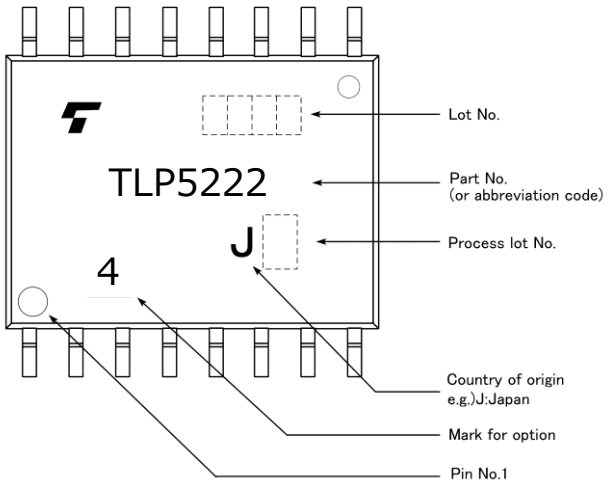


Fig 17.4 Marking Example (Note)

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN 60747.

Figure 1 Partial discharge measurement procedure according to EN 60747
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests, destructive tests)

t_1, t_2	= 1 to 10 s
t_3, t_4	= 1 s
t_p (Measuring time for partial discharge)	= 10 s
t_b	= 12 s
t_{ini}	= 60 s

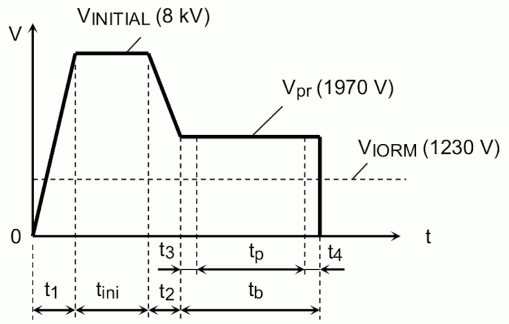


Figure 2 Partial discharge measurement procedure according to EN 60747
Non-destructive test for 100 % inspection.

Method B

(for sample test, non-destructive test)

t_3, t_4	= 0.1 s
t_p (Measuring time for partial discharge)	= 1 s
t_b	= 1.2 s

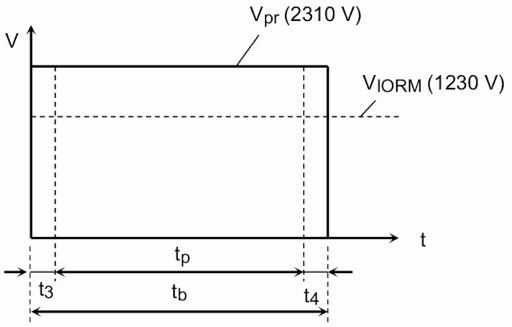


Figure 3 Dependency of maximum safety ratings on ambient temperature

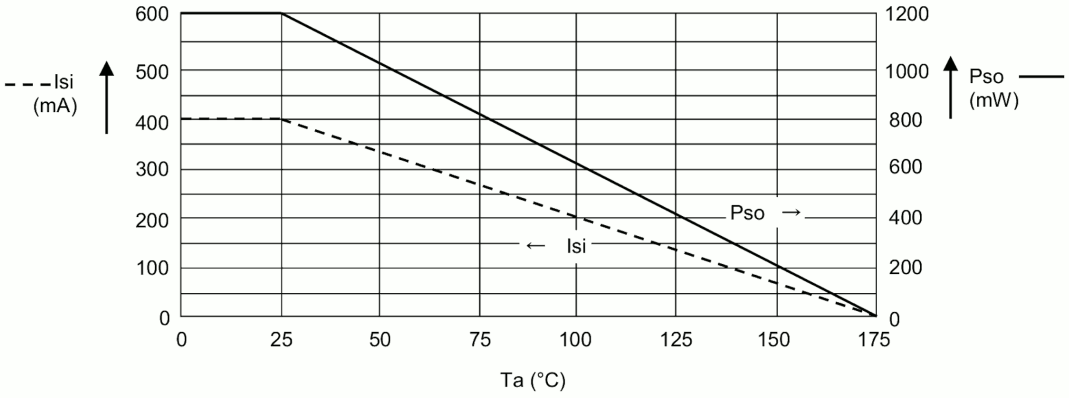


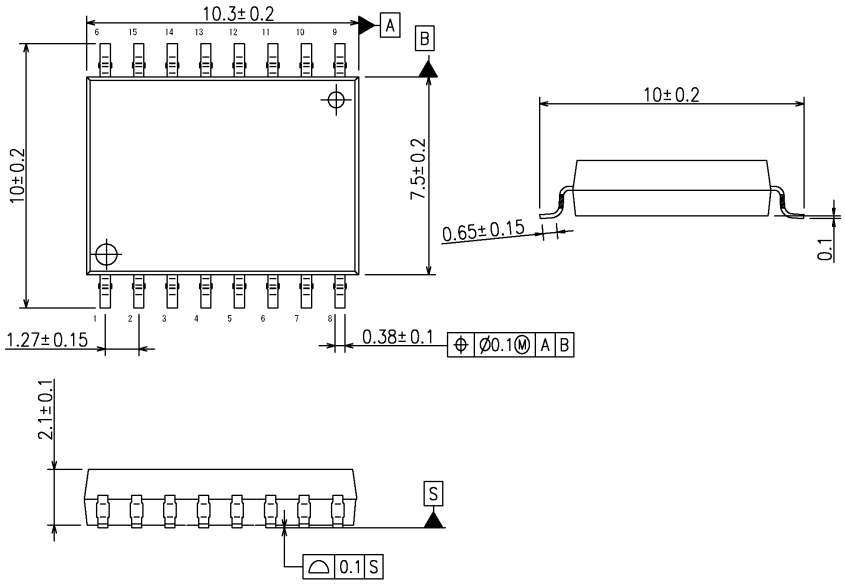
Fig 17.5 Measurement Procedure

18. Ordering Information (Example of Item Name)

Item Name	VDE Option	Packing (MOQ)
TLP5222(E		Magazine (50 pcs)
TLP5222(TP,E		Tape and reel (1500 pcs)
TLP5222(D4,E	EN 60747-5-5	Magazine (50 pcs)
TLP5222(D4-TP,E	EN 60747-5-5	Tape and reel (1500 pcs)

Package Dimensions

Unit: mm



Weight: 0.364 g (typ.)

Package Name(s)
TOSHIBA: 11-10M1

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