SiC MOSFET module
Gate drive
application note

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1. Gate drive for SiC MOSFET Module

1.1. Scope

The scope of this application note covers the following products.

Table 1.1.1 Product covered in this application note

Part No.	Drain-source voltage rating (V_{DSS})	Drain current (I_D)	Gate-source voltage rating (V_{GSS})	Recommended gate drive voltage ($+V_{GG}/-V_{GG}$)
MG600Q2YMS3	1200V	600A	+25V/-10V	+20V/-6V
MG400Q2YMS3	1200V	400A	+25V/-10V	+20V/-6V
MG400V2YMS3	1700V	400A	+25V/-10V	+20V/-6V
MG250V2YMS3	1700V	250A	+25V/-10V	+20V/-6V
MG250YD2YMS3	2200V	250A	+25V/-10V	+20V/-6V
MG800FXF2YMS3	3300V	800A	+25V/-10V	+20V/-6V
MG800FXF1JMS3	3300V	800A	+25V/-10V	+20V/-6V
MG800FXF1ZMS3	3300V	800A	+25V/-10V	+20V/-6V

2. Gate drive circuit

2.1. Gate drive circuit for SiC MOSFET module

An example of gate drive circuit for the SiC MOSFET module is shown in Fig. 2.1.1.

In the case of the example circuit, when a gate-on signal is given between the anode (pins 6 and 7) and the cathode (pins 5 and 8), transistor Q1 is switched on, transistor Q2 is switched off and the gate-on voltage is applied to the gate of the SiC MOSFET. When a gate-off signal changes to off-state, transistor Q1 is switched off, transistor Q2 is switched on, and the gate-off voltage is applied to the gate of the SiC MOSFET.

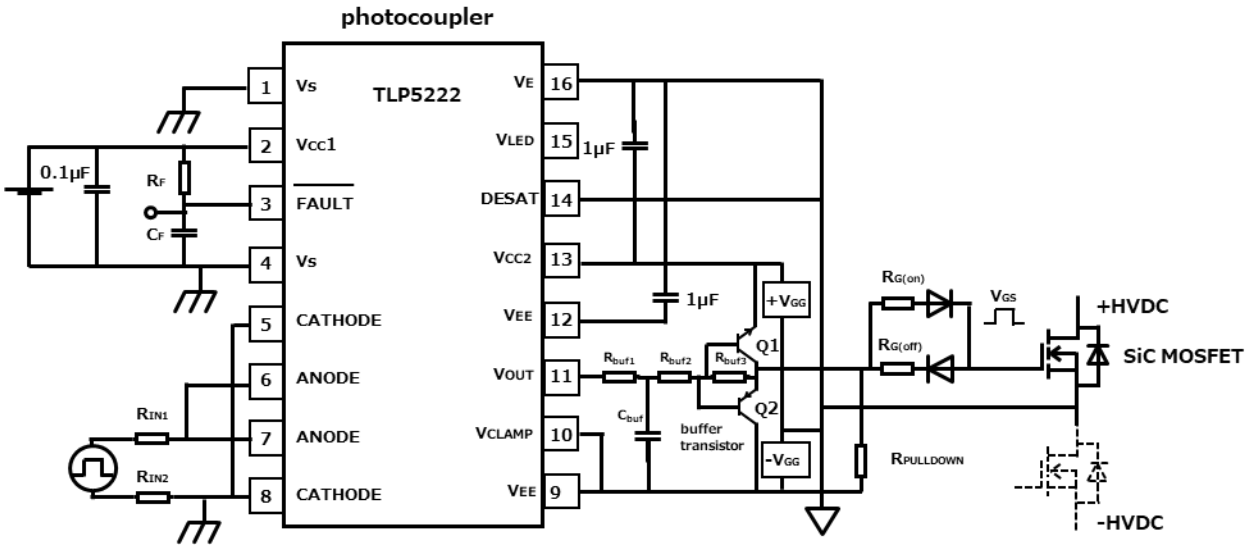


Figure 2.1.1 An example of the gate drive circuit for MG600Q2YMS3

It is recommended to design the gate driver board for mounting on the module.

To avoid interference from external electromagnetic induction, design the gate drive circuit to minimize the length and the area inside of the circuit wire of the buffer transistors and the gate signal terminal of the SiC MOSFET module. Insert the gate resistors ($R_{G(on)}$ and $R_{G(off)}$) nearby the gate terminal. Select a photocoupler that satisfy the required isolation voltage and dv/dt. Design the gate circuit to satisfy the required space and creepage distance.

2.2. Gate drive current

The maximum gate current required for turn-on, $I_{g(on)max}$, can be expressed by the equation (2.2.1) using the difference of gate positive bias voltage ($+V_{GG}$) and negative bias voltage ($-V_{GG}$) and the internal gate resistance r_g of the SiC MOSFET module. Refer to the datasheet of the products for the r_g value.

$$I_{g(on)max}=((+V_{GG})-(-V_{GG}))/(R_{G(on)}+r_g) \quad (2.2.1)$$

The maximum current during the turn-off period ($I_{g(off)max}$) can be expressed by the following equation (2.2.2)

$$I_{g(off)max}=((+V_{GG})-(-V_{GG}))/(R_{G(off)}+r_g) \quad (2.2.2)$$

Select buffer transistors with a current rating large enough for both $I_{g(on)max}$ and $I_{g(off)max}$ (two times greater than the $I_{g(on)max}$ and $I_{g(off)max}$ is recommended).

The voltage rating of the buffer transistor must be higher than the absolute maximum voltage between gate and source (V_{GSS}) of the SiC MOSFET.

2.3. Gate drive power

The average power consumption P_g of the gate drive circuit can be expressed by equation (2.3.1) using the switching frequency f_{SW} of the SiC MOSFET.

$$P_g=E_g \times f_{SW} = ((+V_{GG}) - (-V_{GG})) \times Q_{gtotal} \times f_{SW} \quad (2.3.1)$$

Here, Q_{gtotal} is the amount of the charge stored in the gate capacitance while the gate voltage changes from $-V_{GG}$ to $+V_{GG}$, and the Q_{gtotal} can be read from the Refer to the datasheet of the products for the V_{GS}-Q_g characteristic curve.

The heat dissipation for the buffer transistors must be greater than the power consumption (two times greater than the P_g is recommended).

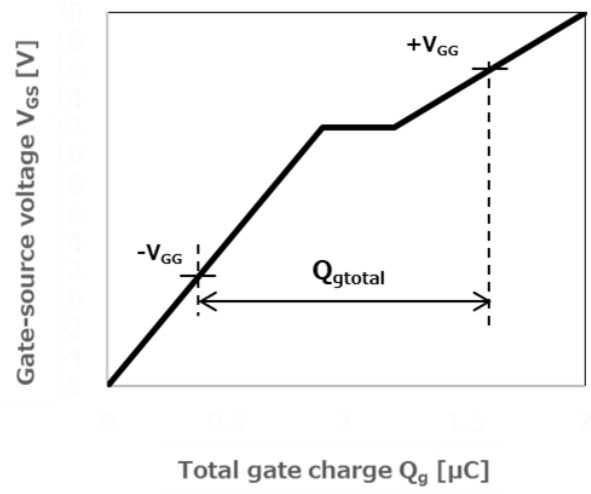


Figure 2.3.2 Definition of Q_{gtotal}

3. Design of gate driver

3.1. Gate voltage

Refer to the datasheet for recommended gate drive voltage. Positive and negative gate voltage surges may occur between the gate and source terminals during the switching. The gate voltage must be within the absolute maximum ratings on the datasheet of the products during all states of the SiC MOSFET, including the “switching”, “on-state” and “off-state”. Care should be taken when one of the SiC MOSFET is switching, which may cause surges between the gate and source terminals of the non-switching-side SiC MOSFET.

3.2. Gate resistance

The switching performance is strongly affected by the gate resistance ($R_{G(on)}$ and $R_{G(off)}$) added to the SiC MOSFET. The peak gate current during switching is determined by the $R_{G(on)}$ and $R_{G(off)}$. It is necessary to decrease the gate resistance and increase the gate current in order to operate the high-speed switching. However, this may result in positive and negative surges between the gate and source terminals. A faster switching speed increases the voltage surge that is generated between the drain and source terminals. Select the optimal $R_{G(on)}$ and $R_{G(off)}$ which do not exceed the gate-source and the drain-source absolute maximum ratings based on the evaluation of your system.

The power consumption of the $R_{G(on)}$ and $R_{G(off)}$ increases in proportion to the switching frequency, therefore select a resistor with optimal power rating.

The method of calculation of power consumption P_g of the gate drive circuit is described in 2.3. The power rating of $R_{G(on)}$ and $R_{G(off)}$ must have a power rating greater than the power consumed at the $R_{G(on)}$ and $R_{G(off)}$ (two times greater than the P_g is recommended).

Insert the gate resistors ($R_{G(on)}$ and $R_{G(off)}$) near the gate terminal to the extent possible.

3.3 Countermeasures for self-turn-on

When the SiC MOSFET is used in inverters or full-bridge circuits (bridged configuration), the change in the V_{DS} of the switching-side SiC MOSFET cause the displacement current ***i***. The displacement current ***i*** charges the capacitance between the gate and drain $C_{gate\text{-}drain}$ of non-switching-side SiC MOSFET (the red line in the figure 3.3.1) and cause the voltage rise between the gate and source terminals. The voltage rise may cause a malfunction of the non-switching-side SiC MOSFET, the phenomena called self-turn-on.

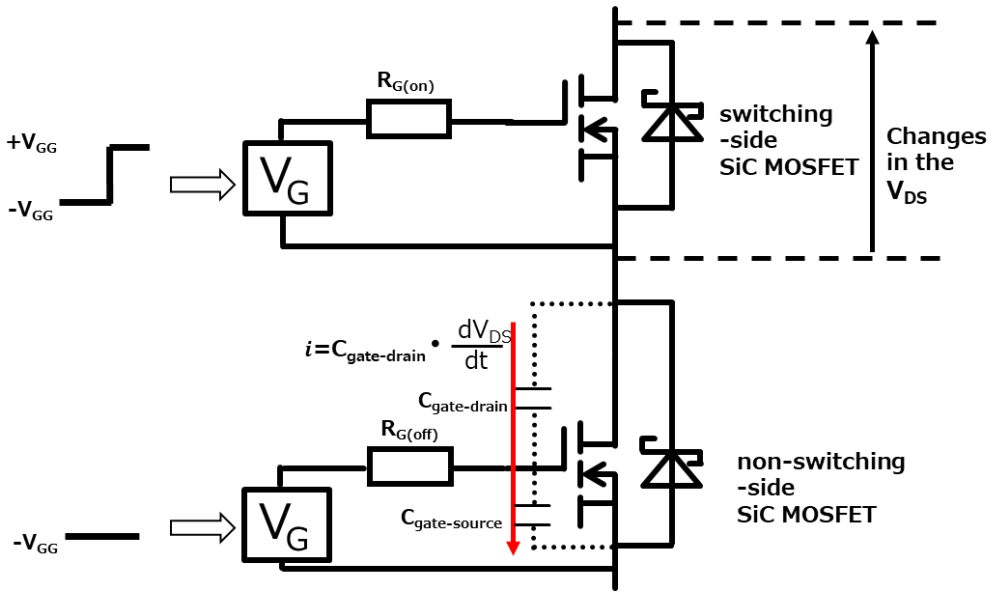
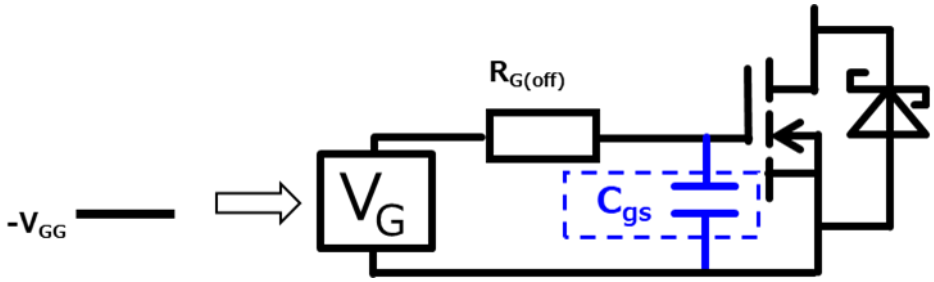


Figure 3.3.1 Self-turn-on caused by displacement current ***i*** generated by dv/dt

Inserting a capacitor (C_{gs}) between the gate and the source is one of the countermeasures to prevent the unintended gate voltage rise that cause a self-turn-on. (Figure 3.3.2) The capacitor should be placed close to the gate and the source terminals.



It is also recommended to use an active miller clamp. The active miller clamp is a function which bypasses the gate resistor $R_{G(off)}$ during off-state of the SiC MOSFET and clamps the gate voltage to the negative bias voltage ($-V_{GG}$) as shown in Figure 3.3.3.

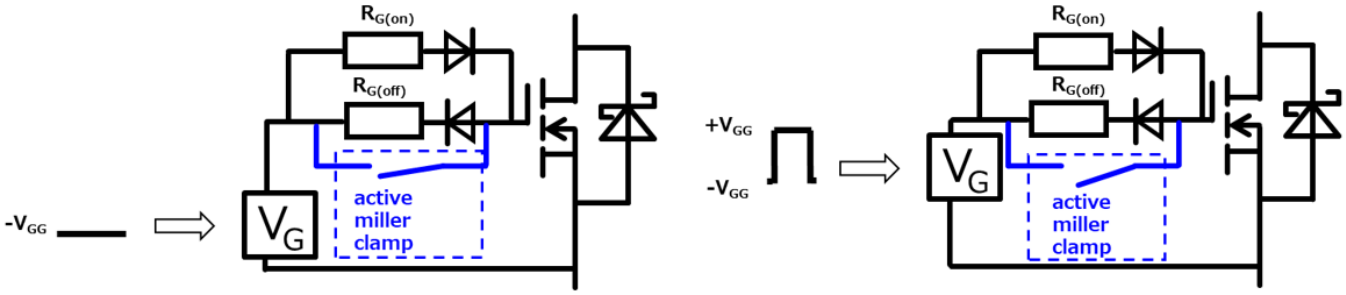


Figure 3.3.3 Function of active miller clamp
(bypasses gate resistor $R_{G(off)}$during the off-state of the SiC MOSFET)

3.4 Dead time

Dead time is the period when both the high and low side SiC MOSFETs are in the off-state.

When the SiC MOSFETs are used in such as inverters or full-bridge circuits (bridged configuration), dead time must be set to avoid DC line short circuit, which may cause damage to the system and/or the SiC MOSFET. Be sure to provide sufficient dead time. If the dead time is too short, then one of the high or low side SiC MOSFETs turns on before the other completes its turn-off, and a large current flows through the high and low side SiC MOSFETs and cause a DC line short circuit. Take into account the propagation delays for both turn-on and turn-off between the controller, gate driver circuit, and SiC MOSFET when determining the dead time.

Determine the dead time based on the evaluation of your system.

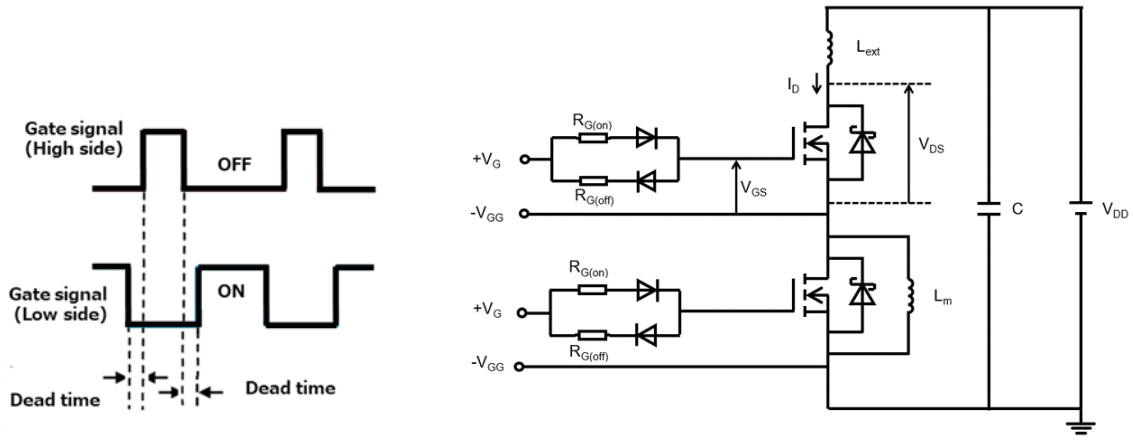


Figure 3.4.1 Definition of dead time

3.5 Gate surge voltage

Because overvoltage to the gate of the SiC MOSFET may damage the device, the gate circuit should be designed with countermeasures against gate surge voltage. The same countermeasures for self-turn-on described in Section 3.3 Figure 3.3.2 (inserting a capacitor between the gate and the source) and Figure 3.3.3 (to use an active miller clamp, which bypasses gate resistor $R_{G(off)}$ during the off-state of the SiC MOSFET) can be applied to suppressing gate surge voltage. Design the gate drive circuit based on the evaluation of your system.

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