

TOSHIBA BiCD Integrated Circuit Silicon Monolithic

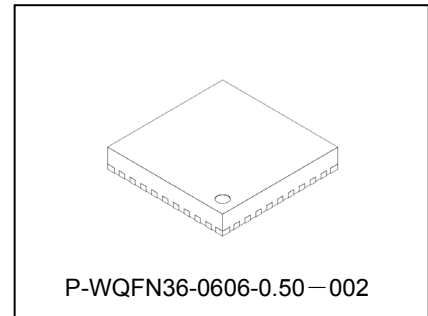
TB67S215FTAG

PWM method CLOCK-IN Bipolar stepping motor driver

The TB67S215FTAG is a pwm method clock-in controlled motor driver for two-phase bipolar stepping motor.

Using the BiCD process, the TB67S215FTAG is rated at 40V/2.5A.(Absolute maximum ratings)

Also, with the built-in VCC regulator, the TB67S215FTAG can be operated with a single motor power(VM) supply.



Weight:0.14(g)

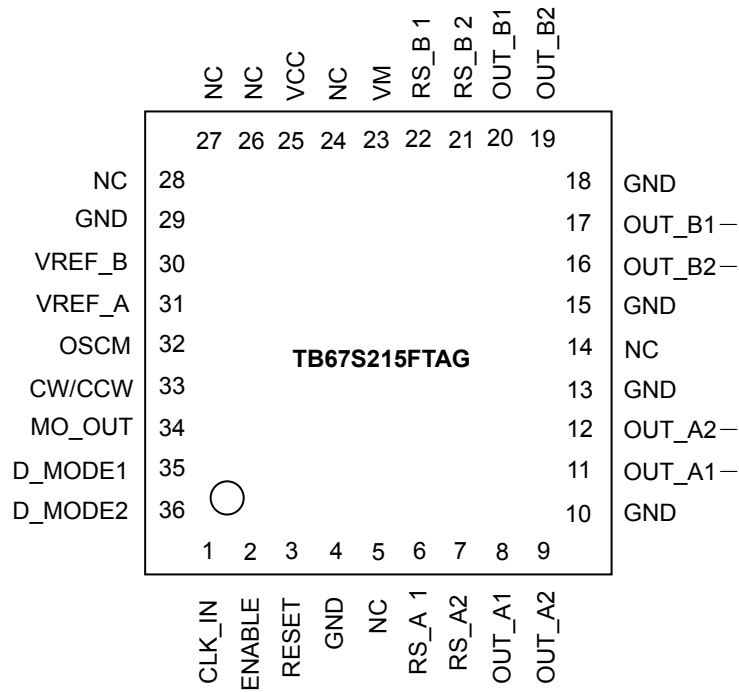
Features

- The TB67S215FTAG can operate a single bipolar stepping motor.
- PWM method current feedback control.
- Operational in Full, Half, and Quarter step resolutions.
- Uses low on-resistance MOSFETs for output stage.
- High voltage and large current. (For specification, please refer to the absolute maximum ratings and operation ranges.)
- Error detection circuits (Thermal Shutdown(TSD), Over current shutdown(ISD), and Power-on reset(POR))
- The built-in VCC regulator allows the TB67S215FTAG to operate with a single VM power supply.
- Customizable PWM chopping frequency using the external components (resistance/capacitor).
- Package: P-WQFN36-0606-0.50-002

Note) Please be careful about thermal conditions during use.

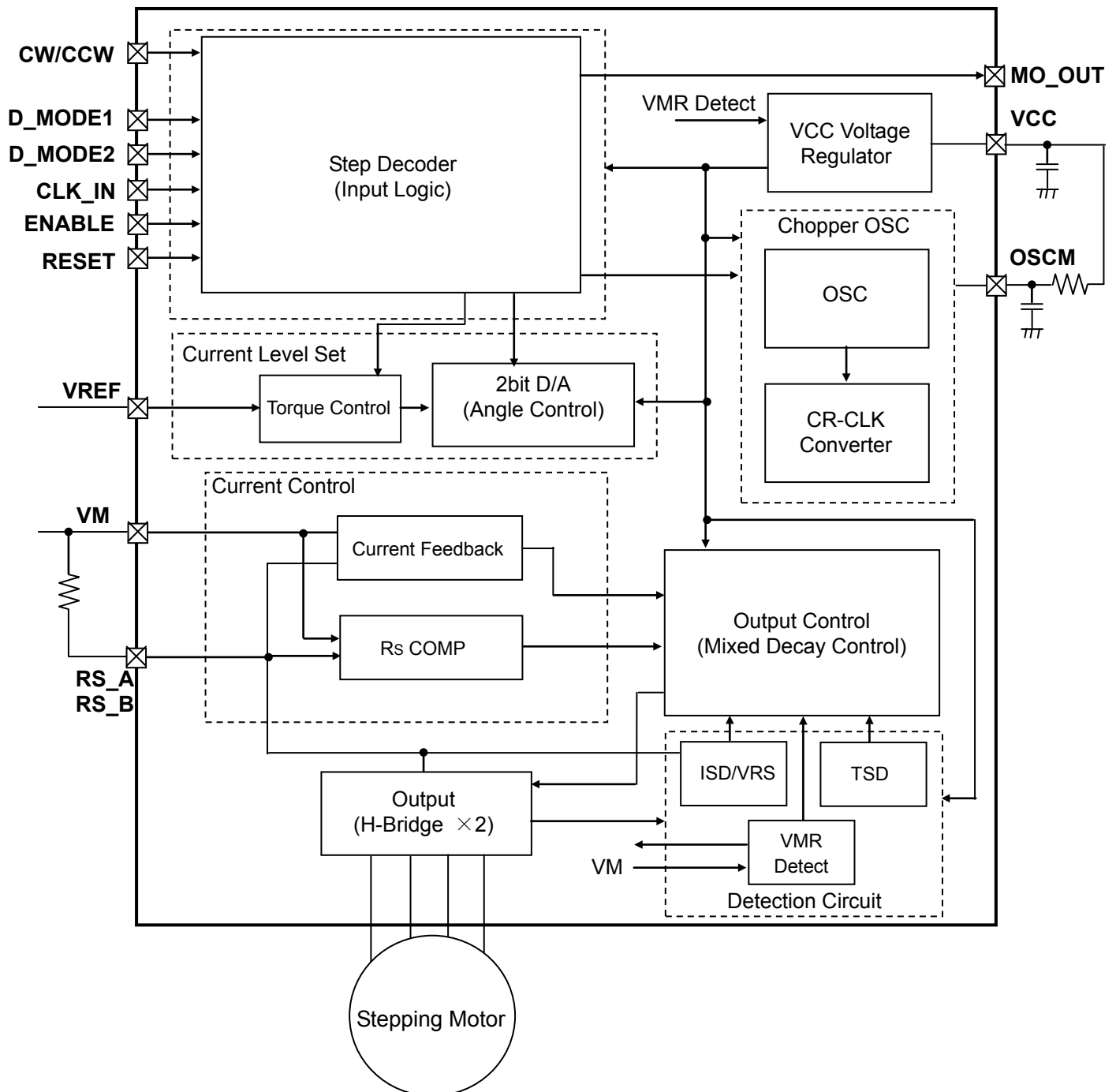
Pin assignment

(Top View)



* Please make sure to short the corner pads and the backside exposed pad to the ground pattern of the board.

Block Diagram



* Please note that in the block diagram, functional blocks or constants may be omitted or simplified for explanatory purposes.

* Please make sure that all GND pins are shorted to the board's ground pattern with a single point. Also, make sure to take extra care with pattern layout, due to heat generation.

Please take extra care while tracing the layout of the VM, GND and output patterns to avoid shortage across output, GND or power supplies. If such shortage occurs, the TB67S215 may be permanently damaged.

The utmost care should also be taken for pattern designing and implementation of the TB67S215. If power-relevant pins such as VM, RS, OUT, and GND (which is capable of running particularly large current) are wired incorrectly, an operation error may occur or the TB67S215 may be destroyed. The logic input pins must also be wired correctly. Otherwise, the TB67S215 may be damaged by a current larger than the specified current running through the IC.

Pin assignment / function

TB67S215FTAG (QFN36)

Pin No.1 – 36

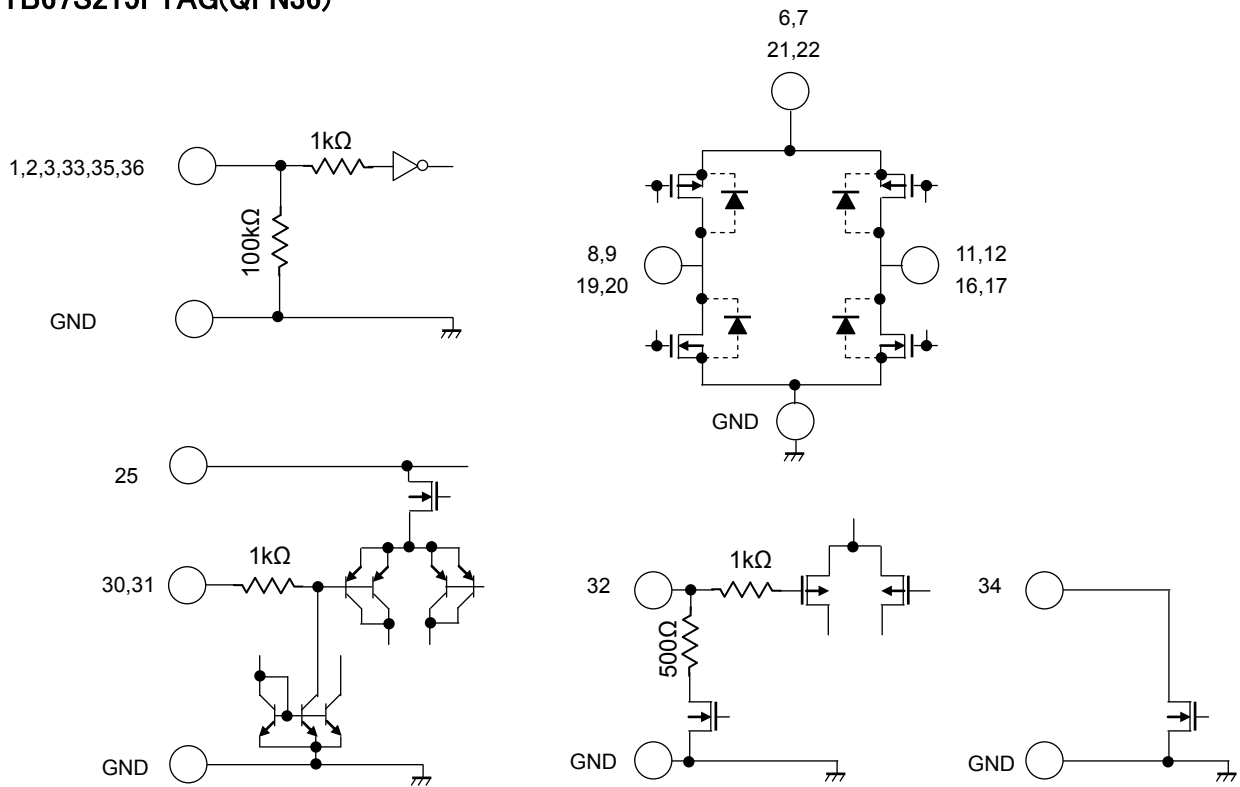
| Pin No. | Pin Name | Function |
|---------|-------------|--|
| 1 | CLK_IN | External CLK input pin |
| 2 | ENABLE | Output stage ON/OFF control pin |
| 3 | RESET | Electric angle reset pin |
| 4 | GND | Ground pin |
| 5 | NC | Non-connection pin |
| 6 | RS_A1 (*) | Motor Ach current sense pin |
| 7 | RS_A2 (*) | Motor Ach current sense pin |
| 8 | OUT_A1 (*) | Motor Ach (+) output pin |
| 9 | OUT_A2 (*) | Motor Ach (+) output pin |
| 10 | GND | Ground pin |
| 11 | OUT_A1- (*) | Motor Ach (-) output pin |
| 12 | OUT_A2- (*) | Motor Ach (-) output pin |
| 13 | GND | Ground pin |
| 14 | NC | Non-connection pin |
| 15 | GND | Ground pin |
| 16 | OUT_B2- (*) | Motor Bch (-) output pin |
| 17 | OUT_B1- (*) | Motor Bch (-) output pin |
| 18 | GND | Ground pin |
| 19 | OUT_B2 (*) | Motor Bch (+) output pin |
| 20 | OUT_B1 (*) | Motor Bch (+) output pin |
| 21 | RS_B2 (*) | Motor Bch current sense pin |
| 22 | RS_B1 (*) | Motor Bch current sense pin |
| 23 | VM | VM power supply pin |
| 24 | NC | Non-connection pin |
| 25 | VCC | Internal VCC regulator monitor pin |
| 26 | NC | Non-connection pin |
| 27 | NC | Non-connection pin |
| 28 | NC | Non-connection pin |
| 29 | GND | Ground pin |
| 30 | VREF_B | Motor Bch current threshold set pin |
| 31 | VREF_A | Motor Ach current threshold set pin |
| 32 | OSCM | Internal Oscillator frequency set pin |
| 33 | CW/CCW | Motor rotation direction set pin (Clock-wise/Counter Clock-wise) |
| 34 | MO_OUT | Electric angle monitor pin |
| 35 | D_MODE1 | Step resolution set pin no.1 |
| 36 | D_MODE2 | Step resolution set pin no.2 |

•Please do not run patterns under NC pins.

(*)Please short the pins with the same pin names, while using the TB67S215FTAG.

Equivalent circuit

TB67S215FTAG(QFN36)



The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

| Pin No | Pin name |
|--------|----------|
| 1 | CLK_IN |
| 2 | ENABLE |
| 3 | RESET |
| 6,7 | RS_A |
| 8,9 | OUT_A+ |
| 11,12 | OUT_A- |
| 16,17 | OUT_B- |
| 19,20 | OUT_B+ |
| 21,22 | RS_B |
| 23 | VM |
| 25 | VCC |
| 30 | VREF_B |
| 31 | VREF_A |
| 32 | OSCM |
| 33 | CW/CCW |
| 34 | MO_OUT |
| 35 | D_MODE1 |
| 36 | D_MODE2 |

Function explanation(Stepping motor control)

1. CLK Function

The CLK pin controls the rotation speed of the motor. Each CLK signal will shift the motor's electrical angle per step, due to each up-edge of the CLK signal.

| CLK Input | Function |
|-----------|--|
| Up-edge | Shifts the electrical angle per step. |
| Down-edge | (State of the electrical angle does not change.) |

2. ENABLE function

The ENABLE pin controls the ON and OFF of the corresponding output stage. (For accurate operation, please set the ENABLE pin to 'L' during VM power-on and power-off sequence.)

| ENABLE Input | Function |
|--------------|---|
| H | Output stage='ON' (Normal operation mode) |
| L | Output stage='OFF' (High impedance mode) |

3. CW/CCW function

The CW/CCW pin controls the rotation direction of the motor.

| CW/CCW Input | Function |
|--------------|----------------------------|
| H | Clockwise rotation |
| L | Counter clockwise rotation |

4. Step resolution select function

The D_MODE pin controls the Standby mode and the step resolution setting.

| D_MODE_1 | D_MODE_2 | Function |
|----------|----------|--|
| L | L | Standby mode (the internal oscillator is disabled and the output stage is set to 'OFF' status) |
| L | H | Full step operation |
| H | L | Half step operation |
| H | H | Quarter step operation |

5. RESET function

The RESET pin controls the resetting of the electrical angle. (For accurate operation, please set the RESET pin to 'H' during power-on. Switch the RESET to 'L' once the VM voltage has reached the operation level.)

| RESET Input | Function |
|-------------|---|
| L | Normal operation mode |
| H | Sets the electrical angle to the initial condition. |

The current setting for each channel (while RESET is applied) is shown in the table below. MO_OUT pin level will show 'L' at this time.

| Step resolution setting | Ach current setting | Bch current setting |
|-------------------------|---------------------|---------------------|
| Full step | 100% | 100% |
| Half step | 100% | 100% |
| Quarter step | 71% | 71% |

About error detection circuits

Thermal shutdown (TSD) circuit

When the junction temperature of the device reaches the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. Once the TSD circuit is triggered, the device keeps the output off until power-on reset (POR), is reasserted or both D_MODE pins are set to Low (Standby mode).

Over-current/voltage shutdown (ISD) circuit

When the output current or the RS pin voltage reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. Once the ISD circuit is triggered, the device keeps the output off until power-on reset (POR), is reasserted or both D_MODE pins are set to Low (Standby mode).

For fail-safe, please insert a fuse to avoid secondary trouble.

Power-on-reset (POR) circuit

While the VM voltage and VCC voltage is below the POR threshold, the POR circuit will keep the output stage to be set to OFF status.

Absolute maximum ratings (Ta = 25° C)

| Characteristics | Symbol | Rating | Unit | Note | |
|----------------------------|---------|------------|------|--------|--------|
| Motor power supply | VM | 40 | V | - | |
| Motor output voltage | VOUT | 40 | V | - | |
| Motor output current | IOUT | 2.5 | A | Note 1 | |
| VCC voltage | VCC | 6.0 | V | - | |
| Digital input voltage | VIN(H) | 6.0 | V | - | |
| | VIN(L) | -0.4 | V | - | |
| MO_OUT output voltage | VMOUT | 6.0 | V | - | |
| MO_OUT output sink current | IMOUT | 30 | mA | - | |
| Power dissipation | QFN36 | PD | 3.76 | W | Note 2 |
| Operating temperature | TOPR | -20 to 85 | °C | - | |
| Storage temperature | TSTR | -55 to 150 | °C | - | |
| Junction temperature | Tj(max) | 150 | °C | - | |

Note 1: While in use, please make sure that the motor current is controlled to be under 80 % of the absolute maximum ratings. (In this case, about 2.0A (max)).

Note 2: The value in the state where it is mounted on the board

Ta: Ambient temperature.

Topr: Operating ambient temperature.

Tj: Operating junction temperature. The maximum junction temperature is limited by the thermal shutdown.

Note: Use the maximum junction temperature (Tj) at 120° C or less.

The maximum current cannot be used under certain thermal conditions.

Note: The absolute maximum ratings

The absolute maximum ratings are a specification that must not be exceeded, even for a moment.

Exceeding the ratings may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

Operating Ranges (Ta=0 to 85°C)

| Characteristics | Symbol | Min | Typ | Max | Unit | Note |
|----------------------------|--------------|-----|------|------|------|---------------------|
| Motor power supply | VM | 10 | 24 | 35 | V | |
| Motor output current | IOUT | - | 1.0 | 2.0 | A | |
| Logic input voltage | VIN(H) | 2.0 | - | 5.5 | V | Logic 'High' level |
| | VIN(L) | 0 | - | 0.8 | V | Logic 'Low' level |
| MO_OUT output voltage | VMOUT | - | 3.3 | 5.0 | V | |
| CLK input frequency | fCLK | - | - | 100 | kHz | |
| PWM signal frequency range | fchop(range) | 40 | 100 | 150 | kHz | |
| VREF reference voltage | Vref | GND | 3.0 | 3.6 | V | |
| RS pin voltage | VRS | - | ±1.0 | ±1.5 | V | Reference value: VM |

Note 1: The actual maximum current may be limited by the operating environment (operating conditions such as excitation mode or operating duration, or by the surrounding temperature or board heat dissipation). Determine a realistic maximum current by calculating the heat generated under the operating environment.

Note 2: The maximum VRS voltage should not exceed the maximum rated voltage.

Electrical Specifications 1 (Ta=25°C, VM=24V, unless specified otherwise)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|----------|-----------|--------------|---|-----|------|------|------|
| Logic input pin voltage | HIGH | VIN(H) | DC | Logic input pins (Note) | 2 | – | 5.5 | V |
| | LOW | VIN(L) | DC | Logic input pins (Note) | 0 | – | 0.8 | V |
| Logic input voltage hysteresis | | VIN(HYS) | DC | Logic input pins (Note) | 100 | – | 300 | mV |
| Logic input pin current | HIGH | IIN(H) | DC | Logic input pins; VIN=3.3V | – | 33 | 50 | μA |
| | LOW | IIN(L) | DC | Logic input pins; VIN=0V | – | – | 1 | μA |
| MO_OUT pin voltage | HIGH | VOH(MO) | DC | IOL=24mA Output:High | 2.4 | – | – | V |
| | LOW | VOL(MO) | DC | IOL=24mA Output:Low | – | – | 0.5 | V |
| Power consumption | | IM1 | DC | Output:OPEN, Standby mode | – | 2 | 3 | mA |
| | | IM2 | DC | Output:OPEN, ENABLE=L | – | 3.5 | 5 | mA |
| | | IM3 | DC | Output:OPEN (Full step setting) | – | 5 | 7 | mA |
| Motor output leakage current | Hi-side | IOH | DC | VRS=VM=40V,VOUT=0V | – | – | 1 | μA |
| | Low-side | IOL | DC | VRS=VM=VOUT=40V | 1 | – | – | μA |
| Bridge-to-Bridge current differential | | ΔIOUT1 | DC | Channel A and B differential | –5 | 0 | 5 | % |
| Output current error relative to the predetermined value | | ΔIOUT2 | DC | IOUT=1.0A | –5 | 0 | 5 | % |
| RS pin current | | IRS | DC | VRS=VM=24V | 0 | – | 10 | μA |
| Drain-source ON-resistance (The sum of high side & low side) | | Ron(S)_PN | | IOUT=2.0A, Tj=25°C, (Hi-side+Low side MOSFET) | – | 0.53 | 0.75 | Ω |

Note: VIN (L → H) is defined as the VIN voltage that causes the outputs (OUT_A+, OUT_A-, OUT_B+ and OUT_B-) to change when a pin under test is gradually raised from 0 V. VIN (H → L) is defined as the VIN voltage that causes the outputs (OUT_A+, OUT_A-, OUT_B+ and OUT_B-) to change when the pin is then gradually lowered.

The difference between VIN (L → H) and VIN (H → L) is defined as the input hysteresis.

Note: The internal circuits are designed to avoid miss-function or leakage current; when the logic signal is applied while the VM voltage is not supplied. But for fail-safe, please control the power supply and logic signal timing correctly.

Electrical Specifications 2 (Ta=25°C, VM=24V, unless specified otherwise)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--------------------------------|------------|--------------|----------------|-------|-------|-------|------|
| Vref input voltage | VREF | DC | VM=24V,VCC=5V | GND | 3.0 | 3.6 | V |
| Vref input current | IREF | | VREF=3.0V | – | 0 | 1 | μA |
| VCC voltage | VCC | | ICC=5.0mA | 4.75 | 5.0 | 5.25 | V |
| VCC current | ICC | | VCC=5.0V | – | 2.5 | 5 | mA |
| Vref gain | VREF(gain) | | VREF=2.0V | 1/5.2 | 1/5.0 | 1/4.8 | – |
| TSD threshold (Note1) | TjTSD | | – | 140 | 150 | 170 | °C |
| VM POR threshold | VMR | | – | 7.0 | 8.0 | 9.0 | V |
| Over current threshold (Note2) | ISD | | – | (3.1) | (4.0) | (5.0) | A |

Note 1: Thermal shutdown (TSD) circuit

When the junction temperature of the device reaches the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. Once the TSD circuit is triggered, the device keeps the output off until power-on reset (POR), is reasserted or both D_MODE pins are set to Low (Standby mode).

Note 2: Over-current/voltage shutdown (ISD) circuit

When the output current or the RS pin voltage reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. Once the ISD circuit is triggered, the device keeps the output off until power-on reset (POR), is reasserted or both D_MODE pins are set to Low (Standby mode).

For fail-safe, please insert a fuse to avoid secondary trouble.

Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.

If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the TB67S215 or other components will be damaged or fail due to the motor back-EMF.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

- The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
- If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
- The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

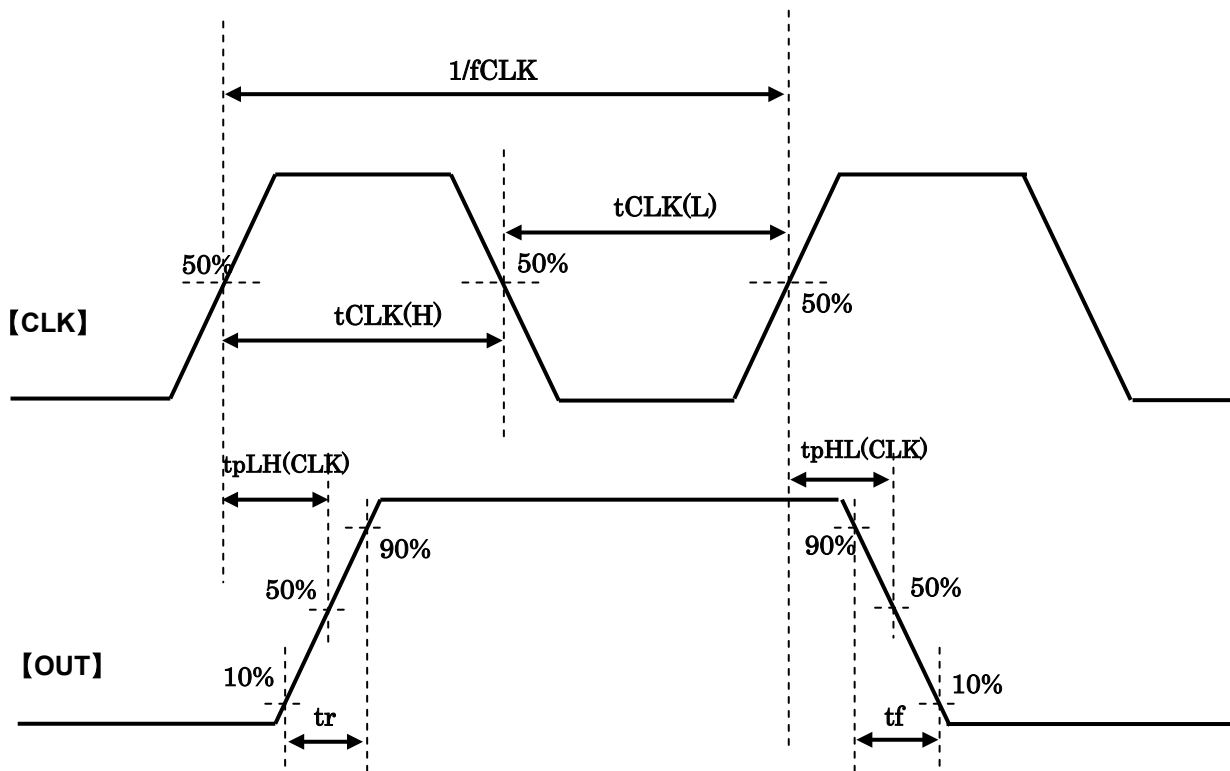
IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

Electrical Specifications 2 (Ta = 25° C, VM = 24 V, 6.8 mH/5.7 Ω)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--|-----------|--------------|---|------|------|------|------|
| CLK input frequency | fCLK | AC | fOSC=1600kHz | - | - | 100 | kHz |
| Minimum CLK High width | tCLK(H) | AC | Minimum CLK width: CLK= 'H' | 300 | - | - | ns |
| Minimum CLK Low width | tCLK(L) | AC | Minimum CLK width: CLK= 'L' | 250 | - | - | ns |
| Output stage Switching specifications | tr | AC | | 100 | 150 | 200 | ns |
| | tf | AC | | 100 | 150 | 200 | ns |
| | tpLH(CLK) | AC | CLK to OUT | - | 1000 | - | ns |
| | tpHL(CLK) | AC | CLK to OUT | - | 1500 | - | ns |
| Analog noise rejection blank time | AtBLK | AC | VM=24V,IOUT=1.0A Analog tBLK | 250 | 400 | 550 | ns |
| Internal oscillator frequency | fOSC | AC | COSC= 270 pF, ROSC =3.6 kΩ | 1360 | 1600 | 1840 | kHz |
| Motor chopping frequency | fchop | AC | Output active (IOUT =1.0 A), fOSC = 1600 kHz | - | 100 | - | kHz |

AC timing chart

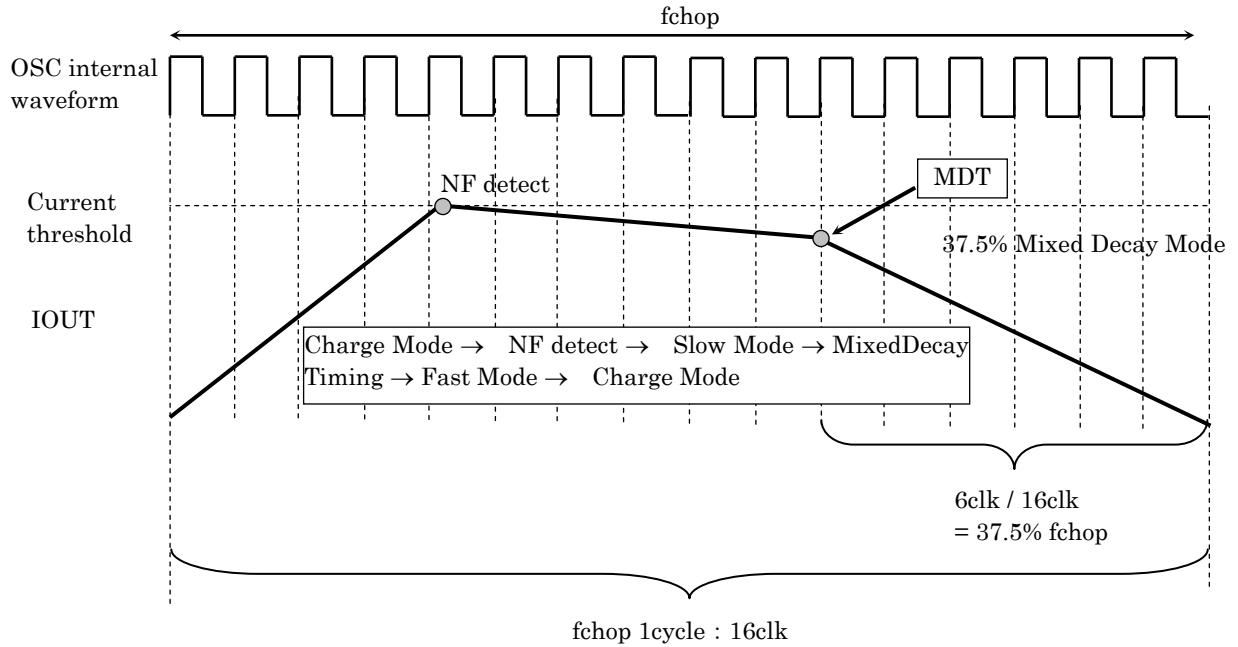


Timing charts may be simplified for explanatory purpose.

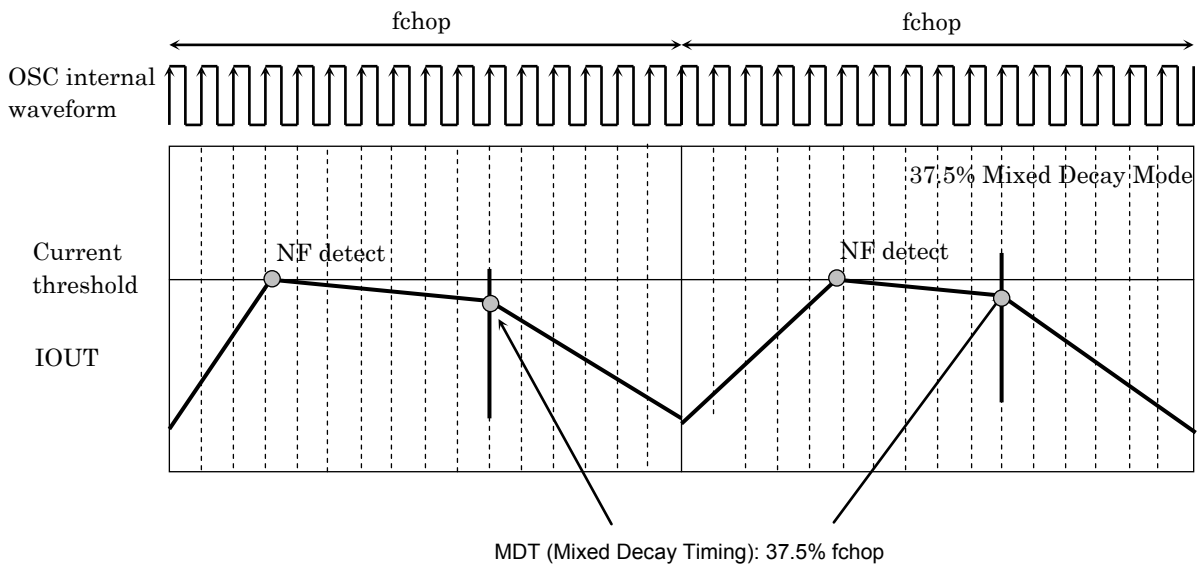
Application Note

Motor control (Current feedback control)

The 'Mixed Decay Timing' is a fixed value of 37.5% of 1 fchop cycle.



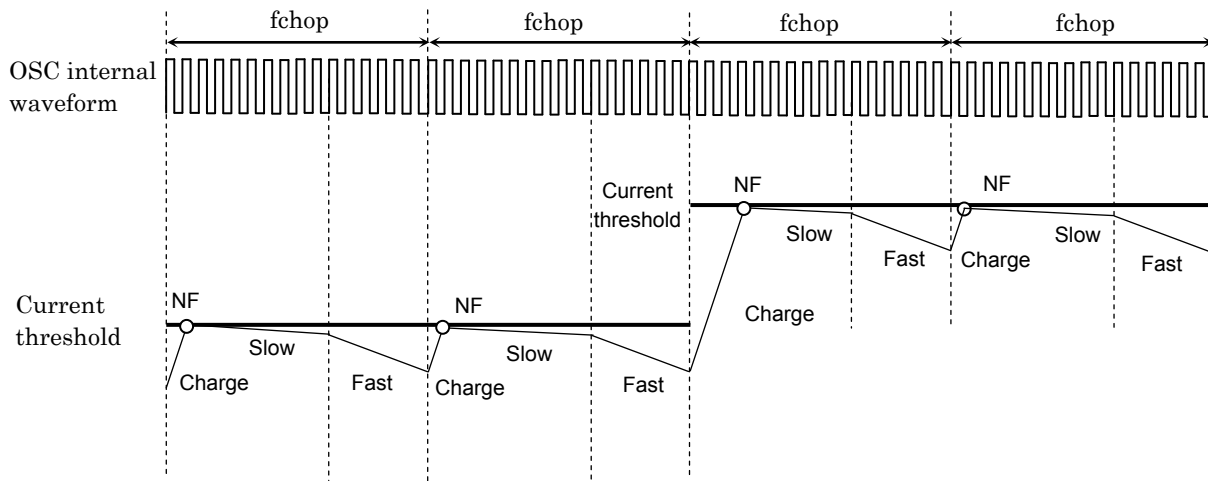
Waveform of Mixed Decay Mode sequence (Motor current)



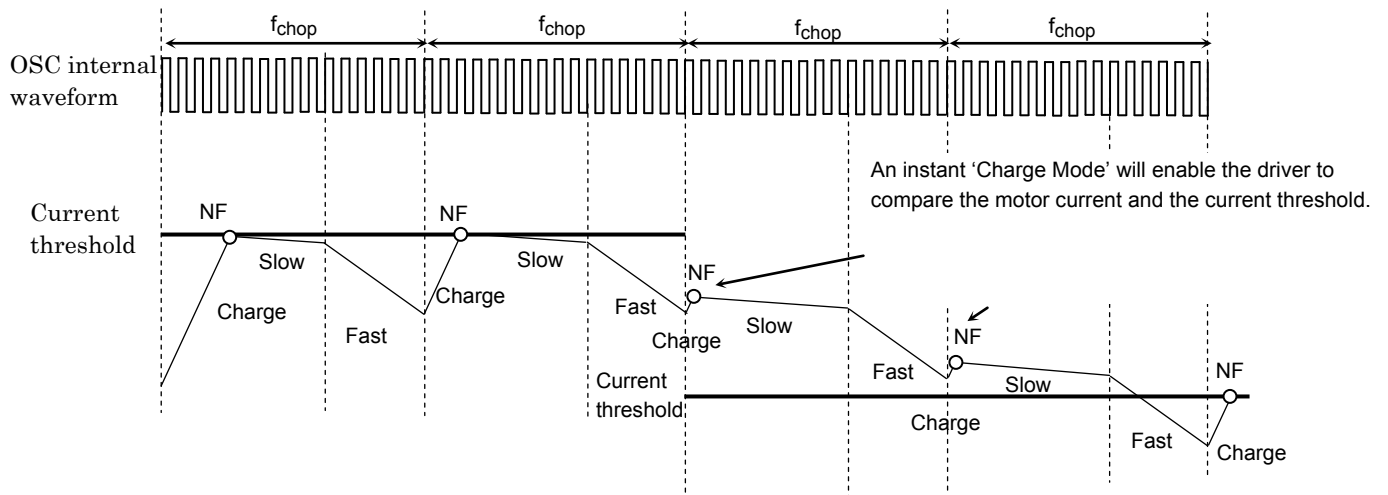
Timing charts may be simplified for explanatory purposes.

Mixed (Slow + Fast) Decay Mode current waveform

•When the next step's current threshold is above the previous step

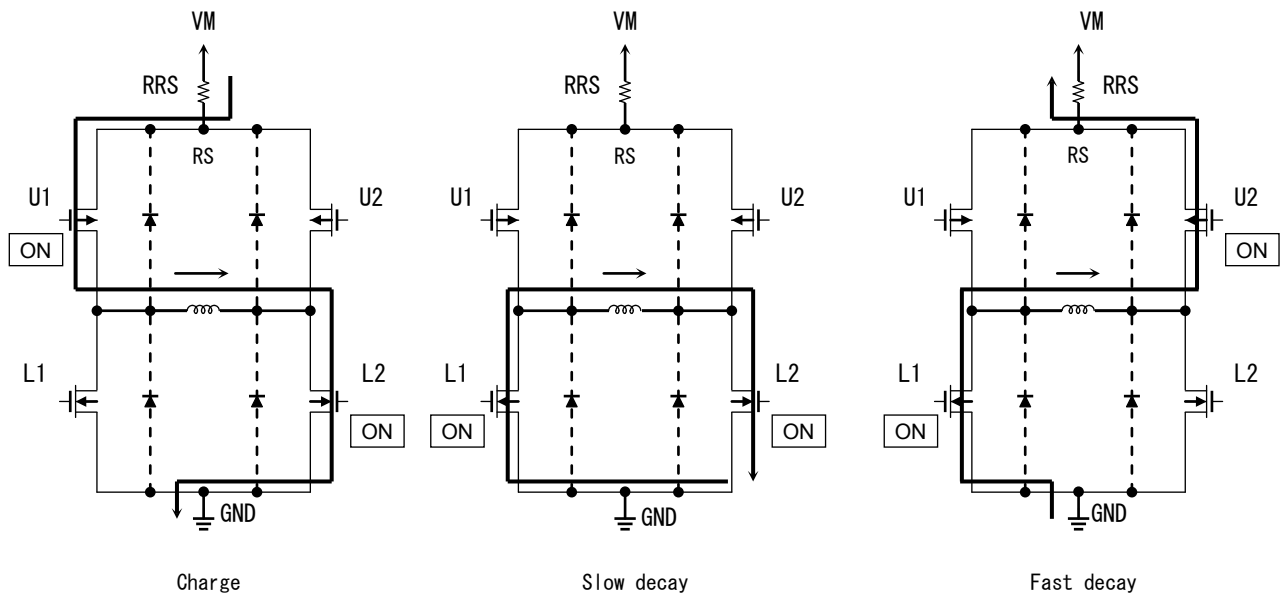


•When the next step's current threshold is below the previous step



Timing charts may be simplified for explanatory purposes.

Output Transistor Operation Mode



Some of the functional blocks, circuits, or constants omitted or simplified for explanatory purpose.

Output Transistor Operational Function

| Mode | U1 | L1 | U2 | L2 |
|------------|-----|-----|-----|-----|
| Charge | ON | OFF | OFF | ON |
| Slow decay | OFF | ON | OFF | ON |
| Fast decay | OFF | ON | ON | OFF |

Note: The parameters shown in the table above are examples when the current flows in the directions shown in the figures above. For the current flowing in the reverse direction, the parameters change as shown in the table below.

| Mode | U1 | L1 | U2 | L2 |
|------------|-----|-----|-----|-----|
| Charge | OFF | ON | ON | OFF |
| Slow decay | OFF | ON | OFF | ON |
| Fast decay | ON | OFF | OFF | ON |

Calculation of the Predefined Output Current

For PWM constant-current control, the TB67S215FTAG uses a clock generated by the CR oscillator. The peak output current can be set via the current-sensing resistor (RRS) and the reference voltage (Vref), as follows:

$$I_{OUT} = V_{ref}/5 \div RRS (\Omega)$$

where, 1/5 is the Vref decay rate, Vref (GAIN). For the value of Vref (GAIN), see the Electrical Characteristics table. For example, when Vref = 3 V, to set the current feedback threshold (Iout)=1.8A, RS resistance is calculated as:

$$RRS = (V_{ref} / 5) \div I_{OUT} = (3/5) \div 1.8 = 0.33 \Omega. (\geq 1.1 W)$$

Calculation of the OSCM oscillation frequency (chopper reference frequency)

An approximation of the OSCM oscillation frequency (fOSCM) and chopper frequency (fchop) can be calculated by the following expressions.

$$f_{OSCM} = 1 / [0.56 \times (C_x(R1 + 500))] \quad \dots\dots\dots C, R1: \text{External components for OSCM (C=270pF, R=3.6k}\Omega \Rightarrow 1.6\text{MHz)}$$

$$f_{chop} = f_{OSCM} / 16$$

IC Power Consumption

The power consumed by the TB67S215FTAG is approximately the sum of the following:

- 1) the power consumed by the output transistors
- 2) the power consumed by the digital logic and pre-drivers.

The power consumed by the output transistors is calculated, using the RON (D-S) value of 0.6Ω.

An approximation of the peak power consumption for H-SW can be calculated by the following expressions.

$$P(\text{out}) = H\text{-SW}(\text{ch}) \times I_{out}(\text{A}) \times I_{out}(\text{A}) \times R_{on}(\Omega) \quad (1)$$

In full step operation (for example, 1.0A), the average power consumption in the output stage is calculated as follows:

$$\begin{aligned} R_{on} &= 0.6 \Omega, I_{out} = 1.0 \text{ A}, VM = 24 \text{ V} \\ P(\text{out}) &= 2(\text{ch}) \times 1.0(\text{A})^2 \times 0.6(\Omega) && (2) \\ &= 1.2(\text{W}) \end{aligned}$$

The power consumption in the IM domain is calculated as:

$$\begin{aligned} P(\text{IM}) &= 24(\text{V}) \times 0.005(\text{A}) && (3) \\ &= 0.12(\text{W}) \end{aligned}$$

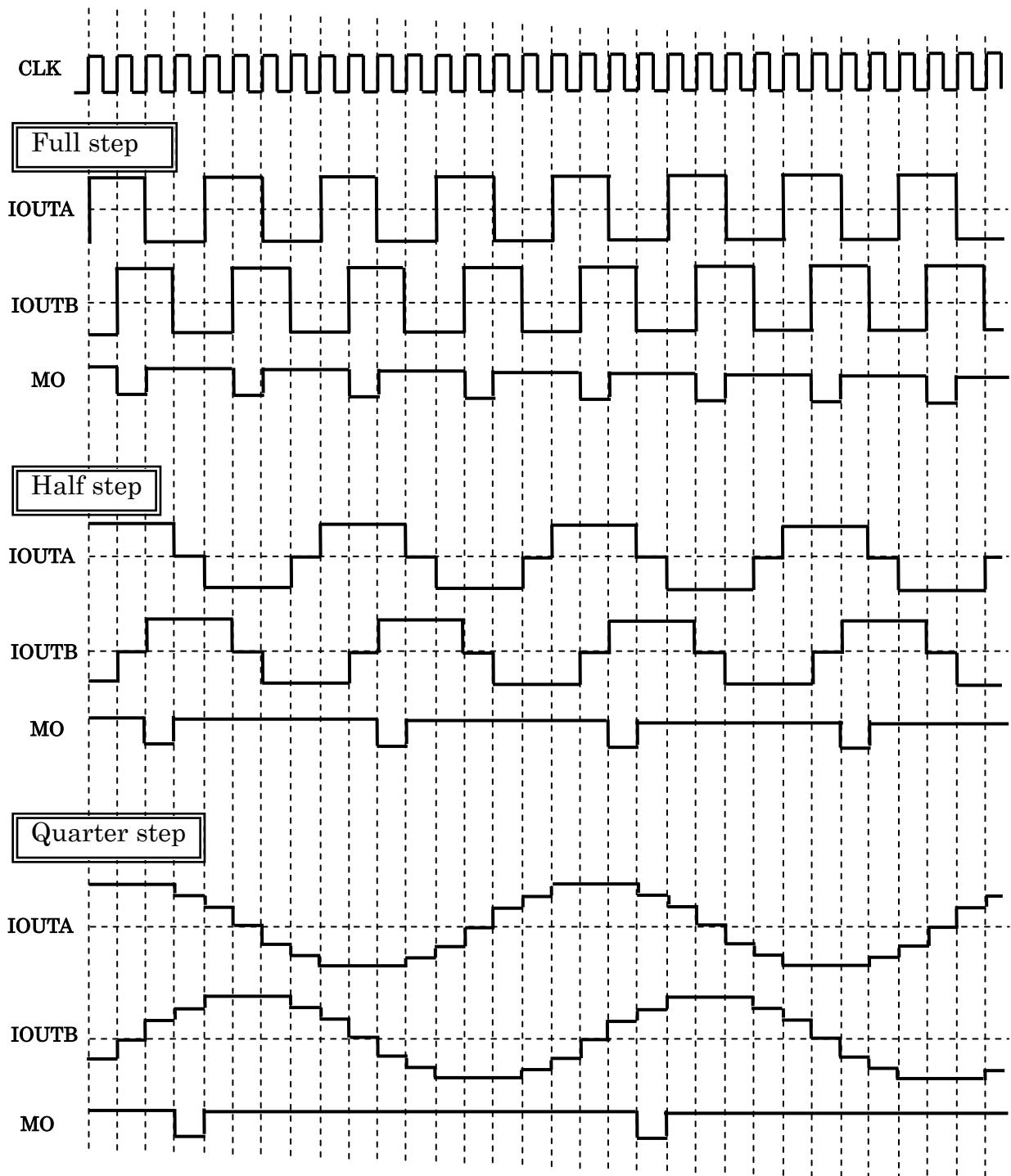
$$(IM3) = 5.0 \text{ mA (typ.)}, VM=24\text{V}$$

All over, the total peak power consumption of TB67S215FTAG is:

$$P = P(\text{out}) + P(\text{IM}) = 1.32(\text{W})$$

Board design should be fully verified, taking thermal dissipation into consideration.

Step resolution timing charts (CLK-IN)

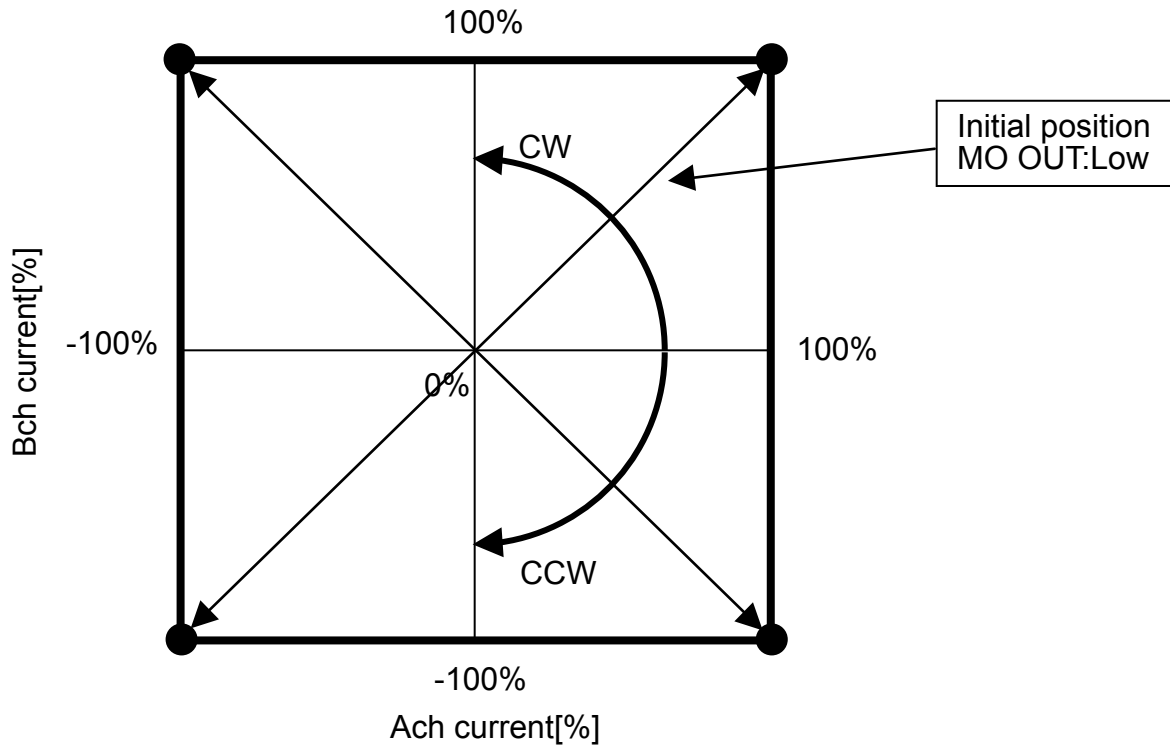


The MO is an open drain output pin. Therefore the High level of the MO waveform shown above, will be the MO pin's pulled up voltage level.

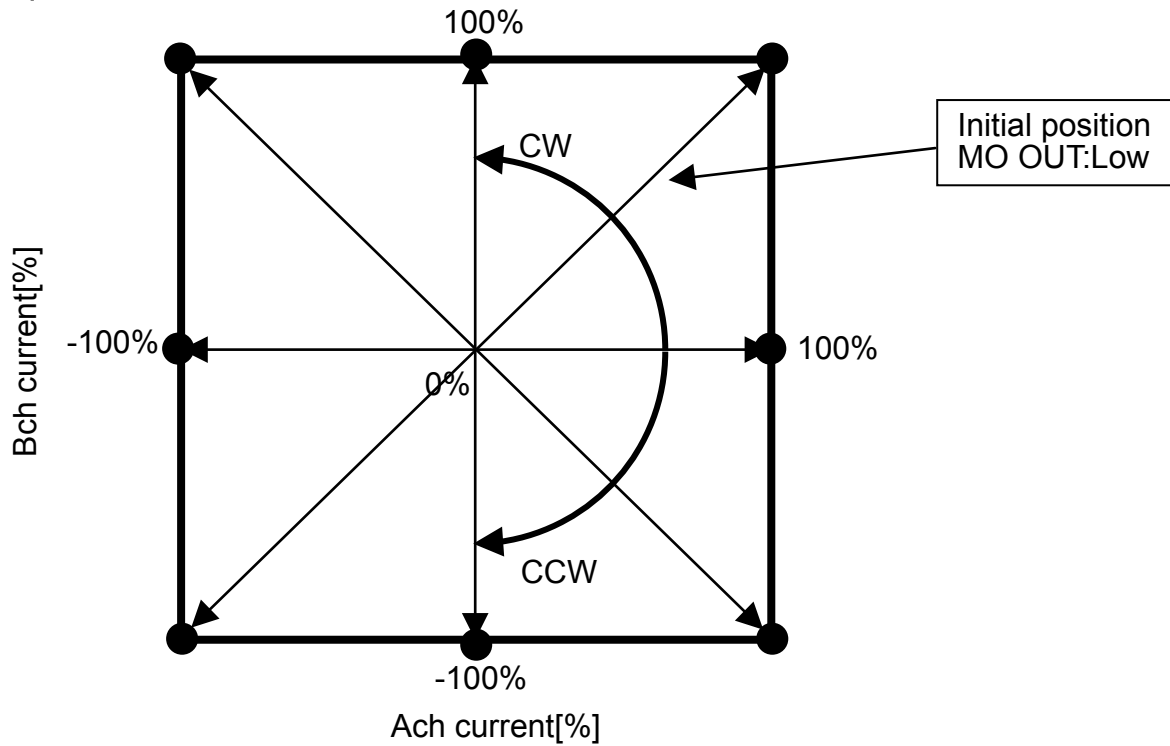
Timing charts may be simplified for explanatory purposes.

Step resolution and initial position

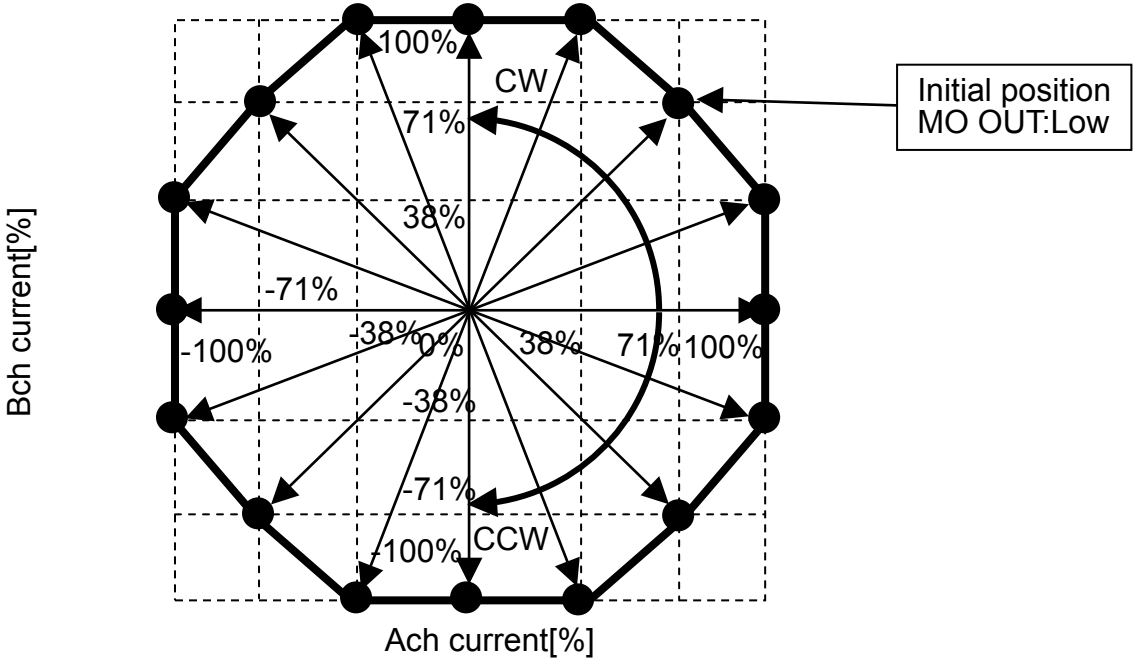
• Full step resolution



• Half step resolution

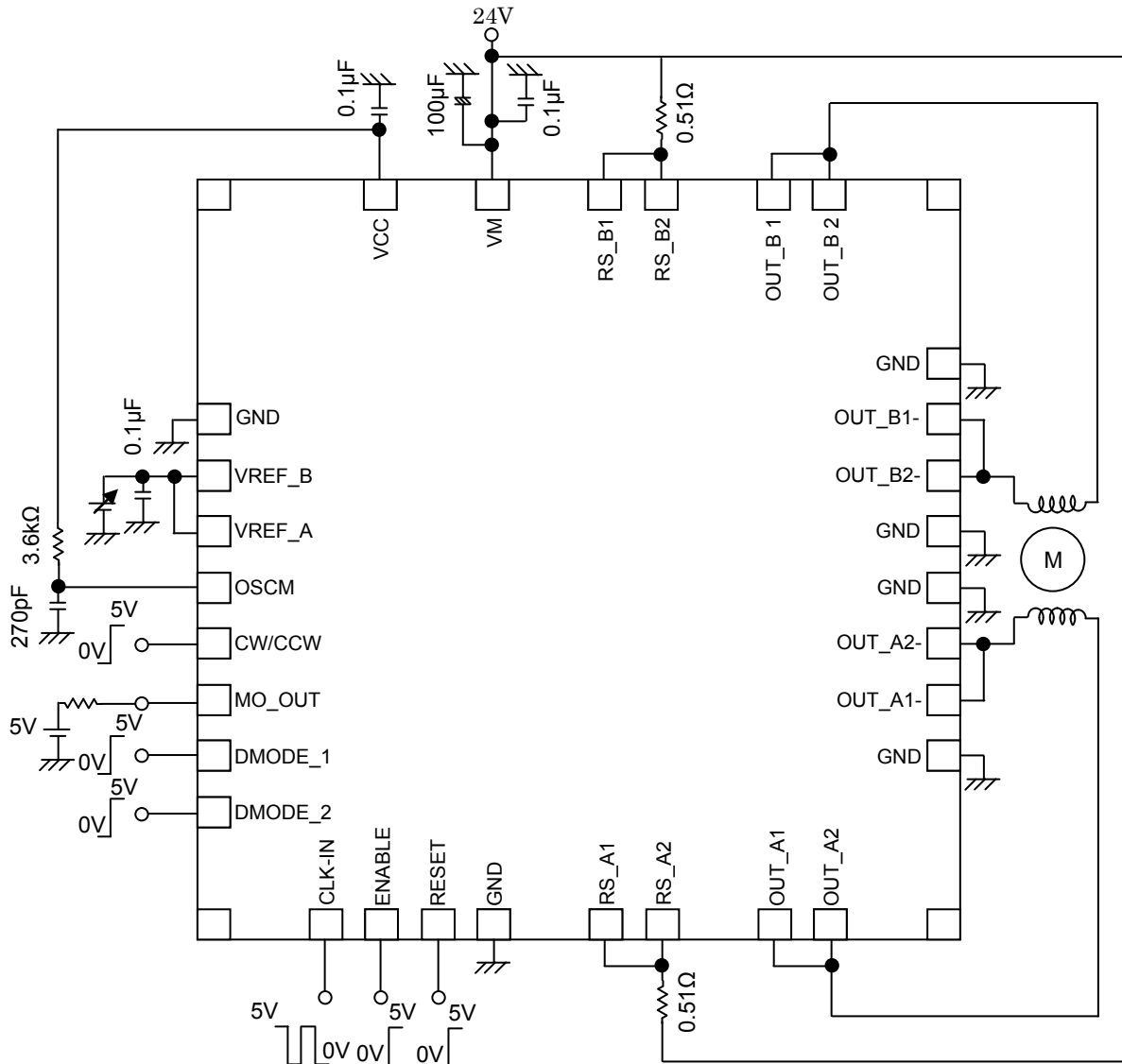


Quarter step resolution



Example Application Circuits

The values shown in the following figure are typical values. For input conditions, see the Operating Ranges.



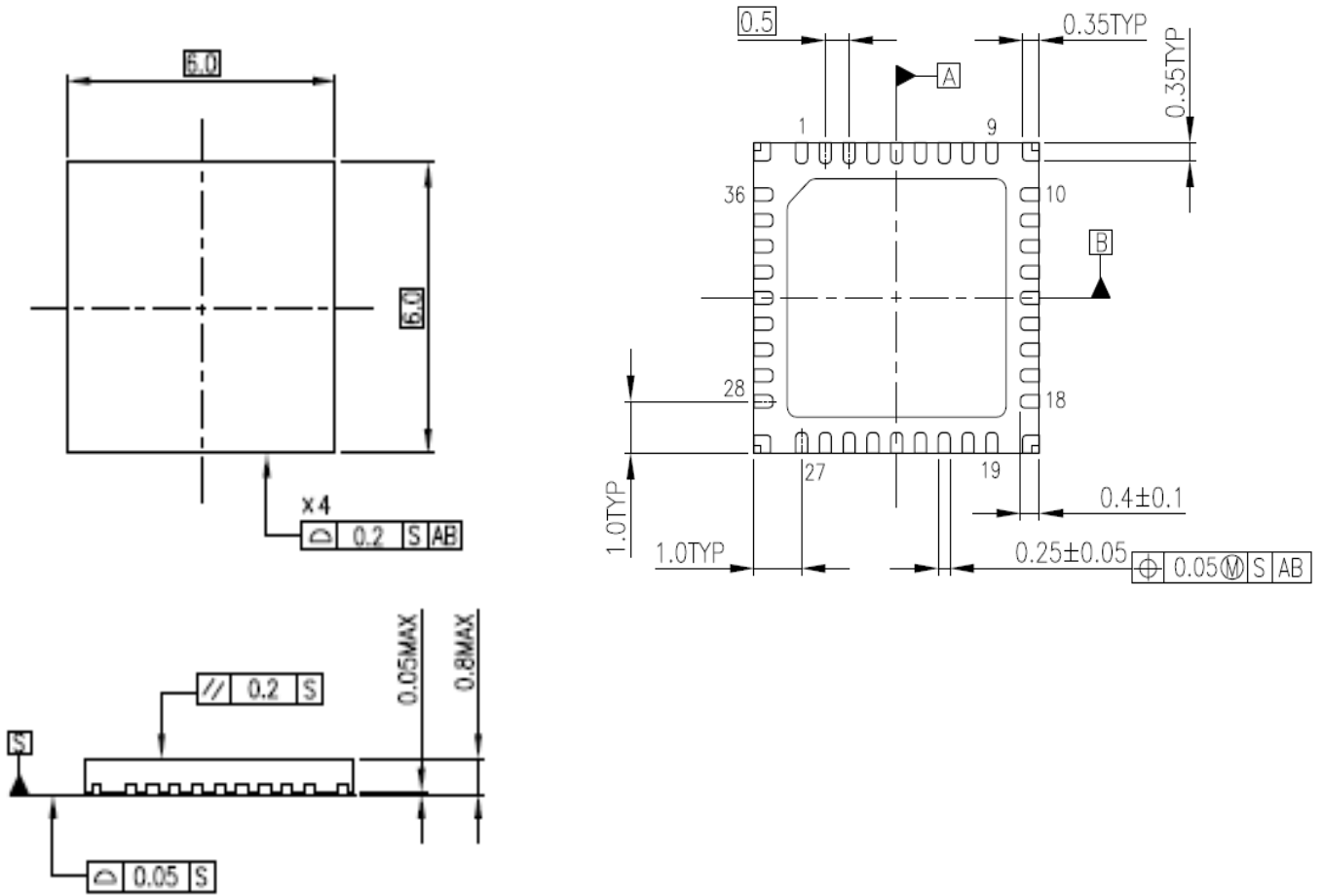
Note: Bypass capacitors should be added as necessary. It is recommended to use a single ground plane for the entire board whenever possible.

The above application circuit example is presented only as a guide and should be fully evaluated prior to production. Also, no intellectual property right is ceded in any way whatsoever in regard to its use.

Package Dimensions

P-WQFN36-0606-0.50-002

Unit:mm



Notes on Contents**Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing Charts

Timing charts may be simplified for explanatory purposes.

Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations**Notes on handling of ICs**

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. In addition, do not use any device that has been inserted incorrectly.

Please take extra care when selecting external components (such as power amps and regulators) or external devices (for instance, speakers). When large amounts of leak current occurs from capacitors, the DC output level may increase. If the output is connected to devices such as speakers with low resist voltage, overcurrent or IC failure may cause smoke or ignition. (The over-current may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

Over current detection circuit

Over current detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current detection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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